${\bf (19)}\ World\ Intellectual\ Property\ Organization$

International Bureau



) | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1881 | 1

(43) International Publication Date 16 March 2006 (16.03.2006) (10) International Publication Number WO 2006/028341 A1

(51) International Patent Classification⁷:

H01L 21/68

(21) International Application Number:

PCT/KR2005/002932

(22) International Filing Date:

5 September 2005 (05.09.2005)

(25) Filing Language:

English

(26) Publication Language:

English

(**30**) **Priority Data:** 10-2004-0071290

7 September 2004 (07.09.2004) KR

- (71) Applicant (for all designated States except US): KO-REA SEMICONDUCTOR SYSTEM CO., LTD. [KR/KR]; 162-19 Dodang-dong, Wonmi-gu, Buchon-si,, kyunggi-Do, 420-805 (KR).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): PARK, Myung-Soon [KR/KR]; 1086-15 Hwagog-dong, Gangsu-gu, Seoul 157-010 (KR).
- (74) Agent: CHOI, Duke Young; Suite 503, Samyoung Building,, 604-19 Guro-dong,, Seoul 152-864 (KR).

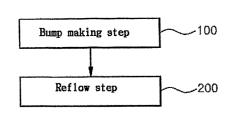
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MAKING BUMP ON SEMICONDUCTOR DEVICE



made at the bump making.

(57) Abstract: The object of this invention is to provide a bump making method, which makes bumps on a semiconductor device using a molten metal compound, thus minimizing an error rate of the bumps, reducing investment costs, and allowing bumps to be easily made on a small amount of semiconductor devices as well as a large amount of semiconductor devices. The bump making method includes a bump making step (100) to make the bump (50) having a predetermined diameter by jetting a molten metal compound (40) onto the semiconductor device (10) at a predetermined speed, and a reflow step (200) to shape the bump into a ball by heating the bump



1

[DESCRIPTION]

[Invention Title]

METHOD OF MAKING BUMP ON SEMICONDUCTOR DEVICE

[Technical Field]

The present invention relates generally to a method of making bumps on a semiconductor device and, more particularly, to a bump making method, which makes bumps on a semiconductor device using a fluid, thus minimizing an error rate of the bumps, reducing investment costs, and allowing bumps to be easily made on a small amount of semiconductor devices as well as a large amount of semiconductor devices.

[Background Art]

Generally, a semiconductor device has several tens of semiconductor chips. Each of the semiconductor chips is provided with under ball metallurgy on which a bump is made to ensure a superior electrical connection, when the semiconductor chip is connected to a substrate.

In order to make bumps on under ball metallurgy, a screen printing method, an electroplating method, a deposition method, etc. have been proposed.

According to the screen printing method, a passivation film is formed on an upper surface of a wafer other than under ball metallurgy so as to protect a pattern formed on the wafer. Next, a three-layered metal film comprising titanium (Ti), tungsten (W), and gold (Au), that is, an upper barrier metal is deposited on the under ball metallurgy and the passivation film through a metal deposition process. Afterwards, a photoresist is applied to the upper barrier metal such that the under ball metallurgy is not electrically connected to each other. Thereafter, part of the upper barrier metal is eliminated through a photolithography process including an exposure step, a development step, an upper-barrier-metal etching step, and a stripping step. Thereby, the upper barrier metal remains on only the under ball metallurgy. In this case, since the upper barrier metal is the three-layered metal film, the upper-barrier-metal etching step is sequentially

executed three times.

After the upper barrier metal is made only on the under ball metallurgy, a screen mask is laminated on the semiconductor device, and solder paste is applied to the under ball metallurgy using a squeezer. In this case, the upper barrier metal serves as a medium which enhances the coupling force between the under ball metallurgy and the solder paste.

After the solder paste has been applied to the under ball metallurgy, flux is applied to the solder paste. In the case of using solder paste containing flux, an additional flux application process is not required. The flux is a kind of solvent which serves to neatly connect the under ball metallurgy to the solder paste, and prevents the formation of oxides, when the under ball metallurgy is connected to the solder paste, thus ensuring reliable connection.

Subsequently, a reflow process is carried out. When the solder paste is heated to a predetermined temperature in the reflow process, the solder paste is shaped into a ball due to the flux. Thereby, bumps are made on the under ball metallurgy. Next, a flux cleaning process is executed to remove flux residue and impurities from the wafer. Therefore, the wafer having the bumps at predetermined positions is obtained.

Meanwhile, the conventional electroplating method is executed as follows. First, a wafer having under ball metallurgy is prepared. A passivation layer is formed on an upper surface of the wafer other than the under ball metallurgy. Next, an upper barrier metal is deposited on the under ball metallurgy and the passivation layer through a metal deposition process. Subsequently, a photoresist is applied to an upper surface of the upper barrier metal, and parts of the photoresist disposed on the under ball metallurgy are eliminated through an exposure operation and a development operation, so that parts of the upper barrier metal disposed on the under ball metallurgy are exposed to the outside. At this time, photoresist residue remaining on the upper barrier metal is eliminated through an etching operation. Thereafter, a plated part is formed in an empty space above the

under ball metallurgy through an electrolytic plating operation. Solder, Au, Ni, and others are used as a material for the plated part. After the plated part has been formed as such, surplus photoresist is stripped and eliminated. Thereafter, the upper barrier metal is etched so that parts of the upper barrier metal other than parts provided under the plated parts are eliminated. In this case, since the upper barrier metal is a three-layered metal film, the etching process is sequentially performed three times.

Thereafter, a dipping operation is carried out. That is, the semiconductor device having the plated parts is dipped into a flux bath so that flux is applied to the plated parts. Next, predetermined heat is applied to the plated parts through a reflow process, so that each plated part is shaped into a ball due to the flux. Thereby, bumps are made on the under ball metallurgy. Afterwards, a flux cleaning process is executed. That is, a cleaning liquid is supplied to the semiconductor device to remove flux residue and impurities from the semiconductor device. Consequently, a semiconductor device having bumps at predetermined positions is obtained.

[Disclosure]

[Technical Problem]

However, the conventional bump making methods have the following problems. That is, the screen printing method is problematic in that the solder paste may be non-uniformly applied due to the operational irregularity of the squeezer and print conditions when the solder paste is applied using the screen mask, so that solder bridging or a height difference may occur between neighboring terminals, or insufficient solder may be applied, thus causing a defective bump, therefore considerably reducing productivity. The electroplating method has a problem in that many processes are required to make a bump, so that it usually takes 30 to 40 minutes to make the bump, thus increasing the bump manufacturing time. The electroplating method has another problem in that expensive plating equipment is needed, so that bump manufacturing costs are increased. The electroplating method has a further problem in that a plating time, an applied current, a voltage, etc. are

4

changed depending on a position of the semiconductor device, so that the plated amount is changed. Thereby, bumps made on an edge of the wafer become small. As such, the shape of the bumps becomes irregular. Further, if the difference in plated amount is large, an open failure may occur when the semiconductor device is connected to the substrate.

[Technical Solution]

Accordingly, the present invention has been made keeping in mind the above problems occurring in the prior art, and an object of the present invention is to provide a method, which makes bumps on a semiconductor device using a fluid, thus minimizing an error rate of the bumps, reducing investment costs, and allowing bumps to be easily made on a small amount of semiconductor devices as well as a large amount of semiconductor devices.

In order to accomplish the above object, the present invention provides a method of making a bump on under ball metallurgy provided on a semiconductor device to enhance electrical connection, including a bump making step to make the bump having a predetermined diameter by jetting a molten metal compound onto the semiconductor device at a predetermined speed, and a reflow step to shape the bump into a ball by heating the bump made at the bump making step.

[Advantageous Effects]

[Description of Drawings]

The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

- FIG. 1 is a block diagram to illustrate a method of making a bump on a semiconductor device, according to the present invention;
- FIG. 2 is a view to illustrate a wafer positioning operation in the bump making method, according to the present invention;
- FIG. 3 is a view to illustrate the operation of making a bump by jetting a molten metal compound, according to the present invention; and
 - FIG. 4 is a view to illustrate the state where a bump is shaped into a

ball through a reflow process of the bump making method, according to the present invention.

[Best Mode]

[Mode for Invention]

Hereinafter, the preferred embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 1 is a block diagram to illustrate a method of making a bump on a semiconductor device, according to the present invention, FIG. 2 is a view to illustrate a wafer positioning operation in the bump making method, according to the present invention, FIG. 3 is a view to illustrate the operation of making a bump by jetting a molten metal compound, according to the present invention, and FIG. 4 is a view to illustrate the state where a bump is shaped into a ball through a reflow process of the bump making method, according to the present invention.

Referring to FIGS. 1 to 4, the bump making method according to the present invention includes a bump making step 100 and a reflow step 200.

In the bump making step 100, a molten metal compound is supplied to a semiconductor device 10 at a predetermined speed, thus making a bump 50 having a predetermined diameter.

In a detailed description, a fluid supply unit 30 jets a predetermined amount of molten metal compound 40 having a predetermined size onto a predetermined position of the semiconductor device 10 at a predetermined speed, so that the bump 50 is made on under ball metallurgy 20. The molten metal compound 40 is selected from the group comprising a mixture of tin and lead, a mixture of tin, silver, and copper, and a mixture of tin and copper. Elements contained in each of the mixtures are melted and mixed with each other in predetermined proportions. The semiconductor device 10 is moved such that preset position coordinates of the semiconductor device 10 are sequentially and precisely located under the fluid supply unit 30. Thus, the molten metal compound 40, supplied from the fluid supply unit 30, precisely falls onto under ball metallurgy 20.

Further, the bump making step 100 includes a bump positioning step 110 and a wafer positioning step 120 that are preliminary steps and are executed before the molten metal compound 40 is supplied to the semiconductor device 10, so that the molten metal compound 40 is precisely supplied to a predetermined position on the semiconductor device 10 to make the bump 50.

In the bump positioning step 110, columns and rows of bumps 50 to be made on the semiconductor device 10 are established. That is, in order to make the bumps 50 at precise positions, accurate position coordinates of the under ball metallurgy 20 provided on the semiconductor device 10 are set and programmed.

The wafer positioning step 120 is executed so as to precisely make the bumps 50 at the preset position coordinates. In the wafer positioning step 120, an initial position A of an object on which the bumps 50 are made, namely, the semiconductor device 10, is detected. The position of the semiconductor device 10 is adjusted so that the initial position A is precisely located at a predetermined position.

When the bump making step 100 has been completed, the reflow step 200 is executed. In the reflow step 200, the bump 50 provided on the under ball metallurgy 20 is heated to a predetermined temperature. The heated bump 50 is shaped into a ball due to surface tension, so that a desired bump 50 is obtained.

According to the present invention, the bumps of the semiconductor wafer are made as follows. That is, the fluid supply unit 30 supplies the molten metal compound 40 to the under ball metallurgy 20 of the wafer 10, in the form of a ball having a predetermined diameter, thus making the bump 50. Therefore, an error rate and equipment costs are considerably reduced, and productivity is dramatically increased. Further, even when a small amount of semiconductor device 10 is produced, profit is high. It is possible to make bumps 50 of various sizes by replacing the nozzle of the fluid supply unit 30 with another one depending on the diameter of a bump to be made, so that workability and productivity are superior, and manufacturing costs are

WO 2006/028341 PCT/KR2005/002932

considerably reduced.

【Industrial Applicability】

As described above, the present invention provides a bump making method, which makes bumps on a semiconductor device using a fluid, thus minimizing an error rate of the bumps, reducing investment costs, and allowing bumps to be easily made on a small amount of semiconductor devices as well as a large amount of semiconductor devices.

[CLAIMS]

[Claim 1]

A method of making a bump on under ball metallurgy provided on a semiconductor device to enhance electrical connection, comprising:

a bump making step to make the bump having a predetermined diameter by jetting a molten metal compound onto the semiconductor device at a predetermined speed; and

a reflow step to shape the bump into a ball by heating the bump made at the bump making step.

[Claim 2]

The method as set forth in claim 1, wherein the molten metal compound comprises a mixture of tin and lead that are melted and mixed with each other in a predetermined proportion.

[Claim 3]

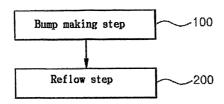
The method as set forth in claim 1, wherein the molten metal compound comprises a mixture of tin, silver and copper that are melted and mixed with each other in a predetermined proportion.

[Claim 4]

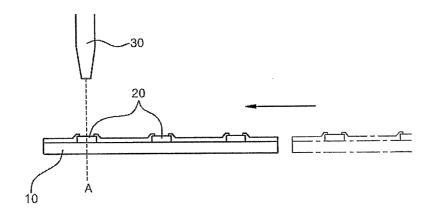
The method as set forth in claim 1, wherein the molten metal compound comprises a mixture of tin and copper that are melted and mixed with each other in a predetermined proportion

[DRAWINGS]

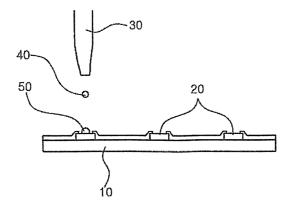
[Figure 1]



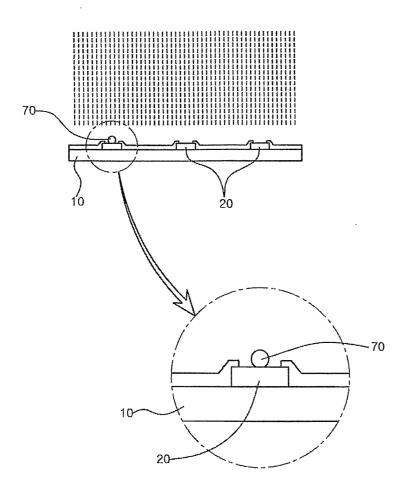
[Figure 2]



[Figure 3]



[Figure 4]



INTERNATIONAL SEARCH REPORT

International application No. PCT/KR2005/002932

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/60(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B23K 31/02(2006.01)i, H01L 21/00(2006.01)i, H01L 21/31(2006.01)i, H01L 21/44(2006.01)i, H01L 21/60(2006.01)i

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean Patents and applications for inventions since 1976.

Korean Utility models and applications for Utility models since 1976.

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used) KIPONET II

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6264090 B1 (SPEEDLINE TECHNOLOGIES, INC.) 24 JULY 2001 * the whole document *	1 - 4
Y	KR 1999-48003 A2 (SAMSUNG ELECTRONICS CO., LTD.) 5 JULY 1999 * the whole document *	1 - 4
A	US 5810988 A (UNIVERSITY OF TEXAS SYSTEM) 22 SEPTEMBER 1998 * the whole document *	1 - 4
A	US 6224180 B1 (MPM CORPORATION) 1 MAY 2001 * the whole document *	1 - 4

Further documents are listed in the continuation of Box C.	See patent family annex.
Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means	step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family
Date of the actual completion of the international search	Date of mailing of the international search report

Name and mailing address of the ISA/KR

Korean Intellectual Property Offi

Facsimile No. 82-42-472-7140

Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Authorized officer

SONG, Won Seon

Telephone No. 82-42-481-5735

12 JANUARY 2006 (12.01.2006)



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2005/002932

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6264090 B1	24.07.01	NONE	
KR 1999-48003 A2	05.07.99	NONE	
US 5810988 A	22.09.98	NONE	
US 6224180 B1	01.05.01	WO 9836864 A2 WO 9836864 A3	27.08.98 03.12.98