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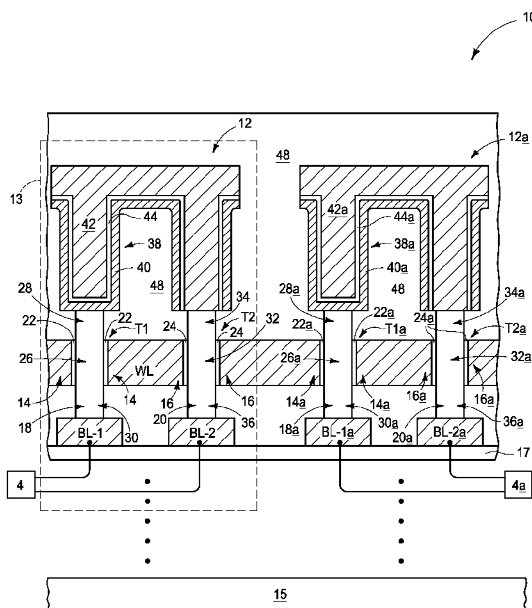

FIG. 2

(57) Abstract: Some embodiments include a memory cell having first and second transistors, and a capacitor vertically displaced relative to the first and second transistors. The capacitor has a first node electrically coupled with a source/drain region of the first transistor, a second node electrically coupled with a source/drain region of the second transistor, and capacitor dielectric material between the first and second nodes. Some embodiments include a memory cell having first and second transistors vertically displaced relative to one another, and a capacitor between the first and second transistors. The capacitor has a first node electrically coupled with a source/drain region of the first transistor, a second node electrically coupled with a source/drain region of the second transistor, and capacitor dielectric material between the first and second nodes.

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DESCRIPTION

MEMORY CELLS AND MEMORY ARRAYS

TECHNICAL FIELD

5 Memory cells, such as memory cells having two transistors and one capacitor (i.e., 2T-1C memory cells). Memory arrays comprising 2T-1C memory cells.

BACKGROUND

Dynamic Random Access Memory (DRAM) is utilized in modern computing 10 architectures. DRAM may provide advantages of structural simplicity, low cost and speed in comparison to alternative types of memory.

Presently, DRAM commonly utilizes memory cells having one capacitor in combination with a transistor (so-called 1T-1C memory cells), with the capacitor being coupled with a source/drain region of the transistor. One of the limitations to scalability 15 of present 1T-1C configurations is that it is proving difficult to incorporate capacitors having sufficiently high capacitance into highly-integrated architectures. Accordingly, it would be desirable to develop new memory cell configurations suitable for incorporation into highly-integrated modern memory architectures. As another DRAM cell, a 2T-1C memory cell configuration is schematically illustrated in FIG. 1 according to the prior 20 art, which includes two transistors and one capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art memory cell having 2 transistors and 1 capacitor.

25 FIG. 2 is a diagrammatic cross-sectional side view of a region of a memory array showing an example configuration for memory cells having 2 transistors and 1 capacitor.

FIG. 3 is a diagrammatic top view of the memory array of FIG. 2.

FIG. 4 is a diagrammatic cross-sectional side view of a memory array showing another example configuration for memory cells having 2 transistors and 1 capacitor.

30 FIG. 5 is a diagrammatic cross-sectional side view of a region of a memory array showing another example configuration for memory cells having 2 transistors and 1 capacitor.

FIG. 6 is a cross-sectional side view of a region another example configuration for a memory cell having 2 transistors and 1 capacitor.

FIG. 7 is a diagrammatic cross-sectional side view of a region of another memory array showing another example configuration for memory cells having 2 transistors and 1 capacitor.

FIG. 8 is a diagrammatic cross-sectional side view of a memory array showing another example configuration for memory cells having 2 transistors and 1 capacitor.

FIGS. 9-13 are expanded regions of one of the transistors of a 2T-1C memory cell showing example embodiment configurations of such transistor.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Some embodiments include 2T-1C configurations in which two or more components are vertically stacked relative to one another in order to increase integration. Specific example embodiments of stacking arrangements are described below with reference to FIGS. 2-13.

Referring again to FIG.1, an example prior art 2T-1C memory cell configuration 2 includes two transistors and one capacitor. The two transistors are labeled as T1 and T2, and the capacitor is labeled as CAP.

A source/drain region of T1 connects with a first node of the capacitor (CAP), and the other source/drain region of T1 connects with a first comparative bitline (BL-1). A gate of T1 connects with a wordline (WL). A source/drain region of T2 connects with a second node of the capacitor (CAP), and the other source/drain region of T2 connects with a second comparative bitline BL-2. A gate of T2 connects with the wordline (WL).

The comparative bitlines BL-1 and BL-2 extend to circuitry 4 which compares electrical properties (e.g., voltage) of the two to ascertain a memory state of memory cell 2. An advantage of the 2T-1C memory cell is that a memory state may be ascertained by comparing the electrical properties of the two comparative bitlines BL-1 an BL-2 to one another, and accordingly a reference bitline associated with prior art memory (for instance, 1T-1C memory) may be omitted.

The 2T-1C configuration of FIG. 1 may be utilized in DRAM (dynamic random access memory) and/or other types of memory.

FIG. 2 shows a region of a memory array 10 comprising example 2T-1C memory cells. Specifically, a pair of adjacent memory cells 12 and 12a are illustrated. A dashed line 13 demarcates an approximate boundary of the memory cell 12. The memory cells 12 and 12a are substantially identical to one another, with the term “substantially

identical" meaning that the memory cells are identical to within reasonable tolerances of fabrication and measurement.

The illustrated portion of memory array 10 is supported by a base 15. The base may comprise semiconductor material; and may, for example, comprise, consist
5 essentially of, or consist of monocrystalline silicon. The base may be referred to as a semiconductor substrate. The term "semiconductor substrate" means any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising
10 other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above. In some applications the base may correspond to a semiconductor substrate containing one or more materials associated with integrated circuit fabrication. Such materials may include, for example, one or more of refractory metal materials, barrier materials, diffusion materials, insulator
15 materials, etc. The base 15 is shown to be spaced from components of array 10 to indicate that other circuitry or components may be between array 10 and the base 15. An interlayer insulating film 17 may intervene between the base 15 and the array 10. Although the film 17 is only shown in FIG. 2, it is to be understood that it may be present in the embodiments shown in other figures as well. The film 17 may comprise
20 any suitable electrically insulative material or combination of insulative materials, including, for example, silicon dioxide, silicon nitride, etc.

In the illustrated embodiment, the insulating film 17 has a substantially planar upper surface, and the comparative bitlines (BL-1, BL-2, BL-1a and BL-2a) are disposed on such upper surface, and in parallel with one another. The term "substantially planar"
25 means planar to within reasonable tolerances of fabrication and measurement.

The memory cell 12 comprises a pair of comparative bitlines BL-1 and BL-2, and comprises transistors T1 and T2 over the bitlines BL-1 and BL-2, respectively. Similarly the memory cell 12a comprises a pair of comparative bitlines BL-1a and BL-2a, and comprises transistors T1a and T2a. The comparative bitlines BL-1 and BL-2 are
30 electrically coupled with circuitry 4 of the type described above with reference to FIG. 1 for comparing electrical properties of the comparative bitlines one another, and similarly the comparative bitlines BL-1a and BL-2a are electrically coupled with circuitry 4a for comparing electrical properties of the comparative bitlines one another. Circuitry 4 and 4a, each serving as a sense amplifier, may be in any suitable location relative to array 10,

and may, for example, be between array 10 and base 15, laterally offset from array 10, etc. Circuitry 4 and 4a may be further incorporated into the base 15 as a sense amplifier together with other electrical circuits that may be used to access to the array 10 to read or write data from or into the array 10. In applications in which an interlayer insulating film
5 intervenes between the array 10 and the base 15, a plurality of vias may be formed in the interlayer insulating film to electrically connect wordlines WL and bitlines BL of the array 10 to the circuits, such as the sense amplifiers 4 and 4a, that may be formed in the base 15.

In the illustrated embodiment the comparative bitlines BL-1 and BL-2 of memory
10 cell 12 are laterally displaced relative to one another, and similarly the transistors T1 and T2 are laterally displaced relative to one another. The transistors T1 and T2 are shown to be in a common horizontal plane as one another (i.e., are horizontally aligned with one another), but in other embodiments may be vertically offset relative to one another.

The transistors T1 and T2 comprise gates 14 and 16; and similarly the transistors
15 T1a and T2a comprise gates 14a and 16a. The memory cells 12 and 12a are in a common row as one another within the memory array, and accordingly a wordline (WL) extends across all of the transistors T1, T1a, T2 and T2a, and comprises the gates of such transistors. The wordline and the bitlines may comprise any suitable electrically conductive material, including, for example, one or more of various metals (e.g.,
20 tungsten, titanium, etc.), metal-containing compositions (e.g., metal nitride, metal carbide, metal silicide, etc.), conductively-doped semiconductor materials (e.g., conductively-doped silicon, conductively-doped germanium, etc.), etc. The wordline and bitlines may comprise the same composition as one another, or may comprise different compositions relative to one another.

25 Semiconductor pillars 18 and 20 extend upwardly from the comparative bitlines BL-1 and BL-2. Such semiconductor pillars may comprise any suitable semiconductor materials including, for example, one or both of silicon and germanium. Similar semiconductor pillars18a and 20a extend upwardly from the comparative bitlines BL-1a and BL-2a.

30 The transistor gate 14 is spaced from the semiconductor pillar 18 by gate dielectric material 22, and the transistor gate 16 is spaced from the semiconductor pillar 20 by gate dielectric material 24. The gate dielectric materials 22 and 24 may comprise any suitable compositions or combinations of compositions; including, for example,

silicon dioxide, silicon nitride, high-K dielectric material, ferroelectric material, etc. Analogous gate dielectric materials 22a and 24a are within the transistors T1a and T2a.

The transistor T1 comprises a channel region 26 within semiconductor material of pillar 18, and comprises source/drain regions 28 and 30 on opposing sides of the
5 channel region. The source/drain regions and channel region may be doped with any suitable dopants. In some embodiments the source/drain regions may be n-type majority doped, and in other embodiments may be p-type majority doped.

The transistor T2 comprises a channel region 32 within semiconductor material of pillar 20, and comprises source/drain regions 34 and 36 on opposing sides of the
10 channel region. In some embodiments the source/drain regions 28 and 30 may be referred to as first and second source/drain regions, respectively; and the source/drain regions 34 and 36 may be referred to as third and fourth source/drain regions, respectively.

The transistors T1a and T2a comprise source/drain regions (28a/30a/34a/36a) and
15 channel regions (26a/32a) analogous those described with reference to transistors T1 and T2.

Memory cell 12 comprises a capacitor 38 which is vertically displaced relative to transistors T1 and T2, and in the illustrated embodiment is over the transistors T1 and T2. The capacitor comprises an outer node (or first node) 40, an inner node (or second
20 node) 42, and capacitor dielectric material 44 between the inner and outer nodes. In the shown embodiment the outer node 40 is container-shaped, and the inner node 42 and capacitor dielectric material 44 extend into the container-shaped outer node. In other embodiments the outer node may have a different configuration (e.g., a planar configuration).

25 The inner and outer nodes 40 and 42 may comprise any suitable electrically conductive compositions or combinations of electrically conductive compositions; including, for example, one or more of various metals (e.g., tungsten, titanium, etc.), metal-containing materials (for instance, metal nitride, metal silicide, metal carbide, etc.), conductively-doped semiconductor materials (for instance, conductively-doped
30 silicon, conductively-doped germanium, etc.), etc. The inner and outer nodes 40 and 42 may comprise the same composition as one another in some embodiments, and in other embodiments may comprise different compositions relative to one another.

The capacitor dielectric material 44 may comprise any suitable composition or combination of compositions. In some embodiments, the capacitor dielectric material

may comprise non-ferroelectric material and may, for example, consist of one or more of silicon dioxide, silicon nitride, aluminum oxide, hafnium oxide, zirconium oxide, etc. In some embodiments the capacitor dielectric material may comprise ferroelectric material. For instance, the capacitor dielectric material may comprise, consist essentially of, or
5 consist of one or more materials selected from the group consisting of transition metal oxide, zirconium, zirconium oxide, hafnium, hafnium oxide, lead zirconium titanate, tantalum oxide, and barium strontium titanate; and having dopant therein which comprises one or more of silicon, aluminum, lanthanum, yttrium, erbium, calcium, magnesium, niobium, strontium, and a rare earth element.

10 In the shown embodiment the outer electrode 40 is electrically coupled with the first source/drain region 28 of transistor T1, and the inner electrode 42 is electrically coupled with the third source/drain region 34 of transistor T2. The second source/drain region 30 of transistor T1 is electrically coupled with comparative bitline BL-1 and the fourth source/drain region 36 of transistor T2 is electrically coupled with comparative
15 bitline BL-2. The capacitor 38, together with transistors T1 and T2, and comparative bitlines BL-1 and BL-2, forms a 2T-1C memory cell of the type described above with reference to FIG. 1.

The inner electrode 42 is shown having a single homogenous composition that extends from inside of the container-shaped outer electrode 40 to outside of the
20 container-shaped outer electrode and into electrical contact with source/drain region 34. In other embodiments at least some of the illustrated portion of the inner electrode 42 outside of the container-shaped outer electrode 40 may be replaced with an electrically conductive interconnect which may or may not have a same composition as the inner electrode 42.

25 The memory cell 12a comprises a capacitor 38a analogous to the capacitor 30 of memory cell 12 (with capacitor 38a comprising a first node 40a, a second node 42a and capacitor dielectric material 44a), and also comprises a 2T-1C memory cell of the type described above with reference to FIG. 1.

Insulative material 48 is shown to surround the various components of memory
30 cells 12 and 12a. Such insulative material may comprise any suitable composition or combination of compositions; including, for example, one or more of silicon dioxide, silicon nitride, borophosphosilicate glass, spin-on dielectric, etc. Although insulative material 48 is shown as a single homogeneous material, in other embodiments the insulative material may include two or more discrete insulative compositions.

FIG. 3 is a top view of a region of memory array 10 showing an example embodiment relationship between a series of wordlines (WL) and comparative bitlines (BL-1, BL-2, BL-1a and BL-2a). The cross-section of FIG. 2 is along the line 2-2 of FIG. 3.

5 In some embodiments configurations analogous to that of FIGS. 2 and 3 may be incorporated into stacked memory array tiers. In such embodiments a second tier may be over a first tier and inverted such that comparative bitlines may be shared between the tiers. FIG. 4 shows a region of an example arrangement 50 of stacked memory array tiers, with a second tier 54 being over a first tier 52.

10 The first tier 52 comprises memory cells 12 and 12a of the type described in FIGS. 2 and 3. The second tier 54 comprises similar memory cells 12b and 12c, except that the second memory cells are inverted relative to the first memory cells. The memory cell 12b comprises first and second transistors T1b and T2b, and the memory cell 12c comprises first and second transistors T1c and T2c. The memory cells 12b and 12c 15 comprise capacitors 38b and 38c, respectively. The wordline extending across the memory cells 12 and 12a is labeled as a first wordline (WL1), and the wordline across the memory cells 12b and 12c is labeled as a second wordline (WL2).

In some embodiments an axis 53 through the comparative bitlines BL-1, BL-2, BL-1a and BL-2a may be considered to define a mirror plane and the memory cells 12b 20 and 12c may be considered to be substantially mirror images of the memory cells 12 and 12a, respectively, across the mirror plane. The term “substantially mirror images” is utilized to indicate that the indicated cells may be mirror images of one another to within reasonable tolerances of fabrication and measurement.

In some embodiments the configuration of FIGS. 2 and 3 may be considered to 25 comprise memory cells within $4F^2$ architecture, and the configuration of FIG. 4 may be considered to comprise memory cells within $8F^2$ architecture.

The embodiment of FIG. 2 shows comparative bitlines BL-1 and BL-2 within a common horizontal plane as one another (i.e., are horizontally aligned with one another). In other embodiments, the comparative bitlines BL-1 and BL-2 may be vertically 30 displaced relative to one another, as described with reference to FIGS. 5-7.

Referring to FIG. 5, a memory array 100 comprises adjacent memory cells 12 and 12a. The memory cells 12 and 12a of memory array 100 are similar to the memory cells 12 and 12a of the memory array 10 discussed above with reference to FIG. 2, except that the second comparative bitlines BL-2/BL-2a are vertically displaced relative to the first

comparative bitlines BL-1/BL-1a in the configuration of FIG. 5. In contrast, the first and second comparative bitlines are not vertically displaced relative to one another in the configuration of FIG. 2.

The configuration of FIG. 5 may be formed with any suitable method. In some embodiments the configuration of FIG. 5 may be formed by including insulative subcomponents of material 48 having first surfaces 49 and second surfaces 51, with first surfaces 49 being above second surfaces 51. Such subcomponents of material 48 may correspond to one or more insulative films in some embodiments.

In the illustrated embodiment of FIG. 5, the second comparative bitlines BL-2/BL-2a are deeper than the first comparative bitlines BL-1/BL-1a, and accordingly pedestals 20/20a are longer than pedestals 18/18a within memory cells 12/12a. In such embodiment, the distance between second comparative bitlines BL-2/BL-2a and the channel regions 32/32a of transistors T2/T2a is lengthened relative to the embodiment of FIG. 2, resulting in the lengthening of the source/drain regions 36/36a of transistors T2/T2a. In some embodiments electrically conductive interconnects (not shown) may be provided along upper surfaces of BL-2/BL-2a to reduce the length of the source/drain regions 36/36a.

The first comparative bitlines BL-1/BL-1a are entirely laterally displaced relative to the second comparative bitlines BL-2/BL-2a for each of the memory cells 12/12a in the embodiment of FIG. 5. FIG. 6 shows an alternative embodiment in which the comparative bitlines BL-1 and BL-2 laterally overlap one another. In the illustrated embodiment of FIG. 6, the pedestal 20 is laterally offset from a center of comparative bitline BL-2. In other embodiments the pedestal 20 may extend to the central region of BL-2 even though the comparative bitlines BL-1 and BL-2 laterally overlap. In yet other embodiments the pedestal 18 may be laterally offset from a center of comparative bitline BL-1 in addition to, or alternatively to, the pedestal 20 being offset from the center of comparative bitline BL-2. The lateral overlap of the comparative bitlines BL-1 and BL-2 in the embodiment of FIG. 6 may provide larger landing pads for the pedestals 18 and 20 which may better compensate for mask misalignment as compared to embodiments having smaller dimensions of the comparative bitlines. Example surfaces 49 and 51 are diagrammatically illustrated in FIG. 6 to illustrate an example method of forming the construction of FIG. 6 through utilization of subcomponents of insulative material 48 having upper surfaces 49 and 51.

FIG. 7 shows a region of an example embodiment memory array 150 with stacked memory cells. Specifically, the array 150 comprises memory cells 12 and 12a-g; with memory cells 12b, 12, 12f and 12d (i.e., cell-1, cell-2, cell-3 and cell-4) being in a first vertical stack, and memory cells 12c, 12a, 12g and 12e (i.e., cell-5, cell-6, cell-7 and
5 cell-8) being in a second vertical stack. The memory cells of the first vertical stack are electrically coupled with a first set of comparative bitlines (i.e.., comparative bitlines BL-1, BL-2, BL-1b and BL-2b); and the memory cells of the second vertical stack are electrically coupled with a second set of comparative bitlines (i.e., comparative bitlines BL-1a, BL-2a, BL-1c and BL-2c). First sensing amplifier circuitry 4 is electrically
10 coupled with the first set of comparative bitlines, and second sensing amplifier circuitry 4a is electrically coupled with the second set of comparative bitlines.

Wordlines WL-1, WL-2, WL-3 and WL-4 extend along rows of the memory array 150.

The embodiments of FIGS. 2-7 have the transistors (e.g., T1 and T2) laterally
15 offset from one another, and the capacitor (e.g., 38 of FIG. 2) provided above (or below) both of such transistors. In other embodiments, the two transistors of a 2T-1C memory cell may be vertically offset relative to one another, and the capacitor may be provided vertically between such transistors. FIG. 8 shows a portion of a memory array 200 illustrating an example embodiment in which the capacitors of 2T-1C memory cells are
20 provided between vertically displaced transistors.

The illustrated region of memory array 200 comprises comparative bitlines BL-1 and BL-2, with such comparative bitlines being vertically offset relative to another and connected to circuitry 4. A pair of adjacent memory cells 12 and 12a are shown, with such adjacent memory cells being in a common column as one another within the
25 memory array (i.e., being along a common bitline, with such bitline being comprised by the comparative bitlines BL-1 and BL-2 in combination). Such is in contrast to the embodiments of FIGS. 2, 4 and 5 in which the adjacent memory cells 12 and 12a are in a common row as one another (i.e., are along a common wordline). In some embodiments the memory cells 12 and 12a may be referred to as substantially identical memory cells
30 along a column of a memory array, with the term “substantially identical” meaning that the memory cells are identical to one another within reasonable tolerances of fabrication and measurement.

The lower comparative bitline (BL-2) is shown to be over and supported by a base 15. Such base may be a semiconductor substrate of the type described above with reference to FIG. 2.

The memory cell 12 comprises transistors T1 and T2, with such transistors being along a first wordline WL1. The adjacent memory cell 12a comprises transistors T1a and T2a, with such transistors being along a second wordline WL2.

A capacitor 38 is vertically between the transistors T1 and T2 of memory cell 12, and a similar capacitor 38a is vertically between the transistors T1a and T2a of memory cell 12a.

The capacitors comprise first nodes 40/40a, second nodes 42/42a and capacitor dielectric material 44/44a. Although the first nodes 40/40a are shown to be container-shaped and the second nodes 42/42a are shown to extend within such container shapes, in other embodiments the first and second nodes may have other configurations. For instance, the first and second nodes may have planar configurations. In the illustrated configuration the first nodes 40/40a may be referred to as outer nodes and the second nodes 42/42a may be referred to as inner nodes.

The pillars 18/18a extend from comparative bitline BL-1 to the outer nodes 40/40a of capacitors 38/38a, and the pillars 20/20a extend from the comparative bitline BL-2 to the inner nodes 42/42a of capacitors 38/38a.

The transistors T1/T1a have first source/drain regions 28/28a extending to the outer nodes 40/40a of capacitors 38/38a, and have second source/drain regions 30/30a extending to the comparative bitline BL-1. The transistors T1/T1a also have channel regions 26/26a between the first and second source/drain regions. Gates 14/14a are along the channel regions and offset from the channel regions by gate dielectric materials 22/22a.

The transistors T2/T2a have third source/drain regions 34/34a extending to the inner nodes 42/42a of capacitors 38/38a, and have fourth source/drain regions 36/36a extending to the comparative bitline BL-2. The transistors T2/T2a also have channel regions 32/32a between the third and fourth source/drain regions. Gates 16/16a are along the channel regions and offset from the channel regions by gate dielectric materials 24/24a.

The embodiment of FIG. 8 advantageously enables the transistors and capacitor of a 2T-1C memory cell to all be vertically stacked, which may enable the memory cells to be packed to high levels of integration.

Although the illustrated embodiment of FIG. 8 comprises a configuration with BL-2 over a supporting substrate 15 and BL-1 over BL-2, in other embodiments the relative orientations of BL-2 and BL-1 could be reversed so that BL-1 is over the supporting substrate and BL-2 is over BL-1. In such other embodiments the illustrated capacitors 38/38a would be inverted relative to the shown configuration and accordingly container-shaped outer nodes 40 would open upwardly instead of downwardly.

An advantage of various embodiments of memory arrays described above with reference to FIGS. 2-8 is that such embodiments may have symmetric layouts relative to the comparative bitlines (e.g., BL-1 and BL-2) extending throughout the memory arrays, and such may reduce resistance/signal mismatches between the comparative bitlines as compared to less symmetric layouts.

The illustrated capacitors in the above-described embodiments may be replaced with other capacitive units in other embodiments. For instance, any of the capacitors may be replaced with a capacitive unit having two or more capacitors in combination.

The transistors T1 and T2 of the above-described embodiments of FIGS. 2-8 may comprise any suitable configurations. For instance, in the illustrated embodiment the transistors are field effect transistors, but in other embodiments other suitable transistors may be substituted for one or more of the transistors T1 and T2; with bipolar junction transistors being an example of a transistor configuration which may be used alternatively to field effect transistors. The field effect transistors described herein may utilize gate dielectric material comprising non-ferroelectric material and/or ferroelectric material depending on the application. The gates of the transistors may have any of numerous configurations, with some example configurations being described with reference to FIGS. 9-13. The figures specifically pertain to the T1 transistor gates, but in other embodiments analogous configurations may be utilized for the T2 transistor gates.

Referring to FIG. 9, the T1 transistor gate 14 is shown in a configuration of the type utilized in the embodiments of FIGS. 2 and 4-8. Specifically, the transistor gate is a block of uniform width, with such width being approximately equal to a length “L” of the channel region 26. In contrast, each of the embodiments of FIGS. 10-13 has the gate narrower than the length of the channel region, and has at least one extension region 90 that extends from the gate and along the channel region. Further, each of the embodiments of FIGS. 10-13 has at least one bent region 92 where the gate 14 joins to an extension region. The embodiment of FIG. 10 shows the gate 14 and extension regions 90 forming a substantially T-shaped configuration, the embodiment of FIG. 11

shows the extension region 90 and gate 14 together forming a substantially U-shaped configuration, and the embodiments of FIGS. 12 and 13 show the gate 14 and extension regions 90 forming substantially shelf-shaped configurations (with FIG. 13 showing the gate 14 as a top shelf over extension regions 90 and FIG. 12 showing the gate 14 as a
5 bottom shelf beneath regions 90).

Advantages of the embodiments of FIGS. 10-13 relative to that of FIG. 9 may include reduced gate resistance and associated reduced current requirements for desired access drive parameters.

The structures and architectures described above may be incorporated into
10 memory (e.g., DRAM, SRAM, etc.) and/or otherwise may be utilized in electronic systems. Such electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

Unless specified otherwise, the various materials, substances, compositions, etc.
15 described herein may be formed with any suitable methodologies, either now known or yet to be developed, including, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

Both of the terms “dielectric” and “electrically insulative” may be utilized to describe materials having insulative electrical properties. The terms are considered
20 synonymous in this disclosure. The utilization of the term “dielectric” in some instances, and the term “electrically insulative” in other instances, may be to provide language variation within this disclosure to simplify antecedent basis within the claims that follow, and is not utilized to indicate any significant chemical or electrical differences.

The particular orientation of the various embodiments in the drawings is for
25 illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings or are rotated relative to such orientation.

30 The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

When a structure is referred to above as being "on" or “against” another structure, it can be directly on the other structure or intervening structures may also be present. In

contrast, when a structure is referred to as being "directly on" or “directly against” another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when
5 a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

Some embodiments include a memory cell having first and second transistors, and a capacitor vertically displaced relative to the first and second transistors. The capacitor has a first node electrically coupled with a source/drain region of the first
10 transistor, a second node electrically coupled with a source/drain region of the second transistor, and capacitor dielectric material between the first and second nodes.

Some embodiments include a memory cell having first and second transistors laterally displaced relative to one another, and a capacitor over the first and second transistors. The capacitor has an outer node electrically coupled with a source/drain
15 region of the first transistor, an inner node electrically coupled with a source/drain region of the second transistor, and capacitor dielectric material between the inner and outer nodes.

Some embodiments include a memory cell having first and second transistors vertically displaced relative to one another, and a capacitor between the first and second
20 transistors. The capacitor has a first node electrically coupled with a source/drain region of the first transistor, a second node electrically coupled with a source/drain region of the second transistor, and capacitor dielectric material between the first and second nodes.

Some embodiments includes an apparatus comprising a semiconductor base, a memory array including a plurality of memory cells, and an insulating film intervening
25 between the semiconductor base and the plurality of memory cells. Each of the memory cells comprises a first transistor, a second transistor and a capacitor, and each of the first transistor, the second transistor and the capacitor is over the insulating film covering the semiconductor base..

CLAIMS

I/we claim,

1. A memory cell, comprising:

first and second transistors; and

5 a capacitor vertically displaced relative to the first and second transistors, the capacitor having a first node electrically coupled with a source/drain region of the first transistor, having a second node electrically coupled with a source/drain region of the second transistor, and having capacitor dielectric material between the first and second nodes.

10 2. The memory cell of claim 1 wherein the first and second transistors are in a common horizontal plane as one another.

3. The memory cell of claim 1 wherein the first and second transistors are not in a common horizontal plane as one another.

4. The memory cell of claim 1 wherein:

15 the first transistor has a first source/drain region and a second source/drain region, and the first node is electrically coupled with the first source/drain region;

the second transistor has a third source/drain region and a fourth source/drain region, and the second node is electrically coupled with the third source/drain region; and

20 the second and fourth source/drain regions are electrically coupled with first and second comparative bitlines, respectively.

5. The memory cell of claim 1 wherein at least one of the first and second transistors has a gate configured to have at least one bent region, and one or more extension regions that extend along a channel region of said at least one of the first and 25 second transistors from said at least one bent region; and wherein the gate and the one or more extension regions together form a substantially T-shaped configuration, substantially shelf-shaped configuration or substantially U-shaped configuration.

6. A memory cell comprising:

first and second transistors laterally displaced relative to one another; and

a capacitor over the first and second transistors, the capacitor having an outer node electrically coupled with a source/drain region of the first transistor, having
5 an inner node electrically coupled with a source/drain region of the second transistor, and having capacitor dielectric material between the inner and outer nodes.

7. The memory cell of claim 6 wherein the outer node is container-shaped; wherein the inner node extends into the container-shaped outer node over the first transistor; and wherein a portion of the inner node extends outwardly of the container-
10 shaped outer node, and extends to the source/drain region of the second transistor.

8. The memory cell of claim 6 wherein the first and second transistors are in a common horizontal plane, and wherein a common wordline extends to both of the first and second transistors and comprises gates of the first and second transistors.

9. The memory cell of claim 6 wherein:
15 the first transistor has a first source/drain region and a second source/drain region, and the outer node is electrically coupled with the first source/drain region;

the second transistor has a third source/drain region and a fourth source/drain region, and the inner node is electrically coupled with the third source/drain region; and
20 the second and fourth source/drain regions are electrically coupled with first and second comparative bitlines, respectively.

10. The memory cell of claim 9 wherein the first and second comparative bitlines are in a common horizontal plane as one another.

11. A memory array comprising the memory cell of claim 10 as one memory
25 cell within a plurality of memory cells; wherein

an axis through the first and second comparative bitlines defines a mirror plane; and

another memory cell is on an opposing side of the mirror plane from said one memory cell and is substantially a mirror image of said one memory cell across the
30 mirror plane; said other memory cell sharing the first and second comparative bitlines with said one memory cell.

12. The memory cell of claim 9 wherein the first and second comparative bitlines are vertically displaced relative to one another.

13. The memory cell of claim 12 wherein the first and second comparative bitlines laterally overlap one another.

5 14. The memory cell of claim 12 wherein the first and second comparative bitlines do not laterally overlap one another.

15. A memory cell comprising:

first and second transistors vertically displaced relative to one another; and

10 a capacitor between the first and second transistors, the capacitor having a first node electrically coupled with a source/drain region of the first transistor, having a second node electrically coupled with a source/drain region of the second transistor, and having capacitor dielectric material between the first and second nodes.

16. The memory cell of claim 15 wherein the first node is container-shaped
15 and the second node extends into the first node, and wherein the first transistor is above the second transistor which in turn is above a semiconductor base.

17. The memory cell of claim 15 wherein the first node is container-shaped and the second node extends into the first node, and wherein the second transistor is above the first transistor which in turn is above a semiconductor base.

20 18. The memory cell of claim 15 wherein:

the first transistor has a first source/drain region and a second source/drain region, and the first node is electrically coupled with the first source/drain region;

the second transistor has a third source/drain region and a fourth source/drain region, and the second node is electrically coupled with the third
25 source/drain region; and

the second and fourth source/drain regions are electrically coupled with first and second comparative bitlines, respectively.

19. The memory cell of claim 18 wherein the first comparative bitline is above the first transistor and the second comparative bitline is below the second
30 transistor.

20. The memory cell of claim 19 being in a memory array; the first and second comparative bitlines being along a column of said memory array; the memory cell being one of a plurality of substantially identical memory cells between the first and second comparative bitlines along said column.

5 21. An apparatus comprising a semiconductor base, a memory array including a plurality of memory cells, and an insulating film intervening between the semiconductor base and the plurality of memory cells;

wherein each of the memory cells comprises a first transistor, a second transistor and a capacitor; and

10 wherein each of the first transistor, the second transistor and the capacitor is formed over the insulating film covering the semiconductor base.

22. The apparatus of claim 21,

wherein the memory array further includes a plurality of pairs of bitlines and a plurality of wordlines, each of the memory cells being coupled to an associated one 15 of the plurality of pairs of bitlines and an associated one of the plurality of wordlines, the first and second transistors and the capacitor being coupled in series between the associated one of the plurality of pairs of bitlines with the first and second transistors sandwiching the capacitor therebetween, and each of the first and second transistors being at a gate to the associated one of the plurality of wordlines.

20 23. The apparatus of claim 22,

wherein the associated one of the plurality of pairs of bitlines includes first and second bitlines;

wherein the insulating film includes a substantially planar surface; and

wherein the first and second bitlines are disposed on the substantially 25 planar surface in parallel to each other.

24. The apparatus of claim 22,

wherein the associated one of the plurality of pairs of bitlines includes first and second bitlines;

wherein the insulating film includes a first surface and a second surface 30 that is different in height from the first surface; and

wherein the first and second bitlines are on the first and second surfaces, respectively.

25. The apparatus of claim 24, wherein the first and second bitlines are formed such that respective portions of the first and second bitlines overlap with each other.

26. The apparatus of claim 22,

5 wherein each of the memory cells comprises the first and second semiconductor pillars extending vertically over the insulating film, the first semiconductor pillar including first and second portions serving as source and drain regions of the first transistor, respectively, and the second semiconductor pillar including third and fourth portions serving as source and drain regions of the second transistor,

10 respectively.

27. The apparatus of claim 26,

wherein the associated one of the plurality of pairs of bitlines includes a first bitline and a second bitline, the first and second bitlines being laterally disposed with each other; and

15 wherein the first and second semiconductor pillars are disposed over the first and second bitlines, respectively.

28. The apparatus of claim 26,

wherein the associated one of the plurality of pairs of bitlines includes a first bitline and a second bitline formed over the first bitline; and

20 wherein the first and second semiconductor pillars are vertically aligned with each other between the first and second bitlines.

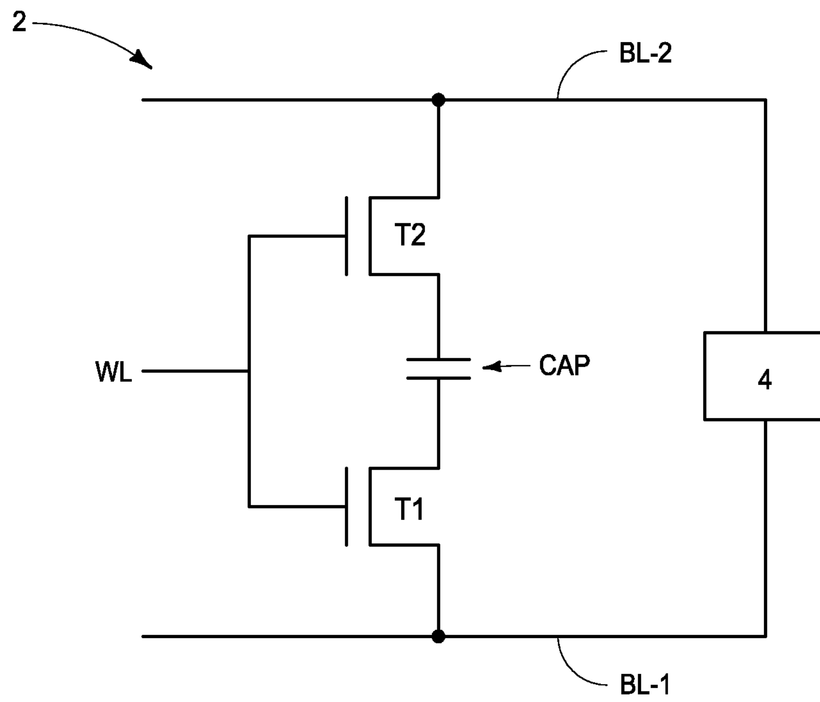

FIG. 1
(PRIOR ART)

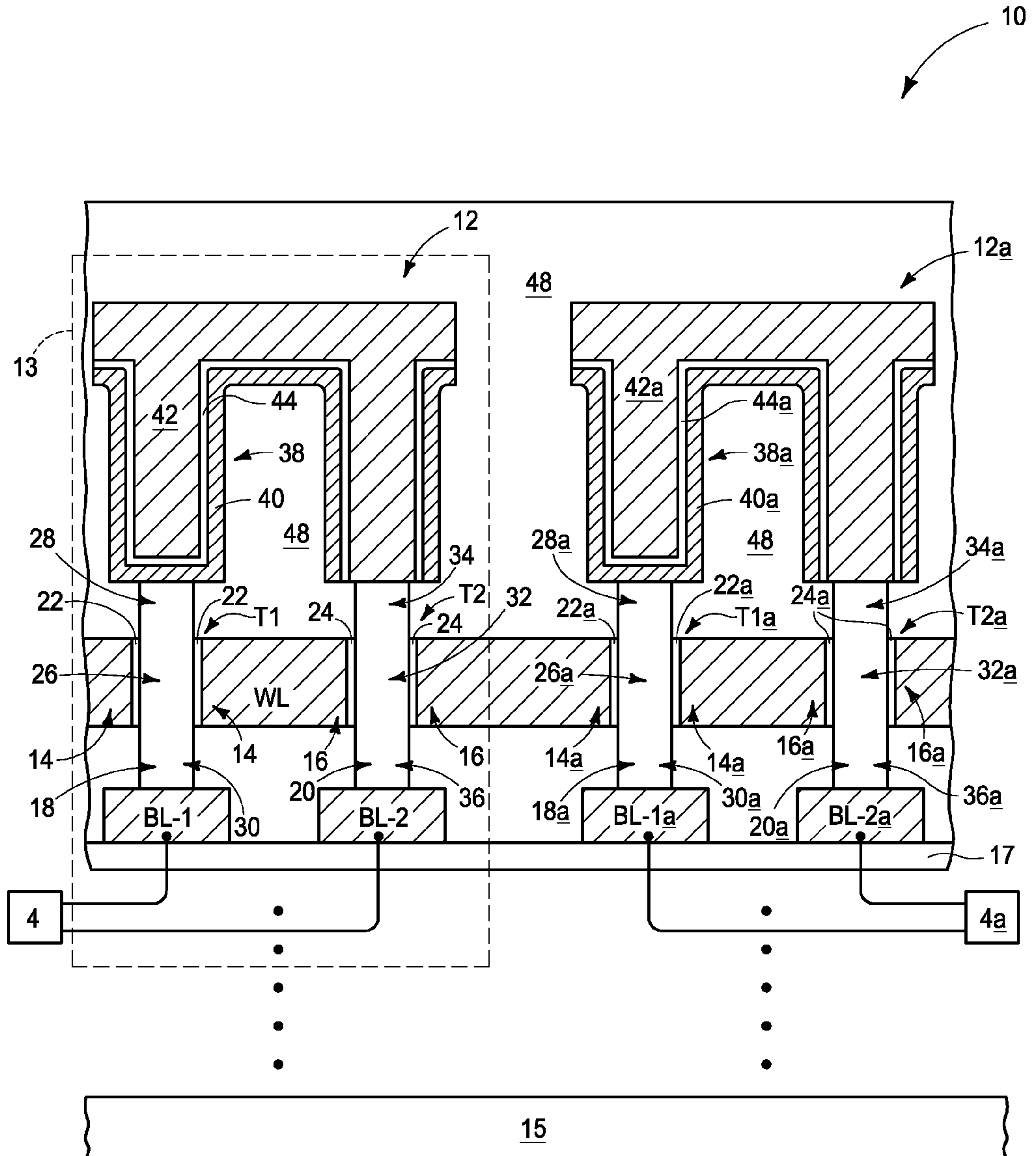

FIG. 2

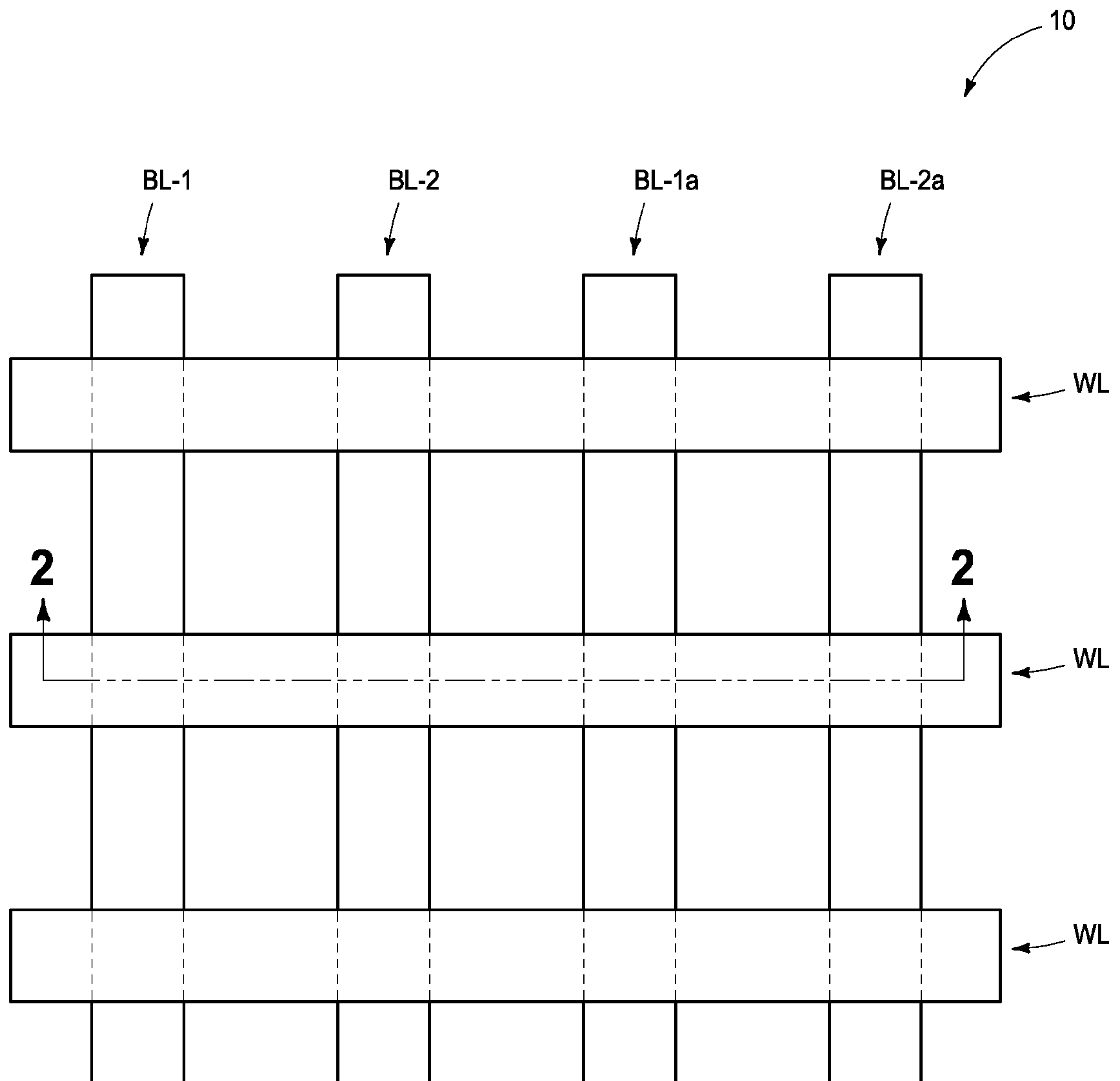

FIG. 3

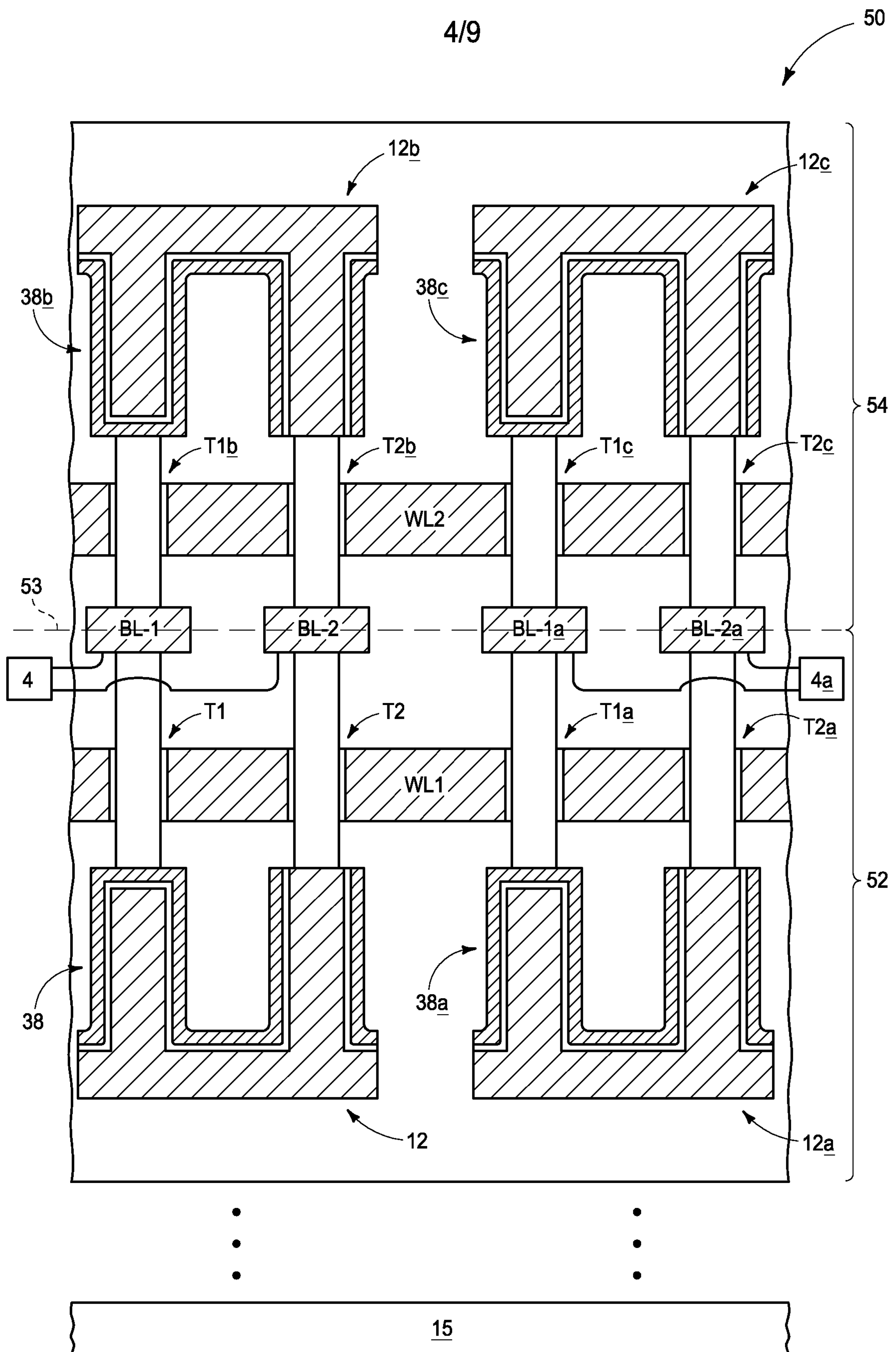

FIG. 4

FIG. 5

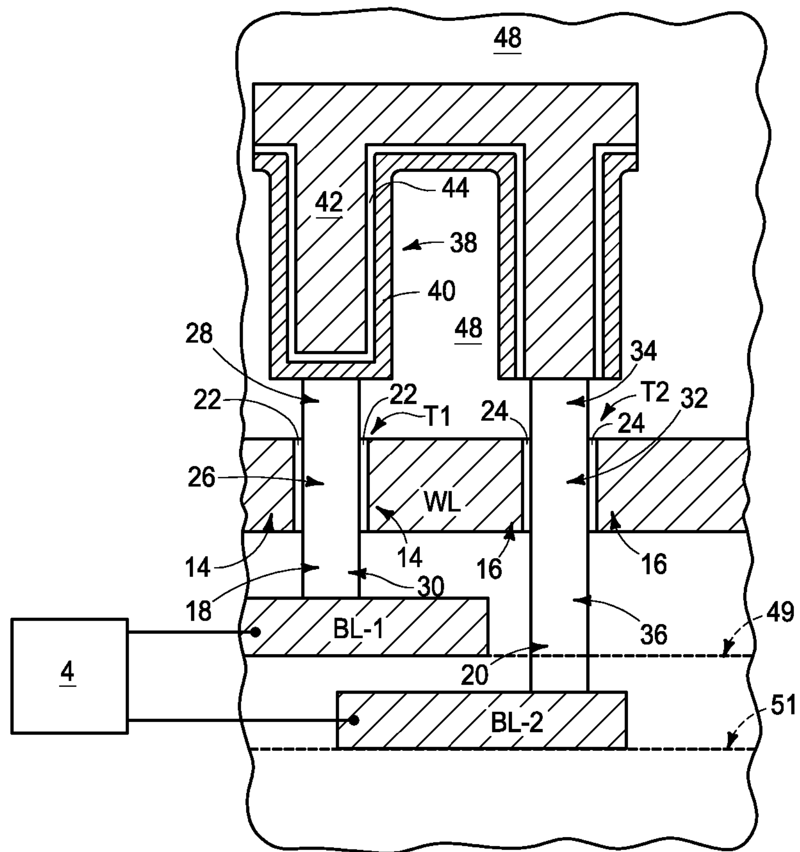

FIG. 6

12b
12c
150
cell-1
cell-5
WL-2
cell-6
BL-1 BL-2 BL-1a BL-2a
WL-1
cell-2
12a
12
cell-7
12g
12f
cell-3
WL-4
BL-1b BL-2b BL-1c BL-2c
WL-3
cell-4
cell-8
4
4a
12d
12e

FIG. 7

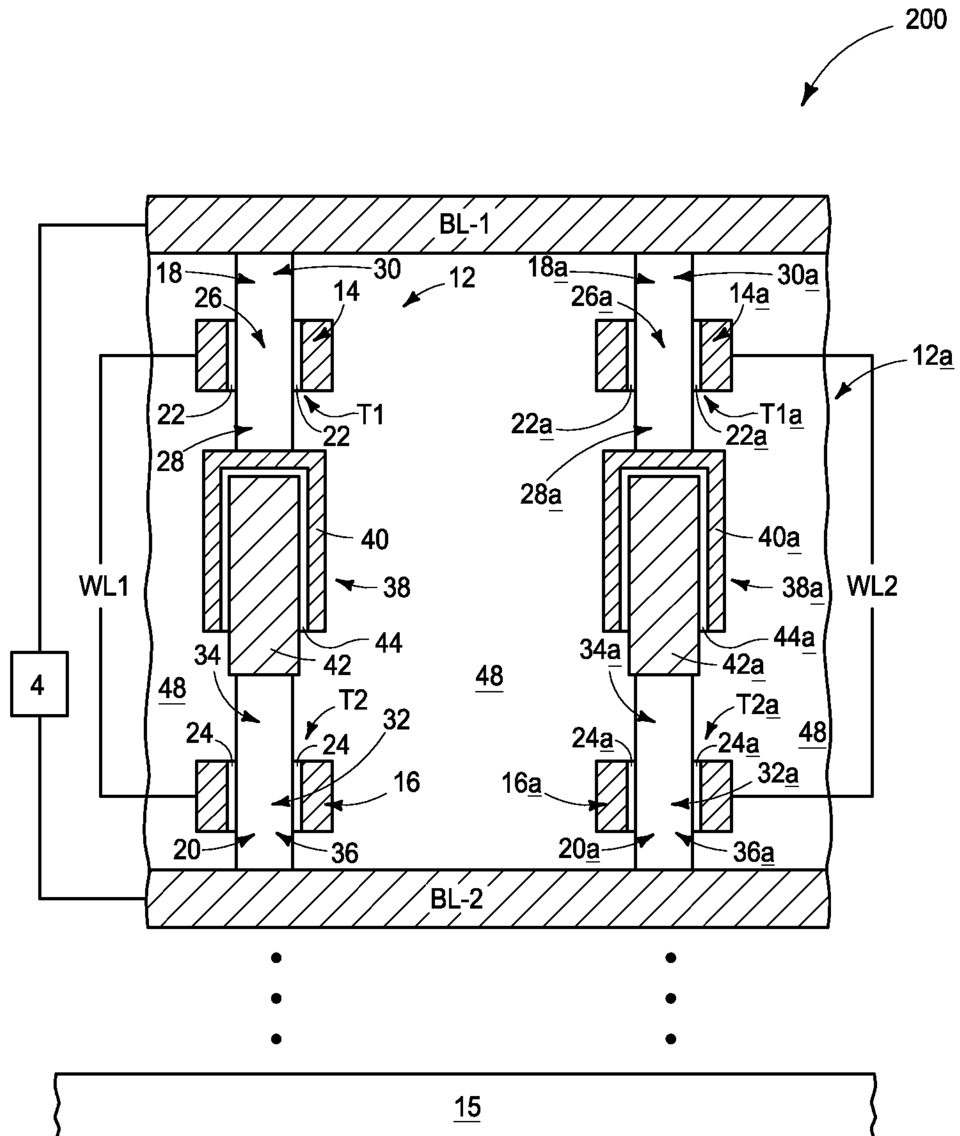

FIG. 8

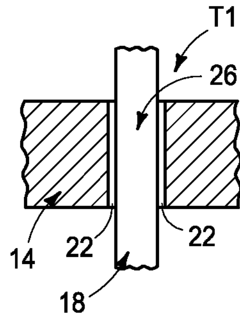

FIG. 9

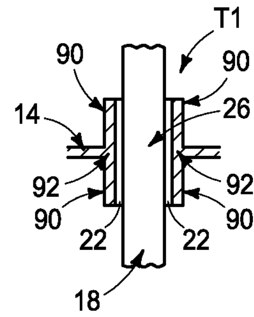

FIG. 10

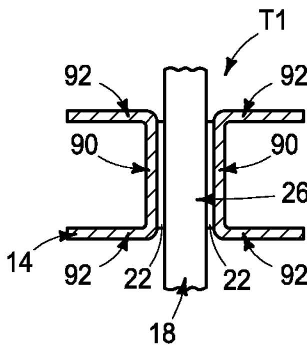

FIG. 11

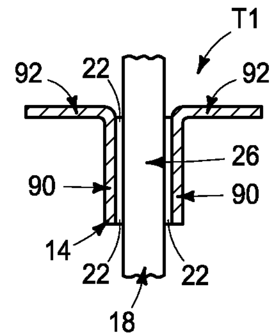

FIG. 12

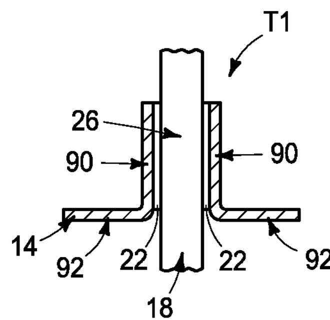

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/044638

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/108(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/108; G11C 15/00; H01L 21/20; G11C 7/00; G11C 5/06; H01L 21/8242; G11C 5/02; H01L 21/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: capacitor, memory, cell, source, second, transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5571743 A (WALTER H. HENKELS et al.) 05 November 1996 See columns 3-4, claim 1 and figures 1-3.	1-10,12-14,21-28
Y		11,15-20
Y	US 2004-0062101 A1 (KENJI KASUGA) 01 April 2004 See claims 17, 20 and figures 4-7.	11
Y	US 5299155 A (MASAHIKO YANAGI) 29 March 1994 See claim 1 and figures 1-2(c).	15-20
A	US 2003-0087499 A1 (RICHARD H. LANE et al.) 08 May 2003 See claims 1-5 and figures 1-15.	1-28
A	US 6563727 B1 (ALAN ROTH et al.) 13 May 2003 See claims 1-3 and figures 1-4.	1-28

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 November 2017 (15.11.2017)	**15 November 2017 (15.11.2017)**

Name and mailing address of the ISA/KR

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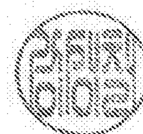
KANG, Sung Chul



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/044638

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