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Levine et al.

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[54] **ELECTRONIC TIMEPIECE**

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[52] **U.S. Cl.** ..... **58/50 R,** 58/23 A, 58/23 BA, 58/85.5

[51] **Int. Cl.** **G04b 19/30,** G04b 27/00

[58] **Field of Search** ..... 58/23 A, 23 R, 23 C, 58/23 AC, 23 BA, 50 R, 85.5; 340/309.4

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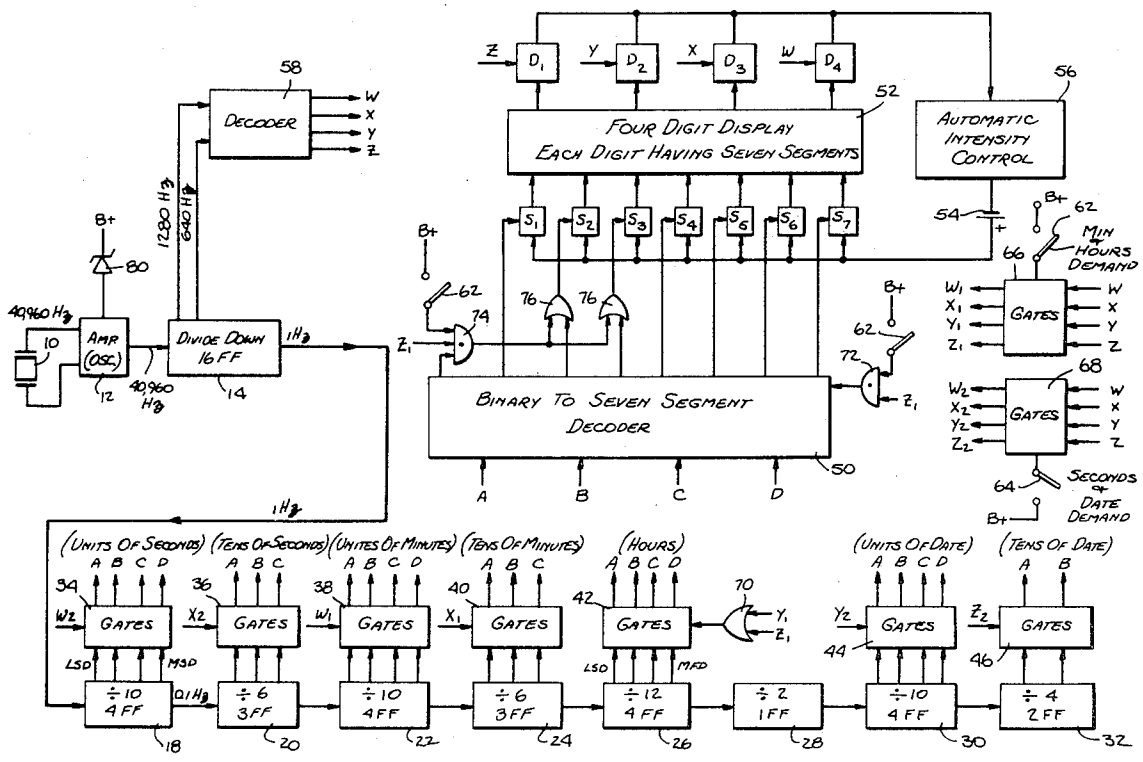
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[57] **ABSTRACT**

An all electronic direct digital read-out timepiece employing a matrix of light emitting diodes which are user actuated to provide a display of the time in response to their actuation. A first demand switch provides a display of hours and minutes. A second demand switch provides a display of time in seconds using the same light emitting diodes as are used for the first display. When the display is turned on, it cycles through three levels of light intensity each lasting a predetermined time period of approximately one second after which the display automatically turns off. The time is set through the actuation of a single time setting switch in addition to the display demand switch. Through successive manipulations of the display demand switch, the time may be set at any predetermined value in advance of the real time, time keeping may be suspended until the real time catches up with the time set, and when the time set is coincident with real time time keeping may be reinstated. The design of the system provides for minimum current drain so that a small watch having reasonable battery life is provided.

15 Claims, 3 Drawing Figures



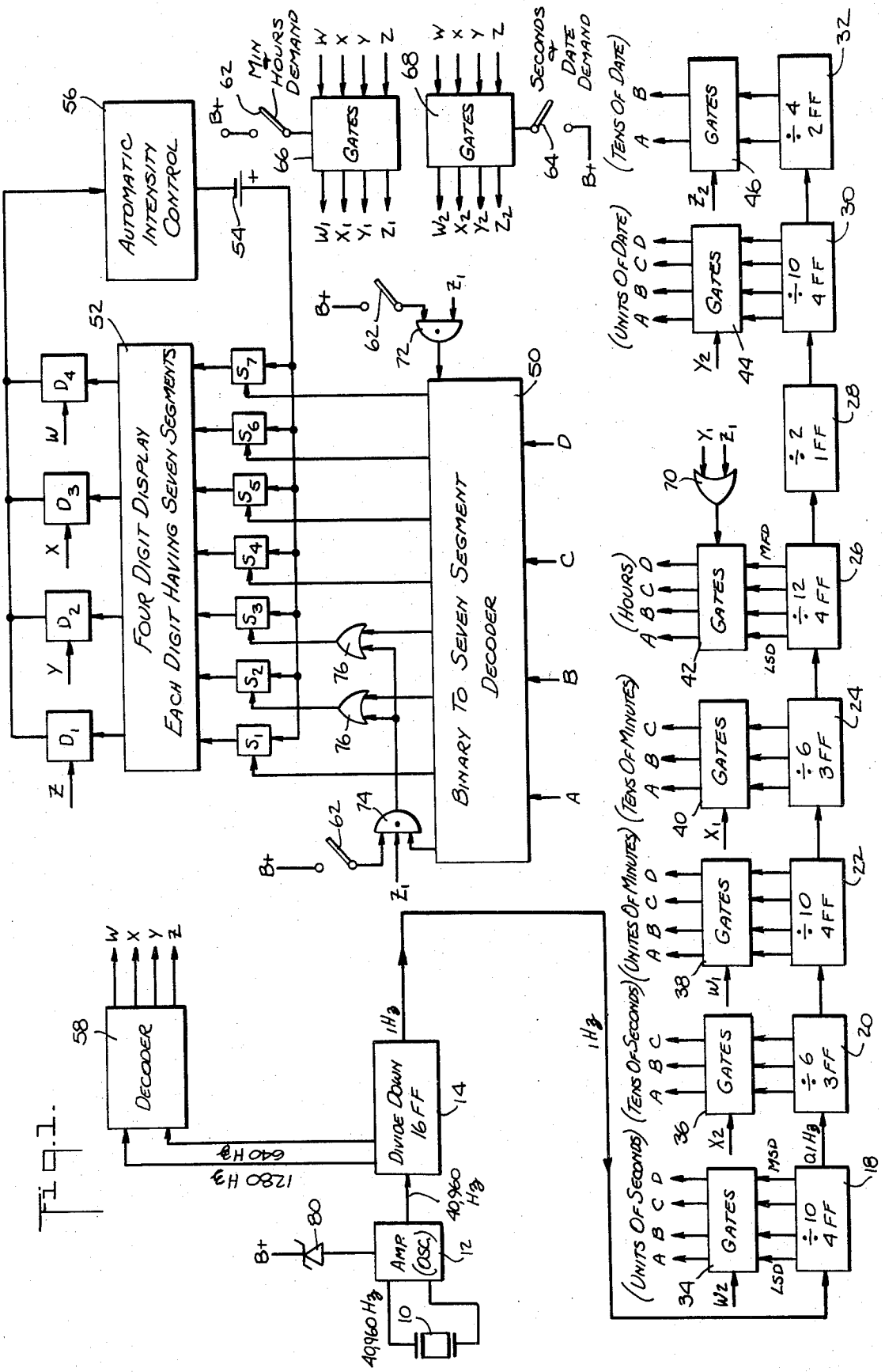
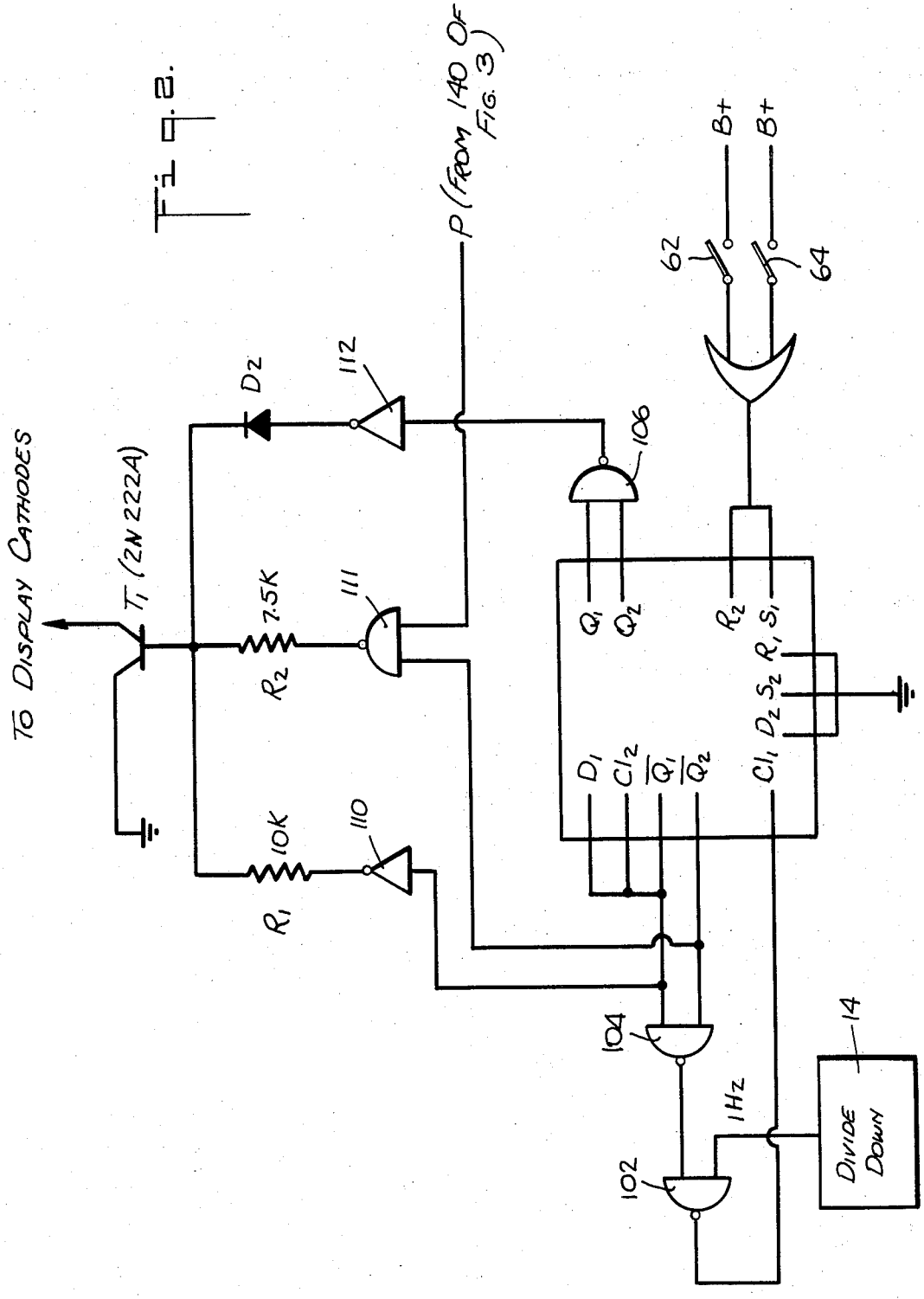

AUTOMATIC INTENSITY CONTROL
FOUR DIGIT DISPLAY EACH DIGIT HAVING SEVEN SEGMENTS
BINARY TO SEVEN SEGMENT DECODER
GATES
DECODER
DIVIDE DOWN 16 FF
AMP (OSC.)
÷ 10 4 FF
÷ 6 3 FF
÷ 12 4 FF
÷ 4 2 FF
÷ 2 1 FF
MIN HOURS DEMAND
SECONDS DATE DEMAND
(UNITS OF SECONDS)
(TENS OF SECONDS)
(UNITS OF MINUTES)
(TENS OF MINUTES)
(HOURS)
(UNITS OF DATE)
(TENS OF DATE)
40960 Hz
1280 Hz
640 Hz
1 Hz
LSD
MSD
B+

Fig. 1.

Fig. 2.


P (FROM 140 OF FIG. 3)
B+
B+
62
64
D2
112
106
TO DISPLAY CATHODES
T1 (2N 2224)
7.5K
R2
111
Q1
Q2
R2
S2
R1
S2
D2
D1
C12
Q1
Q2
C11
10K
R1
110
104
102
1Hz
14
DIVIDE DOWN

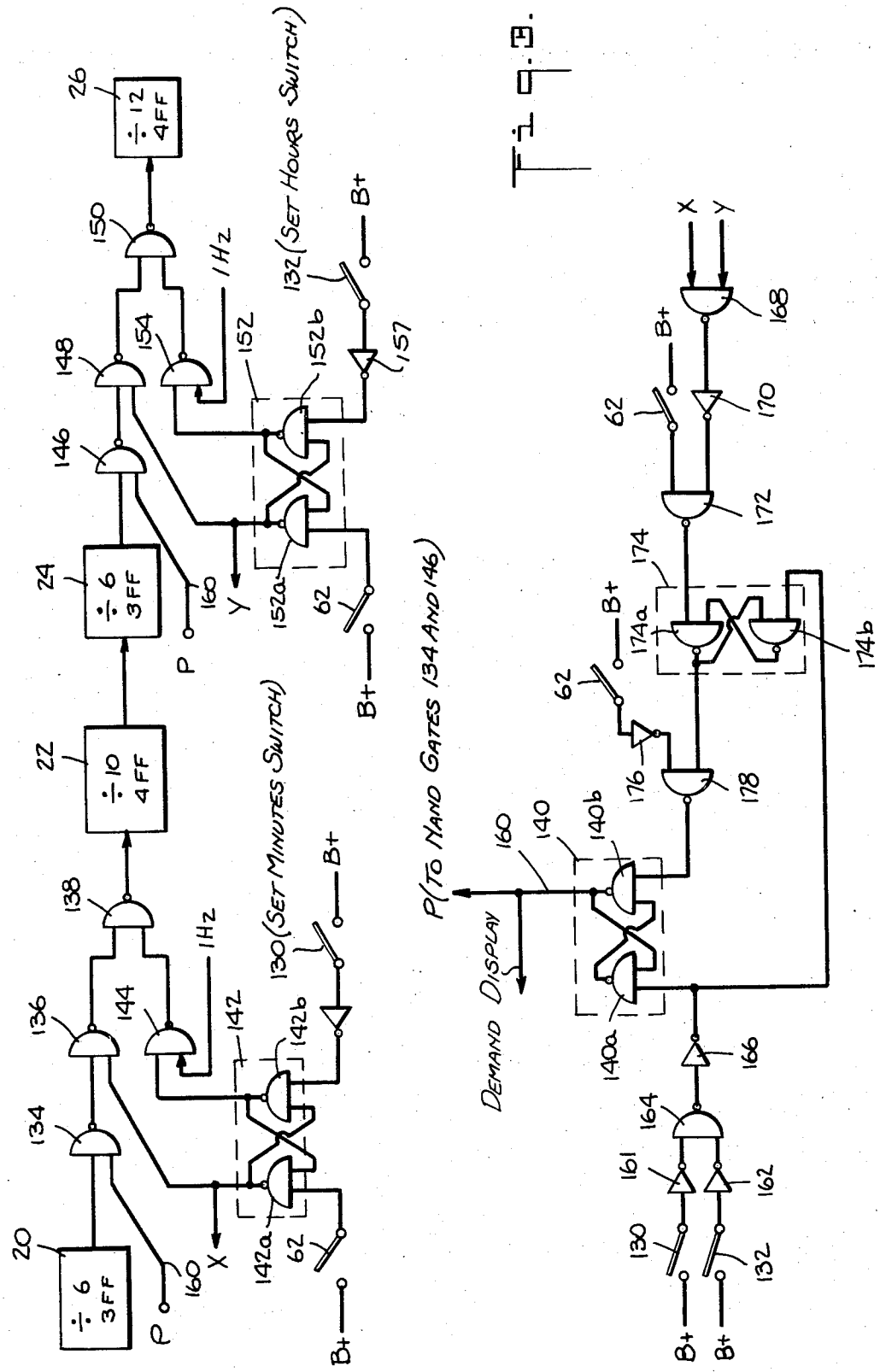

÷ 6 3FF
÷ 10 4FF
÷ 12 4FF
1Hz
P
X
Y
B+
62
160
20
22
24
26
130 (SET MINUTES SWITCH)
132 (SET HOURS SWITCH)
P (TO NAND GATES 134 AND 146)
DEMAND DISPLAY

Fig. 3.

ELECTRONIC TIMEPIECE

This invention relates in general to an electronic timepiece, and more particularly to one whose design and arrangement affords efficient display requiring minimum battery drain thereby providing low cost, small size and long life.

BACKGROUND OF THE INVENTION

Electronic timepieces have long been looked to as the means for making a fundamental departure from the traditional mechanical escapement used in almost all timepieces. The enormous accuracy available from a crystal has long provided an appealing alternative to mechanical escapement. The difficulty has been that electronic designs, which require battery power, call for too great a drain on the battery. As a consequence, either a relatively large battery was required or the battery employed had to be replaced too often. There is no commercially practical compromise available between the weight and size of a large battery and the frequent replacement of a small battery. In addition, in both cases, excessive costs result as contrasted with the traditional mechanical timepieces. Thus these problems became particularly acute when electronic designs were considered in connection with the most common form of timepiece, the wristwatch and pocketwatch.

Electronic time keeping circuits are known. One design is taught in U.S. Pat. No. 3,560,998, issued ot Richard S. Walton. It is also known to provide direct digit read-outs of the use of light emitting diodes in such timepieces.

The development of the metal oxide silicon transistor made feasible the design of complementary-symmetry divide-down flip-flop timing circuits operating off a crystal output which draw current only at the flip-flop cross-over point and thus minimize battery drain. The timepiece illustrated in U.S. Pat. No. 3,560,998 employs this so-called COS/MOS type of design. The RCA CD 4007 integrated circuit is one usable building block employing COS/MOS.

However, for such timepieces to be practical, particularly for watch use, it is essential that the current drain be kept to a minimum. Minimum current drain means a better compromise between size of the battery necessary for the watch and the length of time that the battery will last before it needs replacement.

Accordingly, it is a major purpose of this invention to provide a direct digital read-out electronic timepiece having decreased current drain.

It is a related purpose of this invention to provide this decreased current drain characteristic in a design that involves a reasonably small volume and low weight circuit design and at a reasonable cost so that the long life between battery change and small battery size will be effected in a practical embodiment.

BRIEF DESCRIPTION OF THE INVENTION

In brief, this invention is in an entirely electronic timepiece that is electronic from the crystal that supplies the basic frequency to the light emitting diodes that provide a direct digit display of the time. The only mechanical feature is a set of switches that are manually operated to turn on the light emitting diodes and thus provide a display of the time when desired and to set the time. To save on current drain, the same diode display matrix is employed to provide an hours and minutes display and to provide a date and seconds display, these displays being multiplexed through different display demand switches. To further save on current, a zener diode is employed to drop the battery voltage applied to the amplifier-oscillator operating off the crystal yet permitting adequate battery voltage for excitation of the light emitting diodes.

To provide the ability to use the timepiece in a wide range of ambient light conditions and to further save on current drain, there are three levels of intensity of the display which are cycled through from lowest to highest intensity automatically whenever the demand display switch is actuated.

A time setting mechanism is employed which is actuated by the combination of a time setting switch and a display demand switch. A logic circuit is provided so that solely by successive manipulations of the display demand switch, the user of the watch can in succession set the time at some convenient point ahead of real time, stop the time setting while continuing to inhibit the normal time keeping so that the real time can advance to synchronization with the set time, then start time keeping once real time and set time are synchronized and finally, (all by actuation of the same display demand switch) view the time whenever desired.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an overall block diagram of a timepiece embodying this invention.

FIG. **2** is a block and schematic diagram essentially of the automatic intensity control unit **56** of FIG. **1.**

FIG. **3** is a block diagram of a time setting mechanism that is employed with the time keeping mechanism illustrated in FIG. **1.**

Although the automatic intensity control mechanism illustrated in FIG. **2** is essentially represented by a single block in FIG. **1,** the time setting mechanism shown in FIG. **3** is essentially not represented in FIG. **1.**

DESCRIPTION OF THE PREFERRED EMBODIMENT

Providing The Signals Representing Time

FIG. **1** is a block diagram showing the basic arrangement of a timepiece of this invention. An accurate crystal **10** having a precisely determined output frequency of, for example, 40,960 Herz (Hz.) provides the basic timing signal employed. An amplifier-oscillator **12** provides the basic timing signal with the amplitude sufficient to operate the various circuits in FIG. **1** and also in the form of a pulse train having a repetition rate equal to the frequency of the crystal **10.**

The divide down circuit **14** is essentially sixteen bistable switching circuits, commonly called flip-flop (FF) circuits, the last four flip-flop circuits being connected in a divide by ten configuration The frequencies that can be tapped off. the divide down circuit **14** are a sub-multiple to the power of two of the basic crystal frequency, except that the final output frequency is a 1 Herz signal which is obtained in a known manner by appropriate feed back connections. This one Herz signal is applied to the first divide down circuit **18** in a series of divide down circuits. This 1 Herz signal is a 50 percent duty cycle pulse train having a pulse once per second.

The four flip-flops that constitute the divide down circuit **18** are interconnected so that they will cycle through ten separate states switching from state to state

in response to an input pulse. Accordingly, every ten seconds the four interconnected flip-flops which constitute the divide down by 10 circuit **18** will cycle through ten separate states and each state will have a duration of one second. The four outputs from the divide down circuit **18** will provide a binary coded decimal indication of the 10 states. This binary coded output, therefore, can be used to indicate the units digit of a decimal indication of seconds. The least significant digit (LSD) of this binary output will appear on the line so indicated and the state of that line (that is, wheter it has pulse or no pulse) will change once a second. The most significant digit (MSD) will appear on the line so indicated and the state of that line will cycle once every ten seconds. This most significant digit output is a 0.1 Herz pulse train and is also employed as the input to the next divide down circuit **20.**

The divide down circuit **20** is a divide by six circuit, thus requiring only three flip-flops. ecause it is used to represent the tens digit of a decimal indication of seconds, the circuit **20** only has to represent six of the 10 decimal digits. This divide down circuit **20** as well as the rest of the divide down circuits **22, 24, 26, 28, 30** and **32** operate in a known fashion, are similar to that of the divide down circuit **18** and need not be described in much greater detail. The various divide down circuits **18** through **32** differ to some extent in the amount of division required. Thus, in FIG. **1,** the amount of division performed by each circuit is indicated as is the frequency of that output from each divide down circuit which is supplied as the input to the next divide down circuit. The single flip-flop divide down circuit **28** is required because there are twelve hour sequences in each day. The input state change to the units digit for the date divide down circuit **30** has to be once a day rather than twice a day. Thus the pulse train representing the most significant digit in the hours digit divide down circuit **26** has to have its repetition rate divided by two before being applied as an input to the units of date divide down circuit **30.** The single flip-flop **28** performs this function.

The binary coded decimal digit outputs from the divide down circuits **18** through **32** (except for **28**) are all applied through respective normally closed sets of gates **34** through **46.** These gates **34** through **46** are turned on (that is, enabled) by the signals indicated (W_1, X_1, Y_1, Z_1) or (W_2, X_2, $Y_2$and Z_2) so that each binary coded decimal digit is available for only a brief fraction of time as described below. When any one set of gates **34** through **46** is turned on, the output from the turned on set of gates are identical to their inputs. The outputs from the gates are indicated as outputs A, B, C and D to indicate the manner in which the outputs from the gates are connected as inputs to the binary to seven segment decoder **50.** Only one of the seven sets of gates **34** through **46** is turned on at a time. Thus, the decoder **50** only has to cope with one input number at a time. Except for the hours number, each of these input numbers to the decoder **50** is a one digit decimal number.

Taking the units of seconds output as an example, when the set of four gates **34** is turned on, this output is applied to the decoder **50** as a four bit binary number. The decoder **50** converts this four bit number into a seven bit segment code. Each bit of the seven bit code is applied to a separate one of the normally off segment switches S_1 through S_7. When the bit is high, the switch is turned on. When the bit is low, the switch remains in its normally off state. Each of four digit positions in the visual display **52** has seven segments. It is a well known technique to display a decimal digit by a seven segment digit position. By lighting up selected ones of these seven segments, any one of the 10 decimal numerals can be displayed. In one embodiment, each segment has four light emitting diodes (LED*s*). Thus each position has **28** LED*s* and the four positions require **112** LED*s*.

Each of the segment switches S_1 through S_7 is connected between the positive terminal of a battery **54** and the anode of each of the four LED*s* of a particular one of the seven segments of each of the four digits.

For example, if the output of the gate **34** at any one moment corresponds to the numeral **3,** then five of the segment switches S_1 through S_7 will be turned on. Switch S_1, for example, will connect the anodes of the four diodes at a first segment of each of the four positions to the battery **54.** In effect, S_1 will connect 16 LED anodes to the battery **54.** When the units of seconds gates **34** output is applied to the decoder **50,** it is essential to avoid turning on the LEDs representing the numeral involved in all four positions. With respect to this example, this means it is essential to turn on the appropriate LEDs only in the rightmost position; that is, the position that indicates the units of seconds. This result is achieved by virtue of the digit switches D_1 through D_4. Each of these switches D_1 through D_4 is connected between the cathodes of all the LED*s* in a sepaeate one of the four digit display positions and, through an intensity control unit **56,** to the negative terminal of the battery **54.** For example, the switch D_4 is connected to the cathodes of each of the **28** LED*s* in the rightmost of the four digit positions. The signal W_2 that opens the gate **34** is derived from a signal W that turns on the switch D_4. With D_4 turned on and with the appropriate five of the switches S_1 through S_7 turned on, the units numeral "**3**" will appear in the rightmost position of the display **52.**

The representation of the digits for each of the other positions on the display operates essentially in the same fashion. There is a complication requiring additional gating so that the hours output from the gates **42** when applied to the decoder **50** will permit representation of a two digit number when the hours are 10, 11, or 12. The technique for doing that will be described further on in this specification.

Sequencing of the Display Signals

An important aspect of the arrangement of this invention is the sequencing of the various binary coded decimal (BCD) outputs from the sets of gates **34** through **46** so that only one BCD output is applied to the decoder **50** at a time and so that the right one is applied.

A decoder circuit **58** working in conjunction with the two inputs shown provide four basic signals W, X, Y and Z that make possible the above-mentioned functions. The decoder **58** simply has two basic input pulse trains, which can, for example, have 1,280 Herz and 640 Herz pulse repetition rates. Both of these signals are available from divide down circuit **14.** These two pulse trains, having a two-to-one frequency relationship, provide four different input states for the decoder **58.** The decoder **58,** in a simple and known fashion, converts these four input states to four separate outputs W, X, Y and Z on four separate lines. When a signal is present on any of these output lines, the other three sig-

nals are absent. Thus when a pulse W is present, there are no X, Y and Z pulses. As a consequence, when a set of LEDs are turned on power is delivered for twenty-five percent of the overall time period during which the display is being actuated.

The duration of each W pulse is equal to the duration of a pulse in the input 1,280 Herz pulse train, i.e., approximately 390 microseconds.

In order to provide the ability to display a date of the month and a seconds indication as well as an hours and minutes display, the four digit display **52** has to be multiplexed between an hours and minutes display and a data and seconds display. This multiplexing is done manually by user actuated demand switches **62** and **64.** When the user wishes to view hours and minutes, he closes the switch **62** thereby opening the gates **66** so that the signals W, X, Y and Z are transmitted through the gate **66** to appear as signals W_1, X_1, Y_1 and Z_1. When the user wishes to read the date and seconds, he manually closes switch **64** to open the gates **68** and provide the signals W_2, X_2, Y_2 and Z_2. When the gates **66** or **68** are closed, the outputs from these gates are identical to the inputs to these gates.

With the above enabling and switching arrangement in mind, it can be seen that there is a short (390 microsecond) time period display of each of the four digits in sequence with a relatively long (1,160 microseconds) between successive displays of the same digits.

Again, with reference to the units of seconds display, the user will close the switch **64** thereby opening the gates **68.** This provides the signal W_2. The signal W_2 is applied to the gates **34** to open the gates **34** for a 390 microsecond time period once each 1,160 microseconds. The BCD signal from the gates **34** is decoded by the decoder **50** to provide a seven segment output which turns on the appropriate segment switches S_1 through S_7 to connect the appropriate segments of each of the four digits in the display **52** to one side of the battery **54.** A the same time the signal W closes the digit switch D_4 to connect all of the segments of the fourth digit to the other side of the battery **54.** The result is that for 390 microseconds power is applied to show the appropriate decimal digit indicating the units of seconds in the fourth digit position of the display **52.** At the end of this 390 microsecond period, the pulse X_2 opens the gates **36** to provide the appropriate BCD input to the decoder **50** indicating the tens of seconds digit. Because the signal X simultaneously closes the switch D_3, this tens of seconds numeral is represented at the third digit position on the display **52.** Thus, in sequence, the four display positions on the display **52** are lit up for 390 microsecond periods each. The same display digit position being lit for 390 microseconds once each 1,160 microseconds.

The Hours Display

The handling of the BCD signal representing hours is somewhat special because when it is 10, 11 or 12 o'clock, the output from a single set of gates **42** requires that two digit positions on the display **52** be lit in response to a single BCD signal. The arrangement as shown, and to be immediately described, is somewhat complex from a logic point of view and could have been handled in a more straightforward fashion employing a separate set of flip-flops and gates for the representation of the tens of hours position. Hwever, to handle the hours representation in that fashion would have required an additional flip-flop and thus would have added more to the cost of this device than does the expedient shown in which a few simple gates are employed.

Since the BCD hours output signal from the gates **42** may have to be employed to light up the first and second display digit positions, it is necessary that the outputs from the gates **42** be applied during the time period of both the Y and Z timing signal. Accordingly, the pulses Y_1 and Z_1 are applied through an OR gate **70** to open the gates **42** during both time periods. The decoder **50** responds to the gates **42** output by providing a seven segment output that represents the units of hours decimal digit. During the Y time slot, this unit of hours digit is energized in the second display position of the display unit **52.** However, during the Z time slot, it is obviously necessary to prevent this units of hours input from closing any of the segment switches S_1 through S_7. The AND gate **72** is open at that time, because the switch **62** is closed and the Z_1 output is applied to provide a disabling input to each of the seven AND gate outputs from the decoder **50.** The decoder **50,** however, has an eighth output on a line that is applied to the AND gate **74.** This eighth decoder output is present only when the input to the decoder **50** represents a number ten or greater. Thus, during the Z time slot, if the gates **42** output represents a 10, 11 or 12 o'clock time period, the decoder **50** applies an input to the AND gate **74.** Since at the same time, the demand switch **62** is closed and the Z_1 input is applied, the AND gate **74** will provide an output which is applied to the switches S_2 and S_3 through OR gates **76.** Segment switches S_2 and S_3 are connected to the two segments which provide a numeral "1" display. Since the Z signal turns on first digit switch D_1, the first display position provides a "1" display under the above condition.

The Amplifier **12**

The oscillator circuit **12** which is employed as an amplifier is one of the major drains of current. The reason for this is that the circuitry involved in this invention preferably employes complementary metal oxide semiconductor devices. The use of such is known in the art to provide minimum current drain. Such devices are current flowing only during the cross-over point when they switch. Thus there is no current drain between switch-over times. Obviously, the higher the frequency applied to such devices, the mroe often will switchover occur and the greater will be the drain. Since the amplifier **12** has to handle the highest frequency signal in this unit, it is the amplifier **12** that has the greatest amount of current drain. The other factor that affects the amount of current used is the voltage. One technique which has been found valuable to achieve one of the major purposes of this invention, that is minimum current drain, is to employ a Zener diode **80** to reduce voltage applied to the oscillator amplifier **12.** Circuit B+ voltage (three volts in one embodiment) required for the operation of the display diodes can be cut down to a level (1.8 volts in one embodiment) which permits employment of an amplifier **12** that requires as low an input voltage as is possible. The result is minimized current drain in amplifier **12.**

Automatic Intensity Control (FIG. 2)

FIG. **2** illustrates the design of the automatic intensity control **56** which is shown as a single block in FIG. **1.** With reference to FIG. **2,** a standard dual flip-flop unit **100** is employed in conjunction with various Nand gates **102, 104** and **106** to provide the automatic se-

quencing that cycles the intensity of the display through three levels. The three intensity levels are a low level of intensity that lasts for at least one second, immediately followed by a one second in duration intermediate level of intensity which in turn is immediately followed by a one second in duration high level of intensity. After the three second display, the display automatically turns off and the demand display switch **62** or **64** has to be actuated again in order to provide display. In this fashion, the battery drain in the timepiece is kept to a minimum and battery life is extended so that a practical wristwatch is made available.

The dual flip-flop **100** used in this embodiment is a standard type clocked "D" flip-flop. An example of such a flip-flop is the CD4013 which is sold by the RCA Company and others. The terminals of the dual flip-flop are as indicated, the subscript "1" representing the first of the two flip-flops and the subscript "2" representing the second of the two flip-flops. The mutually exclusive outputs of each of the two bi-stable flip-flops are represented as Q and $\overline{Q}$. The set inputs which force each flip-flop into the state where its output is high and its $\overline{Q}$ output is low are indicated as S. The re-set inputs, which force each flip-flop into the state where its Q is high and its $\overline{Q}$ output is low are indicated with the symbol R.

The Normal State of the FIG. 2 Arrangement

The normal state of the dual flip-flop **100** (that is, the state where the demand display switches **62, 64** are in their normally open position, as shown in FIG. 2) is the re-set state wherein the outputs Q_1 and Q_2 are low while the outputs $\overline{Q}_1$ and $\overline{Q}_2$ are high. Under this normal state, the two input terminals to the Nand gate **104** are high since these two input terminals are connected to the $\overline{Q}_1$ and $\overline{Q}_2$ output terminals of the dual flip-flop **100.** Since both inputs to the Nand gate **104** are high, the output from the Nand gate **104** is low. Thus, since one of the inputs to the Nand gate **102** is low, the output from the Nand gate **102** is high and the 1 Herz pulse train, that is the other input to the Nand gate **102,** does not get through the Nand gate **102.**

Since the two inputs Q_1 and Q_2 to the Nand gate **102** are normally low, the output from the Nand gate **106** is high. Thus, in this normal state, the inputs to the two invert circuits **110** and **112** are high and their outputs are low. Also, the $\overline{Q}_2$ input to Nand gate **111** is high and the other input to Nand gate **110** is high as it is in the normally high output from the flip-flop **140.** Thus the output of Nand gate **111** is low. The result is that the transistor T_1 is biased off (see FIG. 3).

The transistor T_1 is in series with the cathodes of the LEDs in the display unit **52** and thus, since the transistor T_1 is off, none of the display unit **52** diodes will be lit.

In Operation

In order to view the time, the user closes either the switch **62** or the switch **64.** The resulting voltage applied to the set terminal S_1 forces the first flip-flop into the set state; specifically, the state where the output Q_1 is high and the output $\overline{Q}_1$ is low. Since the second flip-flop is in its re-set state there is no effect from applying a voltage to the re-set terminal R_2. With $\overline{Q}_1$ low, the invert circuit **110** goes high and applies an output through the 10,000 ohm resistor R_1 to the base of the transistor T_1 thereby turning on the transistor T_1. The magnitude of the resistor R provides a first level of brightness for the cathode displays which, in this case, is the lowest level of brightness.

Because the Q_1 input to the Nand gate **104** has gone low, the Nand gate **104** output goes high and, as a result, the pulse train input ot the Nand gate **102** goes through the Nand gate to be applied as an input to the clock terminal Cl_1 of the first flip-flop. As long as the switch **62** (or **64**) is closed, these pulses will have no effect on the first flip-flop because of the signal applied to the set input S_1. However, as soon as the switch **62** (or **64**) is released the first flip-flop is released so that the next positive going transistion point in the pulse train at the Cl_1 terminal will force the first flip-flop from its set state into its re-set state. As a consequence, switching of the output terminal $\overline{Q}_1$ from low to high will apply a pulse input to the clock terminal Cl_2 of the second flip-flop because of the fact that these two terminals are wired together. The result is to force the second flip-flop from its re-set state into its set state. Under this condition, Q_2 is high and Q_1 is low, thus maintaining the low output state from the invert circuit **112.** $\overline{Q}_1$ is now high so that the invert circuit **110** output is low. However, $\overline{Q}_2$ is low with the consequence that the output from the Nand gate **111** turns on the transistor T_1 through the 7,500 ohm resistor R_2 thereby providing a second level of brightness for the display cathodes, which second level of brightness is greater than the first level of brightness provided when the transistor T_1 was turned on through the 10,000 ohm resistor.

With Q_2 low and Q_1 high, the Nand gate **104** output remains high and the pulses continue to be applied through the Nand gate **102** to the clock input Cl_1. At the next positive going input to the terminal Cl_1, the first flip-flop is forced from its re-set state to its set state, thereby providing an output from the terminal Q_1 and dropping the output from the terminal $\overline{Q}_1$. At this point, the second flip-flop is not affected because the drop of voltage at the second clock terminal Cl_2 does not cause switching. The result is a state where both inputs to the Nand gate **106** are so that the output from the Nand gate **106** is low and thus the output from the invert circuit **112** is high. This turns on the transistor T_1 through the diode D_2 which means that a minimum resistance is in series with the display cathodes so that the display cathodes are at their maximum brightness.

The output of Nand gate **104** remains high because both inputs are low. Thus, the next pulse in the 1 Herz pulse train will get through the Nand gate **102** and the next positive going pulse transition will clock the first flip-flop once more. This will force the first flip-flop from its set state into its re-set state thereby causing $\overline{Q}_1$ to go high. The going high of $\overline{Q}_1$ will apply a positive going pulse to the clock terminal Cl_2 of the second flip-flop, thereby forcing the second flip-flop from its set state into its re-set state. This returns the FIG. 2 circuit to its normal condition with both $\overline{Q}_1$ and $\overline{Q}_2$ high and both Q_1 and Q_2 low. The result is that the transistor T_1 is turned off and the display extinguished. The output of Nand gate **104** is again brought low, disabling Nand gate **102** and thus turning off the 1 Herz pulse train to Cl_1.

Because the one Herz signal through Nand gate **102** causes each of these transitions, the duration of at least the second level of intensity and the third level of intensity is exactly one second each. The duration of the first level of intensity will depend on how long the user holds down the demand display switch **62** or **64**; but the

duration of the lowest level of intensity will be no more than one second after the user releases the demand display switch **62** or **64.**

Time Setting Mechanism (Fig. **3**)

One of the advantages of the FIG. **3** embodiment, as will be seen in connection with the discussion below, is that it provides a means for very accurately setting the timepiece.

FIG. 3 Under Normal Timepiece Operating Conditions

Under normal timepiece operating conditions (that is, when the time is not being set), the switches are as shown. Specifically, both display demand switches **62** and **64** are open. In addition, there is a set minutes switch **130** and a set hours switch **132,** both of which are open. These switches **130, 132** are closed only when it is desired to set the time.

To understand the operation of setting time, it is best to first understand under normal operations the FIG. **3** circuit. The output of the divide-down circuit **20** (see also FIG. **1**) is a pulse train having one pulse per minute. This pulse train is normally applied through the Nand gates **134, 136** and **138** to be provided as an input to the divide-down circuit **22.** The reason, under normal operating conditions, that this pulse train is applied through these three Nand gates is that the second input to the Nand gate **134** is high by virtue of the normal high output on line **160** from the flip-flop circuit **140,** the second input to the Nand gate **136** is high by virtue of the normal high output from the flip-flop circuit **142** and the second input to the Nand gate **138** is high by virtue of the high output from the Nand gate **144.** The Nand gate **144** has a high output because one of its two inputs is a normally low input from the flip-flop circuit **142.**

In similar fashion, a pulse train from the divide-down circuit **24,** which provides a pulse once an hour, is normally applied through the appropriately enabled Nand gates **146, 148** and **150** to be provided as the input to the divide-down circuit **26.** The flip-flop circuit **152** has the same output characteristics as the flip-flop circuit **142** so that the enabling inputs to the Nand gates **148** and **154** are the same, respectively, as the enabling inputs to the Nand gates **136** and **144.**

Thus it may be seen that when the time is not being set the additional Nand gates between the divide-down circuits **20** and **22,** as well as the additional Nand gates between the divide-down circuits **24** and **26** do not change the manner in which FIG. **1** functions.

Briefly the reason why the flip-flop circuits **142** and **152** have the normal output state described above is as follows. With reference to the flip-flop **142,** an open display demand switch **62** means that one of the inputs to the Nand gate **142***a* is low and thus the output from the Nand gate **142***a* must be continuously high. With the set minutes switch **130** open, the invert circuit **156** provides a continuously high signal at one of the inputs to the Nand gate **142***b*. Since the other input to the Nand gate **142***b* is the output of the Nand gate **142***a*, that other input is also high and thus the output of the Nand gate **142***b* is low. A completely analogous circuit, including a second invert **157,** exists with respect to the flip-flop circuit **152.**

The reason why the line **160,** which connects an output from the flip-flop **140** to inputs to the Nand gates **134** and **136** is normally high is described hereinafter in connection with the circuit arrangement at the bottom of FIG. **3.** For the purpose of describing the top part of FIG. **3,** simply assume that this line **160** is normally high.

It should also be noted that under these normal operating conditions, when the display demand switch **62** is closed, nothing material is affected in the FIG. **3** circuit. Closing the switch **62** will change the corresponding input to the Nand gate **142***a* from a low to a high. But since the other input to this Nand gate **142** is low, there will be no change in the outputs from the flip-flop **142.** The circuit arrangement in connection with the flip-flop circuit **152** is completely analogous.

Setting the Time

Now assume that it is desired to set the minutes display ahead. The user of the timepiece depresses the display demand switch **62** so that he can see the time. By itself, this will change nothing. Now the user depresses the set minute switch **130.** As soon as he does this, the corresponding input to the Nand gate **142***b* goes low and the result is that the output of the Nand gate **142***b* goes high. Since this means that both inputs to the Nand gate **142***a* are now high, the output of the Nand gate **142***a* goes low. Thus the outputs of the set-reset flip-flop **142** are switched and the flip-flop **142** can be considered to be in its switched (not normal) state.

An important point should be noted here. If the set minute switch **130** bounces on initial closing, as is frequently the case with hand actuated switches, the flip-flop **142** will stay in its switched state because the output from the Nand gate **142***a* having gone low will provide at least one low input to the Nand gate **142***b* and thus assure that the Nand gate **142***b* output will remain high. Furthermore, the set minutes switch **130** can be immediately released and the flip-flop **142** will remain in its switched state as long as the minutes display demand switch **62** remains depressed. Switch **130** bounce on opening will also not affect the state of the flip-flop **142.**

With the outputs of the lfip-flop **142** switched, the enabling signalf for the Nand gates **136** and **144** are switched from high to low. As a consequence, the Nand gate **136** is disabled (that is, its output will be continually high) and the time signal from the divide-down circuit **20** ceases to progress through the rest of the divide-down circuitry shown in FIG. **1.** However, a 1 Herz signal from gate **16** (see FIG. **1**) is applied through the Nand gate **144** and Nand gate **138** to the rest of the divide-down circuitry thereby driving the time record forward 1 minute per second.

If it is desired to set the hours ahead, a completely analogous operation takes place with the display command switch **62** input to the flip-flop circuit **152** and with the set hours switch **132.**

Once the desired time has been set, the display demand switch **62** is released and the circuit reverts to its normal state.

With reference to the flip-flop **142,** this release of the switch **62** will mean a low corresponding input to and thus a high output from the Nand gate **142.** As a consequence, the Nand gate **142***b* will have a corresponding high input from the output of the Nand gate **142***a* and since the other input to the Nand gate **142***b* has gone high because the set minute switch **130** has been released (the set minute switch **130** need not be held longer than necessary to initially switch the flip-flop **142**) then the Nand gate **142***a* will also switch. This will restore the normal condition for the flip-flop **142.** As a consequence, the previous enabling condition of the

Nand gates **136** and **144** are re-established and the time signal from the divide-down circuit **20** will proceed to function as normal.

The above description has assumed that the signal on the line **160** has remained high so that the switching back of the flip-flop circuit **142** will re-establish the normal condition. However, in fact the circuitry relating to the flip-flop circuits **140** and **174** modifies this situation for the purpose of permitting very accurate setting of the timepiece. To understand the operation of the circuitry **140,** etc. upstream from the line **160,** it is helpful to appreciate what the purpose of this circuitry is. The purpose of this circuitry **140,** etc. upstream from the line **160** is to permit the user of the timepiece to set the timepiece at a desired point in time somewhat ahead of the real time at which he releases the display demand switch **62** and then to freeze that set time in the timepiece until the display deman switch **62** is further actuated and released so that the user can, on a second release of the display deman switch, synchronize his release with the time standard use.

In order to set the time with the accuracy that is warranted by the circuit of this invention, it is desireable to have this time setting mechanism function so that the user can set the time at some convenient minute or two ahead of the actual time. When so set, the timepiece does not progress any further and when the static display from the timepiece exactly matches the time standard being used, the user depresses an appropriate switch and the timepiece then is switched into its normal dynamic operating state and proceeds to keep time. The lower part of the circuit of FIG. **3** is employed to perform this function.

Again, assuming that it is minutes which are being set, in terms of the user operation, what he does is to press the switches **62** and **130** as indicated above and allow the time to be set ahead at the rate of one minute per second until he has set the display to a convenient two, or three, as the user desires, minutes ahead of the time which he is using as his standard. He then releases the switch **62** (having already released the switch **130** since it does not have to be closed for more than an instant). If he then depresses the switch **62** once more, the display will hold at the time that he has set and the watch will not be keeping time. When the time he is using as a standard matches the time being displayed, he releases the switch **62** for a second time and now the watch will proceed to keep time correctly. If he then immediately or at some time in the future depresses the switch **62** again in order to read the time he will be reading it correctly.

The way in which this multiple function for the switch **62** is achieved arises out of the ability of the FIG. **3** circuit to affect the state of the line **160.** If the output to the point P on the line **160** from the flip-flop circuit **140** is switched from high to low, then the input to the Nand gates **134** and **164** is low, thereby disabling these Nand gates and preventing the regular time signal from progressing through.

First, it is best to understand the lower part of FIG. **3** during normal time keeping operation. Under such conditions the switches **62, 130** and **132** are open as shown. The invert circuits **161, 162** then assure that both inputs to the Nand gate **164** are high so that the Nand gate **164** output is low and thus the invert **166** output is high. This high input to the Nand gate **140***a* together with a low input to the Nand gate **140***b* assures that the flip-flop **140** is in its normal state such that the output P from the Nand gate **140***b* is high. In order to assure this normal flip-flop **140** state, the rest of the circuitry guarantees that the normal input to the Nand gate **140***b* is low.

Both input X and Y to the Nand gate **168** are high, since these are the high outputs from the flip-flop circuits **142** and **152,** respectively. As a consequence the otuput from the Nand gate **168** is low, the output from the invert circuit **170** is high and, since the other input to the Nand gate **172** is high (since **62** is closed), the output from the Nand gate **172** is low. The flip-flop circuit **174** has the same arrangement as the flip-flop circuit **142.** Thus with the input to the Nand gate **174***a* being low, the input to the Nand gate **174***b* being high, the output from the Nand gate **174***a* is high. Because of the invert circuit **176,** the second input to the Nand gate **178** is high and thus the output from the Nand gate **178** is low. With this second input to the flip-flop circuit **140** being low, it can be seen that the output on the line **160** is normally high.

It might also be noted that when the switch **62** is closed in order to read the display, the output P on line **160** is not changed once the flip-flop circuit **140** has this normal state. The output from the Nand gate **140***a* is low and thus the switching of the output from the Nand gate **178** when the switch **62** is closed does not change the fact that there is at least one low input to the Nand gate **140***b* and thus the fact that the output from the Nand gate **140***b* will remain high.

During time setting, the switch **130** is normally not depressed for more than a moment and as soon as it is released, the input to the Nand gate **140** switches back to its normally high value. Since the internal input to the Nand gate **140***a* is low because of the immediately preceding switching of the flip-flop **140,** the output from the Nand gate **140***a* remains high, and thus the internal input to the Nand gate **140***b* remains high. It is thus essential that the external input to the Nand gate **140***b* remain high so that the line **160** will remain low. This occurs by virtue of the fact that display switch **62** is held closed so that at least one input to the Nand gate **178** is low and thus the output from the Nand gate **178** is high.

Now, when setting time, not only is the switch **62** held closed, but the switch **130,** assuming that it is minutes which is being set, is closed at least momentarily. The closing of the switch **130** causes an input to the Nand gate **164** to become low, its output to become high and thus the input to the Nand gate **140***a* to become low. This will switch the output of the Nand gate **140***a* from a low to a high. By itself this is not enough to switch the output from the Nand gate **140***b*. But, it should be noted that the closing of the switch **62** has switched the output of the Nand gate **178** to a high. With the two high inputs to the Nand gate **140***b*, this output on the line **160** goes low.

As a consequence, the Nand gates **134** and **146** are disabled during this time setting operation and, as described above, the one Herz pulse train is applied to the divide-down circuit **22.**

The release of the switch **62** after the time has been set ahead by the desired two or three minutes does not change the output state of the flip-flop **140.** However, it does cause the flip-flop **142** to revert back to its normal condition. As a consequence, both inputs to the Nand gate **168** are high, its output is low and the corre-

sponding input to the Nand gate **172** is again high. But since the switch **62** is open, the other input to the Nand gate **172** is low, and thus the output from the Nand gate **172** is at its normal high state. At this point both external inputs to the flip-flop **174** are high and the output condition of the flip-flop **174** is not changed. This means that the output from the Nand gate **174***a* remains low and thus guarantees that the output from the Nand gate **178** remains high.

The next closing of the switch **62** does not affect the flip-flops **142** and **152** which are in their normal state. However, it does apply a second high input to the Nand gate **172** so that the external input to the Nand gate **174***a* goes low. The result is that the output from the Nand gate **174***a* goes high. But, at the same time the closing of the switch **62** causes the output of the invert circuit **176** to go low and thus maintains the output of the Nand gate **178** high. Thus the second closing of the switch **62** has not affect on the low state of the line **160.**

But now the second releasing of the switch **62** will cause the circuitry to revert back to its normal time keeping state and the line **160** to go high so that the Nand gate **134** is enabled and the regular time keeping signal can proceed from the divide-down circuit **20** to the divide-down circuit **22.** The second opening of the switch **62** causes the corresponding input to the Nand gate **172** to go low so that the output from the nand gate **172** goes high. However, this does not affect the fact that the output from the Nand gate **174***a* is high. But, the opening of the switch **62** does cause the output of the invert circuit **176** to go high so that the output of the Nand gate **178** goes low and the flip-flop circuit **140** switches back to its normal state with the output on the line **160** high.

What is claimed is:

1. In an electronic timepiece, the improvement in a low power drain design comprising in combination:

a matrix of light emitting diodes arranged and multiplexed to provide an N digit display,

first demand switch means to enable said matrix to provide a display of a first N digit item of time information,

second demand switch means to enable said matrix to provide a display of a second N digit item of time information; the type of time information provided by said second demand switch being different from the type of time information provided by said first demand switch,

display duration means for automatically disabling said display a predetermined time period after actuation of either of said demand switch means, and

time information signaling means to provide a time information signal as a train of pulses to energize appropriate ones of said light emitting diodes, said train of pulses being applied to said matrix only during said predetermined time period,

said diodes being enabled only in response to the actuation of either of said demand switch means.

2. The improvement of claim **1** wherein N is four.

3. The improvement of claim **2** wherein said first four digit item of time information is hours and minutes and wherein said second four digit item of time information is days and seconds.

4. In an electronic timepiece, the improvement comprising in combination:

a matrix of light emitting diodes arranged and multiplexed to provide an N digit display,

actuating means to turn on said display to provide a visual indication of the time recorded within the electronic circuitry of said timepiece, said actuating means including at least one display demand switch,

intensity control means responsive to said display demand switch to enable said diodes, said intensity control means including first, second and third loading circuits to determine first, second and third current levels through said light emitting diodes, and

switching means having a normal state, a first state, a second state and a third state, said switching means when in said normal state disconnecting each of said loading circuits from said diodes, said switching means when in said first, second and third states, respectively, connecting said first, second and third loading circuits to said diodes,

said switching means, when said display demand switch is actuated, being responsive to a predetermined pulse train from said electronic circuitry of said timepiece to switch in sequence from said normal state to said first state, to said second state, to said third state, and to said normal state in response to successive pulses of said predetermined pulse train.

5. The timepiece of claim **4** wherein said predetermined pulse train is a normal timing signal from the time keeping circuitry of the time piece.

6. The timepiece of claim **4** further comprising:

manually actuable time setting switch means for setting the time recorded within the timepiece, and

means responsive to the actuation of said time setting switch to disable said switching means and to connect a predetermined one of said first, second and third states to said diodes to provide a constant predetermined display light level during setting.

7. The timepiece of claim **6** wherein said predetermined pulse train is a normal timing signal from the time keeping circuitry of the time piece.

8. The improvement of claim **4** wherein said display demand switch includes:

first and second demand switches, said first and second demand switches being separately actuable, said first demand switch when actuated enabling said matrix to provide a display of a first N digit item of time information,

said second demand switch enabling said matrix to provide a display of a second N digit item of time information; the type of time information provided by said second demand switch being different from the type of time information provided by said first demand switch.

9. The improvement of claim **6** wherein said display demand switch includes:

first and second demand switches, said first and second demand switches being separately actuable, said first demand switch when actuated enabling said matrix to provide a display of a first N digit item of time information,

said second demand switch enabling said matrix to provide a display of a second N digit item of time information; the type of time information provided by said second demand switch being different from the type of time information provided by said first demand switch.

10. In an electronic timepiece, the improvement in a low power drain design comprising in combination:
a crystal providing a basic timing signal,
a complementary metal oxide semi-conductor amplifier-oscillator coupled to said crystal to provide an amplified basic timing signal as an N digit display,
a matrix of display diodes to provide direct read-out of the time,
a battery coupled to said display diodes to provide power for said display diodes at battery voltage,
a Zener diode coupled between said amplifier and said battery to provide power for said amplifier at a voltage substantially less than said battery voltage,
whereby the relatively lower voltage at said devices in said amplifier results in substantially less current drain at each cross-over point during switching than the current drain that would occur if battery voltage were employed.

11. The improvement of claim 10 further comprising:
first demand switch means to enable said matrix to provide a display of a first N digit item of time information,
second demand switch means to enable said matrix to provide a display of a second N digit item of time information; the type of time information provided by said second demand switch being different from the type of time information provided by said first demand switch,
display duration means for automatically disabling said display a predetermined time period after actuation of either of said demand switch means, and
time information signaling means to provide a time information signal as a train of pulses to energize appropriate ones of said light emitting diodes, said train of pulses being applied to said matrix only during said predetermined time period,
said diodes being enabled only in response to the actuation of either of said demand switch means.

12. The improvement of claim 11, further comprising:
intensity control means responsive to said display demand switches to enable said diodes, said intensity control means including first, second and third loading circuits to determine first, second and third current levels through said light emitting diodes, and
switching means having a normal state, a first state, a second state and a third state, said switching means when in said normal state disconnecting each of said loading circuits from said diodes, said switching means when in said first, second and third states, respectively, connecting said first, second and third loading circuits to said diodes,
said switching means, when one of said display demand switches is actuated, being responsive to a predetermined pulse train from said electronic circuitry of said timepiece to switch in sequence from said normal state to said first state, to said second state, to said third state, and to said normal state in response to successive pulses of said predetermined pulse train.

13. The timepiece of claim 12 further comprising:
manually actuable time setting switch means for setting the time recorded within the timepiece, and
means responsive to the actuation of said time setting switch to disable said switching means and to connect a predetermined one of said first, second and third states to said diodes to provide a constant predetermined display light level during setting.

14. In an electronic timepiece having a direct read-out display energizable by a battery, the time setting improvement comprising:
a manually actuable time setting switch for setting a predetermined time unit,
a manually actuable display demand switch coupled to the display with the battery to energize the display when actuated,
a first bi-stable switch having a normal re-set state and a set state, said first switch when in said set state coupling a predetermined pulse train to the circuitry controlling said predetermined time unit, said predetermined pulse train having a pulse repetition rate substantially greater than the pulse repetition rate of the time keeping pulse train normally applied to said circuit controlling said predetermined time unit,
a second bi-stable switch having a normal re-set state and a set state,
a third bi-stable switch having a normal re-set state and a set state, said third switch when in said set state disabling the normal time keeping function of the timepiece as to said predetermined time unit,
each of said first, second and third bi-stable switches switchable into its set state in response to the concurrent actuation of said manually actuable switches,
said first bi-stable switch when in said set state, switching into said re-set state in response to the release of said manually actuable switches to disconnect said predetermined pulse train from said circuitry controlling said predetermined time unit,
said second bi-stable switch when in said set state, switching into said re-set state in response to the actuation of said display demand switch when said first bi-stable switch is in said re-set state,
said third bi-stable switch when in said set state, switching into its re-set state in response to the release of said display demand switch while said second bi-stable switch is in its re-set state,
whereby the closing of said manually operable switches sets said bi-stable switches and causes said predetermined time unit to be set ahead by said predetermined pulse train, the subsequent opening of said manually operable switches causes said time setting to stop without causing the normal time keeping to proceed, the next closing of said display demand switch then re-sets said second bi-stable switch so that the subsequent opening of said display demand switch will re-set said third bi-stable switch and the normal time keeping function will proceed.

15. The improvement of claim 14 wherein said first bi-stable switch when in said set state disables the normal time keeping function of the timepiece as to said predetermined time unit.

* * * * *

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,765,163 Dated October 16, 1973

Inventor(s) Morris Meyer Levine and Arthur F. Cake

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

At Col. 3, line 33, after "are" insert --two--;

At Col. 4, line 67, after "any" insert --one--;

At Col. 7, line 22, after "its" insert --$\overline{Q}$--; and

line 23, delete "$\overline{Q}$" insert --Q--.

Signed and sealed this 19th day of February 1974.

(SEAL)
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