

[54] **TEMPERATURE COMPENSATED BIAS CIRCUIT**

[72] Inventor: **Thomas M. Frederiksen**, Scottsdale, Ariz.
[73] Assignee: **Motorola, Inc.**, Franklin Park, Ill.
[22] Filed: **Aug. 17, 1970**
[21] Appl. No.: **64,549**

Related U.S. Application Data

[62] Division of Ser. No. 701,235, Jan. 29, 1968, Pat. No. 3,538,424.
[52] U.S. Cl. **307/310, 307/318, 330/22, 330/40**
[51] Int. Cl. **H03k 17/14**
[58] Field of Search **330/40, 22; 307/318, 310**

[56] **References Cited**

UNITED STATES PATENTS

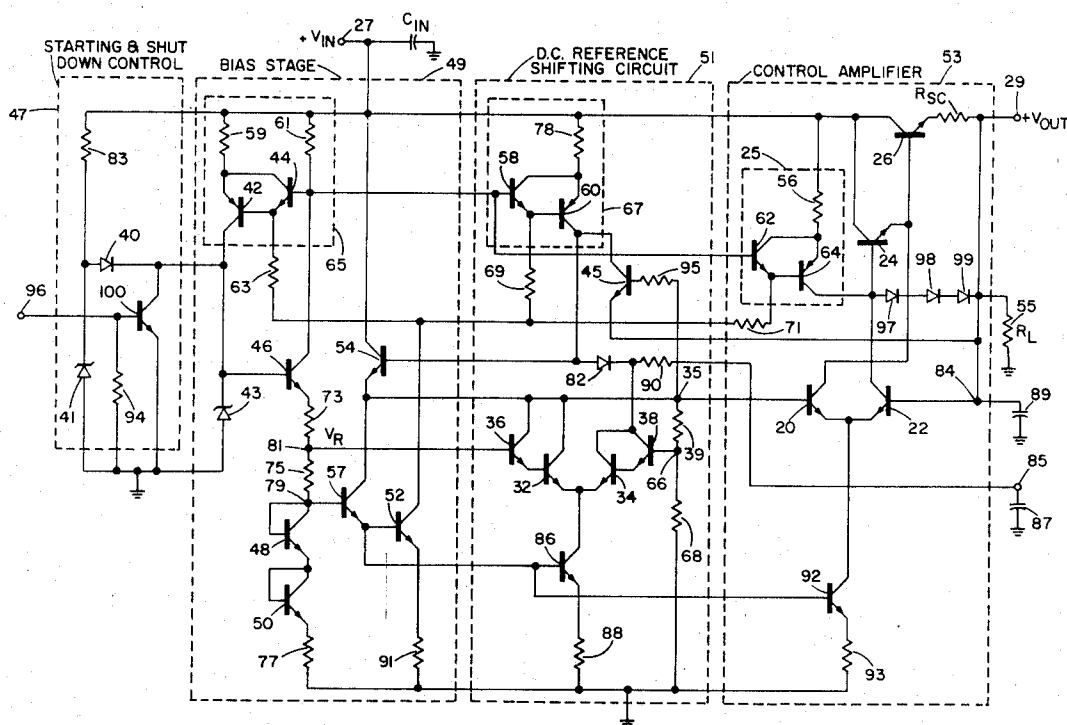
3,436,672	4/1969	Delagrange.....	307/318
3,271,660	9/1966	Hilbiber.....	307/318
3,262,062	7/1966	Langan.....	307/318
3,518,458	6/1970	Camezind.....	330/40
3,566,293	2/1971	Recklinghausen.....	330/22

Primary Examiner—James W. Lawrence
Assistant Examiner—Harold A. Dixon
Attorney—Mueller & Aichele

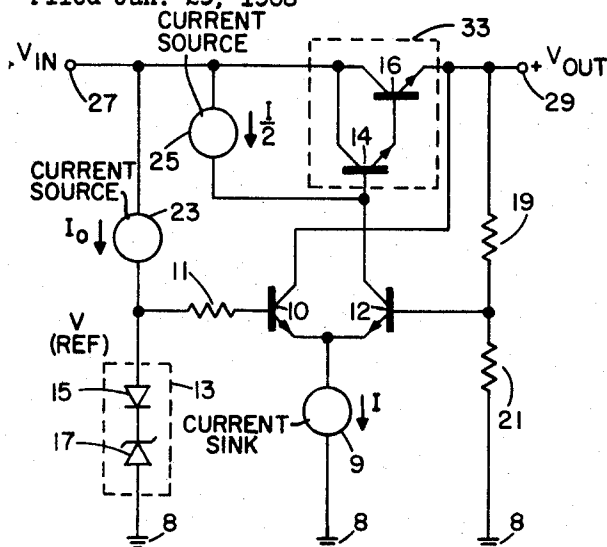
[57] **ABSTRACT**

Disclosed is a monolithic voltage regulator having a high current capability, a constant low output impedance from DC to several hundred kilocycles, and a high ripple reduction factor. The regulator has excellent transient response; it provides a wide range of regulated output voltage and has a low temperature drift. The voltage regulator includes a voltage standard or bias source, an input differential amplifier stage having a pair of transistors coupled to a current sink (a current source passing current to ground), and one of the transistors in the pair is connected through a current gain stage to an output terminal. A DC reference shifting circuit is connected to the input of one transistor in the pair and provides a reference voltage to the differential amplifier stage which has been translated to provide the required voltage level at the output terminal. The output terminal is connected directly to the input of the other transistor in the pair in order to achieve a unity feed back factor to provide excellent constant loop performance independent of the output voltage. The direct coupled feedback connection eliminates any undesirable gain loss and phase shifting due to resistance in the input circuits of the differentially coupled transistor pair.

6 Claims, 5 Drawing Figures



Filed Jan. 29, 1968



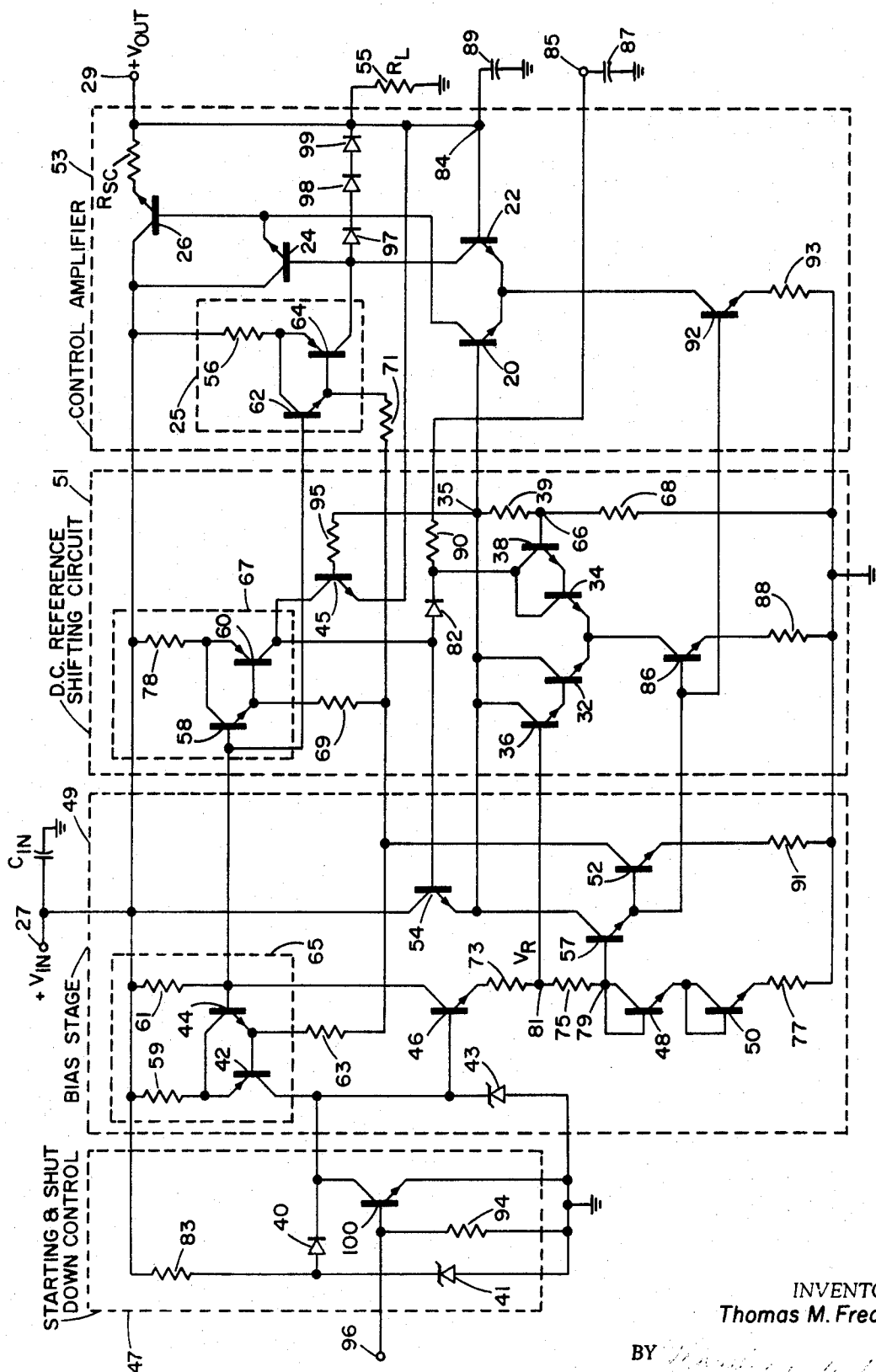


Fig.5

INVENTOR.
Thomas M. Frederiksen

BY *[Signature]*

ATTY'S.

TEMPERATURE COMPENSATED BIAS CIRCUIT

This application is a division of application Ser. No. 701,235, filed Jan. 29, 1968, now U.S. Pat. No. 3,538,424 by Thomas A. Fredericksen for "Voltage Regulator with Continuously Variable DC Reference."

BACKGROUND OF THE INVENTION

This invention relates generally to voltage regulators and more particularly to a monolithic series voltage regulator featuring improved AC and DC performance.

One conventional approach to series voltage regulation involves feeding the output voltage of the regulator back through a resistive divider feedback network to a differential amplifier stage thereof to provide the necessary DC voltage gain to achieve the required DC output voltage from a fixed, temperature-compensated reference voltage. A conventional prior art circuit using this approach is shown in FIG. 1 of the drawings and will be described further below in the detailed description of the invention.

This type of conventional prior art circuit and including various modifications thereof has several operational disadvantages, one of which being that the closed loop gain is dependent upon the output voltage. This output voltage dependence changes the feedback factor of the regulator circuit and degrades the closed loop performance thereof.

Another disadvantage of the prior art circuit in FIG. 1 is that the resistors which are connected in the input circuits of the differential amplifier stage cause a loss of gain of the stage, and further this resistance in combination with unavoidable capacitance produces a phase lag in the loop transmission (loop gain) which degrades the stability and frequency response thereof.

Another disadvantage of the circuit in FIG. 1 is that the resistors which are connected in the base circuits of the transistors of the differential amplifier stage produce undesirable DC voltage drops as a result of base current flow therein. These base resistors require a match in the current gain of the transistors and limit the maximum collector bias currents which can be used in the stage.

A further disadvantage of the conventional prior art circuit in FIG. 1 is that a pole-splitting capacitor (not shown) is usually connected between electrodes of one of the transistors in the differential amplifier stage. This pole-splitting capacitor causes a loss of frequency response within the amplifier and, in combination with additional load capacitance connected to the output of the voltage regulator, can cause the regulator to become unstable and provide undesired oscillations in the output waveform.

SUMMARY OF THE INVENTION

The present invention has been constructed to overcome all of the above-described disadvantages of the prior art circuit in FIG. 1 and includes as one objective thereof the provision of a new and improved monolithic series voltage regulator having both excellent DC temperature stability and improved AC performance.

Another object of this invention is to provide a monolithic series voltage regulator having a constant low output impedance from DC to several hundred kilocycles.

Another object of this invention is to provide a voltage regulator having a high ripple reduction factor and an excellent transient response for abrupt changes in load current.

A further object of this invention is to provide a voltage regulator operative over a wide range of output voltages and having a very low temperature drift of the output voltage.

The present invention features a monolithic series voltage regulator having a wideband feedback loop requiring capacitive compensation only at the output node of the regulator.

Another feature of this invention is the provision of a separate internal voltage regulator to supply a variable reference voltage to the main regulator.

Another feature of this invention is the provision of a series voltage regulator operating with unity closed-loop gain and

having no input resistance connected to the control differential amplifier stage thereof. The elimination of this input resistance results in increased loop gain, improved frequency response and eliminates biasing and DC drift problems due to input base current in the differential amplifier stage. Therefore, the performance of the regulator is independent of the output voltage setting used.

Another feature of this invention is a DC reference shifting circuit which provides a reference voltage for the main regulator and maintains this voltage at a substantially constant value independent of temperature. The low value input base currents to the differential amplifier portion of this reference shifting circuit allows an external resistor divider feedback network to be used to achieve the desired output voltage reference. This reference shifting circuit does not require an exact base resistance match at the input of the differential amplifier portion thereof.

Another feature of the present invention is the provision of tracking between PNP transistors forming constant current source for the collectors of the differential amplifiers in the regulator and the NPN current sinks which are connected to the emitters of these amplifiers. This current sink-current source tracking arrangement prevents the differential amplifiers from degrading the temperature stability of the overall regulator circuit as a result of unequal bias current changes.

Another feature of this invention is a provision of a control amplifier stage including a Darlington output current gain stage connected to a pair of differentially coupled transistors. The DC bias current of the unloaded collector of a transistor in the differential amplifier stage is used to prebias the input transistor of the Darlington stage. This biasing arrangement insures that this input transistor will always conduct a minimum current, i.e., guarantee transistor current gain of this transistor even for very low values of load current.

Another feature of this invention is a provision of bias circuitry to provide a basic reference voltage with a zero temperature coefficient which is derived from a zener diode with a positive temperature coefficient. This bias circuitry also provides a reference current with a zero temperature coefficient. This reference current is used to bias both the PNP current sources and the NPN current sinks in such a manner that both these current sources and sinks also have a zero temperature coefficient and also track in magnitude.

Another feature of this invention is a provision of a starting and shut-down circuit which can be externally electrically controlled to cause the complete regulator to enter a "shut-down" or "standby" mode of operation. When "shut-down," the DC bias current drain of the complete regulator will drop to a very low value and the output voltage will fall to zero volts.

Another feature of this invention is the inclusion of a lateral PNP device connected as a high voltage diode to prevent the discharge to the monolithic regulator circuit of the energy which may be stored on an externally connected noise filter capacitor.

Another feature of this invention is a provision of an internal regulator circuit which is easily made to pass only low frequencies by the use of a relatively small valued external capacitor. This band limiting is used to reduce the rms value of the noise which originates within the zener diode and would otherwise appear at the output of the regulator.

IN THE DRAWINGS

FIG. 1 is a schematic diagram of one conventional prior art circuit which will be described in order that the circuit of this invention may be better understood;

FIG. 2 is a schematic diagram of the main control amplifier portion of the series voltage regulator according to the present invention;

FIG. 3 is a DC reference shifting circuit which is connected between a point of basic zero temperature coefficient reference voltage, VR, and the main control amplifier of FIG. 2;

FIG. 4 is a block diagram illustration of the complete series voltage regulator of the present invention; and

FIG. 5 is a schematic diagram of the series voltage regulator embodying this invention.

DESCRIPTION OF THE INVENTION

Briefly described, the present invention is directed to a series voltage regulator having a main control amplifier portion including a differential transistor pair which is connected to a current sink. A Darlington current gain output stage is connected between one of the transistors in the differential pair and a circuit output terminal, and the other of the transistors in the pair is connected to an intermediate point in the Darlington stage to insure transistor current gain at low values of load current. A DC reference shifting circuit is connected between a reference voltage and the one transistor in the differential pair to provide a desired temperature stabilized DC reference potential for the main control amplifier which is equal to the desired output voltage. The input of the other transistor in the differential pair is connected directly to the output terminal of the regulator so that 100 percent of the output voltage is fed back to the differential pair, resulting in excellent AC performance of the regulator.

Referring in detail to FIG. 1, there is shown a conventional prior art series voltage regulator circuit including a pair of emitter-coupled transistors 10 and 12 connected to a current sink 9. A current gain stage 33 is connected to transistors 10 and 12 and includes transistors 14 and 16 therein which are connected in a Darlington connection. A zero temperature coefficient reference voltage device 13 including forward and zener diodes 15 and 17 respectively, is connected in series with a source of constant current 23 between an input voltage terminal 27 and a point of reference or ground potential 8. A resistive divider network, including resistors 19 and 21, is connected between the voltage output terminal 29 and a point of reference potential 8, and an intermediate point between resistors 19 and 21 is connected to the base of transistor 12. A base resistor 11 is connected between the voltage reference device 13 and the base of transistor 10 to provide a balancing resistance at the base of transistor 10 (equal to the impedance seen by the base of 12) and thus to provide a symmetrical circuit. Transistors 10 and 12 conduct current in the half to one milliamp range and this current is multiplied by the betas, i.e., current gains, of transistors 14 and 16 to provide an output load current in the hundred milliampere range.

In operation, a fraction of the voltage at the output terminal 29 is sampled at the base of transistor 12. If this potential rises higher than the reference voltage applied to transistor 10, transistor 12 will become more conductive than transistor 10 and divert more current from the current source 25 into the collector of 12. Such current diversion away from the base of transistor 14 reduces the output current and thus reduces the output voltage. This action stabilizes the voltage level at the output terminal 29 at a predetermined value. Conversely, when the voltage at the output terminal 29 swings lower than this value, transistor 10 will become more conductive than transistor 12 and thus more current from the current source 25 will begin to flow into the current gain stage 33, increasing the available load current and pulling up the output voltage.

The disadvantages of the prior art circuit in FIG. 1 have been set forth above in some detail but will be restated here with reference to the connections and components in the circuit in FIG. 1. One disadvantage of the circuit in FIG. 1 is that the voltage divider formed by resistors 19 and 21 causes the loop gain (or loop transmission) to change as the output voltage at terminal 29 changes. Accordingly, there is not a constant loop performance in FIG. 1 independent of the output voltage.

Another disadvantage of the circuit in FIG. 1 is that input capacitance, which appears at the bases of transistors 10 and 12, introduces phase lag in the loop which tends to make the circuit unstable. Additionally, the resistance at the base of transistors 10 and 12 will require matched current gains of

these transistors, will limit the maximum base current allowed, and will require matched temperature coefficients of resistance.

With the above disadvantages of the circuit of FIG. 1 in mind, the novel circuit according to the present invention will now be described. In FIG. 2 first and second emitter-coupled transistors 20 and 22 are connected to a current sink 9 and are further connected as shown to the Darlington current gain stage 31. Stage 31 includes transistors 24 and 26 which are connected emitter-to-base in the well known Darlington manner. The collector of transistor 20 is tied to the base of transistor 26 and to the emitter of transistor 24 to insure that the transistor 24 always conducts a minimum current to guarantee current gain of this device for small values of load current.

The base of the second emitter-coupled transistor 22 is tied directly to the output terminal 29 so that 100% of the output voltage is fed-back to transistor 22 and enables the circuit to operate with a feedback factor of one. This large amount of feedback results in excellent AC performance of the circuit. Resistors are not required at the bases of transistors 20 and 22, and the above-described disadvantages associated with these resistors are therefore not present.

The second emitter-coupled transistor 22 samples the output voltage, and compares it with the reference voltages at the base of transistor 20. The output voltage is compared with the reference voltage in such a manner as to compensate for changes in the output voltage due to variations in the load current. The Darlington current gain stage 31 is connected in a manner somewhat similar to the current gain stage 33 in FIG. 1 and a current source 25 is connected to the collector of emitter-coupled transistor 22 and to the base of transistor 24. Current will divide between transistors 22 and 24 during the sample and compare operation. The current source 25 will supply a current of $I/2$ where I is the total current through sink 9.

The reference voltage applied to the base of transistor 20 is provided by a DC reference shifting circuit which is similar to the circuit in FIG. 1 and is illustrated in FIG. 3. Since the circuit of FIG. 1 can be modified by introducing the unbiased Darlington connection shown in FIG. 3, excellent DC characteristics can be obtained. It is worth noting that this very low bias current operation of the input transistors in FIG. 3 provides excellent DC characteristics but degrades the high frequency performance of these devices. Thus not requiring good AC performance the DC operation can be optimized, whereas with the circuit of FIG. 1 the conflicting requirements between AC and DC performance force a compromised design, when the circuit is used as the control amplifier.

The DC reference shifting circuit in FIG. 3 includes a pair of emitter-coupled transistors 32 and 34 connected to a current sink 105 and further connected in a Darlington type connection to transistors 36 and 38. A single output transistor 45 is used for current gain and is connected to the collectors of transistors 32 and 36. A resistive bias network, including resistors 39 and 68, is connected between the terminal 35 and ground potential and provides a feedback signal to transistor 38. The output voltage at terminal 35 is sampled and compared with a reference voltage V_R at the input transistor 36, and the current flow into transistor 45 is controlled in accordance with the comparison of these two voltages to thereby maintain a constant regulated DC reference voltage at the output terminal 35. This reference voltage is used as the DC reference voltage at the base of transistor 20 in FIG. 2. Thus, the reference voltage applied to transistor 20 is temperature stabilized reference voltage equal in magnitude to the desired output voltage $+V_{OUT}$.

The DC reference shifting circuit in FIG. 3 will be better understood from the following description of the complete monolithic voltage regulator circuit illustrated in block diagram in FIG. 4 and in schematic diagram in FIG. 5. The circuit in FIG. 5 can be separated into the various stages shown in FIG. 4 which include a starting and shut-down circuit 47 con-

nected to a bias stage 49. The bias stage 49 is connected directly to the DC reference-shifting circuit 51 which, in turn, is connected to the control amplifier 53 as previously described. The regulator circuit in FIG. 4 further includes a short circuit current sampling resistance 59 connected between the control amplifier 53 and the output load, represented by resistor 55.

Referring now to FIG. 5, the reference numerals used to identify the control amplifier 53 and DC reference-shifting circuit 51 correspond to the reference numerals in FIGS. 2 and 3 respectively. Other reference numerals are used to note the additional circuit components in FIG. 5 not heretofore described, but some correspondence between reference numerals in FIGS. 2, 3, and 5 has been maintained to facilitate the understanding of these circuits.

The reference voltage V_R which is applied to the base of the transistor 36 in the DC reference shifting circuit 51 is derived from the voltage developed across the zener diode 43 in the bias stage 49. A first constant current source 65 provides a substantially constant current into the zener diode 43 so that the ripple feedthrough from the unregulated input is reduced. The voltage drop across resistor 61 establishes the reference voltage for all of the PNP current sources similar to 65, i.e., current sources 65, 67 and 25. This reference voltage is applied to transistor 44 and, as a result of the offsetting base-emitter voltages ($V_{BE's}$) of transistors 42 and 44, the voltage at the emitter of transistor 42 is essentially equal to the reference voltage at the base of transistor 44. Therefore, the voltage at the emitter of transistor 42 is controlled and the resulting current flow through resistor 59 is independent of variations in temperature.

The transistor 52 in the bias stage 49 serves as a constant current sink for the first constant current source 65 previously described and also for second and third constant current sources 67 and 25. These three current sources 65, 67 and 25 are connected to a first current sink transistor 52 via resistors 63, 69 and 71, respectively. The remaining resistive connections to the transistors 58 and 60 and transistors 62 and 64 in the current sources 67 and 25, respectively, are identical to the resistive connections previously described with reference to current source 65.

If transistor 42 in the current source 65 has a high current gain (beta), then the collector and emitter currents thereof will be substantially equal and very little current will flow out of the base lead of transistor 42 into resistor 63. Transistor 44 will therefore supply the required current to resistor 63. However, if the PNP transistor 42 should for some reason have a low beta, then this means that more current will flow out of the base lead of transistor 42 into resistor 63 and transistor 44 tends to turn off. Thus, this circuit automatically compensates for variations in the current gain of the lateral PNP transistor 42 which may exist between different fabrication batches of the circuit.

The base of transistor 42 is driven from the emitter of transistor 44 which has a low value base resistor 61 connected thereto. The resistance of resistor 61 is effectively reduced by the beta of transistor 44 so that transistor 42 is essentially being voltage source driven. Thus, with transistor 42 operating in the common base mode, a very high output impedance for transistor 42 is provided. Such high output impedance is desirable because it reduces the effect that any ripple on the input voltage applied to the regulator would have on the reference diode 43 or the differential amplifiers which are biased by the current sources 67 and 25.

The bias stage 49 further includes a temperature compensating network comprising reference transistor 46, diodes 48 and 50, and resistors 73, 75 and 77. The zener diode 43 and the resistors 73, 75 and 77 have positive temperature coefficients and the base to emitter diode of the transistor 46 and if the diode connected transistors 48 and 50 have negative temperature coefficients, whereby the voltage at the point 81 is independent of temperature. The emitter current of transistor 46 establishes the bias levels for the first, second and third cur-

rent sinks 52, 86 and 92 respectively, and the collector current of transistor 46 sets the current levels in the first, second and third current sources 65, 67 and 25. Thus, the three current sources 65, 67 and 25 and three current sinks 52, 86 and 92 are controlled by the biasing of a single NPN reference transistor 46. If reference transistor 46 has a relatively high alpha, which is 0.98 or higher for a high beta, then the emitter and collector currents of transistor 46 will be substantially equal and the same current will be used to reference all the current sources and all the current sinks in the regulator circuit. This feature insured excellent temperature tracking in the circuit. The current flowing in the above-described bias string, including emitter follower 46, is not dependent upon temperature so that, in effect, there is a zero temperature coefficient for the current flowing in all of the current sources and sinks.

The bias stage 49 further includes a buffer transistor 57 which is connected between the current sink transistor 52 and a point 79 in the bias string. This transistor reduces the loading effects on the current sink transistor 52. Further connected in the bias string 49 in NPN transistor 54 which interconnects the voltage input terminal 27 to the collectors of transistors 57, 36 and 32 and is connected at the base thereof to the diode 82 in the DC reference shifting circuit 51.

The bias stage 49 is so completely independent of the input voltage that, absent the starting and shut-down control circuit 47, the application of an input voltage will not start the regulator by biasing the zener diode 43 into conduction. For this reason, a starting and shut-down control circuit 47 is used and includes diode 40, transistor 100, zener diode 41, and resistors 83 and 94. When an input voltage is applied at terminal 27, current will flow through resistor 83, diode 40 and transistor 46. Current source 65 then becomes active and zener diode 43 comes into conduction. When zener 43 conducts, diode 40 turns off. As a result of zener diode 41, which has the same breakdown voltage as zener diode 43, there is no differential voltage across diode 40. Therefore, current will continue to flow through resistor 83 and into zener diode 41. If resistor 83 is large, e.g., 60 kilohms, and if the source of input voltage is in the order of 30 volts, then there will be approximately 400 microamperes flowing in the starting circuit, resulting in negligible power loss during normal operation of the regulator.

Additional circuitry is included to allow the complete regulator to have a "standby" or "shut-down" mode of operation. To enter "shut-down," clamping transistor 100 is brought into conduction by the application of an external positive voltage to pin 96 across resistor 94. When shut-down, all current sources and sinks go to zero current and the only bias drain is that current through resistor 83. Thus, the output voltage goes to zero and this feature is desired in some application areas where this electronic control would allow seldom needed circuits of a large system to be in a "stand by" mode with a substantial savings in power dissipation. For increased noise immunity in the starting and shut-down control circuit 47, one or more diodes (not shown) may be connected between terminal 96 and transistor 100.

When the external short circuit resistance represented by the external resistor R_{SC} samples large currents (R_{SC} being very small in the order of 1 or 2 ohms) it will threshold the string of three diodes 97, 98, and 99 and cause the available current from transistor 64 to be bypassed around the Darlington output stage consisting of transistors 24 and 26. The output voltage at 29 will therefore fall toward ground. Transistor 45 will detect this reduction in V_{OUT} and will be driven into conduction. This action will cause the reference voltage at point 35 to also fall toward ground.

A resistive divider, including external resistors 39 and 68 is connected in the DC reference shifting circuit 51 between point 35 and ground and is further tied to the base of transistor 38 in the manner described with reference to FIGS. 1 and 3. The bandwidth of the reference shifting circuit 51 is reduced by the external capacitor 87 which serves to stabilize the am-

plifier and reduce the rms value of the zener noise which is present at the output of the regulator. An additional diode 82 is used to isolate capacitor 87 from the circuit in the event of a short circuit at the output node 29, and prevent capacitor 87 from discharging into and possibly damaging the integrated circuit.

In the monolithic version of the voltage regulator shown in FIG. 5, the points 35, 66, 84 and 85 were made external to the die itself and are sometimes referred to as pins. These points or pins may be used to interconnect external capacitors, resistors and the like. For example, resistors 39 and 68 are connected externally to the die in the circuit (FIG. 5) of the type described which was actually built and successfully tested. However, if desired, these resistors could be formed by diffusion or other similar techniques using known NPN monolithic semiconductor processing technology.

Output capacitor 89 is connected directly to the output of the control amplifier 53. This capacitor is used to stabilize the control amplifier and also to maintain a low output impedance at high frequencies. The feedback of circuit 53 is effective from DC out to some high frequency at which the circuit begins to lose bandwidth. At such high frequency, the loop transmission cannot respond sufficiently to prevent the output impedance from rising. In order to counteract this increase in output impedance at high frequencies, the capacitor 89 is connected across the output of stage 53 to hold the output impedance down at high frequencies. Thus, the capacitor 89 can deliver high frequency current to the load without the necessity of having the loop active. Therefore, by adding capacitor 89, a dominant pole is created directly at the output of the regulator and any increased capacitance at the output 29 will improve the stability of the regulator.

Thus, a monolithic voltage regulator circuit has been described wherein a control amplifier stage 53 is connected with a feedback loop tied directly to the output terminal 29 so that 100 percent of the output voltage is fed back to transistor 22. This feature insures excellent AC performance of the regulator. At the same time, a varying DC reference potential is applied at the input of transistor 20 and this potential is derived from a reference shifting circuit 51 having a resistive feedback loop therein. This circuitry enables the control amplifier portion 53 of the voltage regulator to be driven by a varying DC reference voltage which imparts to the overall voltage regulator excellent DC stability.

The following table of values is given by way of illustration only and is not intended to limit the scope of this invention. Such values were used in a circuit of the type described with reference to FIG. 5 which has been actually built and successfully tested.

TABLE

Resistors (R)	Value (Ohms) or fd
R39 Depends on V_{OUT} DESIRED External to die.	3300—For V_{OUT} of 5 volts
R55 Used to simulate current loading of regulator External to die.	
R56	514
R59	514
R61	834
R63	1600
R69	3200
R71	1600
R73	4630
R75	2670
R77	700
R78	1000
R83	60000
R68 Depends on V_{OUT} desired External to die	7500—For V_{OUT} of 5 volts

R88	834
R90	50
R91	625
R93	416
R94	5000
R95	1000
R _{SC} Depends on maximum load current desired	
External to die	1
C _{IN} External to die	2
C87 External to die	0.1
C89 External to die	50
V _R	+3.4 Volts DC
V _{OUT} —For R39 and R68 as listed	+5.0 Volts DC
V _{IN}	+8.2 Volts Min 30 Volts Max.

What is claimed is:

1. A temperature-independent bias stage for producing a standard voltage, having an input terminal and an output terminal, comprising:

a Zener diode;

constant current means for causing a constant current to flow through the Zener diode to a first terminal so that a constant voltage is produced across the Zener diode;

a reference transistor, having two main electrodes oppositely positioned between the input terminal and the output terminal, and having a control electrode;

at least one other diode connected between the output terminal and the first terminal; two of said semi-conducting elements having opposite temperature coefficients, and

means for connecting the control electrode between the constant current means and the Zener diode so that the constant voltage appears across the control electrode and the other diode, causing a constant current to flow through the two main electrodes of the reference transistor and the other diode to the first terminal, to produce a reference voltage between the output terminal and the first terminal for application to a load.

2. The invention of claim 1 in which the constant current means comprises a PNP and an NPN transistor each having an emitter, a collector and a base, a connection to a source terminal by way of respective resistors to the emitter of said PNP transistor and to the base of said NPN transistor, and a connection between the emitter of said NPN transistor to the base of said PNP transistor, said collector of said PNP transistor being connected to said Zener diode.

3. The invention of claim 1 in which said diode comprises an NPN transistor having its base short circuited to its collector.

4. The invention of claim 3 in which a resistor is connected between a main electrode of the reference transistor and said other diode and the output terminal is connected to a point between said resistor and the reference transistor.

5. The invention of claim 4 in which a fourth and a fifth transistor each having main electrodes and a control electrode are provided, the output terminal being connected to the control electrode of said fourth transistor, and a main electrode of said fourth transistor being connected to the control electrode of said fifth transistor and the emitter of said NPN transistor being connected by way of the main electrode of said fifth transistor to the first terminal, whereby said fourth transistor acts to prevent said fifth transistor from loading the circuit between the reference transistor and said first terminal.

6. The invention of claim 5 in which said Zener diode has positive temperature coefficient voltage produced thereacross, said first resistor has positive temperature coefficient of resistance, the reference transistor and said other diode have negative coefficient of voltage drop from the base to the emitters thereof, whereby the variation in the voltage applied to said load with variations in temperature is reduced.

* * * * *