(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 366 495 B1**

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **07.09.94 Bulletin 94/36**

(51) Int. Cl.^{5} : **G04G 15/00**

(21) Application number : **89311133.6**

(22) Date of filing : **27.10.89**

(54) Numerical value setting device.

(30) Priority : **28.10.88 JP 272460/88**

(43) Date of publication of application : **02.05.90 Bulletin 90/18**

(45) Publication of the grant of the patent : **07.09.94 Bulletin 94/36**

(84) Designated Contracting States : **AT BE CH DE ES FR GB GR IT LI LU NL SE**

(56) References cited :
GB-A- 2 188 749
PATENT ABSTRACTS OF JAPAN, vol. 10, no. 229 (P-485)(2285) 8 August 1986; & JP-A-61 062 891
PATENT ABSTRACTS OF JAPAN, vol. 7, no. 220 (P-226) 30 September 1983; & JP-A-58 113 889

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EP 0 366 495 B1

Description

This invention relates to a method of registering numerical values and an apparatus therefor which can set numerical values regardless or its connection to or disconnection from an electric power source.

A conventional electronic numerical value setting device exists in which a numerical value may be set by a keying operation whether or not the device is connected to an electric power source. The numerical value thus set is automatically registered by the device for a predetermined period of time after the keying operation.

However, this conventional electronic numerical value setting device has several disadvantage. The power supply may be interrupted or restored during the keying operation, or during an automatic registering latency time. The automatic registering latency time is that period of time which elapses between the completion of a keying operation and the registering of the numerical value. Power supply interruption during the keying operation or the latency time results in setting an incomplete numerical value. Since the incomplete numerical value set is different from the intended numerical value, erroneous operation or the system results.

In addition, it is also possible that numerical data is registered during the latency time which elapses from the instant that the keying operation is ended until the desired numerical value is automatically registered. The value registered during the latency period before the time instant at which automatic registering normally occurs cannot be corrected. Accordingly the setting of the numerical value must be carried out again. This is rather troublesome for an operator.

Accordingly, it is an object of the invention to eliminate the above-described difficulties accompanying a conventional numerical value setting device. More specifically, an object of the invention is to provide a numerical value setting device in which, if the power supply is interrupted or restored during a numerical value setting operation, the numerical value being keyed will not be registered and the keying operation is not adversely affected. When the power supply is interrupted or restored during the automatic registering latency time, the numerical value set is registered after a lapse of the remaining latency time, that is, at the automatic registering time.

JP-A-61-062891 discloses a device for setting a timer in which a value is set, then automatically registered after a predetermined time. The power supply for the device is not discussed in detail.

GB-A-2188749 discusses a timer device with a back-up supply which is based on a microprocessor. The microprocessor runs at a constant clock frequency, but is arranged to be powered up or down at varying intervals, depending on whether or not a main supply is connected. The timer is set by entering values, and manually registering them by pressing an "ENTER" key.

JP-A-58-113889 discusses a timer device in which a back-up supply is provided, and operation is switched from a precision high-frequency oscillator to a low power, low-frequency oscillator when the back-up supply is used.

The present invention provides a method of registering numerical values comprising:

setting an automatic registration latency time;

setting a counter to operate as a timer;

setting a numerical value;

counting with said timer a number of clock cycles after setting the numerical value, to determine the end of said automatic registration latency time;

registering the numerical value at the end of said automatic registration latency time; wherein the timer runs at a first clock rate in the presence of a main power supply, and at a second clock rate in the absence of the main power supply; and

a change in the clock rate between the first and second clock rates causes a variation in the number of clock cycles to be counted such that the latency time is unchanged.

The present invention provides an apparatus for registering numerical values comprising:

input means for setting numerical values;

means for setting an automatic registration latency time;

a timer for counting a number of clock cycles after setting the numerical value to determine the end of said automatic registration latency time;

means for registering the numerical value at the end of said automatic registration latency time;

means for displaying the numerical value;

wherein there are means for detecting the presence or absence of a main power supply;

the timer is arranged to operate at a first clock rate in the presence of the main power supply, and at a second clock rate in the absence of the main power supply; and

there are means for calculating the number of clock cycles to be counted in response to a change in the clock rate between the first and second clock rates such that latency time is unchanged.

Thus the present invention may provide a numerical value setting device capable of setting and registering a numerical value, without the time for registering the value being affected, regardless of the main power supply condition.

That is, the numerical value setting device of the invention is so designed that the operation of setting a numerical value, the operation of registering the set value, and the automatic set value registering time are not affected even when the electric power supply condition is changed. Even if the electric power supply is interrupted or restored while setting a numerical value, a numerical value which has not been com-

pletely set will not be registered, and the true value can be set later as usual. Hence, the device will not incorrectly register a numerical value other than the desired numerical value. Furthermore, even if the electric power supply to the device is suspended or restored during the automatic registering latency time, which occurs after the keying operation for setting a numerical value, the st value can be corrected during that automatic registering latency time. Thus, the numerical value setting device of the invention has practical use.

In the drawings:

FIG. 1 is a diagram showing one example of the use of the preferred embodiment of the invention.

FIG. 2 is a block diagram showing the arrangement of the counter shown in FIG. 1.

FIG. 3 is a diagram of the front panel of the counter shown in FIG. 1.

FIGS. 4 and 5 are flow charts describing the operation of an embodiment of the invention.

FIGS. 6 through 10 are explanatory diagrams which describe the operation of the embodiment of the invention.

FIG. 6 shows the display of the present count (3000) and a zero suppressed preset value (2500).

FIG. 7 shows the display of a flickering place of the present value.

FIG. 8 shows the operation of the shift key.

FIG. 9 shows the operation of the up key.

FIG. 10 shows display of the present count and present value when the number of stages is one.

The preferred embodiment of this invention will be described with reference to the accompanying drawings.

As one application of the invention, and not by way of limitation,, FIG. 1 shows that a slider 10 is moved back and forth as a ball screw 12 rotates. The ball screw 12 is rotated through a speed reducer 14 by an electric motor 16. The electric motor 16 is provided with a rotary encoder 18. The output pulse of the rotary encoder 18 is applied to an counter 20 to which the technical concept of the invention is applied.

As shown in FIG. 2, the counter 20, has an input circuit 22 to which the encoder 18 can be connected, a key switch circuit 24, a function setting circuit 26, an LCD driving clock generating circuit 28, a system clock generating circuit 30, an LCD reference voltage generating circuit 32, and LCD display unit 34, a non-contact output inversion circuit 36, an output circuit 38, a power source circuit 40, a battery 42, serving as an auxiliary power source for supplying the electric power when the ordinary power source is interrupted, a power supply interruption detecting circuit 44, and a data processing circuit 46. The data processing circuit 46 has a ROM 48, a RAM 50, and LCD driver 52, a counter circuit 54, an a CPU 56.

When the count value of the output pulses of the encoder 18, which are applied to the input circuit 22, coincides with a value preset by a key sequence, the output circuit 38 supplies a coincidence signal to a control circuit (not shown). A switching signal provided by an output inversion switch (not shown) is applied to the non-contact output inversion circuit 36.

FIG. 3 shows the front panel of the counter 20. The LCD display 34, a teach mode key 58, a mode key 60, a shift key 62, and up key 64, a teach key 66, and a reset key 68 are provided on the front panel of counter 20.

The LCD display unit 34 has mode displays 300, 302, and 304 displaying a number of stages of a preset value, and input and output modes. A "power on" display is indicated at 306. A control output display is indicated at 308. A count value display is indicated at 310 to display a current count value with zero suppression. A preset value display is indicated at 312 to display the contents of an operation mode when set.

FIGS. 4 and 5 are flow charts describing the operation of the embodiment of the invention. In Step 400, a digit of a numerical value begins flickering, and then a flickering timer is reset in Step 402. In Step 404 it is detected whether or not a key input is provided.

If no key input is detected, in Step 406 it is determined whether or not the flickering timer reset in step 402 has timed out. If the flickering timer has not yet timed out, Step 404 is repeated. Otherwise Step 308 is activated.

In step 408, detects whether or not a numerical value is being displayed. If "yes", the display of the numerical value is stopped in Step 410; and if "no", the display of the numerical value is carried out again in Step 412. In each case, Step 402 is effected again, resetting the flickering timer. Thus, on the LCD display unit 34, the display of the numerical value at the designated place flickers for a predetermined period of about one second.

If in Step 404 a key is detected, then in step 500 it is determined whether or not the operation key detected is the reset key 68. If "yes", a reset operation is carried out. If "no", in Step 502 it is next determined whether or not the operation key is the mode key 60. If "no", in Step 504 it is determined whether or not the operation key is the shift key 62. If "yes" a shifting operation described below is performed. If "no", it is determined in Step 506 whether or not the operation key is the up key 64. If it is determined that all these keys are not operated, Step 406 is carried out again. If either the shift or up key is operated, control is returned to Step 402 upon completion of the corresponding operation.

Operation of the mode key 60, causes selecting the stage number for a preset value. FIG. 6. shows an example of a display when the operation causes setting a preset value at the second stage. The present count, "3000", is displayed (Step 518), and a preset value "2500" is displayed being zero-suppressed.

When, under this condition, the shift key 62 or the up key 64 is operated (Step 520), a numerical value can be set (Step 522), so that the display of the least significant digit "0" of the preset value is flickered, as shown in FIG. 7.

The location of the flickering is shifted as shown in FIG. 8 each time the shift key 62 is operated (Step 508). The previously flickering digit is displayed continuously (Step 510). The display of the digit at the new flickering location is then forcibly stopped in Step 512, and Step 402 which initiates a flickering timer (FIG. 4) is carried out again.

On the other hand each time the up key 64 is operated, the numerical value at the flickering location is incremented consecutively (Step 514), as shown in FIG. 9, the incremented digit at the flickering location is displayed at each time of pressing the up key 64 (Step 516).

Thus, when the movement of the flickering location is indicated by operating the shift key 62, the display of the digit at the place to be changed is stopped temporarily (Steps 512, 402, 408, 410 and 412).

Therefore, the place to be changed can be readily detected, and the set value (preset value) can be quickly and readily changed by operating the up key 64. When the change is accepted in Step 524, the set value is registered (Step 526).

In the case where the number of stages is one that is at the first stage, the number of stages of a preset value is not displayed as shown in FIG. 10.

The above-described operation is applicable not only to a numerical value such as a preset value but also to other set parameters.

During a numerical value setting operation with the up key 64 or the shift key 62, or when the keying operation is ended (Step 524), a set value registering timer is started (Step 530) to run for a predetermined period of time. Thus, at the lapse of the time set in the set value registering timer, the set value is automatically registered.

The specific feature of the numerical value setting device according to the invention resides in that, when the power supply is interrupted or restored during the numerical value setting operation or during the automatic registering latency time, the device is not already effected. That is, the device can achieve the numerical value setting operation and the set value registering operation satisfactorily, as described below.

In the numerical value setting device of the invention, the CPU operating clock frequency is changed depending on whether or not the power supply is interrupted, because power consumption varies in proportion to the variations in the clock frequency. In an ordinary state, the clock frequency is about several MHz whereas it is about 100 KHz when the battery is employed on behalf of the ordinary power supply. When the power supply is interrupted or restored during operation of the set value registering timer; i.e., before the set value is registered, as in Step 528, it is necessary to change the value set in the set value registering timer separately according to the states of the power supply (Step 532).

A procedure for changing the value set in the set value registering timer is described below.

In the numerical value setting device of the invention, the automatic registering latency time is previously set to 5 sec in the set value resistering timer by the manufacturer.

When electrical power is supplied to the device, clock pulses counted by the set value resistering timer, have a clock period of 5 ms. Therefore, counting 1000 clock pulses reaches 5 sec. When the electric power supply to the device is interrupted, the clock pulses counted by the set value registering timer have a clock period of 60 ms. Thus, when the electric power supply to the device is interrupted, counting 83 clock pulses reaches 5 sec. It should be noted that when electric power is interrupted, the circuits of the device can be powered by battery 42.

Consider the case where the electric power supply is maintained unchanged and then interrupted. Assume while the electric power supply to the device is maintained unchanged, and the electric power supply to the device is interrupted when two seconds is counted by the set value registering timer. Beginning at this time it is necessary to operate a set value registering timer to input 60 ms-period clock pulses (Step 525) for the case where the electric power supply to the device is interrupted. For this purpose, in Step 532 the number of clock pulses, that is, the number of interruptions used for counting the resistering latency time, which is set in the set value registering timer when the electric power supply is interrupted, is calculated. First, in order to detect the remaining three seconds, the following arithmetic operation is carried out:

Remaining time = 5 sec. -{(the number of clock pulses counted during the electric power supply) x 5 ms) The calculation will result in 3 seconds (Step 527).

Next, the count value X, that is, the number of clock pulses counted by the set value registering timer when the electric power supply to the device is interrupted is obtained as follows:

$$X = (\text{remaining time}) \times \frac{1}{60\text{ms}}$$

The value x = 50 is thus obtained and newly set in the set value registering timer. As previously noted, the 60 ms-period clock pulses are used when the electric power supply to the device is interrupted, e.g. after 2 seconds of maintained electric power, as in the present example.

In the case where the electric power supply to the device is restored, the operation is carried out in the same but a reverse manner. Thus, the operation in

Step 532 has ben accomplished.

That is, in the device of the invention, when the up key operation or shift key operation is accomplished under the normal condition ("yes" in Step 524), the set value registering timer starts (Step 530), and at the end of a predetermined period of time (the automatic registering latency time), the set value is automatically registered (Step 526).

On the other hand, in the case where, during or after the above-described key operation, the set value registering timer starts, and the electric power supply condition is changed ("yes" in Step 528), a count value set in the set value registering timer is changed, and a new count value (to count, for example, three seconds as in the above-described case) is newly set in the timer. Therefore, even when the electric power supply to the device is interrupted, the desired set value can be correctly registered. Even if the electric power supply to the device is interrupted during the automatic registering latency time after the key operation has been accomplished for setting a numerical value, the set value is automatically registered at the end of the predetermined latency time as usual, and therefore the set value can be corrected during the automatic registering latency time.

As was described above, even when the electric power supply to the numerical value setting device is interrupted or restored during the numerical value setting operation or the automatic registering latency time, the device is not affected thereby; that is, it can register the set value in the same manner at all times.

Claims

1. A method of registering numerical values comprising:

setting an automatic registration latency time;

setting a counter to operate as a timer (54);

setting a numerical value;

counting with said timer (54) a number of clock cycles after setting the numerical value, to determine the end of said automatic registration latency time;

registering the numerical value at the end of said automatic registration latency time (526);

characterised in that:

the timer runs at a first clock rate in the presence of a main power supply (40), and at a second clock rate in the absence of the main power supply (40); and

a change in the clock rate between the first and second clock rates causes a variation in the number of clock cycles to be counted such that the latency time is unchanged.

2. A method according to claim 1, wherein registering the numerical value comprises detecting the end of said automatic registration latency time with said timer (54).

3. A method according to claim 1 or claim 2, wherein said automatic registration latency time is set to a constant value.

4. A method according to any one of the preceding comprising:

calculating the time elapsed since the setting of the numerical value, based on the number of clock cycles counted by said timer at one of said clock rates in a corresponding one of two power supply conditions, the conditions being respectively presence or absence of the main power supply;

detecting the other one of said power supply conditions;

subtracting the elapsed time from said automatic registrations latency time to determine said remaining time; and

dividing said remaining time by the other one of said clock rates to determine the number of clock cycles to be counted by said timer at said other one of said clock rates to reach the end of said automatic registration latency time.

5. Apparatus for registering numerical values comprising:

input means (63,64) for setting numerical values;

means for setting an automatic registration latency time;

a timer (54) for counting a number of clock cycles after setting the numerical value to determine the end of said automatic registration latency time;

means for registering the numerical value at the end of said automatic registration latency time;

means (34) for displaying the numerical value;

characterised in that:

there are means (44) for detecting the presence or absence of a main power supply;

the timer (54) is arranged to operate at a first clock rate in the presence of the main power supply, and at a second clock rate in the absence of the main power supply; and

there are means for calculating the number of clock cycles to be counted in response to a change in the clock rate between the first and second clock rates such that latency time is unchanged.

6. Apparatus according to claim 5, comprising

means for setting said automatic registration latency time to a constant value.

7. Apparatus according to claim 5 or 6, comprising:
means for calculating the time elapsed since the setting of the numerical value, based on the number of clock cycles counted by said timer at one of said clock rates in a corresponding one of two power supply conditions, the conditions being respectively presence or absence of the main power supply;
means for subtracting the elapsed time from said automatic registration latency time to determine said remaining time;
means for dividing said remaining time by the other one of said clock rates to determine the number of clock cycles to be counted by said timer at said one of said clock rates to read the end of said automatic registration latency time.

Patentansprüche

1. Verfahren zum Registrieren eines numerischen Wertes umfassend:
das Setzen bzw. Einstellen einer automatischen Registrierungslatenzzeit;
das Setzen bzw. Einstellen eines Zählers, um als Zeitnehmer (54) zu dienen;
das Setzen bzw. Einstellen eines Zahlenwertes;
das Zählen mit genanntem Zeitnehmer (54) einer Anzahl an Taktzyklen nach dem Setzen bzw. Einstellen des Zahlenwerts, um das Ende der genannten automatischen Registrierungslatenzzeit zu bestimmen;
das Registrieren des Zahlenwerts am Ende der genannten automatischen Registrierungslatenzzeit (526);
dadurch gekennzeichnet, daß
der Zeitnehmer mit einer ersten Taktrate bei Vorhandensein einer Hauptstromversorgung (40) läuft und mit einer zweiten Taktrate bei Nichtvorhandensein der Hauptstromversorgung (40) läuft; und
eine Änderung in der Taktrate zwischen der ersten und der zweiten Taktrate eine Variation der Anzahl an zu zählenden Taktzyklen bewirkt, sodaß die Latenzzeit unverändert bleibt.

2. Verfahren nach Anspruch 1, worin das Registrieren des Zahlenwerts das Erkennen des Endes der genannten automatischen Registrierungslatenzzeit mit dem genannten Zeitnehmer (54) umfaßt.

3. Verfahren nach Anspruch 1 oder Anspruch 2, worin die genannte automatische Registrierungslatenzzeit auf einen konstanten Wert eingestellt ist.

4. Verfahren nach einem der vorhergehenden Ansprüche umfassend:
das Errechnen der abgelaufenen Zeit seit dem Setzen bzw. Einstellen des Zahlenwerts auf der Grundlage der Anzahl an Taktzyklen, die durch den genannten Zeitnehmer mit einer der genannten Taktraten entsprechend den zwei Stromversorgungsbedingungen gezählt wurde, wobei die Bedingungen jeweils das Vorhandensein oder Nichtvorhandensein der Hauptstromversorgung sind;
das Erkennen der anderen der genannten Stromversorgungsbedingungen;
das Subtrahieren der abgelaufenen Zeit von der genannten automatischen Registrierungslatenzzeit, um die genannte verbleibende Zeit zu bestimmen; und
das Dividieren der genannten verbleibenden Zeit durch die andere der genannten Taktraten, um die Anzahl an Taktzyklen zu bestimmen, die durch den genannten Zeitnehmer bei der anderen der genannten Taktraten zu zählen ist, um das Ende der genannten automatischen Registrierungslatenzzeit zu erreichen.

5. Vorrichtung zum Registrieren von Zahlenwerten umfassend:
Eingabemittel (63, 64) zum Setzen bzw. Einstellen von Zahlenwerten;
Mittel zum Setzen bzw. Einstellen einer automatischen Registrierungslatenzzeit;
einen Zeitnehmer (54) zum Zählen einer Anzahl an Taktzyklen nach dem Einstellen des Zahlenwerts, um das Ende der genannten automatischen Registrationslatenzzeit zu bestimmen;
Mittel zum Registrieren des Zahlenwerts am Ende der genannten automatischen Registrationslatenzzeit;
Mittel (34) zum Anzeigen des Zahlenwerts;
dadurch gekennzeichnet, daß:
Mittel (44) zum Erkennen der Gegenwart oder Abwesenheit einer Hauptstromversorgung vorhanden sind;
der Zeitnehmer (54) angeordnet ist, um bei einer ersten Taktfolge in Gegenwart der Hauptstromversorgung und bei einer zweiten Taktfolge in Abwesenheit der Hauptstromversorgung zu funktionieren; und
Mittel zum Errechnen der Anzahl an Taktzyklen vorhanden sind, die als Reaktion auf eine Änderung der Taktfolge zwischen der ersten und zweiten Taktfolge zu zählen ist, sodaß die Latenzzeit unverändert bleibt.

6. Vorrichtung nach Anspruch 5, umfassend Mittel zum Einstellen der genannten automatischen Re-

gistrierungslatenzzeit auf einen konstanten Wert.

7. Vorrichtung nach Anspruch 5 oder 6, umfassend:
Mittel zum Errechnen der abgelaufenen Zeit seit dem Einstellen des Zahlenwerts auf der Grundlage der Anzahl an Taktfolgen, die durch den genannten Zeitnehmer bei einer der genannten Taktfolgen in einer entsprechenden der zwei Stromversorgungsbedingungen gezählt wurde, wobei die Bedingungen jeweils das Vorhandensein oder Nichtvorhandensein der Hauptstromversorgung sind;
Mittel zum Subtrahieren der abgelaufenen Zeit von der genannten automatischen Registrierungslatenzzeit, um die genannte verbleibende Zeit zu bestimmen;
Mittel zum Dividieren der genannten verbleibenden Zeit durch die andere der genannten Taktraten, um die Anzahl an Taktzyklen zu bestimmen, die durch den genannten Zeitnehmer bei einer der genannten Taktraten zu zählen ist, um das Ende der genannten automatischen Registrierungslatenzzeit zu erkennen.

Revendications

1. Procédé d'enregistrement de valeurs numériques comprenant :
ajuster un temps de latence d'enregistrement automatique;
ajuster un compteur pour fonctionner comme une temporisation (54);
ajuster une valeur numérique;
compter avec ladite temporisation (54) un nombre de cycles d'horloge après l'ajustage de la valeur numérique, pour déterminer la fin du temps de latence d'enregistrement automatique;
enregistrer la valeur numérique à la fin du temps de latence d'enregistrement automatique (526);
caractérisé en ce que :
la temporisation s'écoule à une première fréquence d'horloge en la présence d'une alimentation en courant du secteur (40), et à une seconde fréquence d'horloge en l'absence de l'alimentation en courant du secteur (40);
un changement dans la fréquence d'horloge entre les première et seconde fréquences d'horloge provoque une variation dans le nombre de cycles d'horloge à compter de sorte que le temps de latence est inchangé.

2. Procédé selon la revendication 1, dans lequel l'enregistrement de la valeur numérique comprend la détection de la fin du temps de latence d'enregistrement automatique précité par la temporisation précitée (54).

3. Procédé selon la revendication 1 ou la revendication 2, dans lequel le temps de latence d'enregistrement automatique précité est ajusté à une valeur constante.

4. Procédé selon l'une quelconque des revendications précédentes comprenant :
calculer le temps écoulé depuis l'ajustement de la valeur numérique, sur la base du nombre de cycles d'horloge comptés par la temporisation précitée à l'une précitée des fréquences d'horloge dans l'une correspondante de deux conditions d'alimentation, les conditions étant respectivement la présence ou l'absence de l'alimentation de courant du secteur;
détecter l'autre desdites conditions d'alimentation;
soustraire le temps écoulé à partir du temps de latence d'enregistrement automatique pour déterminer le temps restant; et
diviser le temps restant par l'autre desdites fréquences d'horloge pour déterminer le nombre de cycles d'horloge à compter par la temporisation à l'autre desdites fréquences d'horloge pour atteindre la fin du temps de latence d'enregistrement automatique.

5. Dispositif pour enregistrer les valeurs numériques comprenant :
un moyen d'entrée (63, 64) pour ajuster des valeurs numériques;
un moyen pour ajuster un temps de latence d'enregistrement automatique;
une temporisation (54) pour compter un nombre de cycles d'horloge après ajustage de la valeur numérique pour déterminer la fin de temps de latence d'enregistrement automatique;
un moyen pour enregistrer la valeur numérique à la fin du temps de latence d'enregistrement automatique;
un moyen (34) pour visualiser la valeur numérique;
caractérisé en ce que :
des moyens (44) sont prévus pour détecter la présence ou l'absence d'une alimentation en courant du secteur;
la temporisation (54) est agencée pour fonctionner à une première fréquence d'horloge en la présence de l'alimentation en courant du secteur, et à une seconde fréquence d'horloge en l'absence de l'alimentation en courant du secteur; et
des moyens sont prévus pour calculer le nombre de cycles d'horloge à compter en réponse à un changement dans la fréquence d'horloge entre les première et seconde fréquences d'horloge de telle sorte que le temps de latence est inchangé.

6. Dispositif selon la revendication 5, comprenant un moyen pour ajuster le temps de latence d'enregistrement automatique précité à une valeur constante.

7. Dispositif selon la revendication 5 ou 6, comprenant :

un moyen pour calculer le temps écoulé depuis l'ajustement de la valeur numérique, sur la base du nombre de cycles d'horloge compté par la temporisation précitée à l'une des fréquences d'horloge précitées dans l'une correspondante de deux conditions d'alimentation, les conditions étant respectivement la présence ou l'absence de l'alimentation en courant du secteur;

un moyen pour soustraire le temps écoulé du temps de latence d'enregistrement automatique pour déterminer le temps restant;

un moyen pour diviser le temps restant par l'autre desdites fréquences d'horloge pour déterminer le nombre de cycles d'horloge à compter par la temporisation à l'une desdites fréquences d'horloge pour lire la fin du temps de latence d'enregistrement automatique.

FIG. 1

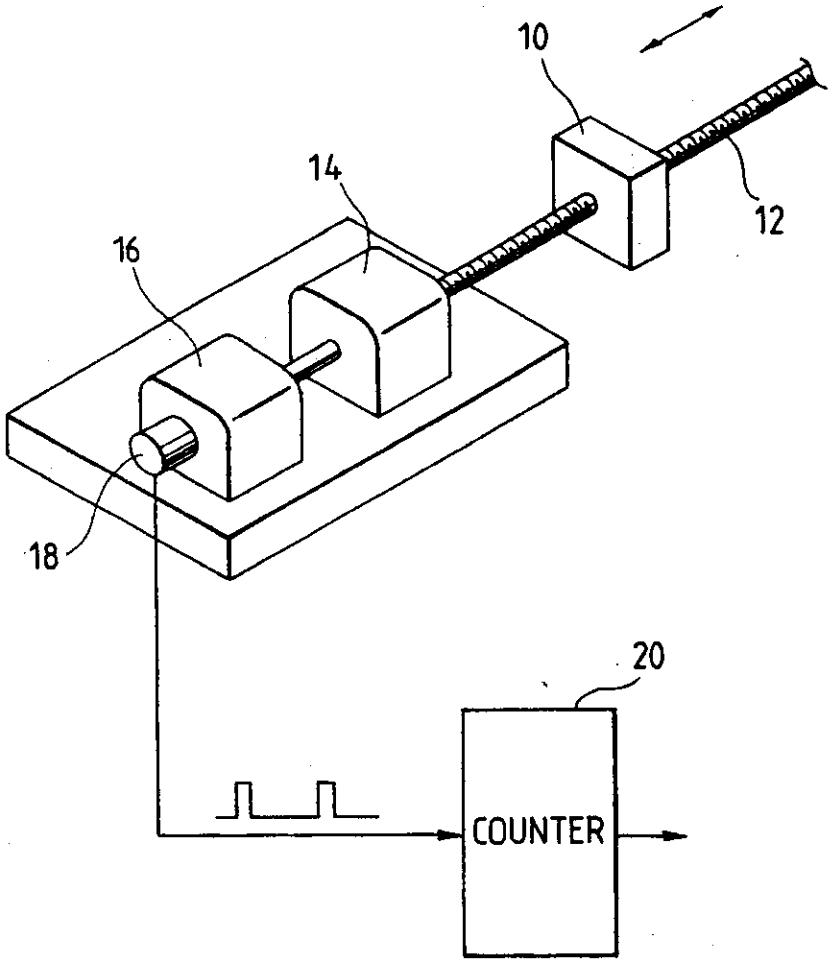


FIG. 2

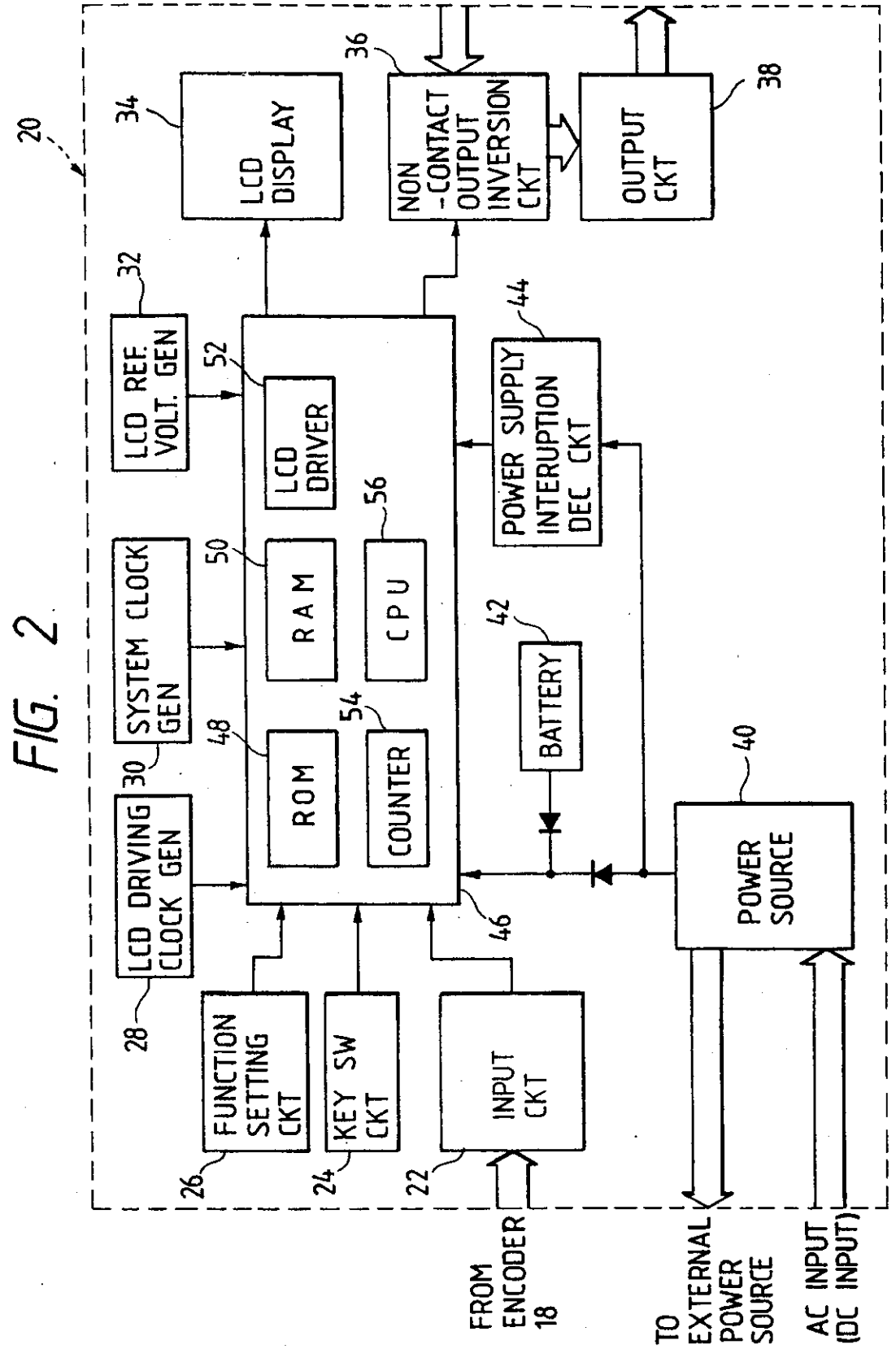

20
LCD DISPLAY
34
NON -CONTACT OUTPUT INVERSION CKT
36
OUTPUT CKT
38
LCD REF. VOLT. GEN
32
LCD DRIVER
52
POWER SUPPLY INTERUPTION DEC CKT
44
SYSTEM CLOCK GEN
30
RAM
50
CPU
56
BATTERY
42
ROM
48
COUNTER
54
LCD DRIVING CLOCK GEN
28
POWER SOURCE
40
FUNCTION SETTING CKT
26
KEY SW CKT
24
INPUT CKT
22
46
FROM ENCODER 18
TO EXTERNAL POWER SOURCE
AC INPUT (DC INPUT)

FIG. 3

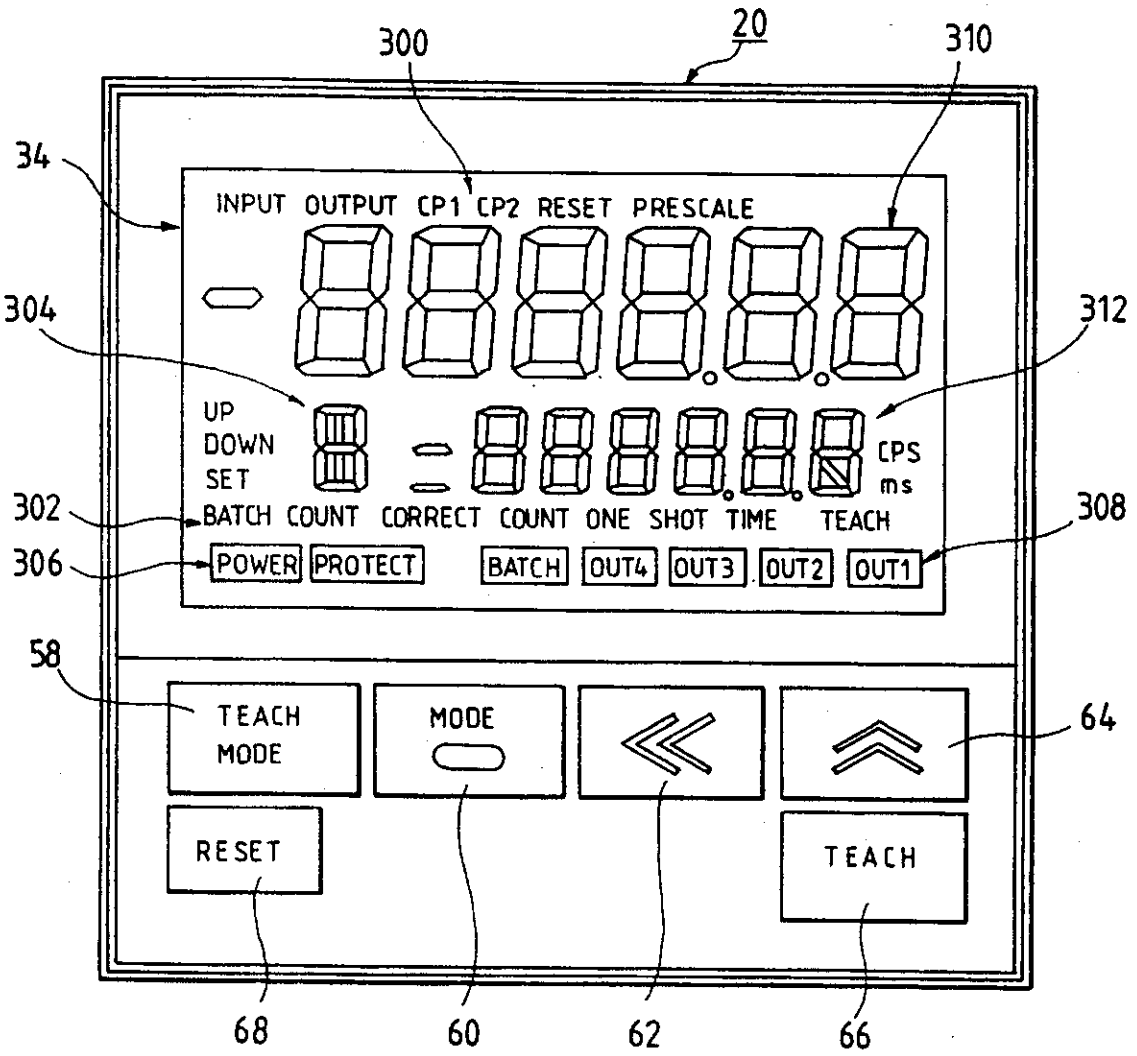

20
300
310
34
INPUT OUTPUT CP1 CP2 RESET PRESCALE
304
312
UP
DOWN
SET
CPS
ms
302
BATCH COUNT CORRECT COUNT ONE SHOT TIME TEACH
308
306
POWER
PROTECT
BATCH
OUT4
OUT3
OUT2
OUT1
58
TEACH MODE
MODE
64
RESET
TEACH
68
60
62
66

FIG. 4

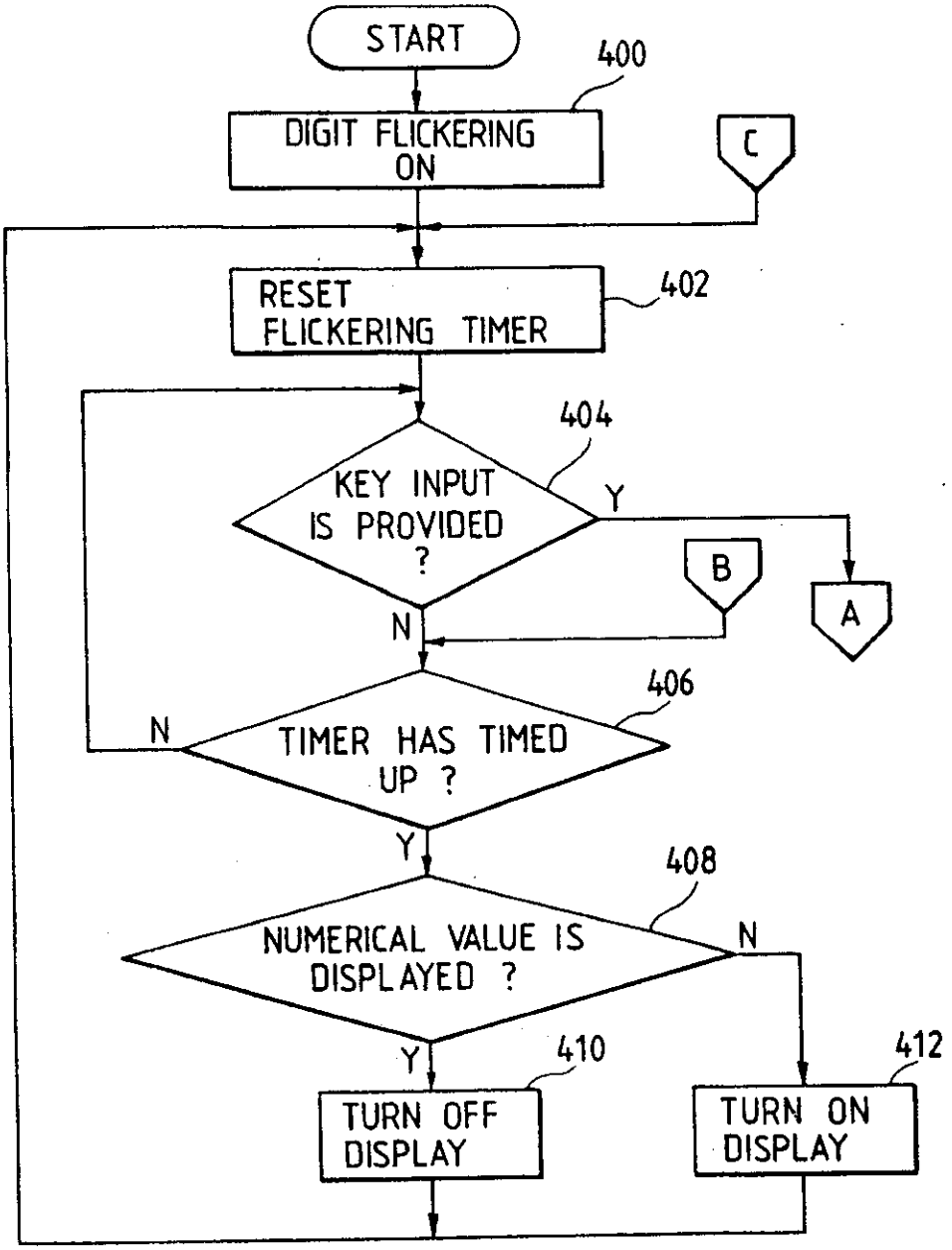

START
400
DIGIT FLICKERING ON
C
RESET FLICKERING TIMER
402
404
KEY INPUT IS PROVIDED ?
Y
B
A
N
406
N
TIMER HAS TIMED UP ?
Y
408
NUMERICAL VALUE IS DISPLAYED ?
N
Y
410
412
TURN OFF DISPLAY
TURN ON DISPLAY

FIG. 5

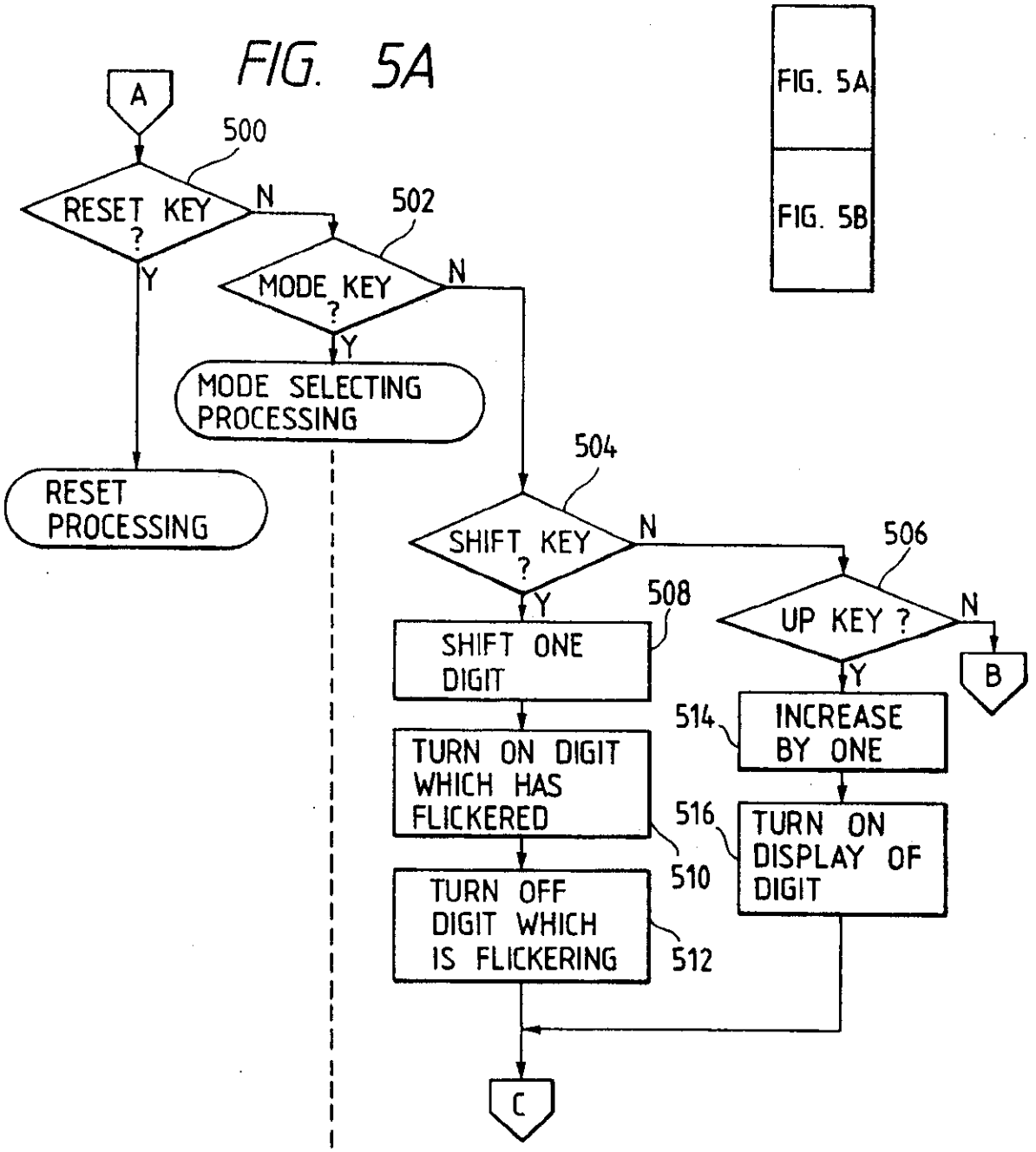


FIG. 5A
FIG. 5B
A
500
RESET KEY ?
N
Y
502
MODE KEY ?
N
Y
MODE SELECTING PROCESSING
RESET PROCESSING
504
SHIFT KEY ?
N
Y
506
UP KEY ?
N
Y
B
508
SHIFT ONE DIGIT
514
INCREASE BY ONE
516
TURN ON DISPLAY OF DIGIT
TURN ON DIGIT WHICH HAS FLICKERED
510
TURN OFF DIGIT WHICH IS FLICKERING
512
C
TO FIG. 5B

FIG. 5B

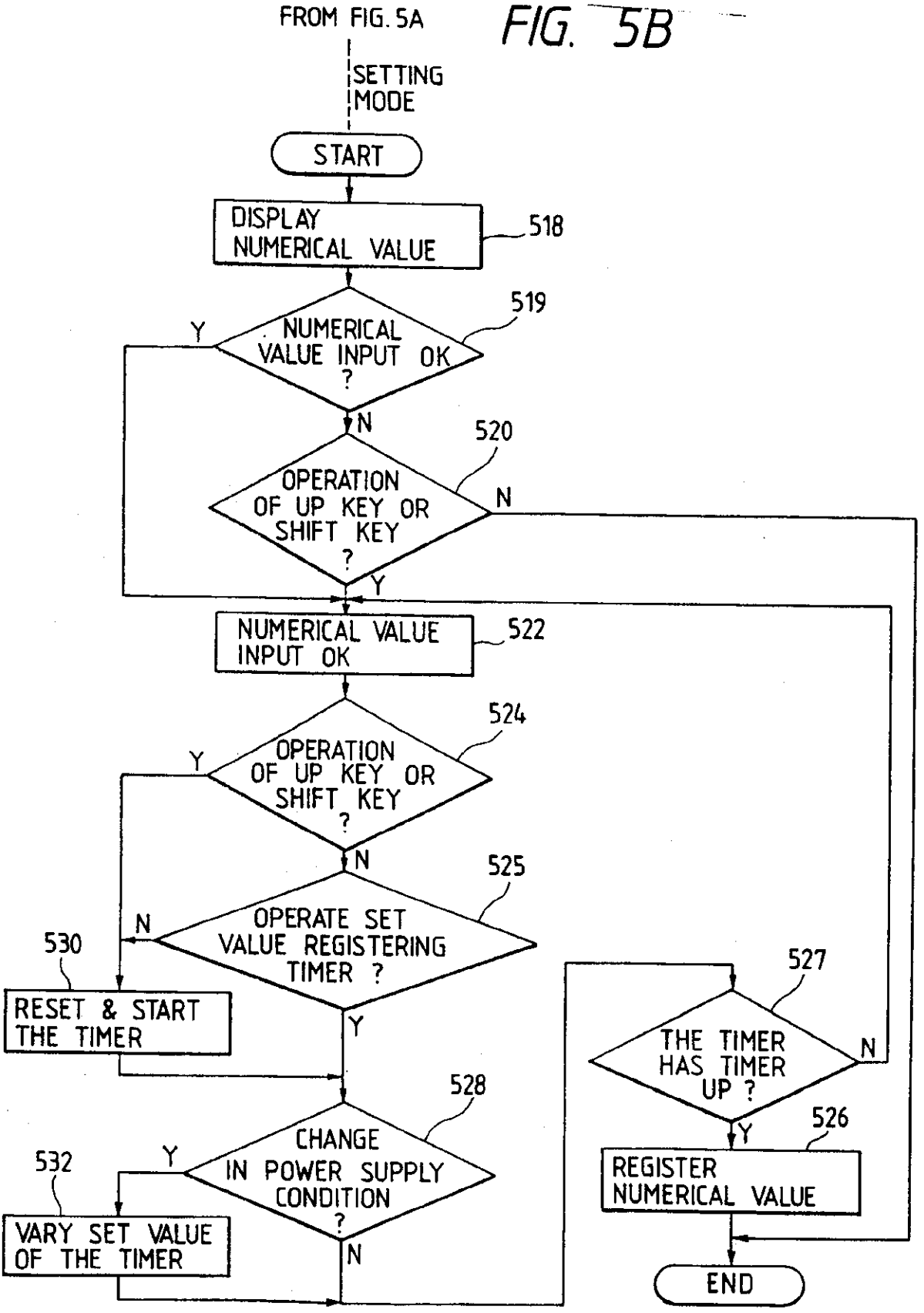

FROM FIG. 5A
SETTING MODE
START
DISPLAY NUMERICAL VALUE
518
NUMERICAL VALUE INPUT OK ?
519
Y
N
OPERATION OF UP KEY OR SHIFT KEY ?
520
N
Y
NUMERICAL VALUE INPUT OK
522
OPERATION OF UP KEY OR SHIFT KEY ?
524
Y
N
OPERATE SET VALUE REGISTERING TIMER ?
525
N
Y
530
RESET & START THE TIMER
CHANGE IN POWER SUPPLY CONDITION ?
528
Y
N
532
VARY SET VALUE OF THE TIMER
THE TIMER HAS TIMER UP ?
527
N
Y
REGISTER NUMERICAL VALUE
526
END

FIG. 6

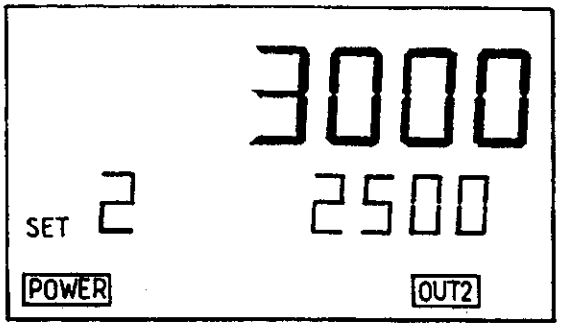


FIG. 7

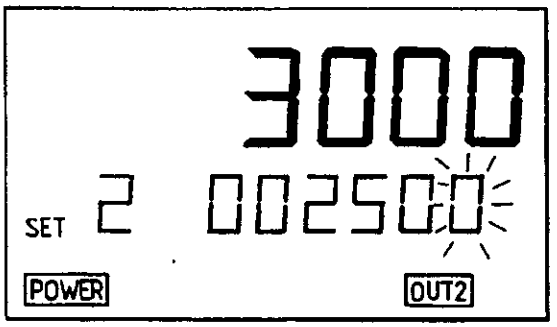


FIG. 8

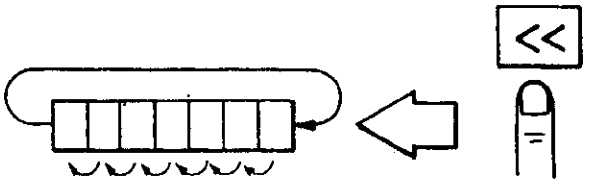


FIG. 9

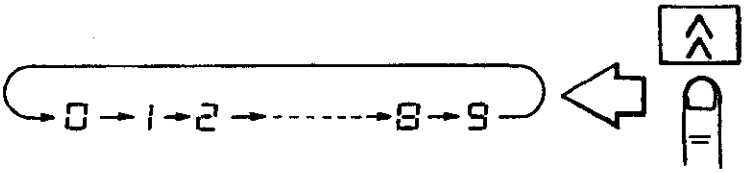
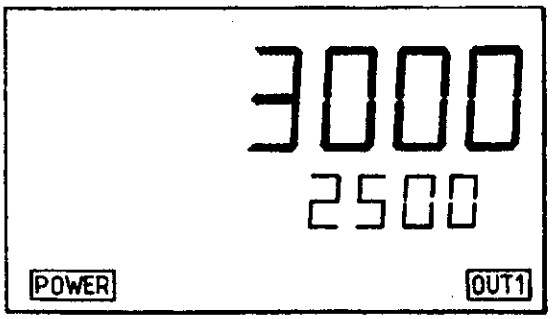


FIG. 10



REGISTER ENTRY FOR EP0366495

European Application No EP89311133.6 filing date 27.10.1989

Priority claimed:
28.10.1988 in Japan - doc: 63272460

Designated States BE CH DE ES FR GB GR IT LI LU NL SE AT

Title NUMERICAL VALUE SETTING DEVICE.

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Publication No EP0366495 dated 02.05.1990
Publication in English

Examination requested 01.06.1992

Patent Granted with effect from 07.09.1994 (Section 25(1)) with title NUMERICAL VALUE SETTING DEVICE.

26.05.1990 Notification from EPO of change of Applicant/Proprietor details
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Entry Type 25.14 Staff ID. RD06 Auth ID. EPT

23.12.1991 EPO: Search report published on 22.01.1992
Entry Type 25.11 Staff ID. RD06 Auth ID. EPT

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Entry Type 25.14 Staff ID. RD06 Auth ID. EPT

**** END OF REGISTER ENTRY ****

RENEWAL DETAILS

PUBLICATION NUMBER	EP0366495

PROPRIETOR(S)

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DATE FILED	27.10.1989
DATE GRANTED	07.09.1994
DATE NEXT RENEWAL DUE	27.10.1995
DATE NOT IN FORCE	
DATE OF LAST RENEWAL	17.10.1994
YEAR OF LAST RENEWAL	06
STATUS	PATENT IN FORCE