

METHOD FOR THIN FILM THERMOELECTRIC MODULE FABRICATIONRelated Applications

[0001] This application claims the benefit of provisional patent application serial number 61/248,691, filed October 5, 2009, the disclosure of which is hereby incorporated herein by reference in its entirety.

Field of the Disclosure

[0002] The present disclosure relates to thermoelectric modules and more specifically relates to fabrication of thin film thermoelectric modules.

Background

[0003] Technologies based upon semiconductor materials and devices have a remarkable track record of commercial achievement. Silicon-based solid state electronics have given us computing technology that has doubled in performance every two years (Moore's Law) for over forty years. Additionally, compound semiconductor optoelectronics, mostly Gallium Arsenide (GaAs) and Indium Phosphide (InP) based III-V semiconductor laser diodes, have given us communications technology that doubles the data coming out of an optical fiber every nine months (Butter's Law of Photonics). Semiconductor technology is now being applied to energy and energy efficiency. Solar cell devices based on Silicon and other semiconductor materials have recently experienced significant commercial success. However, it is widely recognized that there is little room left for significant improvement in solar cell power production efficiencies. In other words, there appears to be no equivalent opportunity for a Moore's Law type of improvement with solar cells. By contrast, thermoelectric materials for power generation from heat sources are increasingly being recognized as having the potential for a Moore's Law type of sustained performance improvement in the clean technology area.

[0004] In general, thermoelectric materials can be used to form thermoelectric generators and thermoelectric coolers. More specifically, Figure 1A illustrates a

traditional two-leg thermoelectric generator (TEG) 10. As illustrated, the TEG 10 includes a bulk-shaped N-type thermoelectric material 12, a bulk-shaped P-type thermoelectric material 14, a top conductive metal layer 16, and a bottom conductive metal layer 18. In order to generate power, heat is applied to the top conductive metal layer 16, thereby creating a heat differential between the top conductive metal layer 16 and the bottom conductive metal layer 18. This heat differential induces electrical current flow in the TEG 10 as illustrated. The electrical current flow through the N-type thermoelectric material 12 and the P-type thermoelectric material 14 is parallel to the direction of heat transference in the TEG 10. The induced electrical current flow supplies power to a resistive load 20.

[0005] Figure 1B illustrates a traditional two-leg thermoelectric cooler (TEC) 22. Like the TEG 10, the TEC 22 includes a bulk-shaped N-type thermoelectric material 24, a bulk-shaped P-type thermoelectric material 26, a top conductive metal layer 28, and a bottom conductive metal layer 30. In order to effect thermoelectric cooling, an electrical current is applied to the TEC 22 as shown. The direction of current transference in the N-type thermoelectric material 24 and the P-type thermoelectric material 26 is parallel to the direction of heat transference in the TEC 22. As a result, cooling occurs at the top conductive metal layer 28 by absorbing heat at the top surface of the TEC 22 and releasing heat at the bottom surface of the TEC 22.

[0006] The primary figure of merit for thermoelectric materials is ZT , where ZT is defined as:

$$ZT = S^2 \sigma T / k ,$$

where S is the Seebeck coefficient of the thermoelectric material, σ is the electrical conductivity of the thermoelectric material, k is the thermal conductivity of the thermoelectric material, and T is the temperature in kelvins. Thus, a good thermoelectric material will have low thermal conductivity, high electrical conductivity, and a high Seebeck coefficient. Presently, commercial thermoelectric materials have ZT values of around 1.0. However, ZT values of

3.0 or higher are desired. As such, there is a need for a thermoelectric material having a high ZT value.

[0007] Embodiments of a thin film thermoelectric material having a high ZT value are disclosed herein. Because the disclosed thermoelectric material is a thin film material, traditional pick-and-place techniques used to fabricate thermoelectric modules cannot be used. More specifically, traditional thermoelectric modules are formed from traditional thermoelectric devices such as those of Figures 1A and 1B. These traditional thermoelectric devices have bulk shaped thermoelectric material legs, which have dimensions on the order of millimeters. In contrast, the thin film thermoelectric material disclosed herein results in thermoelectric devices having thermoelectric material legs having dimensions on the order of a few to tens of microns. As such, the traditional pick-and-place techniques that are used to fabricate traditional thermoelectric devices having thermoelectric material legs on the millimeter scale are not suitable for use in fabrication of thermoelectric devices having thermoelectric material legs on the micrometer scale. As such, there is also a need for a method of fabricating a thin film thermoelectric module.

Summary

[0008] Methods of fabrication of a thermoelectric module from thin film thermoelectric material are disclosed. In general, a thin film thermoelectric module is fabricated by first forming an N-type thin film thermoelectric material layer on a substrate. One or more metallization layers are then formed on the N-type thin film thermoelectric material layer. The one or more metallization layers and the N-type thin film thermoelectric material layer are then etched to form a number of N-type thermoelectric material legs. A first electrode assembly is then bonded to a first portion of the N-type thermoelectric material legs, and the first electrode assembly including the first portion of the N-type thermoelectric material legs is removed from the substrate. In a similar manner, a P-type thin film thermoelectric material layer is formed on a substrate. One or more metallization layers are formed on the P-type thin film thermoelectric material

layer. The one or more metallization layers and the P-type thin film thermoelectric material layer are then etched to form a number of P-type thermoelectric material legs. A second electrode assembly is then bonded to a first portion of the P-type thermoelectric material legs, and the second electrode assembly including the first portion of the P-type thermoelectric material legs is removed from the substrate. The first and second electrode assemblies, including the N-type and P-type thermoelectric material legs bonded thereto, are then bonded using a flip-chip bonding process to complete the fabrication of the thermoelectric module.

[0009] In one embodiment, a third electrode assembly is bonded to a remaining portion of the N-type thermoelectric material legs, and the third electrode assembly including the remaining portion of the N-type thermoelectric material legs is removed from the substrate. A fourth electrode assembly is then bonded to a remaining portion of the P-type thermoelectric material legs, and the fourth electrode assembly including the remaining portion of the P-type thermoelectric material legs are removed from the substrate. The third and fourth electrode assemblies, including the N-type and P-type thermoelectric material legs bonded thereto, are then bonded using a flip-chip bonding process to complete fabrication of the second thermoelectric module.

[0010] Those skilled in the art will appreciate the scope of the present invention and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0011] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the invention, and together with the description serve to explain the principles of the invention.

[0012] Figures 1A and 1B illustrate exemplary thermoelectric devices according to the prior art;

[0013] Figure 2 illustrates a thin film thermoelectric material including a heterostructure formed of IV-VI semiconductor materials, wherein the heterostructure includes a potential barrier material layer having a thickness approximately equal to a mean free path of charge carriers for a desired temperature according to one embodiment of the present disclosure;

[0014] Figure 3 is an energy band diagram for the heterostructure of the thin film thermoelectric material of Figure 2, wherein a Fermi energy of the heterostructure is at or near a barrier height of the potential barrier material layer according to one embodiment of the present disclosure;

[0015] Figure 4 illustrates a thin film thermoelectric material including a heterostructure formed of IV-VI semiconductor materials, wherein the heterostructure includes multiple potential barrier material layers having thicknesses that are approximately equal to mean free paths of charge carriers for corresponding temperatures in an expected temperature gradient across the thin film thermoelectric material when incorporated into a thermoelectric cooler (TEC) according to one embodiment of the present disclosure;

[0016] Figure 5 is an energy band diagram for the heterostructure of the thin film thermoelectric material of Figure 4, wherein a Fermi energy of the heterostructure is at or near a barrier height of the potential barrier material layers according to one embodiment of the present disclosure;

[0017] Figure 6 illustrates a thin film thermoelectric material including a heterostructure formed of IV-VI semiconductor materials, wherein the heterostructure includes multiple potential barrier material layers having thicknesses that are approximately equal to mean free paths of charge carriers for corresponding temperatures in an expected temperature gradient across the thin film thermoelectric material when incorporated into a thermoelectric generator (TEG) according to one embodiment of the present disclosure;

[0018] Figure 7 is an energy band diagram for the heterostructure of the thin film thermoelectric material of Figure 6, wherein a Fermi energy of the heterostructure is at or near a barrier height of the potential barrier material layers according to one embodiment of the present disclosure;

[0019] Figure 8 illustrates a thermoelectric module fabricated to include a number of thermoelectric device couples connected in series according to one embodiment of the present disclosure;

[0020] Figures 9A through 9K graphically illustrate a process for fabricating the thermoelectric module of Figure 8 according to one embodiment of the present disclosure;

[0021] Figures 10A through 10P graphically illustrate a process for fabricating the thermoelectric module of Figure 8 according to another embodiment of the present disclosure; and

[0022] Figures 11A through 11O graphically illustrate a process for fabricating the thermoelectric module of Figure 8 according to another embodiment of the present disclosure.

Detailed Description of the Preferred Embodiments

[0023] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the invention and illustrate the best mode of practicing the invention. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the invention and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0024] Figure 2 illustrates a thin film thermoelectric material 32 (hereinafter “thermoelectric material 32”) having a high ZT value according to one embodiment of the present disclosure. The thermoelectric material 32 includes a heterostructure 34 formed of Group IV-VI semiconductor materials. More specifically, in this embodiment, the heterostructure 34 includes a first matrix material layer 36, a potential barrier material layer 38 (hereinafter “barrier material layer 38”) that is adjacent to the first matrix material layer 36, and a second matrix material layer 40 that is adjacent to the barrier material layer 38 opposite the first matrix material layer 36. In order to operate as a potential barrier, the barrier material layer 38 has a bandgap that is greater than a

bandgap of the first and second matrix material layers 36 and 40, and is therefore referred to herein as being formed of a wide bandgap material. A resulting barrier height of the barrier material layer 38 is preferably in the range of and including 25 milli-electron-Volts (meV) to 100 meV, but is not limited thereto.

5 In the preferred embodiment, the first and second matrix material layers 36 and 40 are PbSnSe, and the barrier material layer 38 is PbSe. However, other IV-VI semiconductor materials such as, but not limited to, PbTe, PbSnTe, PbSrSe, PbSrTe, and related alloys may be used. For example, in one alternative embodiment, the first and second matrix material layers 36 and 40 are PbSnTe,
10 and the barrier material layer 38 is PbTe. In another alternative embodiment, the first and second matrix material layers 36 and 40 are PbSnSeTe, and the barrier material layer 38 is PbSe. Further, the PbSnSeTe/PbSe combination can be specified as lattice-matched, a feature that will help to improve cross plane charge carrier conduction. In operation, energetic thermally excited electrons, or
15 holes depending on the conductivity type of the thermoelectric material 32, are selectively “skimmed” off and transported from the first matrix material layer 36 across the barrier material layer 38 into the second matrix material layer 40. The first matrix material layer 36 operates as an emitter of charge carriers, and the second matrix material layer 40 operates as a collector of charge carriers.

20 **[0025]** In this embodiment, a thickness (t_{BL}) of the barrier material layer 38 is approximately equal to, or on the order of, a mean free path for charge carriers (i.e., electrons or holes) in the barrier material layer 38 between scattering events at a desired temperature. In one embodiment, the desired temperature is room temperature (i.e., 300 kelvins). However, the desired temperature may be any
25 desired temperature in which a thermoelectric device formed of the thermoelectric material 32 is to be operated. By letting the thickness (t_{BL}) of the barrier material layer 38 be approximately equal to the mean free path for charge carriers between scattering events at the desired temperature, ballistic transport of charge carriers from the first matrix material layer 36 through the barrier
30 material layer 38 and into the second matrix material layer 40 is enabled, thereby

increasing the Seebeck coefficient of the thermoelectric material 32 and thus the ZT value of the thermoelectric material 32.

[0026] If the thermoelectric material 32 is N-type, the mean free path for electrons is defined as:

$$5 \quad l_{mfp}^e = \frac{\mu_n}{q} \sqrt{3kTm_e^*}, \quad (\text{Eqn. 1})$$

where l_{mfp}^e is the mean free path for electrons in the barrier material layer 38, μ_n is the electron mobility of the barrier material layer 38, q is the charge of an electron, k is Boltzmann's constant, T is temperature in kelvins, and m_e^* is electron mass. As such, if the thermoelectric material 32 is N-type, the thickness
10 (t_{BL}) of the barrier material layer 38 is preferably defined as:

$$t_{BL} \equiv l_{mfp}^e = \frac{\mu_n}{q} \sqrt{3kTm_e^*}. \quad (\text{Eqn. 2})$$

Similarly, if the thermoelectric material 32 is P-type, the mean free path for holes is defined as:

$$l_{mfp}^h = \frac{\mu_p}{q} \sqrt{3kTm_h^*}, \quad (\text{Eqn. 3})$$

15 where l_{mfp}^h is the mean free path for holes in the barrier material layer 38, μ_p is the electron mobility of the barrier material layer 38, q is the charge of an electron, k is Boltzmann's constant, T is temperature in kelvins, and m_h^* is hole mass. As such, if the thermoelectric material 32 is P-type, the thickness (t_{BL}) of the barrier material layer 38 is preferably defined as:

$$20 \quad t_{BL} \equiv l_{mfp}^h = \frac{\mu_p}{q} \sqrt{3kTm_h^*}. \quad (\text{Eqn. 4})$$

[0027] As an example, in the preferred embodiment, the barrier material layer 38 is PbSe. For this example, assume that the desired temperature is room temperature (i.e., 300 kelvins). As such, using Equation 2, the mean free path for electrons in lightly doped PbSe at room temperature is 16.9 nanometers (nm)
25 as shown in the following table:

N_d (cm^{-3})	μ_n (cm^2/vs)	m_e^* ($\times m_o$)	l_{mfp}^e (nm)
1×10^{18}	1,000	0.1	16.9

In a similar manner, using Equation 4, the mean free path for holes in lightly doped PbSe at room temperature is 105 nm as shown in the following table:

N_a (cm^{-3})	M_p (cm^2/vs)	m_h^* ($\times m_o$)	l_{mfp}^h (nm)
2×10^{17}	600	0.1	10.1

Thus, in this example, the thickness of the barrier material layer 38 is approximately 16.9 nm if the thermoelectric material 32 is N-type and

- 5 approximately 10.1 nm if the thermoelectric material 32 is P-type. Note, however, that the mean free path of charge carriers in PbSe can range from tens of nanometers at high temperatures to hundreds of nanometers at cryogenic temperatures.

[0028] In addition, in this embodiment, a thickness (t_{ML}) of the second matrix material layer 40 is greater than or equal to three times the thickness of the barrier material layer 38. By letting the thickness (t_{ML}) of the second matrix material layer 40 be greater than or equal to three times the thickness (t_{BL}) of the barrier material layer 38, charge carriers passing from the first matrix material layer 36 through the barrier material layer 38 and into the second matrix material layer 40 are allowed to relax thermally by scattering at least three times. In other words, the charge carriers are allowed to reach a thermal equilibrium level. Note that the thickness of the first matrix material layer 36 is not relevant with respect to allowing the charge carriers to relax thermally. As such, the thickness of the first matrix material layer 36 may be any desired thickness.

20 [0029] Figure 3 is an exemplary energy band diagram for the thermoelectric material 32 of Figure 2 according to one embodiment of the present disclosure. In this example, the thermoelectric material 32 is N-type. However, this discussion is also applicable for the case where the thermoelectric material 32 is P-type. In this embodiment, alloying of the barrier material layer 38, doping of the first and second matrix material layers 36 and 40, or both is selected or controlled such that a Fermi energy (E_f) of the thermoelectric material 32 is at or

near a barrier height (Δ) of the barrier material layer 38. Since the Fermi energy (E_f) defines an energy level at which the Fermi-Dirac probability distribution function is 0.5 (i.e., the energy level above which half of the charge carriers are expected to reside), by increasing the Fermi energy (E_f) such that it is at or near the barrier height (Δ), there are more electrons at or above the barrier height (Δ). As a result, cross-plane effective carrier density is increased, which in turn increases the ZT value for the thermoelectric material 32. The Fermi energy (E_f) may be approximately equal to the barrier height (Δ) or within a range of values near the barrier height (Δ).

[0030] For example, in the preferred embodiment, the first and second matrix material layers 36 and 40 are PbSe, and the barrier material layer 38 is PbSnSe. The barrier height (Δ) may be controlled via the Sn content. More specifically, increasing the Sn content increases the barrier height (Δ). In addition or alternatively, the Fermi energy (E_f) may be controlled via doping of the Group IV-VI semiconductor materials by adding an impurity such as, for example, Bismuth (Bi). Increasing the doping level moves the Fermi energy (E_f) more into the conduction band (N-type) or more into the valence band (P-type). The Sn content and/or the doping can be controlled to set the Fermi energy (E_f) at or near the barrier height (Δ). In this example, the Fermi energy (E_f) may be set approximately equal to the barrier height (Δ), be within a range of the barrier height (Δ) plus or minus approximately $0.1 \cdot kT$ (where k is Boltzmann's constant and T is temperature in kelvins), be within a range of the barrier height (Δ) minus approximately $0.1 \cdot kT$, or the like. For example, at room temperature with a thermal energy (kT) of 26 meV, the Fermi energy (E_f) may be controlled to be the barrier height (Δ) ± 3 meV.

[0031] Figure 4 illustrates a thin film thermoelectric material 42 (hereinafter "thermoelectric material 42") having a high ZT value according to another embodiment of the present disclosure. The thermoelectric material 42 includes a heterostructure 44 formed of Group IV-VI semiconductor materials. The heterostructure 44 includes an alternating series of matrix material layers 46 and potential barrier material layers 48 (hereinafter "barrier material layers 48"). In

order to operate as a potential barrier, the barrier material layers 48 have a bandgap that is greater than a bandgap of the matrix material layers 46, and are therefore referred to herein as being formed of a wide bandgap material. A resulting barrier height of the barrier material layers 48 is preferably in the range of and including 25 meV to 100 meV, but is not limited thereto. In the preferred embodiment, the matrix material layers 46 are PbSnSe, and the barrier material layers 48 are PbSe. However, other Group IV-VI semiconductor materials may be used. In this exemplary embodiment, the heterostructure 44 includes an initial matrix material layer 46-0 and an alternating series of barrier material layers 48-1 through 48-4 and matrix material layers 46-1 through 46-4. Note that in this exemplary embodiment, there are five matrix material layers 46-0 through 46-4, which are generally referred to herein as matrix material layers 46, and four barrier material layers 48-1 through 48-4, which are generally referred to herein as barrier material layers 48. However, the heterostructure 44 is not limited thereto. The heterostructure 44 may include any number of alternating matrix material layers 46 and barrier material layers 48 as long as the heterostructure 44 includes at least two barrier material layers 48.

[0032] In this embodiment, the thermoelectric material 42 is designed for operation in a thermoelectric cooler (TEC) such that, during operation, a top surface 50 of the thermoelectric material 42 will be cold and a bottom surface 52 of the thermoelectric material 42 will be hot. As a result, the thermoelectric material 42 will have, or will experience, a corresponding temperature gradient 54. Thicknesses of the barrier material layers 48 are approximately equal to, or on the order of, the mean free paths of charge carriers between scattering events at corresponding temperatures in the temperature gradient 54 for the thermoelectric material 42. By letting the thicknesses of the barrier material layers 48 be approximately equal to the mean free paths for charge carriers between scattering events at the corresponding temperatures in the temperature gradient 54 of the thermoelectric material 42, ballistic transport of charge carriers across the barrier material layers 48 is enabled, thereby increasing the Seebeck coefficient of the thermoelectric material 42.

[0033] If the thermoelectric material 42 is N-type, the thickness (t_{BLi}) of the i th barrier material layer 48 in the thermoelectric material 42 is preferably defined as:

$$t_{BLi} \cong l_{mfp}^e = \frac{\mu_n}{q} \sqrt{3kT_i m_e^*}, \quad (\text{Eqn. 5})$$

where T_i is the temperature (in kelvins) in the temperature gradient 54 at a position of the i th barrier material layer 48 in the thermoelectric material 42, μ_n is the electron mobility of the barrier material layer 48 at temperature T_i , q is the charge of an electron, k is Boltzmann's constant, and m_e^* is electron mass.

Similarly, if the thermoelectric material 42 is P-type, the thickness (t_{BLi}) of the i th barrier material layer 48 in the thermoelectric material 42 is preferably defined as:

$$t_{BLi} \cong l_{mfp}^h = \frac{\mu_p}{q} \sqrt{3kT_i m_h^*}, \quad (\text{Eqn. 6})$$

where T_i is the temperature (in kelvins) in the temperature gradient 54 at a position of the i th barrier material layer 48 in the thermoelectric material 42, μ_p is the electron mobility of the barrier material layer 48 at temperature T_i , q is the charge of an electron, k is Boltzmann's constant, and m_h^* is hole mass.

Depending on the material quality that can be obtained and the absolute temperatures in the thermoelectric material 42, the thicknesses of the barrier material layers 48 designed for high temperatures may be as thin as a few nanometers while barrier material layers 48 designed for low temperatures may be as thick as a 100 nanometers or more.

[0034] In addition, in this embodiment, a thickness of each of the matrix material layers 46 that is downstream of an adjacent barrier material layer 48 in the direction of charge carrier flow is greater than or equal to three times the thickness of the immediately preceding barrier material layer 48. More specifically, in this embodiment, the thickness (t_{ML1}) of the matrix material layer 46-1 is greater than or equal to three times the thickness (t_{BL1}) of the barrier material layer 48-1, the thickness (t_{ML2}) of the matrix material layer 46-2 is greater than or equal to three times the thickness (t_{BL2}) of the barrier material layer 48-2, the thickness (t_{ML3}) of the matrix material layer 46-3 is greater than or equal to three times the thickness (t_{BL3}) of the barrier material layer 48-3, and the

thickness (t_{ML4}) of the matrix material layer 46-4 is greater than or equal to three times the thickness (t_{BL4}) of the barrier material layer 48-4. By letting the thicknesses (t_{ML1} through t_{ML4}) of the matrix material layers 46-1 through 46-4 be greater than or equal to three times the thicknesses (t_{BL1} through t_{BL4}) of the corresponding barrier material layers 48-1 through 48-4, charge carriers are allowed to relax thermally by scattering at least three times after passing through the barrier material layers 48-1 through 48-4. In other words, the charge carriers are allowed to reach a thermal equilibrium level. Note that the thickness of the matrix material layer 46-0 is not relevant with respect to allowing the charge carriers to relax thermally. As such, the thickness of the matrix material layer 46-0 may be any desired thickness.

[0035] It should be noted that in one embodiment, incorporation of quantum wells in the collector layers (e.g., the matrix material layers 46-1 through 46-4) can facilitate capture and thermalization of electrons due to electrophonon resonance associated with the subband degeneracy splitting effect. Quantum well incorporation can be useful since it would allow the collector layers to be thinner, thus enabling more barrier material layers 48 with a given device structure thickness. A further benefit is that incorporating periodic quantum well layers will decrease lattice thermal conductivity because of increased phonon scattering associated with Umklapp processes. These as well as other variations and combinations of similar material design concepts are considered within the scope of this disclosure.

[0036] Figure 5 is an exemplary energy band diagram for the thermoelectric material 42 of Figure 4 according to one embodiment of the present disclosure.

In this example, the thermoelectric material 42 is N-type. However, this discussion is also applicable for the case where the thermoelectric material 42 is P-type. In this embodiment, alloying of the barrier material layers 48, doping of the matrix material layers 46, or both is selected or controlled such that a Fermi energy (E_f) of the thermoelectric material 42 is at or near a barrier height (Δ) of the barrier material layers 48. Since the Fermi energy (E_f) defines an energy level at which the Fermi-Dirac probability distribution function is 0.5 (i.e., the

energy level above which half of the charge carriers are expected to reside), by increasing the Fermi energy (E_f) such that it is at or near the barrier height (Δ), there are more electrons at or above the barrier height (Δ). As a result, cross-plane effective carrier density is increased, which in turn increases the ZT value for the thermoelectric material 42. The Fermi energy (E_f) may be approximately equal to the barrier height (Δ) or within a range of values near the barrier height (Δ). For example, the Fermi energy (E_f) may be set approximately equal to the barrier height (Δ), be within a range of the barrier height (Δ) plus or minus approximately $0.1 \cdot kT$ (where k is Boltzmann's constant and T is temperature in kelvins), be within a range of the barrier height (Δ) minus approximately $0.1 \cdot kT$, or the like.

[0037] Figure 6 illustrates a thin film thermoelectric material 56 (hereinafter "thermoelectric material 56") having a high ZT value according to another embodiment of the present disclosure. This embodiment is substantially the same as that of Figure 4. However, the thermoelectric material 56 is designed for use in a thermoelectric generator (TEG) rather than a TEC. The thermoelectric material 56 includes a heterostructure 58 formed of Group IV-VI semiconductor materials. The heterostructure 58 includes an alternating series of matrix material layers 60 and potential barrier material layers 62 (hereinafter "barrier material layers 62"). In order to operate as a potential barriers, the barrier material layers 62 have a bandgap that is greater than a bandgap of the matrix material layers 60, and are therefore referred to herein as being formed of a wide bandgap material. A resulting barrier height of the barrier material layers 62 is preferably in the range of and including 25 meV to 100 meV, but is not limited thereto. In the preferred embodiment, the matrix material layers 60 are PbSnSe, and the barrier material layers 62 are PbSe. However, other Group IV-VI semiconductor materials may be used. In this exemplary embodiment, the heterostructure 58 includes an initial matrix material layer 60-0 and an alternating series of barrier material layers 62-1 through 62-4 and matrix material layers 60-1 through 60-4. Note that in this exemplary embodiment, there are five matrix material layers 60-0 through 60-4, which are generally referred to herein as

matrix material layers 60, and four barrier material layers 62-1 through 62-4, which are generally referred to herein as barrier material layers 62. However, the heterostructure 58 is not limited thereto. The heterostructure 58 may include any number of alternating matrix material layers 60 and barrier material layers 62 as long as the heterostructure 58 includes at least two barrier material layers 62.

[0038] In this embodiment, the thermoelectric material 56 is designed for operation in a TEG such that, during operation, a top surface 64 of the thermoelectric material 56 will be hot and a bottom surface 66 of the thermoelectric material 56 will be cold. As a result, the thermoelectric material 56 will have, or will experience, a corresponding temperature gradient 68.

Thicknesses of the barrier material layers 62 are approximately equal to, or on the order of, the mean free paths of charge carriers between scattering events at corresponding temperatures in the temperature gradient 68 for the thermoelectric material 56. By letting the thicknesses of the barrier material layers 62 be approximately equal to the mean free paths for charge carriers between scattering events at the corresponding temperatures in the temperature gradient 68 of the thermoelectric material 56, ballistic transport of charge carriers across the barrier material layers 62 is enabled, thereby increasing the Seebeck coefficient of the thermoelectric material 56.

[0039] If the thermoelectric material 56 is N-type, the thickness (t_{BLi}) of the i th barrier material layer 62 in the thermoelectric material 56 is preferably defined as:

$$t_{BLi} \cong l_{mfp}^e = \frac{\mu_n}{q} \sqrt{3kT_i m_e^*}, \quad (\text{Eqn. 7})$$

where T_i is the temperature (in kelvins) in the temperature gradient 68 at a position of the i th barrier material layer 62 in the thermoelectric material 56, μ_n is the electron mobility of the barrier material layer 62 at temperature T_i , q is the charge of an electron, k is Boltzmann's constant, and m_e^* is electron mass.

Similarly, if the thermoelectric material 56 is P-type, the thickness (t_{BLi}) of the i th barrier material layer 62 in the thermoelectric material 56 is preferably defined as:

$$t_{BLi} \cong l_{mfp}^h = \frac{\mu_p}{q} \sqrt{3kT_i m_h^*}, \quad (\text{Eqn. 8})$$

where T_i is the temperature (in kelvins) in the temperature gradient 68 at a position of the i th barrier material layer 62 in the thermoelectric material 56, μ_p is the electron mobility of the barrier material layer 62 at temperature T_i , q is the charge of an electron, k is Boltzmann's constant, and m_h^* is hole mass.

- 5 Depending on the material quality that can be obtained and the absolute temperatures in the thermoelectric material 56, the thicknesses of the barrier material layers 62 designed for high temperatures may be as thin as a few nanometers while barrier material layers 62 designed for low temperatures may be as thick as a 100 nanometers or more.
- 10 **[0040]** In addition, in this embodiment, a thickness of each of the matrix material layers 60 that is downstream of an adjacent barrier material layer 62 in the direction of charge carrier flow is greater than or equal to three times the thickness of the immediately preceding barrier material layer 62. More specifically, in this embodiment, the thickness (t_{ML1}) of the matrix material layer
- 15 60-1 is greater than or equal to three times the thickness (t_{BL1}) of the barrier material layer 62-1, the thickness (t_{ML2}) of the matrix material layer 60-2 is greater than or equal to three times the thickness (t_{BL2}) of the barrier material layer 62-2, the thickness (t_{ML3}) of the matrix material layer 60-3 is greater than or equal to three times the thickness (t_{BL3}) of the barrier material layer 62-3, and the
- 20 thickness (t_{ML4}) of the matrix material layer 60-4 is greater than or equal to three times the thickness (t_{BL4}) of the barrier material layer 62-4. By letting the thicknesses (t_{ML1} through t_{ML4}) of the matrix material layers 60-1 through 60-4 be greater than or equal to three times the thicknesses (t_{BL1} through t_{BL4}) of the corresponding barrier material layers 62-1 through 62-4, charge carriers are
- 25 allowed to relax thermally by scattering at least three times after passing through the barrier material layers 62-1 through 62-4. In other words, the charge carriers are allowed to reach a thermal equilibrium level. Note that the thickness of the matrix material layer 60-0 is not relevant with respect to allowing the charge carriers to relax thermally. As such, the thickness of the matrix material layer 60-
- 30 0 may be any desired thickness.

[0041] It should be noted that in one embodiment, incorporation of quantum wells in the collector layers (e.g., the matrix material layers 60-1 through 60-4) can facilitate capture and thermalization of electrons due to electrophonon resonance associated with the subband degeneracy splitting effect. Quantum well incorporation can be useful since it would allow the collector layers to be thinner, thus enabling more barrier material layers 62 with a given device structure thickness. A further benefit is that incorporating periodic quantum well layers will decrease lattice thermal conductivity because of increased phonon scattering associated with Umklapp processes. These as well as other variations and combinations of similar material design concepts are considered within the scope of this disclosure.

[0042] Figure 7 is an exemplary energy band diagram for the thermoelectric material 56 of Figure 6 according to one embodiment of the present disclosure. In this example, the thermoelectric material 56 is N-type. However, this discussion is also applicable for the case where the thermoelectric material 56 is P-type. In this embodiment, alloying of the barrier material layers 62, doping of the matrix material layers 60, or both is selected or controlled such that a Fermi energy (E_f) of the thermoelectric material 56 is at or near a barrier height (Δ) of the barrier material layers 62. Since the Fermi energy (E_f) defines an energy level at which the Fermi-Dirac probability distribution function is 0.5 (i.e., the energy level above which half of the charge carriers are expected to reside), by increasing the Fermi energy (E_f) such that it is at or near the barrier height (Δ), there are more electrons at or above the barrier height (Δ). As a result, cross-plane effective carrier density is increased, which in turn increases the ZT value for the thermoelectric material 56. The Fermi energy (E_f) may be approximately equal to the barrier height (Δ) or within a range of values near the barrier height (Δ). For example, the Fermi energy (E_f) may be set approximately equal to the barrier height (Δ), be within a range of the barrier height (Δ) plus or minus approximately $0.1 \cdot kT$ (where k is Boltzmann's constant and T is temperature in kelvins), be within a range of the barrier height (Δ) minus approximately $0.1 \cdot kT$, or the like.

[0043] Figure 8 illustrates a thermoelectric module 70 that includes a number of thin film thermoelectric devices 72-1 through 72-10 (generally thermoelectric devices 72) connected in series in a serpentine configuration according to one embodiment of the present disclosure. Preferably, the thermoelectric devices 72 are formed of the thermoelectric material 32, 42, or 56 described above. As illustrated, when configured as a TEG, heat is applied to a top surface of the thermoelectric module 70 (not shown so that the serpentine configuration of the thermoelectric devices 72 can be seen) such that a heat differential is created between the top surface of the thermoelectric module 70 and a bottom surface 74 of the thermoelectric module 70. As a result, a current is created in the thermoelectric module 70 that flows through the thermoelectric devices 72 in a serpentine path as illustrated (i.e., through thermoelectric device 72-1, to thermoelectric device 72-2, to thermoelectric device 72-3, to thermoelectric device 72-4, and so on). In contrast, when configured as a TEC, a current is applied to the thermoelectric module 70 such that the current flows through the thermoelectric devices 72 in the illustrated serpentine path. As a result, the top surface of the thermoelectric module 70 is cooled.

[0044] Figures 9A through 9J graphically illustrate a process for fabricating the thermoelectric module 70 of Figure 8 according to one embodiment of the present disclosure. The process starts with a substrate 76, as illustrated in Figure 9A. In one embodiment, the substrate 76 is a Silicon (Si) substrate. However, the present disclosure is not limited thereto. Other types of substrates such as for example Sapphire substrates, may be used. Next, as illustrated in Figure 9B, a release layer 78 is formed on the substrate 76. In one embodiment, the release layer 78 is Barium Fluoride (BaF_2), which is easily dissolvable in water. Note, however, that other types of release layers may be used to allow structures formed on the substrate 76 to separate from the substrate 76.

[0045] Next, an N-type thermoelectric material layer 80 is formed on the release layer 78 as illustrated in Figure 9C. Preferably, the N-type thermoelectric material layer 80 is formed of the thermoelectric material 32, 42, or 56 described above. However, the present disclosure is not limited thereto. Other types of

thin film thermoelectric materials may be used. The N-type thermoelectric material layer 80 is formed using known thin film fabrication techniques such as molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), or metal organic chemical vapor deposition (MOCVD). In one embodiment, the N-type

5 thermoelectric material layer 80 has a thickness in a range of and including 5 micrometers (μm) to 25 μm . A metallization layer (ML) 82 is then formed on the N-type thermoelectric material layer 80, as illustrated in Figure 9D. The metallization layer 82 serves multiple functions and therefore may be comprised of one or more different materials, or sub-layers. Preferably, the metallization

10 layer 82 includes an ohmic contact sub-layer adjacent to the N-type thermoelectric material layer 80 to achieve a low specific contact resistance, a diffusion barrier sub-layer to prevent migration of atomic species into the N-type thermoelectric material layer 80, a eutectic bonding metal for low temperature attachment to another metal, and an oxidation barrier sub-layer such as Gold.

15 The thickness of the metallization layer 82 is preferably in the range of and including 1.0 to 5.0 microns. The metallization layer 82 is formed via a blanket metallization process such as, for example, electron beam deposition or electroplating. The metallization layer 82 preferably includes materials having high electrical and thermal conductivities. For example, Copper or Silver may be

20 used.

[0046] Next, a photoresist layer 84 is deposited and patterned as illustrated in Figure 9E. The metallization layer 82 and the N-type thermoelectric material layer 80 are then etched completely through the N-type thermoelectric material layer 80 down to the release layer 78 in the regions of the removed photoresist

25 layer 84 to form a number of N-type thermoelectric material legs 86-1 through 86-20 (generally referred to herein as N-type thermoelectric material legs 86), as illustrated in Figure 9F. A combination of wet chemical and dry plasma etching or dry plasma etching alone can be used. Note that while twenty N-type thermoelectric material legs 86 are illustrated, there may be any desired number

30 of one or more N-type thermoelectric material legs 86. Each of the N-type

thermoelectric material legs 86 includes a corresponding portion of the N-type thermoelectric material layer 80 and the metallization layer 82.

[0047] Next, a first electrode assembly 88 is bonded to a first portion of the N-type thermoelectric material legs 86 as illustrated in Figure 9G. The first

5 electrode assembly 88 includes an Aluminum Nitride (AlN) ceramic 90 and a number of Copper traces 92-1 through 92-10 (only 92-1 through 92-3 are visible in Figure 9G). Again, Copper is exemplary. Other materials having high electrical and thermal conductivity may be used. For example, Silver may alternatively be used. In this embodiment, the Copper traces 92-1 through 92-10
10 (generally referred to herein as Copper traces 92) are metalized with a eutectic bonding material (EBM) such as, for example, Gold-Tin, Lead-Tin, Gold-Indium, Indium, or the like. The eutectic bonding material preferably has a thickness in the range of and including 0.5 to 5.0 microns. The eutectic bonding material is a low melting temperature material that requires significantly less pressure for
15 bonding when liquid than, for example, Copper-to-Copper diffusion bonding. As a result, the chance of the N-type thermoelectric material being damaged as a result of pressure during bonding is substantially reduced. The bonding step is preferably performed in a vacuum environment to prevent formation of unwanted oxides. Note, however, that the present disclosure is not limited to eutectic
20 bonding. It should also be noted that AlN is exemplary. Any material having low electrical conductivity and high thermal conductivity may be used (e.g., diamond, Beryllium Oxide, Alumina, or the like).

[0048] In this embodiment, the Copper traces 92 are "L" shaped. In one embodiment, at their thickest point, the "L" shaped Copper traces 92 have a
25 thickness in a range of and including 2 μm to 5 μm and, at their thinnest point, the "L" shaped Copper traces 92 have a thickness in a range of and including 1 μm to 2 μm . Multiple deposition steps using physical vapor or electrochemical deposition methods can be used to form the "L" shaped traces. Additive techniques involving use of shadow masks or subtractive techniques involving
30 photolithographic masks and chemical etching can be used. Preferably, the Copper traces 92 will be coated with a eutectic bonding metal for facilitating low

temperature attachment to the metallized TE leg segments. The N-type thermoelectric material legs 86-1, 86-3, 86-5, 86-7, 86-9, 86-11, 86-13, 86-15, 86-17, and 86-19 are bonded to the Copper traces 92-1 through 92-10, respectively. The thin portions of the "L" shaped Copper traces 92 are locations at which P-type thermoelectric material legs will subsequently be bonded to complete fabrication of the thermoelectric module 70.

[0049] At this point, the release layer 78 is dissolved such that the N-type thermoelectric material legs 86 are released from the substrate 76. In one embodiment, the release layer 78 is Barium Fluoride (BaF_2) and is dissolved in water. The first electrode assembly 88 is then lifted from the substrate 76 as illustrated in Figure 9H. The exposed N-type thermoelectric material surfaces of the N-type thermoelectric material legs 86 are then metallized with a metallization layer 93 as illustrated in Figure 9I. Preferably, the metallization layer 93 includes an ohmic contact sub-layer adjacent to the N-type thermoelectric material to achieve a low specific contact resistance, a diffusion barrier sub-layer to prevent migration of atomic species into the N-type thermoelectric material, a eutectic bonding metal for low temperature attachment to another metal, and an oxidation barrier sub-layer such as Gold. The metallization layer 93 on the surface of each of the N-type thermoelectric material legs 86 can be formed by a direct line-of-sight physical vapor deposition technique such as electron beam evaporation such that the metallization layer 93 does not coat the sidewalls of the N-type thermoelectric material legs 86. If necessary, the sidewalls of the N-type thermoelectric material legs 86 can be coated with photoresist for protection from metal deposition. Standard metallization lift-off techniques familiar to those skilled in the art can then be used to obtain electrode assembly structures where the metallization layer 93 covers only the top surfaces of the N-type thermoelectric material legs 86.

[0050] The process of Figures 9A through 9I is also performed for P-type thermoelectric material in order to form P-type thermoelectric material legs 94 bonded to a second electrode assembly 96, as illustrated in Figure 9J. Like the first electrode assembly 88, the second electrode assembly 96 includes an AlN

ceramic 98 and a number of Copper traces 100-1 through 100-10 (generally referred to herein as Copper traces 100). The Copper traces 100-1 through 100-10 are bonded to a corresponding portion of the P-type thermoelectric material legs 94, namely, the P-type thermoelectric material legs 94-2, 94-4, 94-6, 94-8, 94-10, 94-12, 94-14, 94-16, 94-18, and 94-20. Note that the second electrode assembly includes a Copper trace 100-0 that has a thinner portion, a position at which a corresponding P-type thermoelectric material leg 94 is to be bonded.

[0051] Again, after removing the second electrode assembly 96 including the P-type thermoelectric material legs 94 from a corresponding substrate, the

exposed P-type thermoelectric material surfaces of the P-type thermoelectric material legs 96 are metalized with a metallization layer 101, as is also illustrated in Figure 9J. Preferably, the metallization layer 101 includes an ohmic contact sub-layer adjacent to the P-type thermoelectric material to achieve a low specific contact resistance, a diffusion barrier sub-layer to prevent migration of atomic species into the P-type thermoelectric material, a eutectic bonding metal for low temperature attachment to another metal, and an oxidation barrier sub-layer such as Gold. The eutectic bonding metal used here will preferably have a lower liquidus temperature than the eutectic bonding metal on the other side of the TE leg material. For example, a AuIn eutectic bonding metal can be used without allowing a higher liquidus temperature AuSn bonding metal to become liquid on the other side of the TE leg. The metallization layer 101 on the surface of each of the P-type thermoelectric material legs 94 can be formed by a direct line-of-sight physical vapor deposition technique such as electron beam evaporation such that the metallization layer 101 does not coat the sidewalls of the P-type thermoelectric material legs 94. If necessary, the sidewalls of the P-type thermoelectric material legs 94 can be coated with photoresist for protection from metal deposition. Standard metallization lift-off techniques familiar to those skilled in the art can then be used to obtain electrode assembly structures where the metallization layer 101 covers only the top surfaces of the P-type thermoelectric material legs 94.

[0052] Lastly, the first electrode assembly 88 of Figure 9I is bonded to the second electrode assembly 96 of Figure 9J using a flip-chip bonding process as illustrated in Figure 9K. The bonding temperature will be high enough to liquefy the eutectic bonding metal but below the liquidus temperature of the previously used eutectic bonding metal on the other side of the TE material. At this point, fabrication of the thermoelectric module 70 is complete. Specifically, the N-type thermoelectric material leg 86-1 and the P-type thermoelectric material leg 94-2 form a first thermoelectric device, the N-type thermoelectric material leg 86-3 and the P-type thermoelectric material leg 94-4 form a second thermoelectric device coupled in series with the first thermoelectric device, and so on.

[0053] Figures 10A through 10P illustrate fabrication of the thermoelectric module 70 of Figure 8 according to another embodiment of the present disclosure. Many aspects of this process are the same as that described above. Again, the process starts with the substrate 76, as illustrated in Figure 10A.

Next, as illustrated in Figure 10B, the release layer 78 is formed on the substrate 76. Next, the N-type thermoelectric material layer 80 is formed on the release layer 78 as illustrated in Figure 10C. A magnetic metallization layer (MML) 102 is then formed on the N-type thermoelectric material layer 80, as illustrated in Figure 10D. In this embodiment, the magnetic metallization layer 102 is substantially the same as the metallization layer 82 of Figure 9D described above but further includes a magnetic material. In one preferred embodiment, the magnetic metallization layer 102 includes a sub-layer of a magnetic material such as Cobalt (Co). The Cobalt sub-layer is preferably 50 nanometers (nm) to 300 nm thick. Note that other types of magnetic materials that have high electrical and thermal conductivity may be used. The sub-layer of magnetic material, such as Cobalt (Co), may be positioned at any desired location within the sub-layers of the magnetic metallization layer 102. For instance, the sub-layer of magnetic material may be the first sub-layer of the magnetic metallization layer 102 adjacent to the N-type thermoelectric material layer 80, an upper most sub-layer of the magnetic metallization layer 102, or any sub-layer in between the top and bottom surface of the magnetic metallization layer 102. The magnetic

metallization layer 102 is formed via a blanket metallization process such as, for example, PVD or electroplating.

[0054] Next, the photoresist layer 84 is deposited and patterned as illustrated in Figure 10E. The magnetic metallization layer 102 and the N-type

5 thermoelectric material layer 80 are then etched down completely through the N-type thermoelectric material layer 80 to the release layer 78 in the removed regions of the patterned photoresist layer 84 to form the N-type thermoelectric material legs 86, as illustrated in Figure 10F. Each of the N-type thermoelectric material legs 86 includes a corresponding portion of the N-type thermoelectric material layer 80 and the magnetic metallization layer 102. Next, the first electrode assembly 88 is bonded to the first portion of the N-type thermoelectric material legs 86 as illustrated in Figure 10G. Again, in this embodiment, the Copper traces 92 are metalized with the eutectic bonding material such as, for example, Gold-Tin, Lead-Tin, Gold-Indium, Indium, or the like.

10 **[0055]** At this point, a magnet 104 is placed under the substrate 76 opposite the N-type thermoelectric material legs 86. The release layer 78 is then dissolved. The first electrode assembly 88 is then lifted from the substrate 76 as illustrated in Figure 10H. The exposed N-type thermoelectric material surfaces of the N-type thermoelectric material legs 86 are then metalized with the metallization layer 93 as illustrated in Figure 10I. Preferably, the metallization layer 93 includes an ohmic contact sub-layer adjacent to the N-type thermoelectric material to achieve a low specific contact resistance, a diffusion barrier sub-layer to prevent migration of atomic species into the N-type thermoelectric material, a eutectic bonding metal for low temperature attachment to another metal, and an oxidation barrier sub-layer such as Gold. The eutectic bonding metal used here will preferably have a lower liquidus temperature than the eutectic bonding metal on the other side of the TE leg material. For example, a AuIn eutectic bonding metal can be used without allowing a higher liquidus temperature AuSn bonding metal to become liquid on the other side of the TE leg. The metallization layer 93 on the surface of each of the N-type thermoelectric material legs 86 can be formed by a direct line-of-sight physical

vapor deposition technique such as electron beam evaporation such that the metallization layer 93 does not coat the sidewalls of the N-type thermoelectric material legs 86. If necessary, the sidewalls of the N-type thermoelectric material legs 86 can be coated with photoresist for protection from metal deposition.

- 5 Standard metallization lift-off techniques familiar to those skilled in the art can then be used to obtain electrode assembly structures where the metallization layer 93 covers only the top surfaces of the N-type thermoelectric material legs 86.

[0056] Due to the magnetic force between the magnet 104 and the magnetic
10 metallization layer portion of the N-type thermoelectric material legs 86, the N-type thermoelectric material legs 86 that are not bonded to the first electrode assembly 88 remain on the substrate 76 after the release layer 78 is dissolved. Without the magnetic force, the unharvested N-type thermoelectric material legs 86 (i.e., the N-type thermoelectric material legs 86 that are not bonded to the first
15 electrode assembly 88) are lost when the release layer 78 is dissolved. Thus, yield can be increased from 50% to 100%.

[0057] Because the remaining portion of the N-type thermoelectric material legs 86 remain on the substrate 76 due to the magnetic force, in this embodiment, the remaining portion of the N-type thermoelectric material legs 86
20 can be harvested by bonding a third electrode assembly 106 to the remaining portion of the N-type thermoelectric material legs 86 as illustrated in Figure 10J. The third electrode assembly 106 includes an AlN ceramic 108 and a number of Copper traces 110-1 through 110-10 (only 110-1 and 110-2 are visible in Figure 10J), which are generally referred to herein as Copper traces 110. Note that
25 there is also a Copper trace 110-0 that is not "L" shaped defining a position at which a P-type thermoelectric material leg 94 is to be bonded. Again, Copper is exemplary. Other materials having high electrical and thermal conductivity may be used. For example, Silver may alternatively be used. In this embodiment, the Copper traces 110 are metalized with a eutectic bonding material (EBM) such as,
30 for example, Gold-Tin, Lead-Tin, Gold-Indium, Indium, or the like. The eutectic bonding material preferably has a thickness in the range of and including 0.5 to

5.0 microns. The eutectic bonding material is a low melting temperature material that requires significantly less pressure for bonding when liquid than, for example, Copper-to-Copper diffusion bonding. As a result, the chance of the N-type thermoelectric material being damaged as a result of pressure during bonding is substantially reduced. The bonding step is preferably performed in a vacuum environment to prevent formation of unwanted oxides. Note, however, that the present disclosure is not limited to eutectic bonding. It should also be noted that AlN is exemplary. Any material having low electrical conductivity and high thermal conductivity may be used (e.g., diamond, Beryllium Oxide, Alumina, or the like).

[0058] In this embodiment, the Copper traces 110 are "L" shaped. In one embodiment, at their thickest point, the "L" shaped Copper traces 110 have a thickness in a range of and including 2 μm to 5 μm and, at their thinnest point, the "L" shaped Copper traces 110 have a thickness in a range of and including 1 μm to 2 μm . Multiple deposition steps using physical vapor or electrochemical deposition methods can be used to form the "L" shaped traces. Additive techniques involving use of shadow masks or subtractive techniques involving photolithographic masks and chemical etching can be used. Preferably, the Copper traces 110 will be coated with a eutectic bonding metal for facilitating low temperature attachment to the metallized TE leg segments. The N-type thermoelectric material legs 86-2, 86-4, 86-6, 86-8, 86-10, 86-12, 86-14, 86-16, 86-18, and 86-20 are bonded to the Copper traces 110-1 through 110-10, respectively. The thin portions of the "L" shaped Copper traces 110 are locations at which P-type thermoelectric material legs will subsequently be bonded to complete fabrication of the thermoelectric module 70.

[0059] The third electrode assembly 106, including the N-type thermoelectric material legs 86, is then lifted from the substrate 76 as illustrated in Figure 10K. Note that the magnet 104 may be moved away from the substrate 76 (or vice versa) in order to release the remaining portion of the N-type thermoelectric material legs 86 from the substrate 76. Again, the exposed N-type thermoelectric material surfaces of the N-type thermoelectric material legs 86 are then

metalized with the metallization layer 93 as illustrated in Figure 10L in the manner described above.

[0060] The process of Figures 10A through 10L is also performed for P-type thermoelectric material in order to form the P-type thermoelectric material legs 94 bonded to the second electrode assembly 96 and a fourth electrode assembly 112, as illustrated in Figures 10M and 10N, respectively. Like the other electrode assemblies, the fourth electrode assembly 112 includes an AlN ceramic 114 and a number of Copper traces 116-1 through 116-10 (generally referred to herein as Copper traces 116). The Copper traces 100-1 through 100-10 of the second electrode assembly 96 are bonded to a corresponding portion of the P-type thermoelectric material legs 94, namely, the P-type thermoelectric material legs 94-2, 94-4, 94-6, 94-8, 94-10, 94-12, 94-14, 94-16, 94-18, and 94-20. Likewise, the Copper traces 116-1 through 116-10 of the fourth electrode assembly 112 are bonded to the remaining portion of the P-type thermoelectric material legs 94, namely, the P-type thermoelectric material legs 94-1, 94-3, 94-5, 94-7, 94-9, 94-11, 94-13, 94-15, 94-17, and 94-19.

[0061] Lastly, the first electrode assembly 88 of Figure 10I is bonded to the second electrode assembly 96 of Figure 10M using a flip-chip bonding process as illustrated in Figure 10O. The bonding temperature will be high enough to liquefy the eutectic bonding metal but below the liquidus temperature of the previously used eutectic bonding metal on the other side of the TE material. At this point, fabrication of the thermoelectric module 70 is complete. In the same manner, the third electrode assembly 106 of Figure 10L and the fourth electrode assembly 112 of Figure 10N are bonded together using a flip-chip bonding process to fabricate a second thermoelectric module 118 as illustrated in Figure 10P.

[0062] Figures 11A through 11O illustrate fabrication of the thermoelectric module 70 of Figure 8 according to another embodiment of the present disclosure. Many aspects of this process are the same as that described above. Again, the process starts with the substrate 76, as illustrated in Figure 11A. Next, as illustrated in Figure 11B, the release layer 78 is formed on the substrate

76. Next, the N-type thermoelectric material layer 80 is formed on the release layer 78 as illustrated in Figure 11C. The metallization layer 82 is then formed on the N-type thermoelectric material layer 80, as illustrated in Figure 10D. Next, the photoresist layer 84 is deposited and patterned as illustrated in Figure 11E.

5 **[0063]** The metallization layer 82 and the N-type thermoelectric material layer 80 are then etched down to a predetermined thickness (t) from a bottom of the N-type thermoelectric material layer 80, which in this embodiment is the predetermined thickness (t) from the release layer 78, through the removed portions of the patterned photoresist layer 84 to form the N-type thermoelectric material legs 86, as illustrated in Figure 11F. Each of the N-type thermoelectric material legs 86 includes a corresponding portion of the N-type thermoelectric material layer 80 and the metallization layer 82. In one embodiment, the predetermined thickness (t) may be, for example, 0.5 μm to 2 μm . In another embodiment, the predetermined thickness is 10% to 20% of the thickness of the N-type thermoelectric material layer 80. As discussed below, by not etching all the way through the N-type thermoelectric material layer 80, the bottom surface of the N-type thermoelectric material layer 80 is a continuous surface that is suitable for blanket metallization.

15 **[0064]** Next, the release layer 78 is dissolved to remove the N-type thermoelectric material legs 86 from the substrate 76, and blanket metallization is performed to form a magnetic metallization layer 120 on the continuous bottom surface of the N-type thermoelectric material legs 86 as illustrated in Figure 11G. The magnetic metallization layer 120 preferably includes a number of sub-layers including a sub-layer of magnetic material such as Cobalt (Co). In one embodiment, the magnetic metallization layer 120 includes a Cobalt (Co) sub-layer, where the Cobalt (Co) sub-layer has a thickness in the range of and including 50 nm to 300 nm. The magnetic metallization layer 120 may also include an ohmic contact sub-layer adjacent to the N-type thermoelectric material to achieve a low specific contact resistance, a diffusion barrier sub-layer to prevent migration of atomic species into the N-type thermoelectric material, a eutectic bonding metal for low temperature attachment to another metal, and an

oxidation barrier sub-layer such as Gold. The overall thickness of the magnetic metallization layer 120 is preferably in the range of and including 1.0 and 5.0 microns. Note that Cobalt is exemplary. Other types of magnetic materials having high electrical and thermal conductivity may be used.

5 **[0065]** The N-type thermoelectric material legs 86 are then placed on a substrate 122, and the first electrode assembly 88 is bonded to the first portion of the N-type thermoelectric material legs 86 as illustrated in Figure 11H. The first electrode assembly 88 includes the AlN ceramic 90 and the Copper traces 92. At this point, a magnet 124 is placed under the substrate 122 opposite the N-type
10 thermoelectric material legs 86 as also illustrated in Figure 11H. As result of the mechanical force from lifting the first electrode assembly 88 and the magnetic force between the magnet 124 and the Cobalt, the N-type thermoelectric material legs 86 are broken apart to provide the first electrode assembly 88 having the first portion of the N-type thermoelectric material legs 86 bonded thereto, as
15 illustrated in Figure 11I. Note that the unharvested N-type thermoelectric material legs 86 (i.e., the N-type thermoelectric material legs 86 that are not bonded to the first electrode assembly 88) remained attached to the substrate 122. In this embodiment, the third electrode assembly 106 is bonded to the remaining portion of the N-type thermoelectric material legs 86 as illustrated in
20 Figure 11J. The third electrode assembly 106 includes the AlN ceramic 108 and the Copper traces 110. The third electrode assembly 106, including the N-type thermoelectric material legs 86, is then lifted from the substrate 76 as illustrated in Figure 11K.

[0066] The process of Figures 11A through 11K is also performed for P-type
25 thermoelectric material in order to form the P-type thermoelectric material legs 94 bonded to the second electrode assembly 96 and the fourth electrode assembly 112, as illustrated in Figures 11L and 11M, respectively. Lastly, the first electrode assembly 88 of Figure 11I is bonded to the second electrode assembly 96 of Figure 11L using a flip-chip bonding process as illustrated in Figure 11N.
30 At this point, fabrication of the thermoelectric module 70 is complete. In the same manner, the third electrode assembly 106 of Figure 11K and the fourth

electrode assembly 112 of Figure 11M are bonded together using a flip-chip bonding process to fabricate the second thermoelectric module 118 as illustrated in Figure 11O.

[0067] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A method of fabrication of a thermoelectric module comprising:
 - 5 forming an N-type thin film thermoelectric material layer on a first substrate;
 - forming a first metallization layer on the N-type thin film thermoelectric material layer;
 - etching the first metallization layer and the N-type thin film thermoelectric material layer to form a plurality of N-type thermoelectric material legs;
 - 10 bonding a first electrode assembly to a first portion of the plurality of N-type thermoelectric material legs;
 - removing the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs from the first substrate;
 - 15 forming a P-type thin film thermoelectric material layer on a second substrate;
 - forming a second metallization layer over the P-type thin film thermoelectric material layer;
 - etching the second metallization layer and the P-type thin film thermoelectric material layer to form a plurality of P-type thermoelectric material legs;
 - 20 bonding a second electrode assembly to a first portion of the plurality of P-type thermoelectric material legs;
 - removing the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs from the second substrate; and
 - 25 bonding the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs to the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs via a flip-chip bonding process to form a thermoelectric module comprising a plurality
 - 30 of thermoelectric devices connected in series.

2. The method of claim 1 wherein:

etching the first metallization layer and the N-type thin film thermoelectric material layer comprises etching the first metallization layer and the N-type thin film thermoelectric material layer completely through the N-type thin film

5 thermoelectric material layer; and

etching the second metallization layer and the P-type thin film thermoelectric material layer comprises etching the second metallization layer and the P-type thin film thermoelectric material layer completely through the P-type thin film thermoelectric material layer.

10

3. The method of claim 2 wherein:

removing the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs from the first substrate comprises dissolving a release layer situated between the first substrate and the N-type thin film thermoelectric material layer to thereby separate the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs bonded thereto from the first substrate; and

15

removing the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs from the second substrate comprises dissolving a release layer situated between the second substrate and the P-type thin film thermoelectric material layer to thereby separate the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs bonded thereto from the second substrate.

20

25 4. The method of claim 2 wherein the first metallization layer is a first magnetic metallization layer comprising a magnetic material, and the second metallization layer is a second magnetic metallization layer comprising a magnetic material.

30 5. The method of claim 4 wherein:

etching the first metallization layer and the N-type thin film thermoelectric material layer comprises etching the first magnetic metallization layer and the N-type thin film thermoelectric material layer completely through the N-type thin film thermoelectric material layer; and

5 etching the second metallization layer and the P-type thin film thermoelectric material layer comprises etching the second magnetic metallization layer and the P-type thin film thermoelectric material layer completely through the P-type thin film thermoelectric material layer.

10 6. The method of claim 5 wherein removing the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs from the first substrate comprises:

placing a magnet adjacent to a surface of the first substrate opposite the plurality of N-type thermoelectric material legs; and

15 dissolving a release layer situated between the first substrate and the N-type thin film thermoelectric material layer to thereby separate the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs bonded thereto from the first substrate;

wherein a magnetic force between the magnet and magnetic material that remains from the first magnetic metallization layer maintains a remaining portion of the plurality of N-type thermoelectric material legs that are not bonded to the first electrode assembly on the first substrate.

25 7. The method of claim 6 wherein removing the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs from the second substrate comprises:

placing a magnet adjacent to a surface of the second substrate opposite the plurality of P-type thermoelectric material legs; and

30 dissolving a release layer situated between the second substrate and the P-type thin film thermoelectric material layer to thereby separate the second

electrode assembly including the first portion of the plurality of P-type thermoelectric material legs bonded thereto from the second substrate;

wherein a magnetic force between the magnet and magnetic material that remains from the second magnetic metallization layer maintains a remaining
5 portion of the plurality of P-type thermoelectric material legs that are not bonded to the second electrode assembly on the second substrate.

8. The method of claim 7 further comprising:

10 bonding a third electrode assembly to the remaining portion of the plurality of N-type thermoelectric material legs;

bonding a fourth electrode assembly to the remaining portion of the plurality of P-type thermoelectric material legs; and

15 bonding the third electrode assembly to the fourth electrode assembly via the flip-chip bonding process to form a second thermoelectric module comprising a plurality of thermoelectric devices connected in series.

9. The method of claim 1 wherein:

20 etching the first metallization layer and the N-type thin film thermoelectric material layer comprises etching the first metallization layer and the N-type thin film thermoelectric material layer to a predetermined thickness from a bottom of the N-type thin film thermoelectric material layer; and

25 etching the second metallization layer and the P-type thin film thermoelectric material layer comprises etching the second metallization layer and the P-type thin film thermoelectric material layer to a predetermined thickness from a bottom of the P-type thin film thermoelectric material layer.

10. The method of claim 9 wherein removing the first electrode assembly including the first portion of the plurality of N-type thermoelectric material legs from the first substrate comprises:

30 dissolving a release layer positioned between the first substrate and the N-type thin film thermoelectric material layer to thereby remove the plurality of N-

type thermoelectric material legs from the first substrate, the plurality of N-type thermoelectric material legs having a continuous bottom surface as a result of etching to the predetermined thickness from the bottom of the N-type thin film thermoelectric material layer;

- 5 forming a third metallization layer on the continuous bottom surface of the plurality of N-type thermoelectric material legs; and
 separating the plurality of N-type thermoelectric material legs.

11. The method of claim 10 wherein separating the plurality of N-type
10 thermoelectric material legs comprises separating the plurality of N-type thermoelectric material legs by mechanical force.

12. The method of claim 10 wherein separating the plurality of N-type thermoelectric material legs comprises:

- 15 attaching the continuous bottom surface of the plurality of N-type thermoelectric material legs comprising the third metallization layer to a substrate; and
 after bonding the first electrode assembly to the first portion of the plurality of N-type thermoelectric material legs, lifting the first electrode assembly such
20 that the first portion of the plurality of N-type thermoelectric material legs are separated from a remaining portion of the plurality of N-type thermoelectric material legs by mechanical force.

13. The method of claim 10 wherein the third metallization layer on the
25 continuous bottom surface of the plurality of N-type thermoelectric material legs is a magnetic metallization layer that comprises a magnetic material, and separating the plurality of N-type thermoelectric material legs comprises:

- placing the continuous bottom surface of the plurality of N-type thermoelectric material legs comprising the magnetic metallization layer on a
30 substrate;

placing a magnet adjacent to a surface of the substrate opposite the plurality of N-type thermoelectric material legs; and

after bonding the first electrode assembly to the first portion of the plurality of N-type thermoelectric material legs, lifting the first electrode assembly such
5 that the first portion of the plurality of N-type thermoelectric material legs are separated from a remaining portion of the plurality of N-type thermoelectric material legs by mechanical force and the remaining portion of the plurality of N-type thermoelectric material legs are maintained on the substrate as a result of a magnetic force between the magnet and corresponding portions of the magnetic
10 metallization layer on the continuous bottom surface of the plurality of N-type thermoelectric material legs.

14. The method of claim 10 wherein the third metallization layer on the continuous bottom surface of the plurality of N-type thermoelectric material legs
15 comprises a Copper sub-layer.

15. The method of claim 10 wherein removing the second electrode assembly including the first portion of the plurality of P-type thermoelectric material legs from the second substrate comprises:

20 dissolving a release layer positioned between the second substrate and the P-type thin film thermoelectric material layer to thereby remove the plurality of P-type thermoelectric material legs from the second substrate, the plurality of P-type thermoelectric material legs having a continuous bottom surface as a result of etching to the predetermined thickness from the bottom of the P-type thin film
25 thermoelectric material layer;

forming a fourth metallization layer on the continuous bottom surface of the plurality of P-type thermoelectric material legs; and

separating the plurality of P-type thermoelectric material legs.

16. The method of claim 15 wherein separating the plurality of P-type thermoelectric material legs comprises separating the plurality of P-type thermoelectric material legs by mechanical force.

5 17. The method of claim 15 wherein separating the plurality of P-type thermoelectric material legs comprises:

attaching the continuous bottom surface of the plurality of P-type thermoelectric material legs comprising the fourth metallization layer to a substrate; and

10 after bonding the second electrode assembly to the first portion of the plurality of P-type thermoelectric material legs, lifting the second electrode assembly such that the first portion of the plurality of P-type thermoelectric material legs are separated from a remaining portion of the plurality of P-type thermoelectric material legs by mechanical force.

15

18. The method of claim 16 wherein the fourth metallization layer on the bottom surface of the plurality of P-type thermoelectric material legs is a magnetic metallization layer that comprises a magnetic material, and separating the plurality of P-type thermoelectric material legs comprises:

20 placing the continuous bottom surface of the plurality of P-type thermoelectric material legs comprising the magnetic metallization layer on a substrate;

placing a magnet adjacent a surface of the substrate opposite the plurality of P-type thermoelectric material legs; and

25 after bonding the second electrode assembly to the first portion of the plurality of P-type thermoelectric material legs, lifting the second electrode assembly such that the first portion of the plurality of P-type thermoelectric material legs are separated from a remaining portion of the plurality of P-type thermoelectric material legs by mechanical force and the remaining portion of the plurality of P-type thermoelectric material legs are maintained on the substrate as
30 a result of a magnetic force between the magnet and corresponding portions of

the magnetic metallization layer formed on the continuous bottom surface of the plurality of P-type thermoelectric material legs.

19. The method of claim 15 wherein the fourth metallization layer on the continuous bottom surface of the plurality of P-type thermoelectric material legs comprises a Copper sub-layer.

20. The method of claim 16 further comprising:

bonding a third electrode assembly to the remaining portion of the plurality of N-type thermoelectric material legs;

bonding a fourth electrode assembly to the remaining portion of the plurality of P-type thermoelectric material legs; and

bonding the third electrode assembly to the fourth electrode assembly via the flip-chip bonding process to form a second thermoelectric module comprising a plurality of thermoelectric devices connected in series.

21. The method of claim 9 wherein the predetermined thickness from the bottom of the N-type thin film thermoelectric material layer is in a range of about 10% to 20% of a thickness of the N-type thin film thermoelectric material layer, and the predetermined thickness from the bottom of the P-type thin film thermoelectric material layer is in a range of about 10% to 20% of a thickness of the P-type thin film thermoelectric material layer.

22. A thermoelectric device comprising:

an N-type thermoelectric material leg comprising an N-type thin film thermoelectric material, wherein a thickness of the N-type thin film thermoelectric material is in a range of about 5 micrometers (μm) to 25 μm ; and

a P-type thermoelectric material leg comprising a P-type thin film thermoelectric material, wherein a thickness of the P-type thin film thermoelectric material is in a range of about 5 μm to 25 μm .

23. The thermoelectric device of claim 24 wherein the N-type thin film thermoelectric material and the P-type thin film thermoelectric material are formed of Group IV-VI semiconductor materials.

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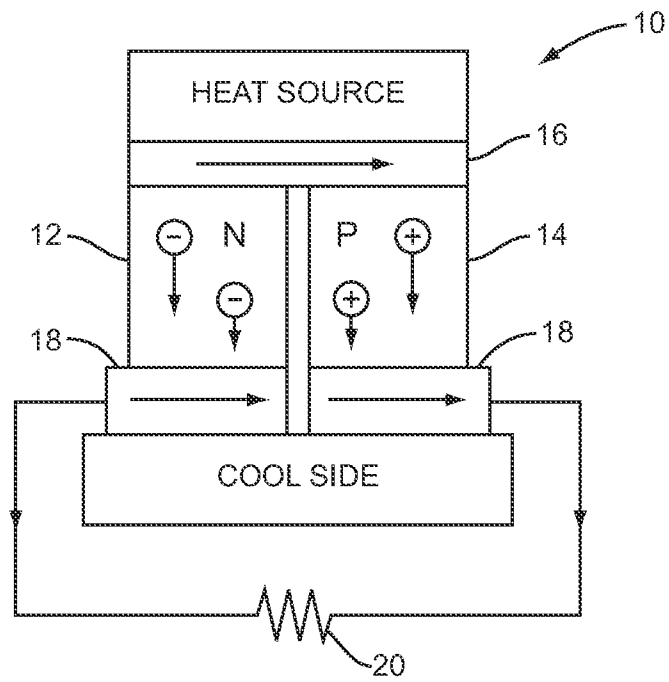


FIG. 1A
(PRIOR ART)

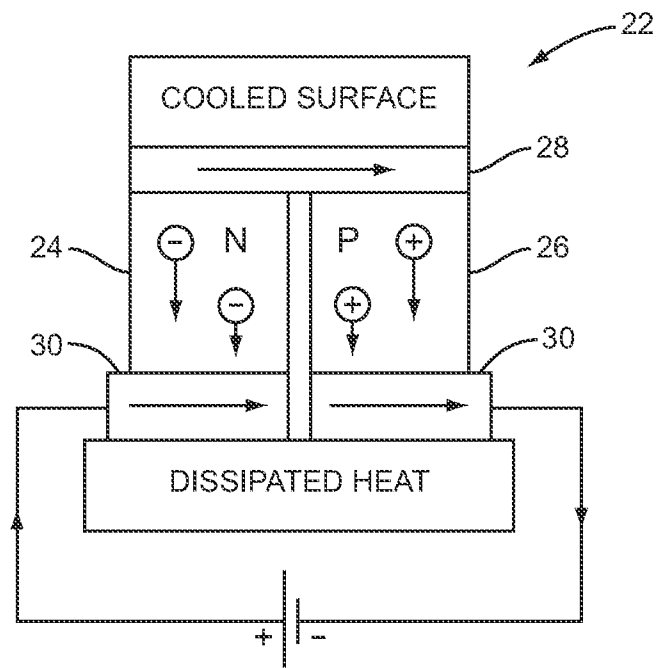
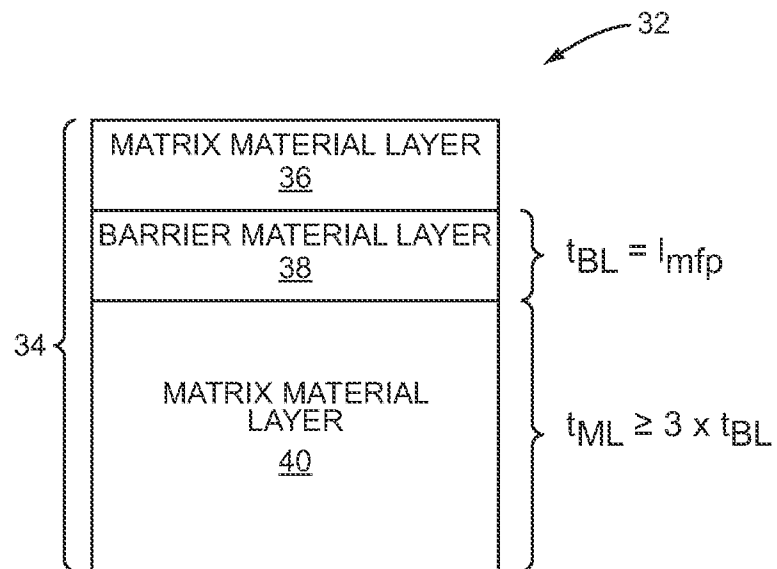
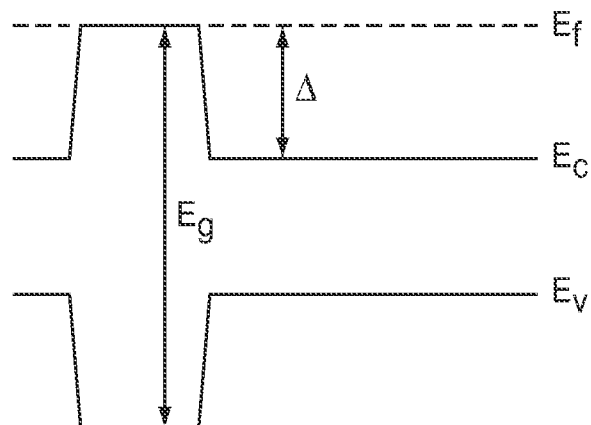
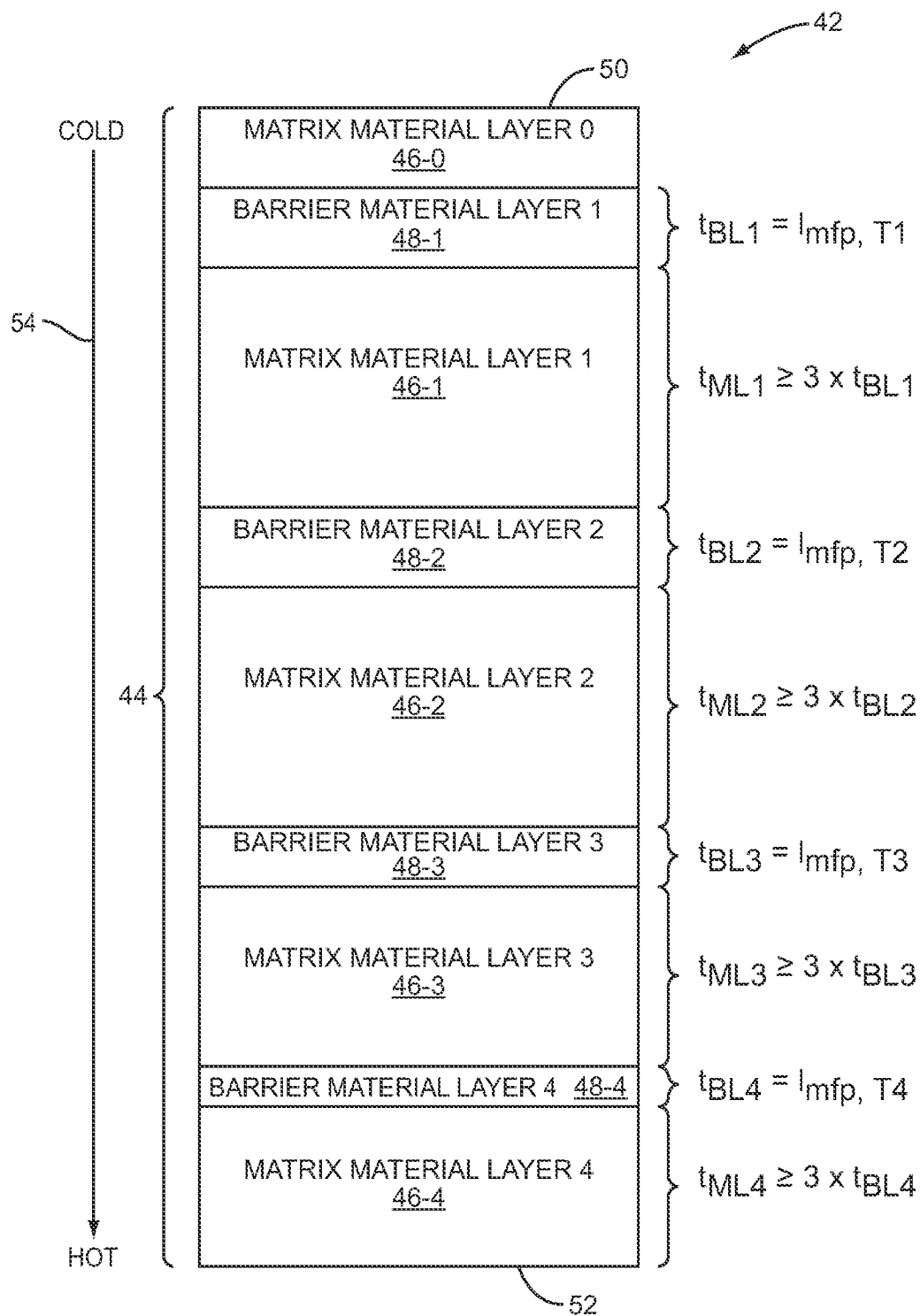


FIG. 1B
(PRIOR ART)

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**FIG. 2****FIG. 3**

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**FIG. 4**

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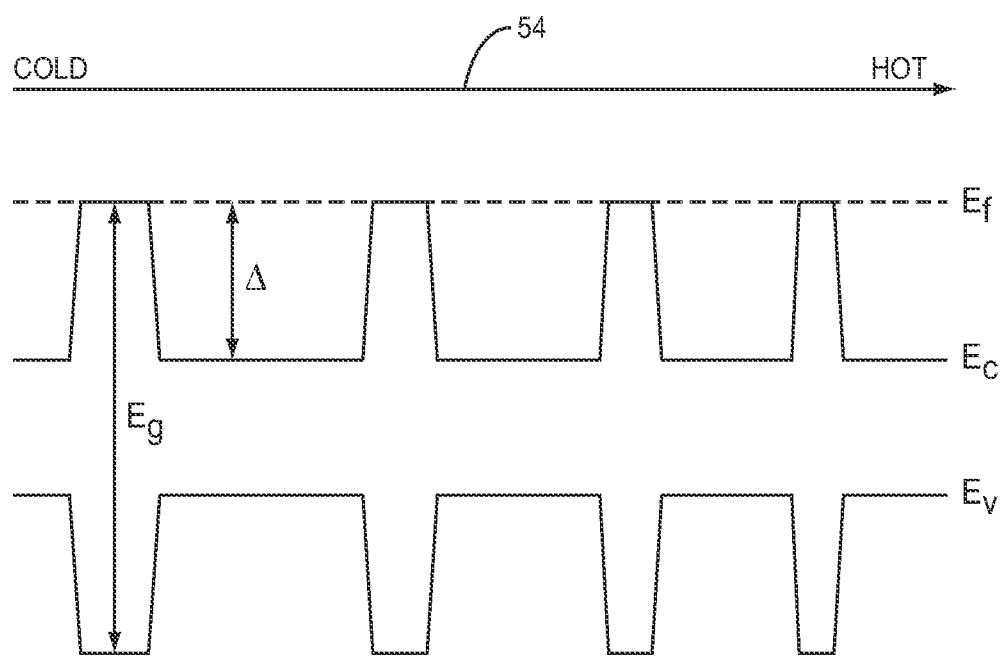


FIG. 5

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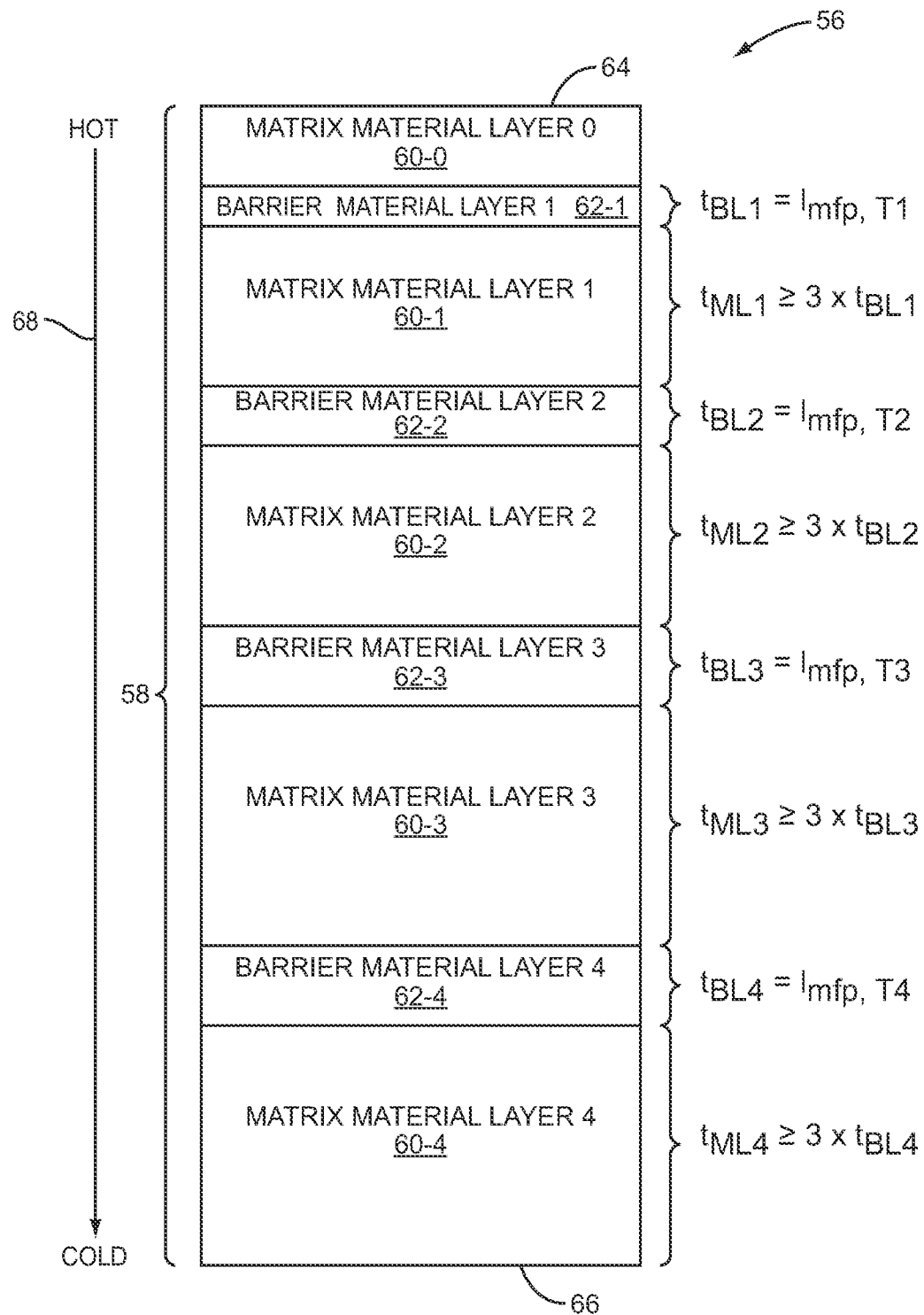


FIG. 6

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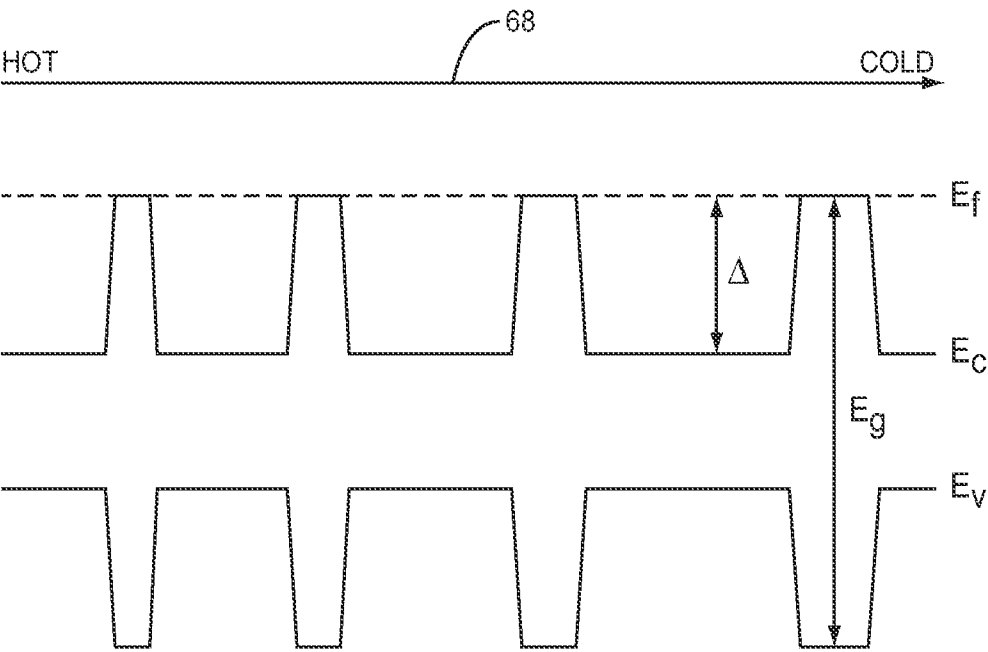


FIG. 7

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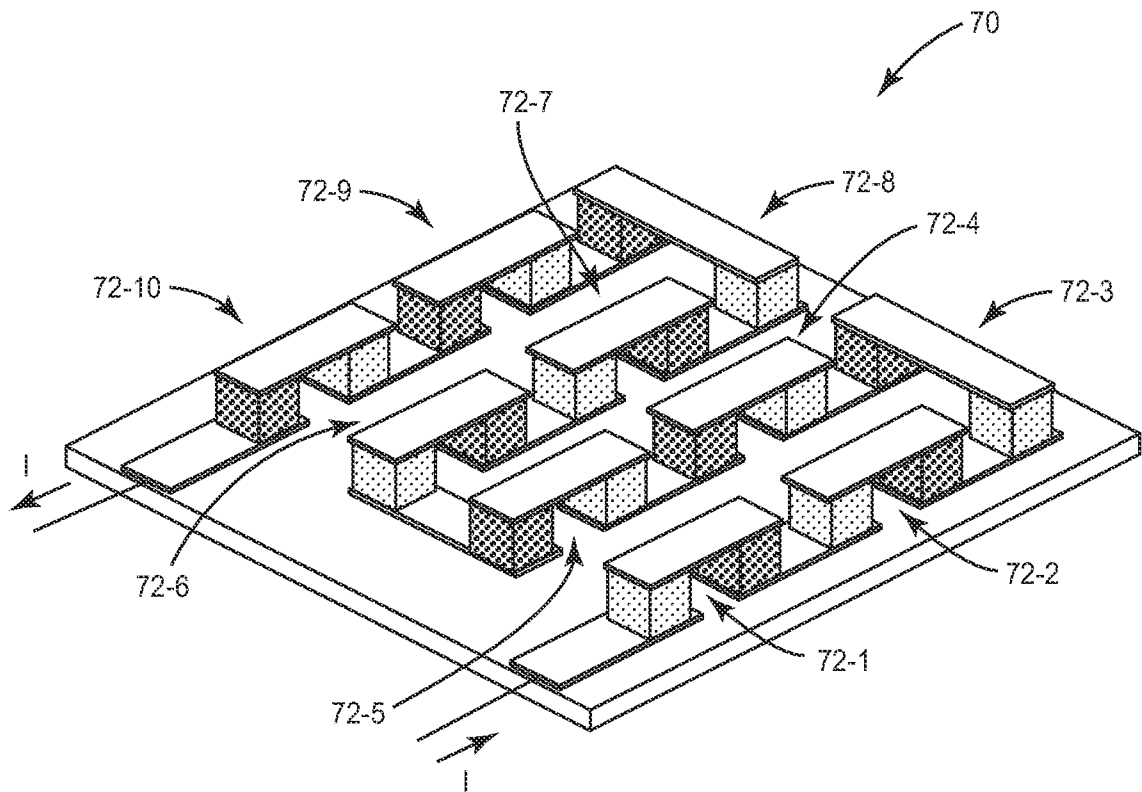


FIG. 8

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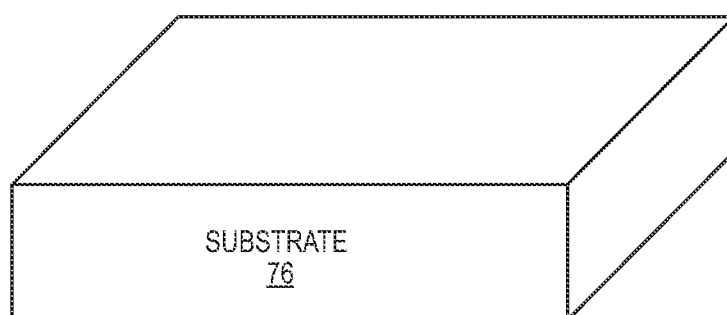


FIG. 9A

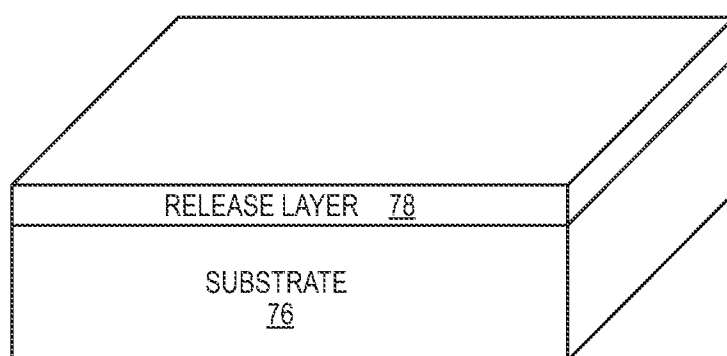


FIG. 9B

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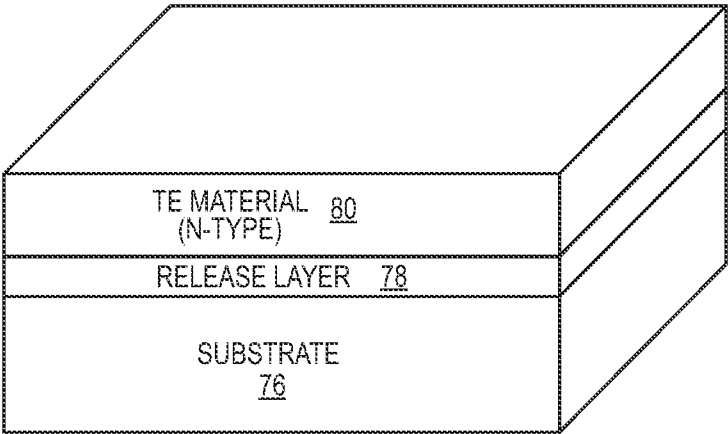


FIG. 9C

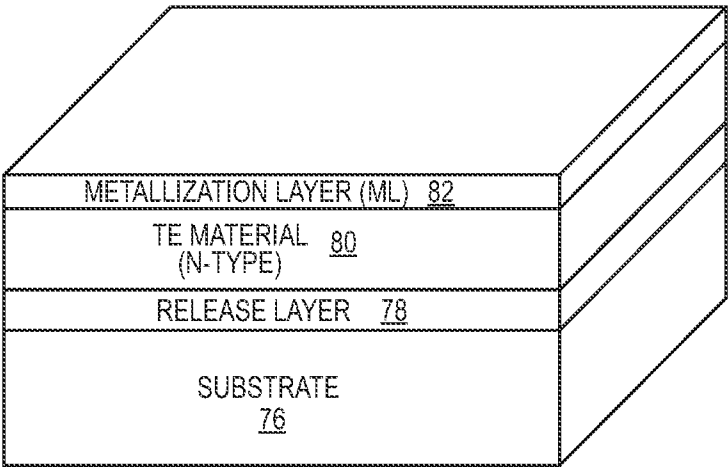


FIG. 9D

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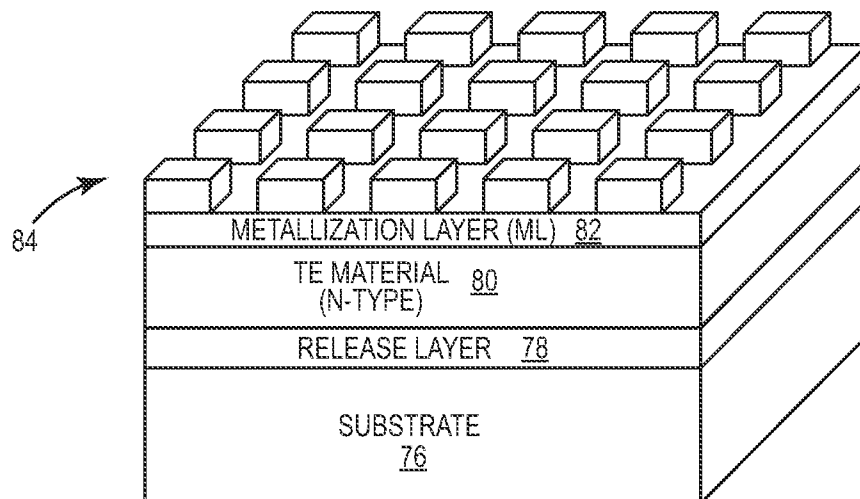


FIG. 9E

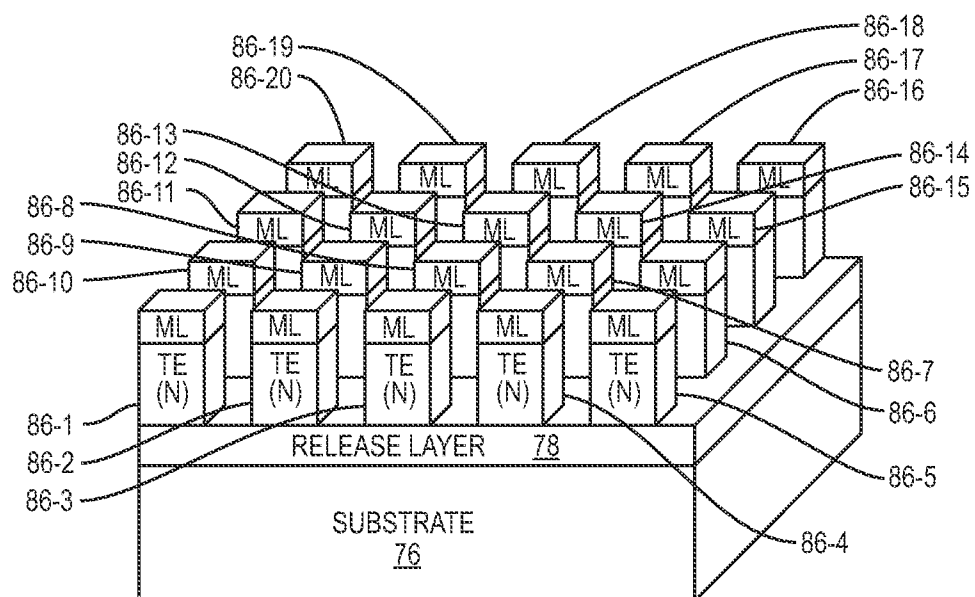


FIG. 9F

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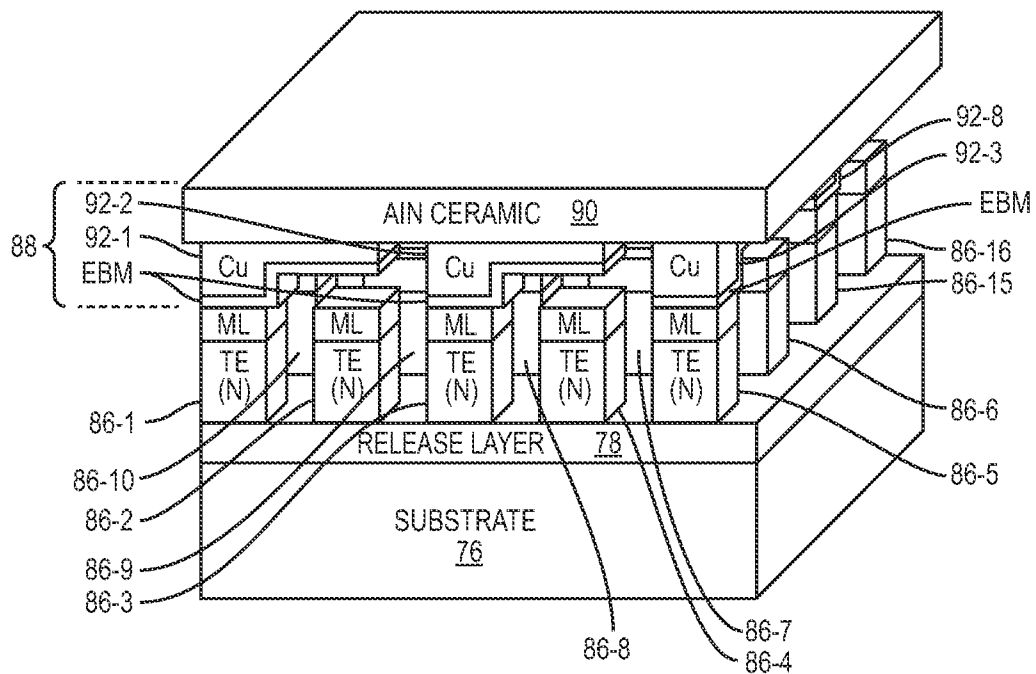


FIG. 9G

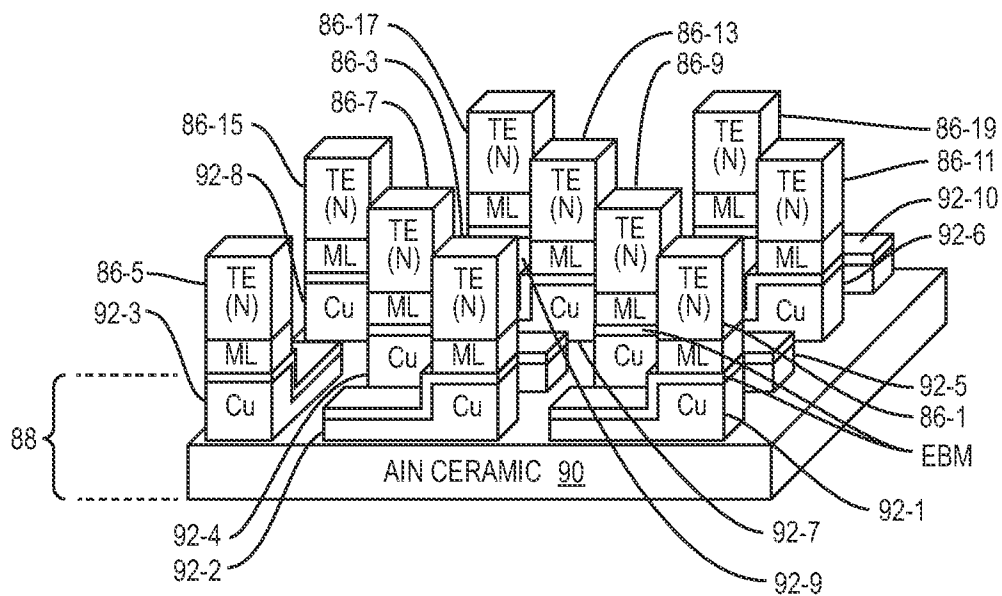


FIG. 9H

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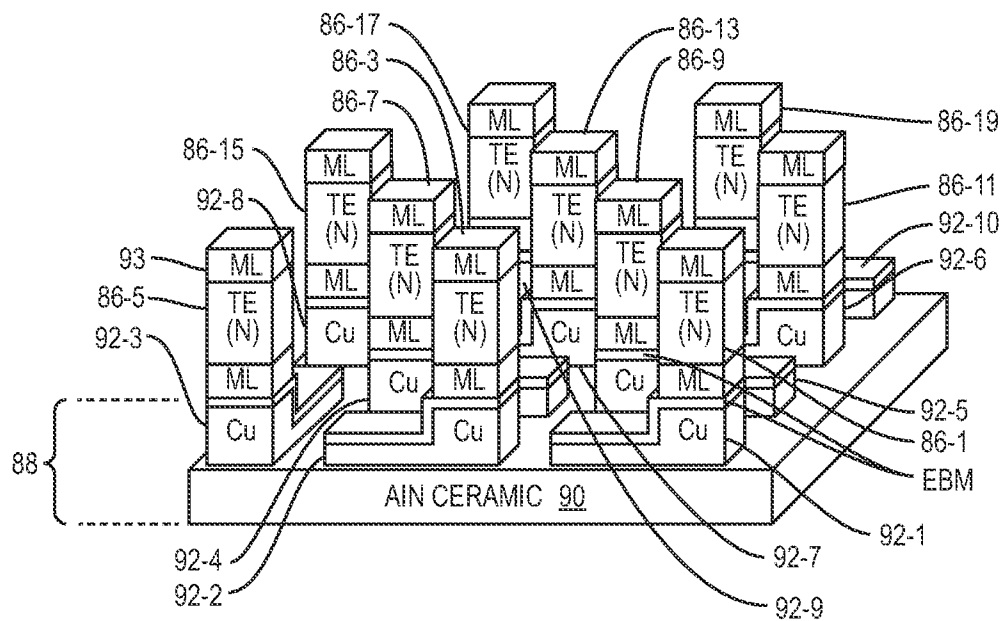


FIG. 9I

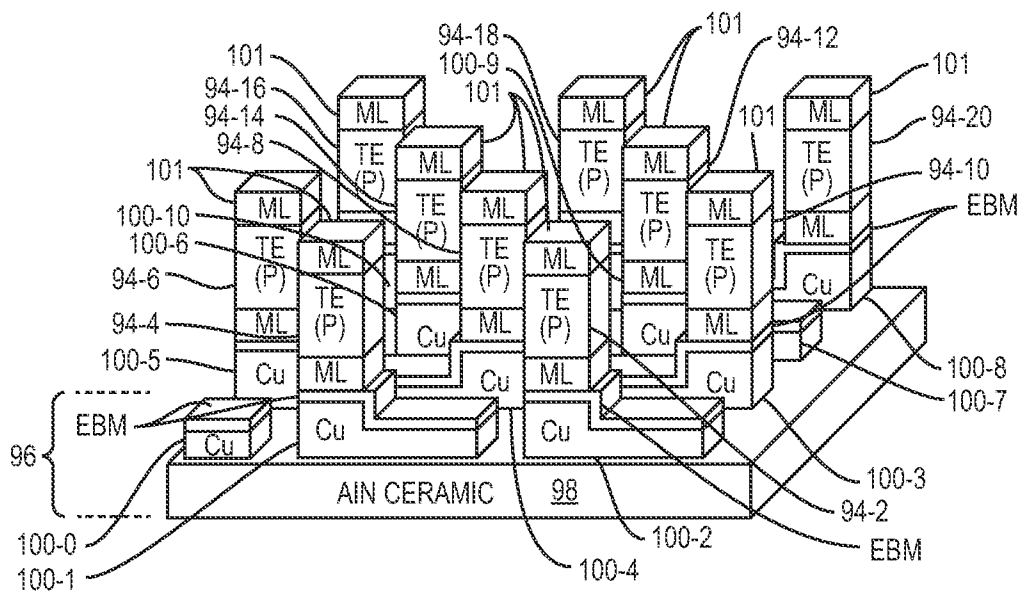


FIG. 9J

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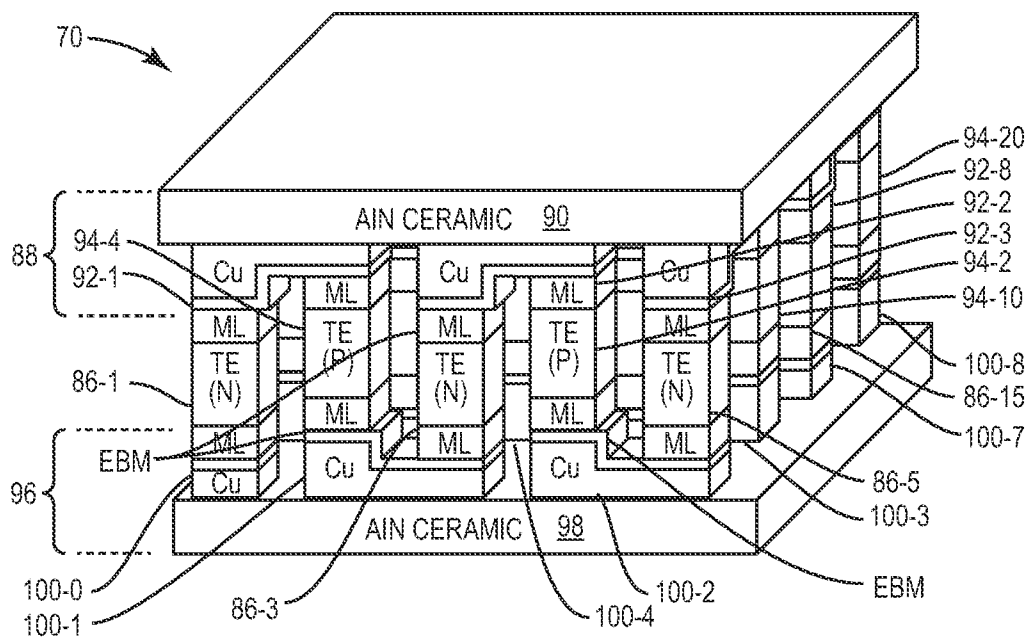


FIG. 9K

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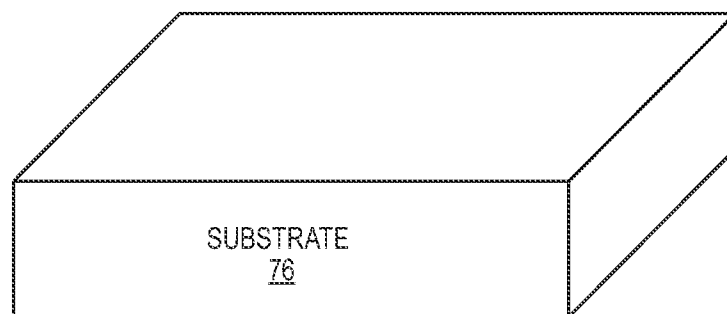


FIG. 10A

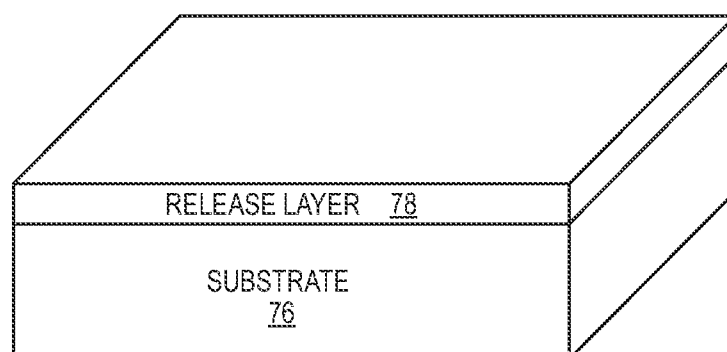


FIG. 10B

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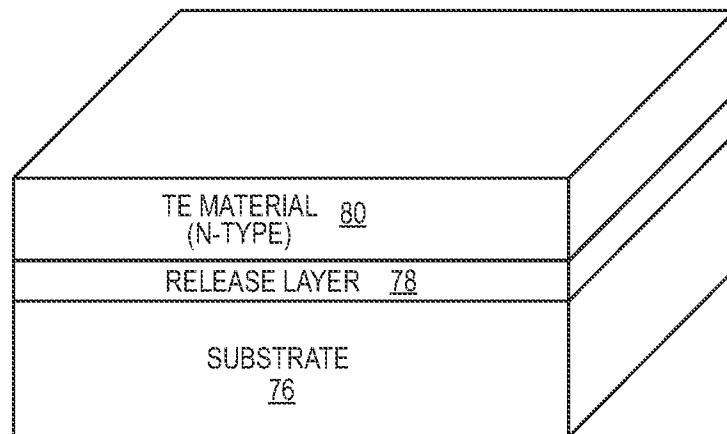


FIG. 10C

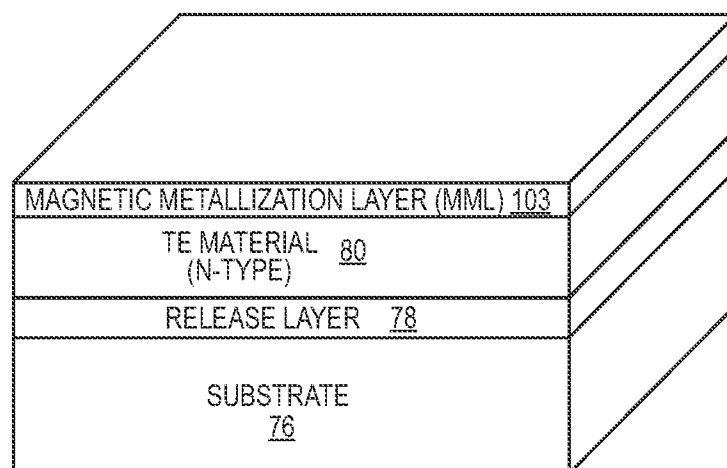


FIG. 10D

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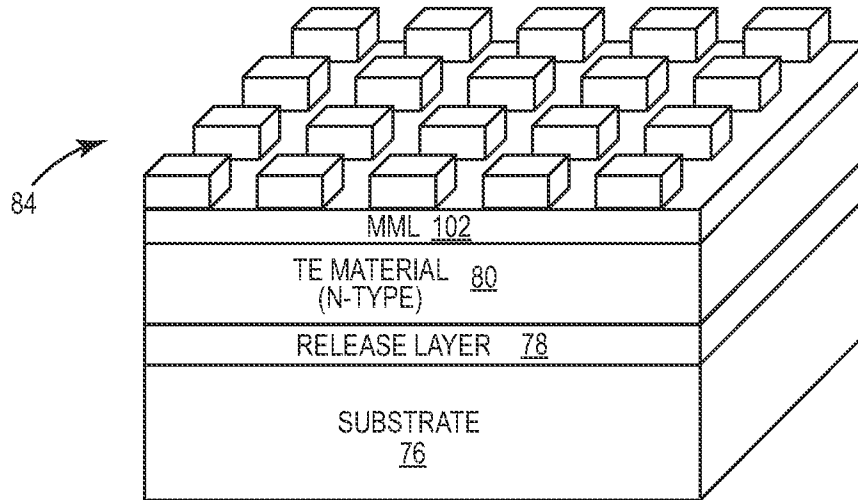


FIG. 10E

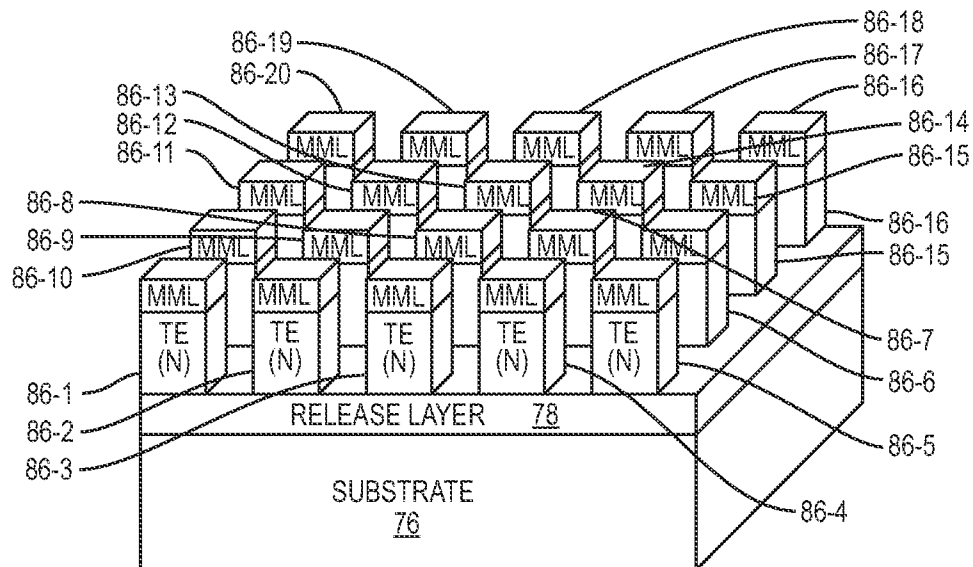


FIG. 10F

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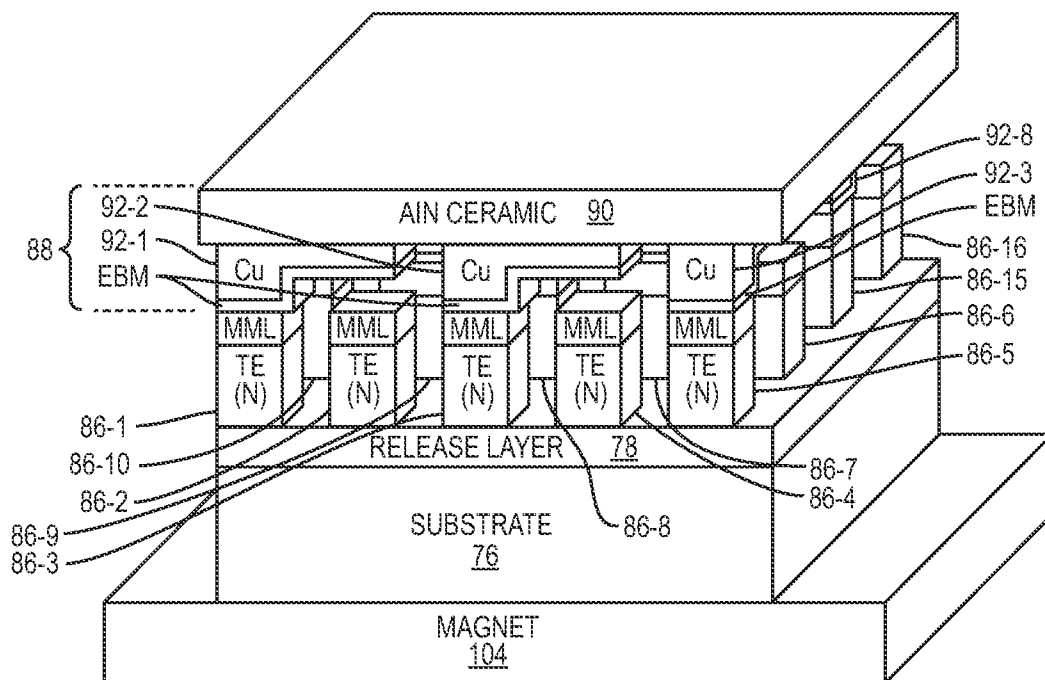


FIG. 10G

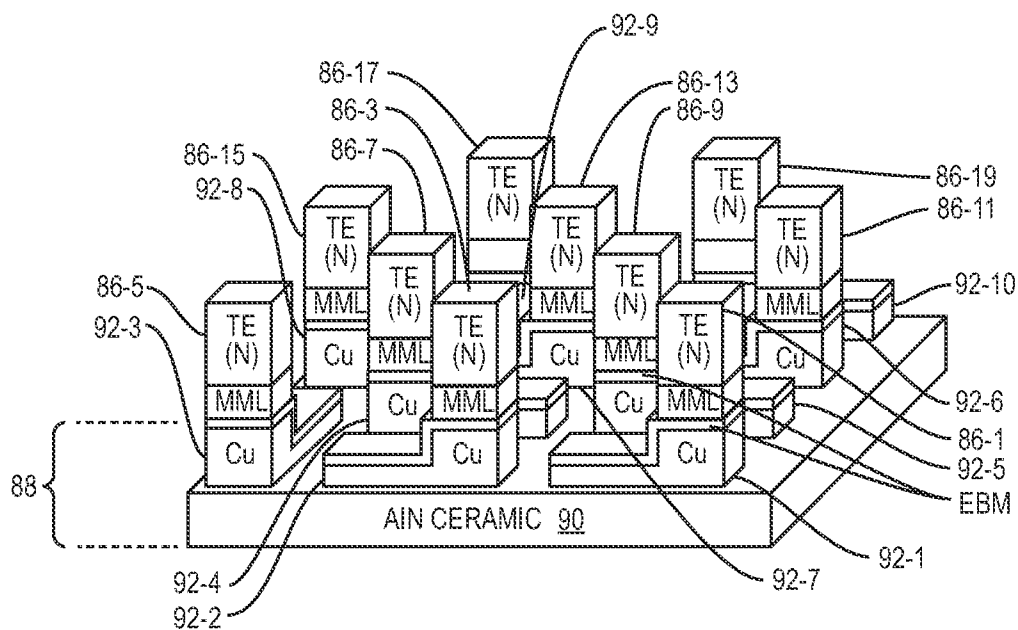


FIG. 10H

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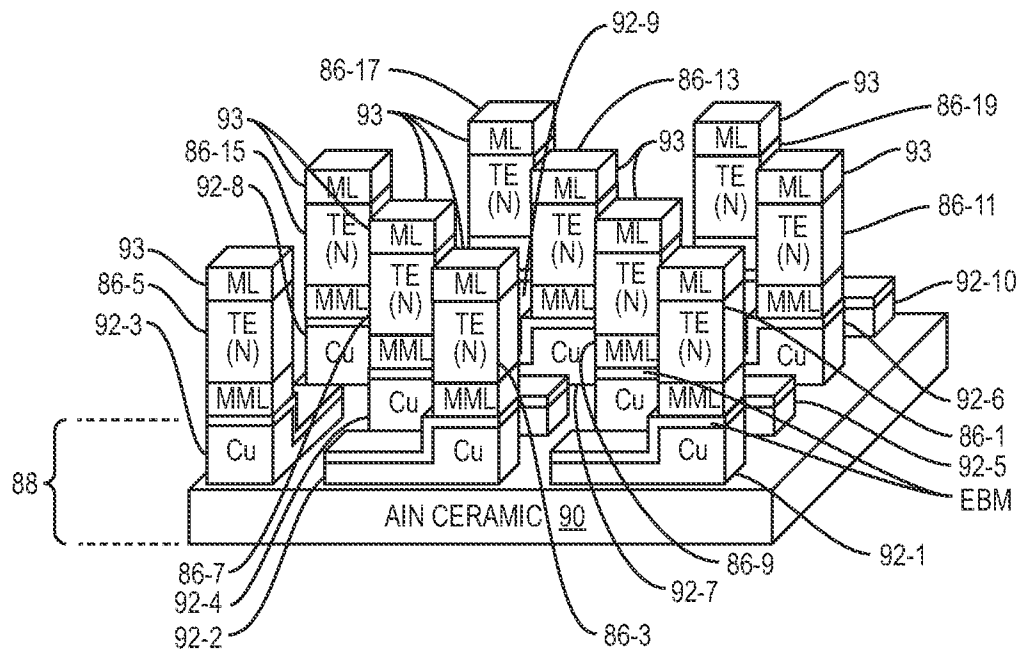


FIG. 10I

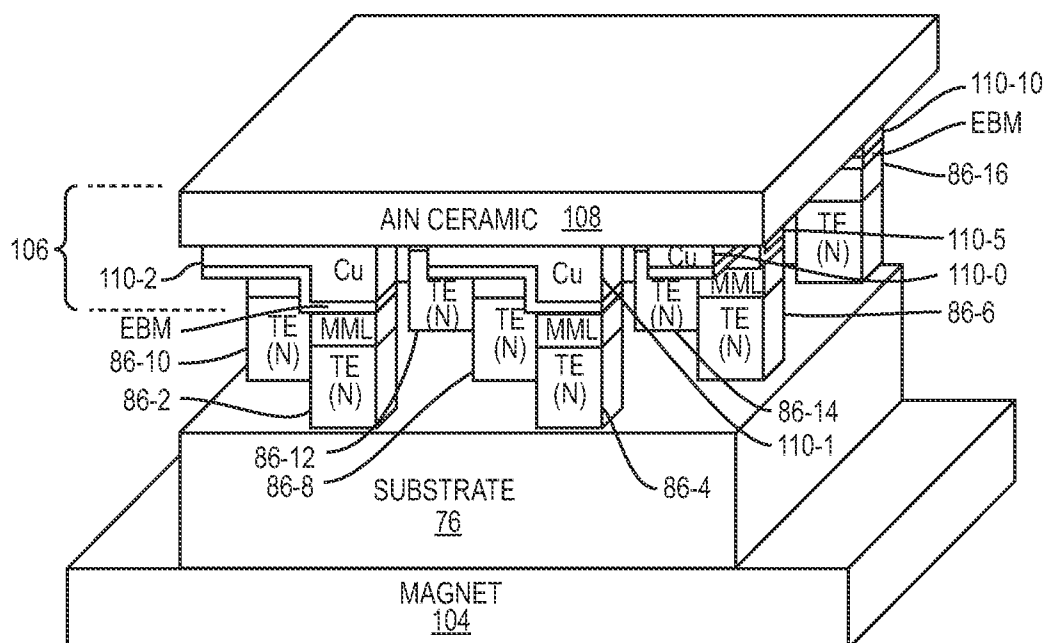


FIG. 10J

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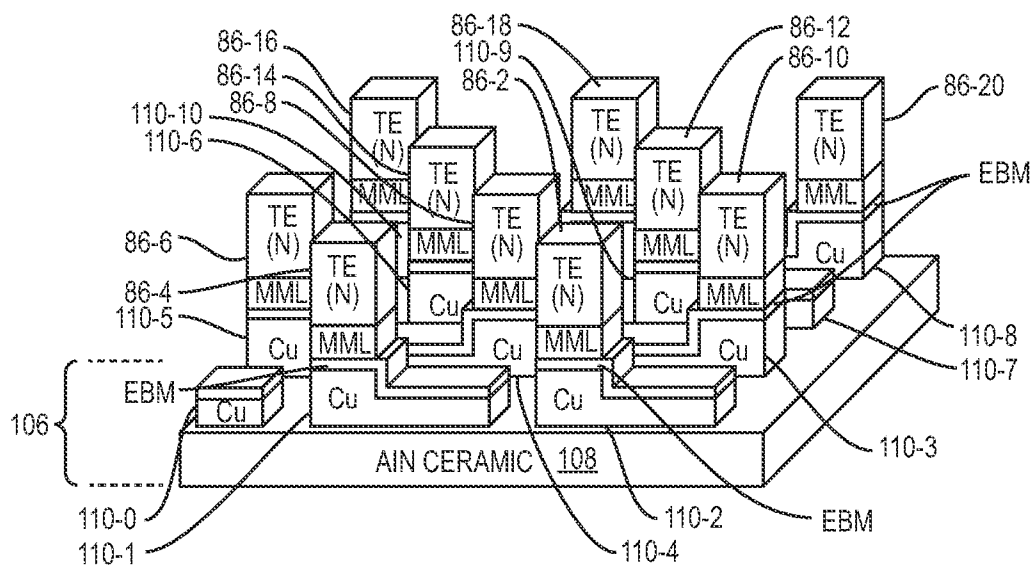


FIG. 10K

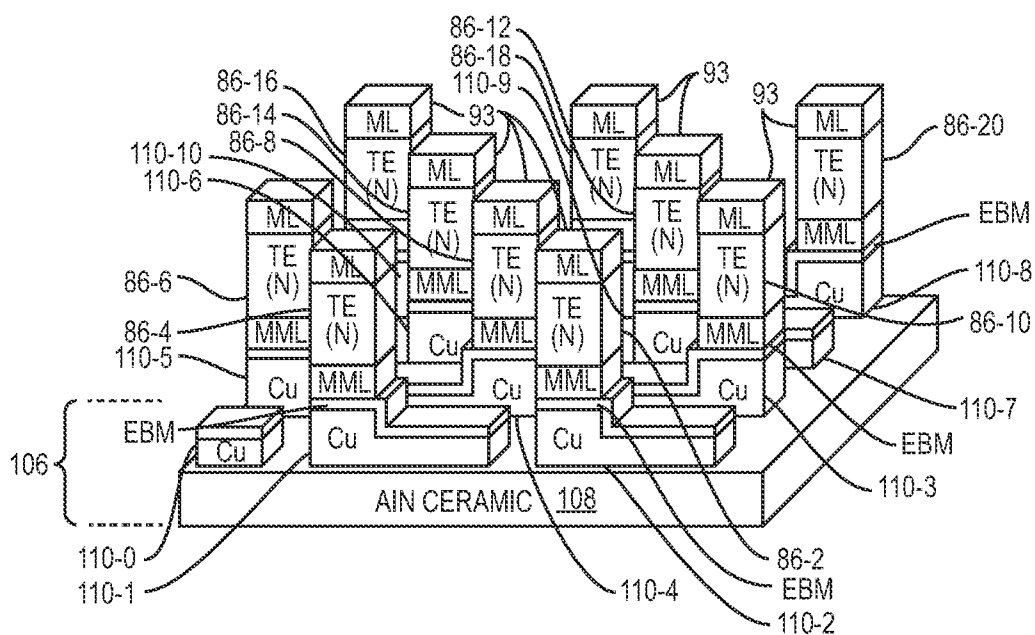
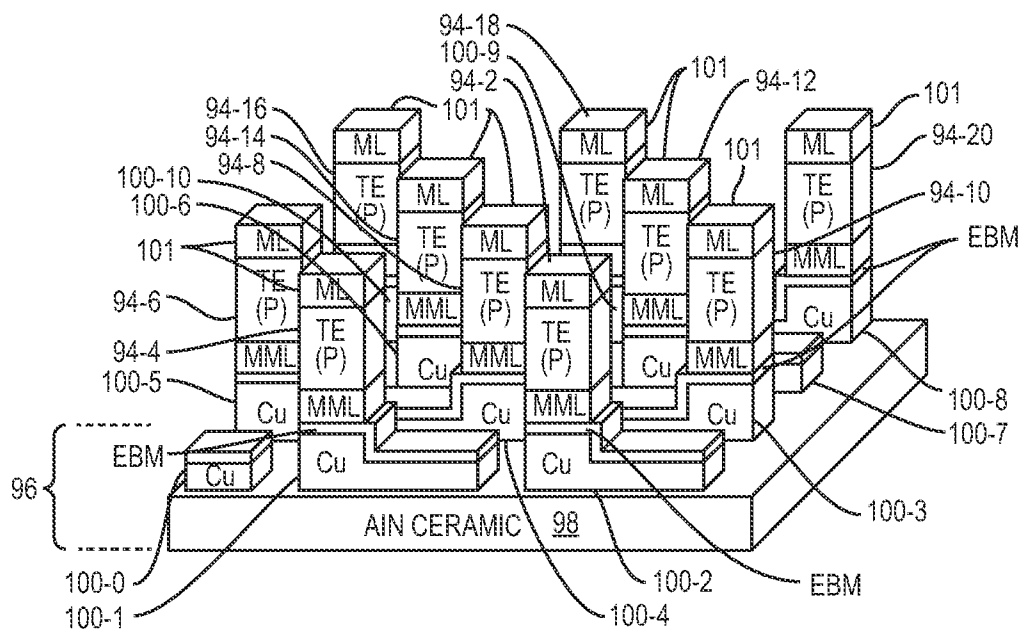
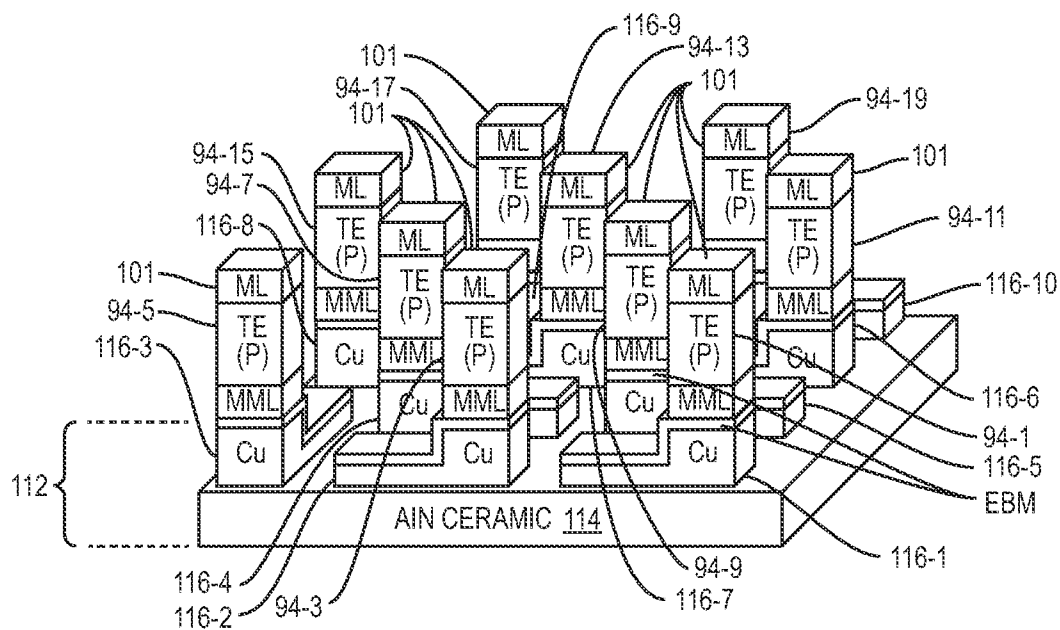


FIG. 10L

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**FIG. 10M****FIG. 10N**

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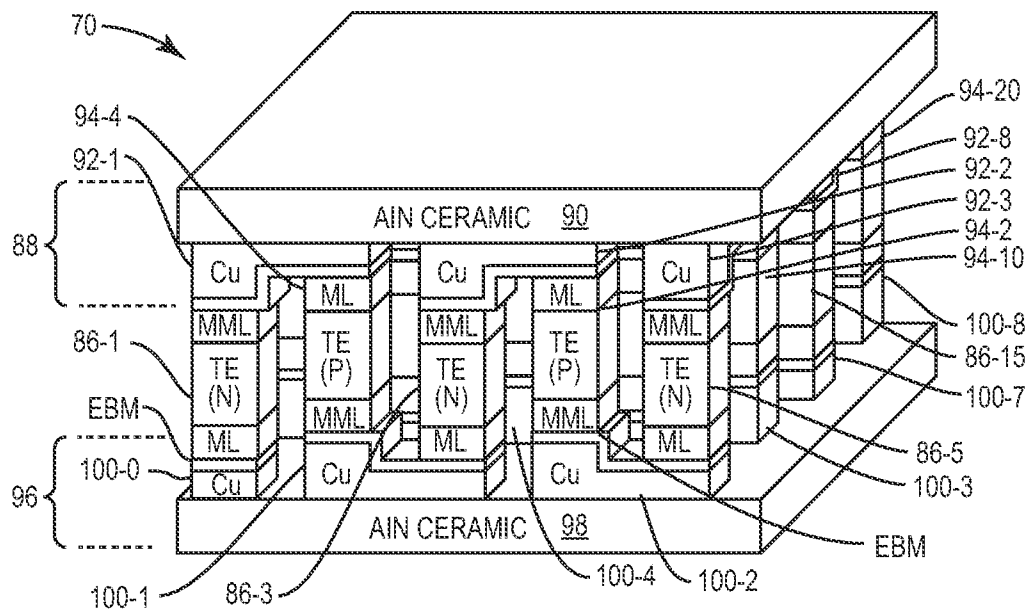


FIG. 100

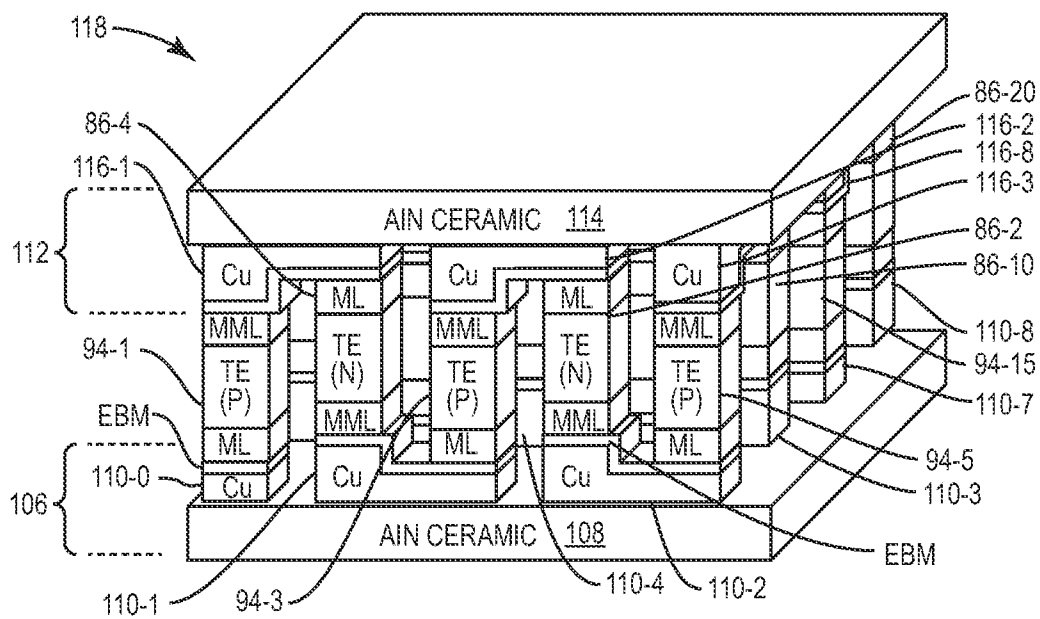


FIG. 10P

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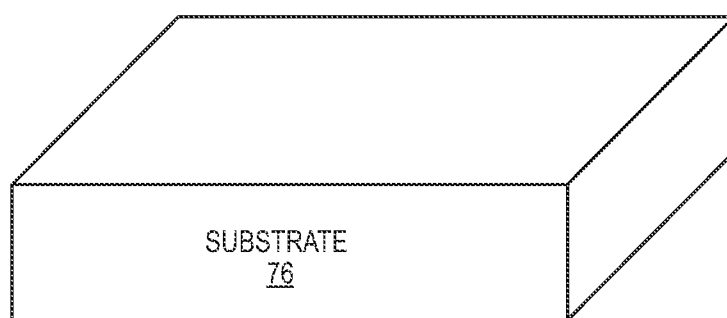


FIG. 11A

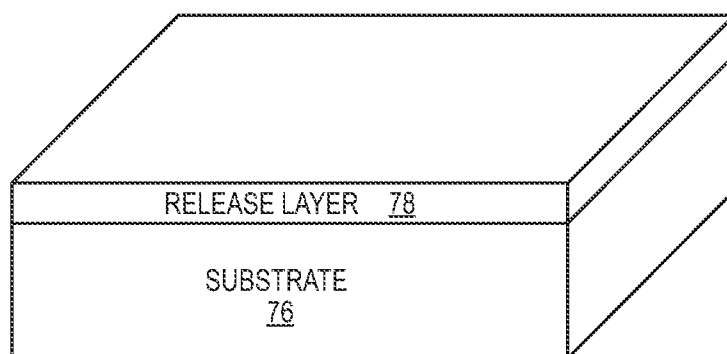


FIG. 11B

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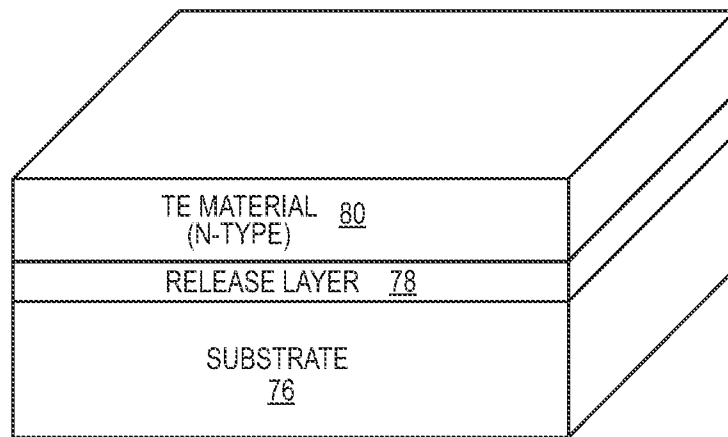


FIG. 11C

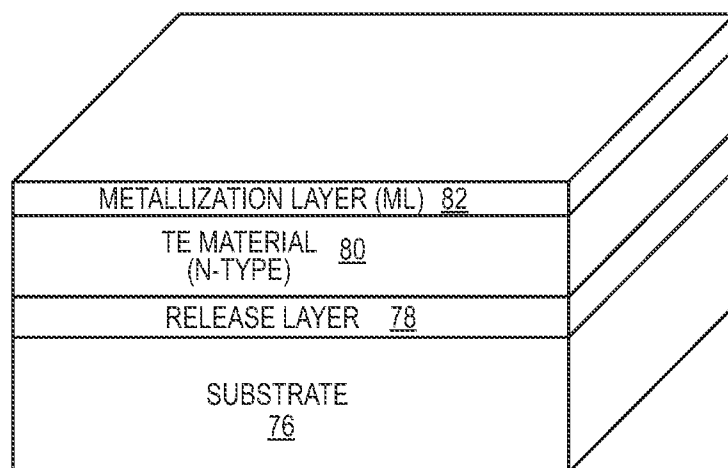


FIG. 11D

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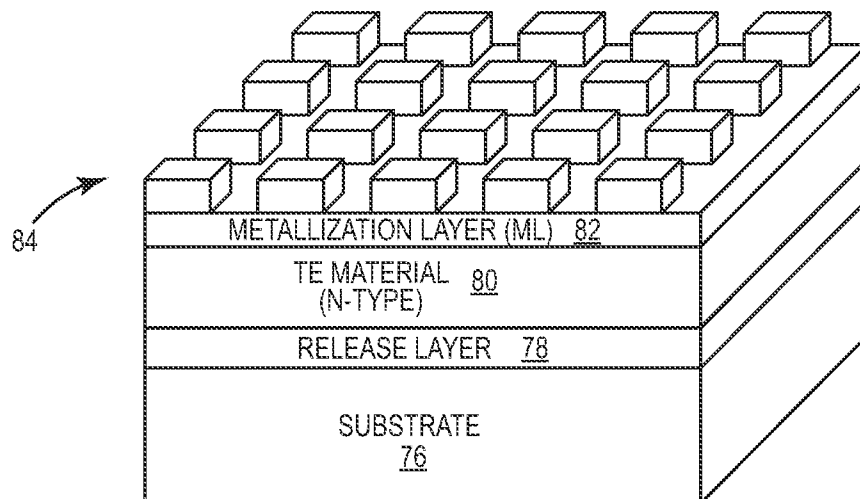


FIG. 11E

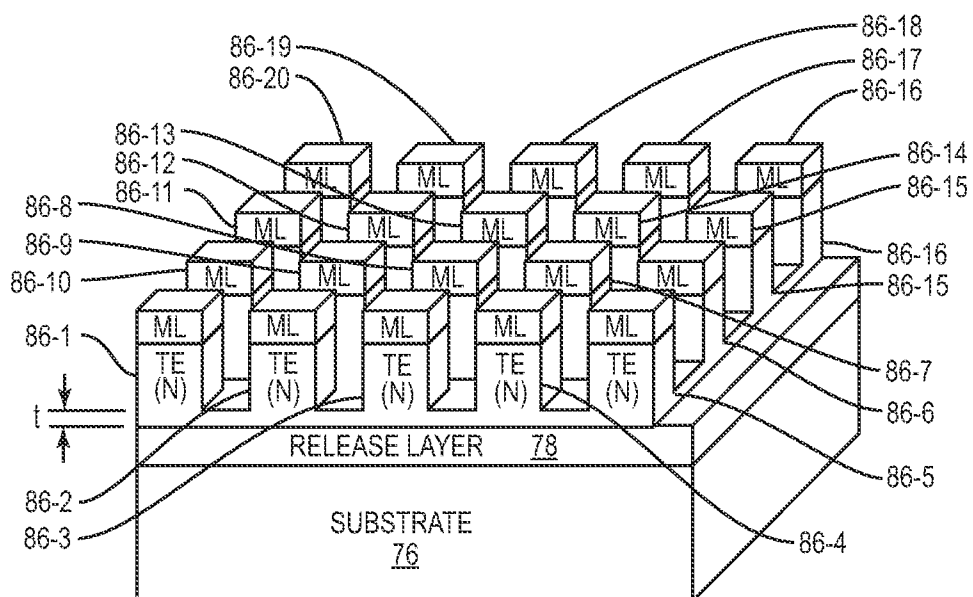


FIG. 11F

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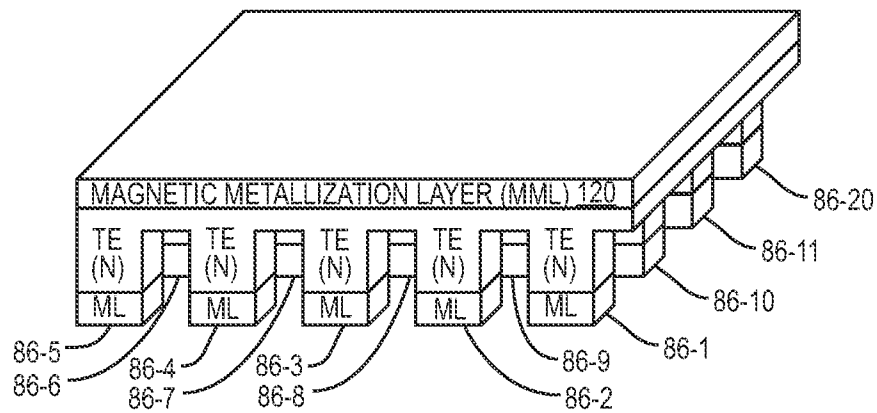


FIG. 11G

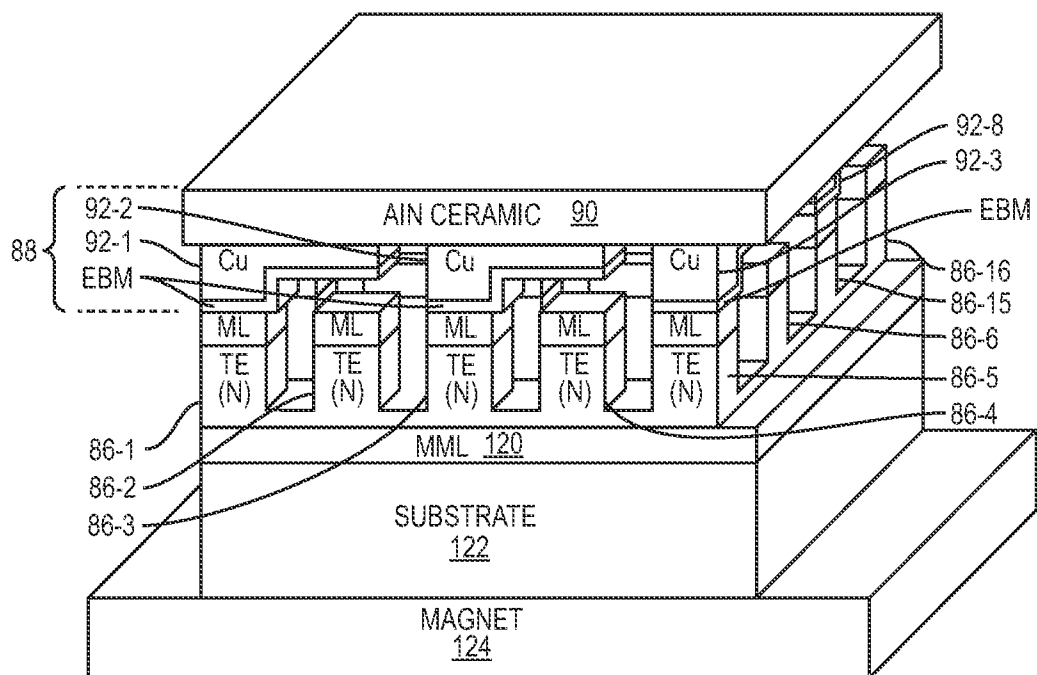


FIG. 11H

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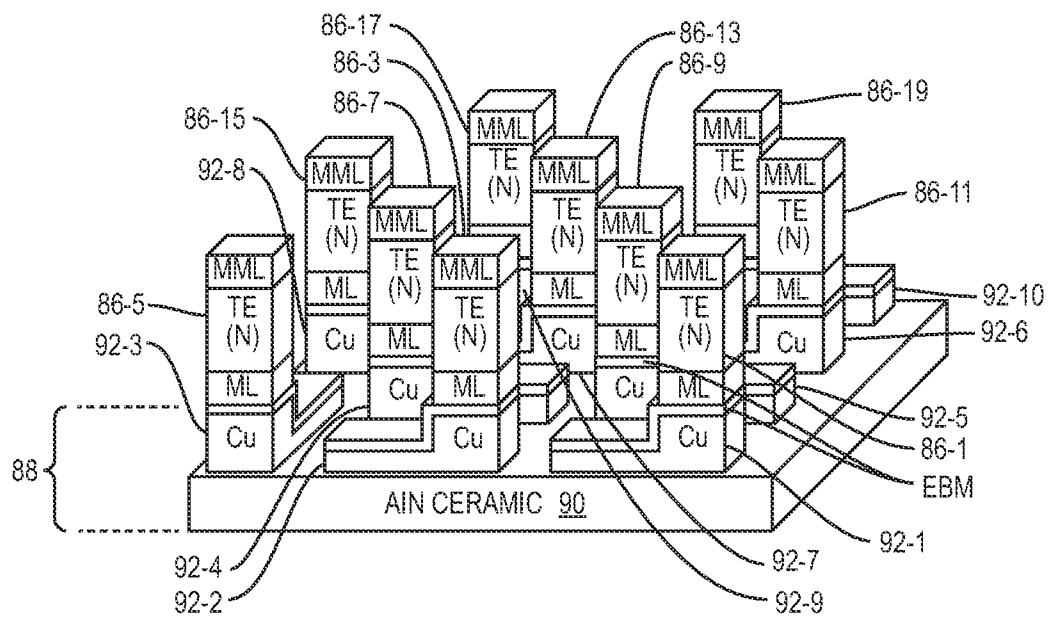


FIG. 11I

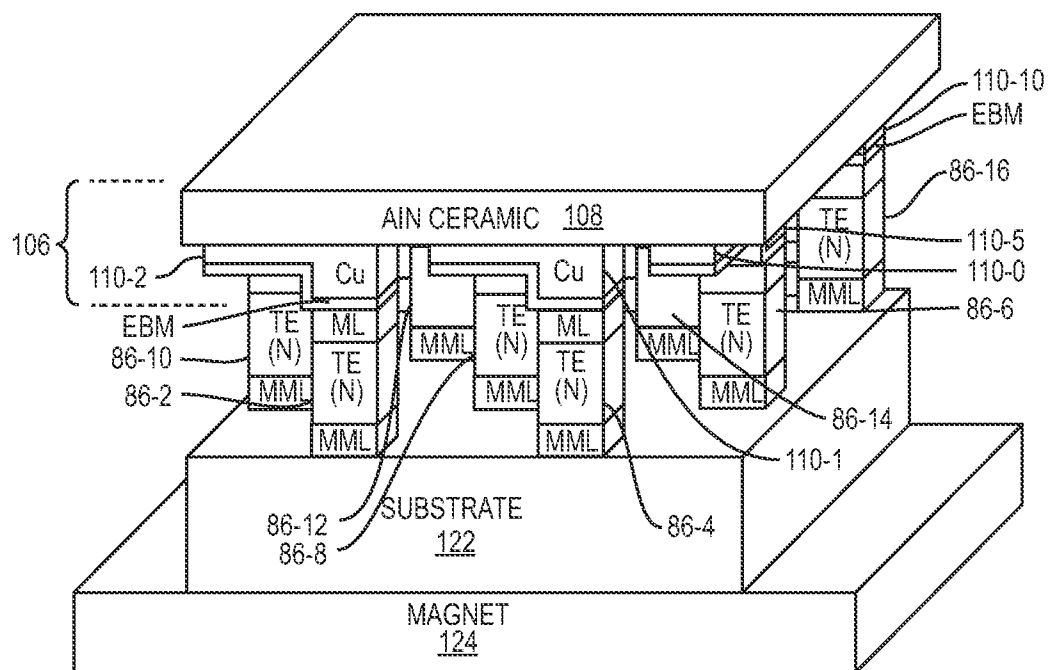


FIG. 11J

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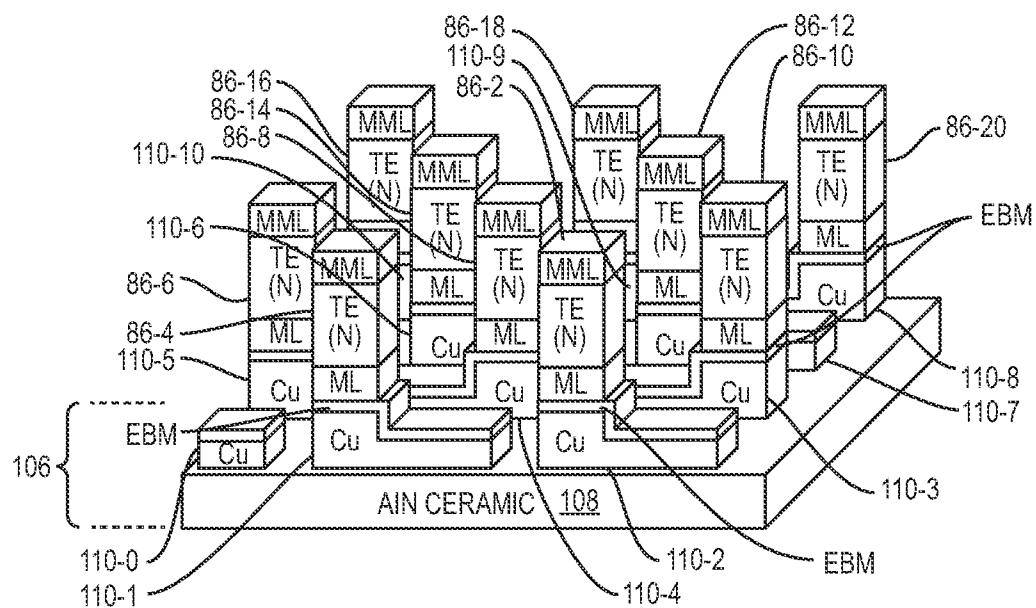


FIG. 11K

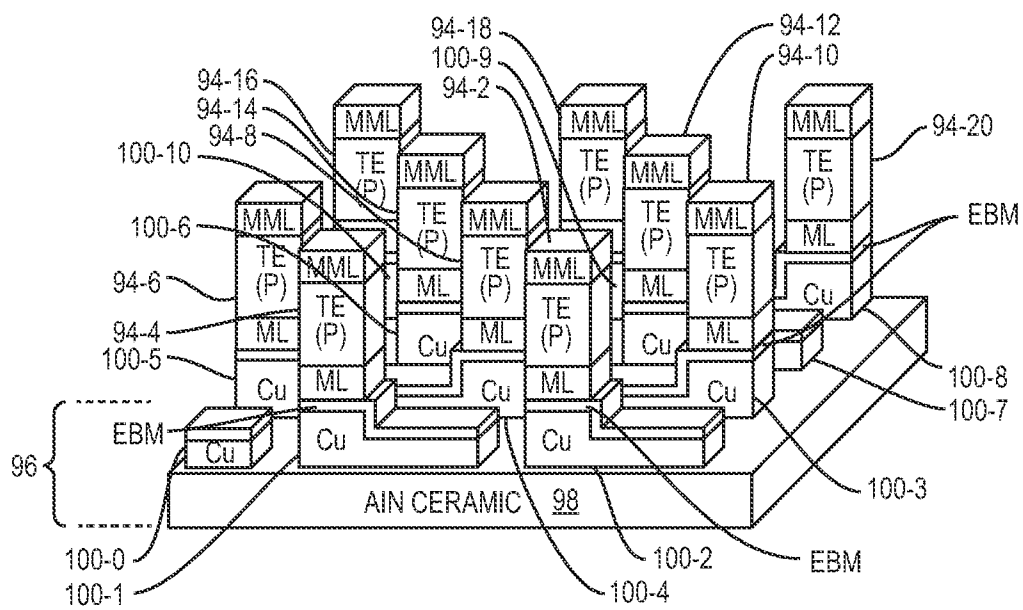


FIG. 11L

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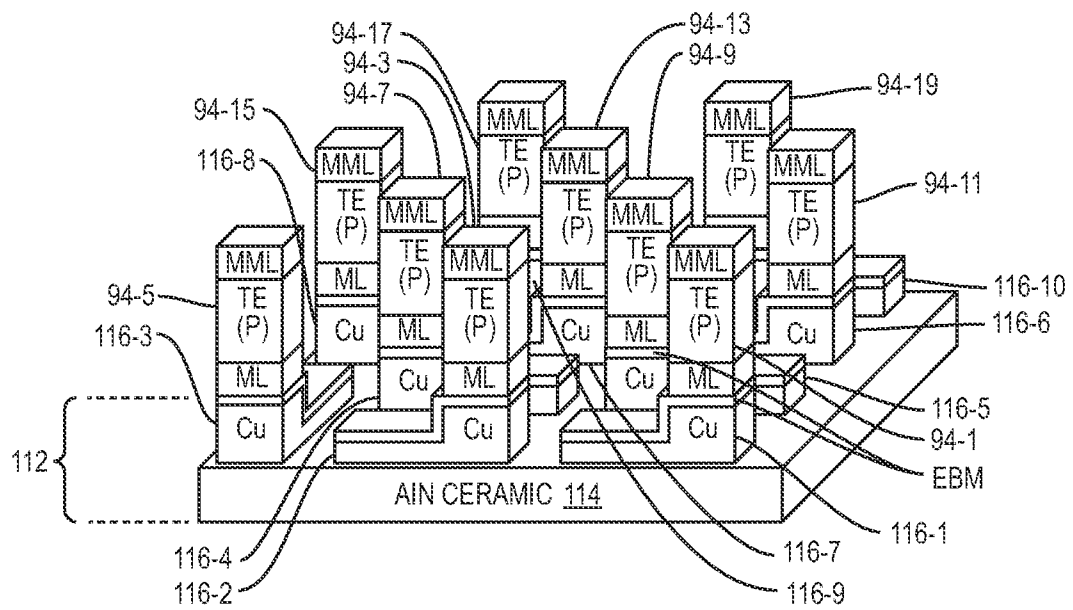


FIG. 11M

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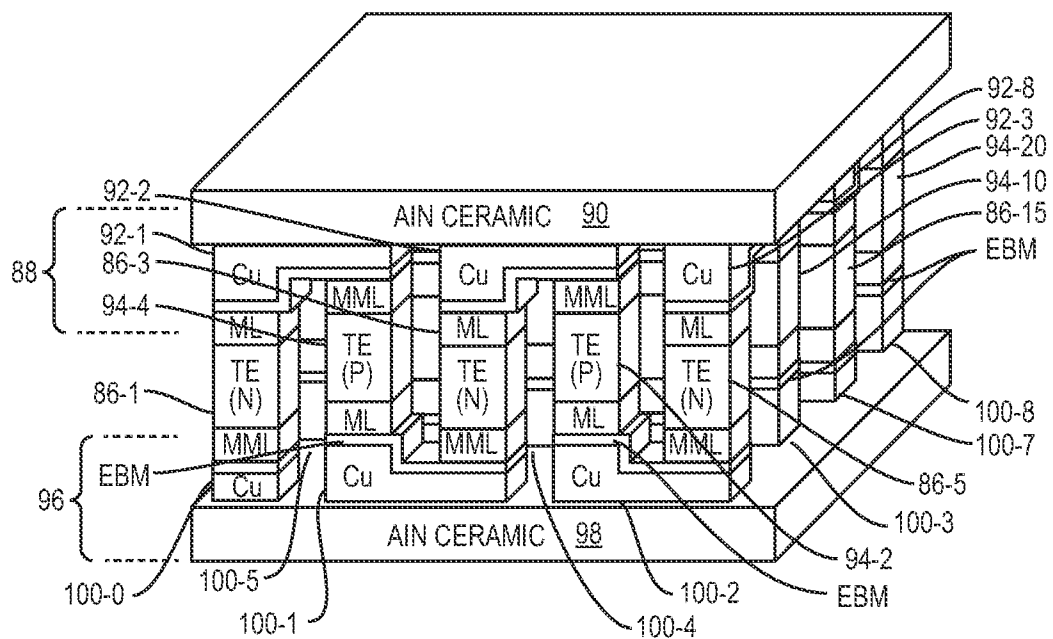


FIG. 11N

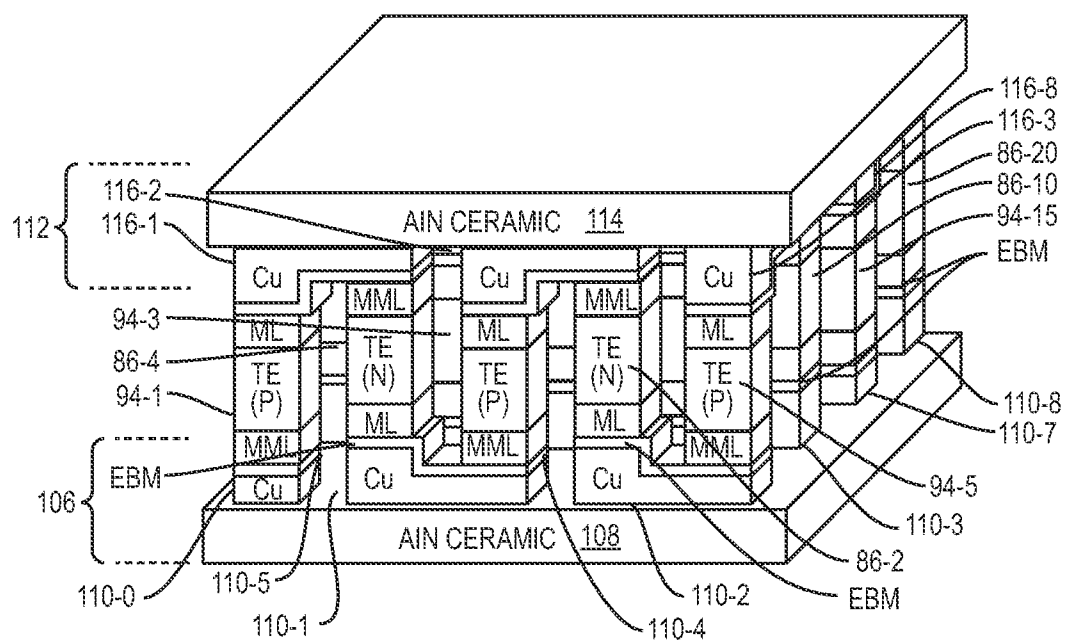


FIG. 11O