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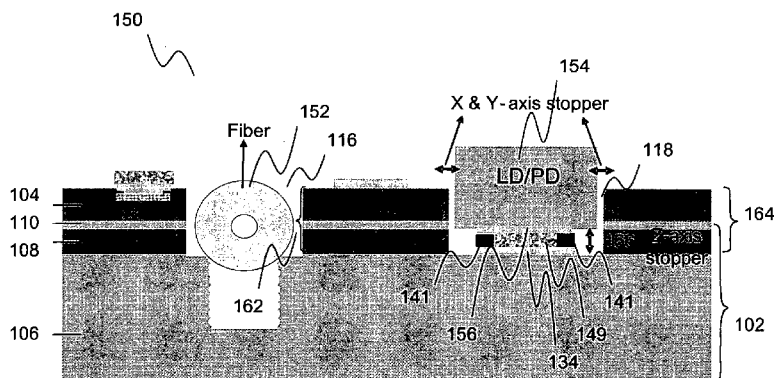


Figure 1J

(57) Abstract: According to one embodiment of the present invention, an integrated assembly is provided. The integrated assembly includes a substrate with an integrated circuit, an interconnect structure disposed above the substrate, wherein the interconnect structure comprises a metallization plane; a first dielectric cavity is formed through the interconnect structure and at least a part of the substrate to accommodate a first optical component; wherein the integrated circuit and the first optical component are provided on the same side of the substrate. A method of manufacturing an integrated assembly is also provided.

AN INTEGRATED ASSEMBLY AND A METHOD OF MANUFACTURING THE
SAME

Field

[0001] The present invention relates generally to an integrated assembly and a method of manufacturing the same.

Background

[0002] Silicon Opto-Electronic Integrated Circuits (SOEICs) have emerged as the enabling technology for a new generation of optical networking modules. SOEICs utilize mature materials processing and extensive electronic functionality of silicon.

[0003] Just like fiber optic networks have enabled the rapid expansion of the Internet by enabling users to exchange huge amounts of data from anywhere in the world, a related technology known as “silicon nanophotonics” is bringing similar capabilities to the level of the computer chip. Using silicon optical waveguides, or nanometer-sized “light pipes,” integrated on the same piece of silicon material as the chip multi-processor, the huge amount of data which needs to be passed back and forth between all the cores can be carried by pulses on a beam of laser light, using much less total power than is used by electrical signals. Therefore, much of the electrical wiring within the multi-processor can potentially be replaced with a network of silicon waveguides, which will act as the “nervous system” of future on-chip supercomputers.

[0004] One of the key components needed for any such optical network is a silicon optical modulator, which has the job of transferring high-speed electrical signals traveling

on wires into pulses of laser light, traveling along a silicon waveguide. However, one of the biggest obstacles to the implementation of optical interconnects is the cost.

[0005] Having said that, a couple of factors may hamper the breakthrough of photonic ICs. Firstly, the current technology lacks a large-scale market to push development, this is a situation that is beginning to change with the introduction of all-optical networks. Secondly, integrating a variety of photonic devices on a single substrate material presents technical complications. Thirdly, passive integrated optical devices and optical interconnects are significantly larger than their electronic counterparts.

[0006] A couple of processing techniques have been proposed to overcome these problems. One technique is the universal substrate approach in which only a single compromise structure is grown. The design of this structure is such that perhaps all of the individual device structures depart from optimum to an extent, but their integration offers an overall functional advantage. Another technique uses multiple growth steps and etch processes to yield separately optimized device structures. However, the technique complicates waveguide alignment and coupling. A further technique relies on selective area growth, which gives a certain degree of freedom to selectively determine the local band gap of different devices within a single plane simultaneously.

[0007] However, there is still a need for an integrated assembly which can solve the above-mentioned problems.

Summary of the Invention

[0008] According to one embodiment of the present invention, an integrated assembly is provided. The integrated assembly includes a substrate with an integrated

circuit; an interconnect structure disposed above the substrate, wherein the interconnect structure comprises a metallization plane; a first dielectric cavity formed through the interconnect structure and at least a part of the substrate to accommodate a first optical component; wherein the integrated circuit and the first optical component are provided on the same side of the substrate.

[0009] According to one embodiment of the present invention, a method of manufacturing an integrated assembly is provided. The method includes forming an integrated circuit on a substrate; forming an interconnect structure on or above the substrate; forming a first dielectric cavity through the interconnect structure and at least a part of the substrate to accommodate a first optical component; and providing the integrated circuit and the first optical component on the same side of the substrate; wherein the interconnect structure comprises a metallization plane.

Brief Description of the Drawings

[0010] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

FIGS. 1A to 1J shows a method of manufacturing an integrated assembly according to one embodiment of the present invention;

FIGS. 2A to 2J shows a method of manufacturing an integrated assembly according to one embodiment of the present invention;

FIGS. 3A to 3K shows a method of manufacturing an integrated assembly according to one embodiment of the present invention;

FIG. 4 shows a flowchart of a method of manufacturing an integrated assembly corresponding to FIGS. 1A to 1J and FIGS. 2A to 2J according to one embodiment of the present invention;

FIG. 5 shows a flowchart of a method of manufacturing an integrated assembly corresponding to FIGS. 3A to 3K according to one embodiment of the present invention; and

FIG. 6 shows a top-view of an integrated assembly according to one embodiment of the present invention.

Description

[0011] FIGS. 1A to 1J shows a method of manufacturing an integrated assembly according to one embodiment of the present invention. FIG. 1A shows an integrated assembly 150 including a substrate 102 and an interconnect structure 104 disposed above the substrate 102. The substrate 102 includes a silicon-on-insulator (SOI) structure. In particular, the substrate 102 includes a support substrate 106, a first insulating layer 108 disposed above the support substrate 106 and a semiconductor layer 110 disposed above the first insulating layer 108. The interconnect structure 104 includes a metallization plane (not shown) and a second insulating layer (not shown). The integrated assembly 150 further includes a metallic pad 112 provided on the interconnect structure 104.

[0012] In one embodiment, the integrated assembly 150 may include an integrated circuit provided on the semiconductor layer 110. Optical passive structures may also be

formed in the semiconductor layer 110. The optical passive structures may include nano-tapered structures. Alignment keys may also be included in the integrated assembly 150 for alignment between the substrate 102 fabricated in a front end process and the interconnect structure 104 fabricated in a back end process.

[0013] In one embodiment, the interconnect structure 104 includes a stack layer of a plurality of metallization planes and second insulating layers, which may be termed as a multi-level metallization or dielectric stack.

[0014] In one embodiment, the support substrate 106 includes a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride. The first insulating layer 108 and the second insulating layer respectively include a material selected from the group consisting of silicon oxide, a polymer or any other dielectric material. The semiconductor layer 110 includes a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium. The metallization plane includes conductor tracks for example made of Tungsten, Copper or Aluminium. The metallic pad 112 includes Aluminium or any other combinations of metals like Under-Bump Metallization (UBM)

[0015] In one embodiment, the thickness of the support substrate 106 is in the range of between about few hundred microns to full thickness of the substrate, depending on the wafer diameter. The thickness of the first insulating layer 108 can vary from sub-micron dimensions to several microns. The thickness of the semiconductor layer 110 is in the range of between tens of nanometers to about few microns. The thickness of the interconnect structure 104 is in the range of between few microns to tens of microns.

[0016] In FIG. 1B, two dielectric cavities 116 and 118 are formed in the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 to expose two portions of the support substrate 106 by a suitable lithography process. First, a layer of photoresist 114 is deposited on the interconnect structure 104. The photoresist layer 114 is then patterned to form two openings or contact windows to expose two portions of the support substrate 106 by suitable lithography and etching techniques. Portions of the interconnect structure 104, semiconductor layer 110 and the first insulating layer 108 not covered by the photoresist 114 are being etched to form two dielectric cavities 116, 118 to expose two portions of the support substrate 106. The exposed portions of the support substrate 106 inside the dielectric cavities 116 and 118 provide a reference plane on which optical components can be assembled. A reference plane is important for aligning all external components with device structures in the support substrate 106 during the optical component assembly process. The support substrate 106 may therefore be termed as an optical sub-assembly platform. Accordingly, the two portions of the support substrate 106 exposed by the respective dielectric cavities 116 and 118 may be used for assembling optical components like for example a laser diode and a detector. After forming the two cavities 116, 118, the photoresist layer 114 is removed or stripped away by a plasma resist strip and a wet clean process. This process in FIG. 1B may be termed as contact window or reference window lithography.

[0017] In this regard, any other suitable techniques or processes may also be used in order to provide greater flexibility with respect to forming the dielectric cavities 116, 118. In one embodiment, suitable lithography processes include deep ultra-violet lithography, i-line lithography. Suitable etching processes include wet etching and dry

etching like Plasma Etching (PE), Reactive Ion Etch (RIE) and Deep Reactive Ion Etching (DRIE).

[0018] In FIG. 1C, a trench 120 is formed at the bottom of a first dielectric cavity 116 by a suitable lithography process. Another layer of photoresist (not shown) is deposited on the interconnect structure 104 and on a portion of the support substrate 106. The photoresist layer is then patterned to form an opening thereby exposing a portion of the support substrate 106 at the bottom of the first dielectric cavity 116 by suitable lithography techniques. The portion of the support substrate 106 not covered by the photoresist is being etched to form the trench 120 in the support substrate 106. The trench 120 may be used for subsequent placement of optical components for example laser diode, optical detector, fiber and lens. After forming the trench 120, the photoresist layer is removed or stripped away by a plasma resist strip and a wet clean process. This process in FIG. 1C may be termed the fiber cavity or guide slot lithography.

[0019] In this regard, any other suitable techniques or processes may also be used in order to provide greater flexibility with respect to forming the trench 120 in the support substrate 106. In one embodiment, suitable lithography processes include deep ultra-violet lithography, i-line lithography or broadband UV lithography by using conventionally coated positive or negative photoresist, laminated dry resist film, Spray coated resist or electroplated photoresist. Suitable etching processes includes wet chemical etching and dry etching processes for example a deep reactive-ion etching (DRIE), Plasma Etching (PE) and Reactive Ion Etch (RIE) process. Each of the DRIE, PE and RIE processes is an anisotropic etch process used to create deep, steep-sided holes and trenches in substrates.

[0020] In an embodiment, a thin layer of dielectric (not shown) such as silicon nitride, silicon oxy-nitride, silicon oxide, silicon carbide in the range of about 50A to about 1000A is deposited globally by plasma enhance chemical vapor deposition (PECVD) after forming of the trench 120 to improve the adhesion of a subsequently deposited under bump metallization (UBM) layer or UBM film stack with the underlying support substrate 106. The dielectric layer can be deposited as a single layer or a combination of two or more layers. The dielectric layer thus serves as an adhesion promoter between the support substrate and the deposited UBM metal or UBM film stack. The UBM layer or UBM film stack is composed of an adhesion layer like Titanium or Chromium, a solder diffusion barrier like Nickel or Platinum and finally a solder wetting layer like Gold or Copper.

[0021] In FIG. 1D, a dry resist film 122 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for UBM is transferred onto the dry resist film 122 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 122 is performed by a selective exposure to a radiation source, such as ultraviolet (UV) light. Then selective portions of the dry resist film 122 may be dissolved by a suitable developer solution, giving rise to three patterns 124, 126, 128 in the dry resist film 122. The three patterns 124, 126, 128 formed in the dry resist film 122 include a first pattern 124 which exposes a portion on the metallic pad 112, a second pattern 126 which exposes a portion of the interconnect structure 104 and a third pattern 128 which exposes a portion of the support substrate 106. It may be noted that, depending on whether a positive or negative photoresist is used, the UV exposed portion or unexposed

portion is dissolved in a developer solution to form the final lithographic pattern. In case of positive photoresist, the exposed areas are developed selectively. In case of negative photoresist, the unexposed areas are selectively developed.

[0022] Next, a UBM layer or UBM film stack 129 is deposited over the dry resist film 122 and into the respective exposed patterns 124, 126, 128 formed in the dry resist film 122 using a suitable deposition process like for example e-beam evaporation or sputtering process. The UBM layer portion 130 deposited on the metallic pad 112 may serve for a subsequent die attachment and wire-bonding, the UBM layer portion 132 deposited on the portion of the interconnect structure 104 may serve for a subsequent placement of a seal ring and the UBM layer portion 134 deposited on the portion of the support substrate 106 may serve for a subsequent placement of a laser diode. In one embodiment, the UBM film stack 129 is composed of a combination of 0.025 to 0.3 μm Titanium (Ti) , 0.025 to 0.3 μm Platinum (Pt) ,0.5 to 2 μm Gold (Au) multi-layer metal stack. The UBM film stack 129 can also be composed of other multi-layered metal stacks like for example 0.025 to 0.3 μm Chromium (Cr)/0.5-2 μm Gold (Au) and 0.025 to 0.3 μm Titanium (Ti)/0.025-0.3 μm Nickel (Ni)/0.5-2 μm Gold (Au). The UBM layer or UBM film stack 129 is annealed at a temperature preferably in the range of about 200 to about 350 $^{\circ}\text{C}$ to improve the respective adhesion between the UBM layer portion 130 and the Aluminum pad 112, the UBM layer portion 132 and the interconnect structure 104 and the UBM layer portion 134 and the underlying support substrate 106. The annealing helps in improving the adhesion between UBM layer and any surface it is making contact with.

[0023] In FIG. 1E, the dry resist film 122 and any unwanted UBM layer 129 over the dry resist film 122 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 1D and FIG. 1E may be termed as dry film lithography process for lift-off metallization of UBM metal stack for a die attachment, wire-bonding and for seal ring fabrication to protect the laser diode. The photolithography process can be any one of the following commonly known methods like for example contact or proximity alignment lithography or projection lithography.

[0024] In FIG. 1F, another dry resist film 136 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable flow-stop pattern is transferred onto the dry resist film 136 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 136 is performed by a selective exposure to a radiation source, such as UV light. Then a selective portion of the dry resist film 136 may be dissolved away by a suitable developer solution, giving rise to two patterns 138 in the dry resist film 136. The two patterns 138 formed in the dry resist film 136 respectively expose two corresponding portions on the UBM layer portion 134 previously deposited on the portion of the support substrate 106.

[0025] Next, a flow-stop layer 140 is deposited over the dry resist film 136 and through the two patterns 138, onto the UBM layer portion 134 on the support substrate 106 using for example an e-beam evaporator or sputtering process. This provides for two flow-stop layer portions 141 positioned adjacent to each other on the UBM layer portion 134. In one embodiment, a material for the flow-stop layer 140 and the flow-stop layer portions 141 is a material which does not react with a conductive material (for example solder) to be subsequently deposited in between the two flow-stop layer

portions. Some examples include metals such as Aluminium (Al), Nickel (Ni) and Platinum (Pt) and non-metals such as dielectric or polymer. In one embodiment, the thickness of the flow-stop layer 140 is in the range of between about 0.5 μm to a few μm . It is essential that the material for the flow-stop layer 140 is thermally stable at the conductive material reflow temperature which is typically in the range from about 100 °C to about 350 °C.

[0026] In FIG. 1G, the dry resist film 136 and any unwanted flow-stop layer 140 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 1F and FIG. 1G may be termed as dry film lithography process for lift-off metallization of flow-stop pattern. The dry resist film patterning process may also be termed as a contact or proximity alignment or projection lithography.

[0027] In FIG. 1H, a further dry resist film 142 is again laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for a conductive layer deposition is transferred onto the dry resist film 142 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 142 is performed by a selective exposure to a radiation source, such as UV light. Then a selective portion of the dry resist film 142 may be dissolved by a suitable developer solution, giving rise to two patterns 144, 146 in the dry resist film 142. The two patterns 144, 146 include a first pattern 144 which exposes the UBM layer portion 130 previously deposited on the metallic pad 112 and a second pattern 146 which exposes a combination of the UBM layer portion 134 previously deposited on the support substrate 106 and the flow-stop layer portions 141 deposited on the UBM layer portion 134.

[0028] Next, a conductive layer is deposited by evaporation or sputtering process over the dry resist film 142 and through the two patterns 144, 146 thereby giving rise to a first conductive layer portion 148 onto the UBM layer portion 130 on the metallic pad 112 and a second conductive layer portion 149 onto the UBM layer portion 134 on the support substrate 106, between the two flow-stop layer portions 141 using an e-beam evaporator. The two flow-stop layer portions 141 may serve as a boundary for the second conductive layer portion 149 and helps to prevent the second conductive layer portion 149 from flowing out of a designated area. The first conductive layer portion 148 and the second conductive layer portion 149 may be a solder layer.

[0029] In FIG. 1I, the dry resist film 142 and any unwanted conductive layer are removed by a suitable process, for example, a lift-off process. The processes in FIG. 1H and FIG. 1I may be termed as dry film lithography process to deposit a conductive layer for die attachment and electrical interconnection. The dry resist film patterning process may also be termed as a contact or proximity alignment or projection lithography.

[0030] FIG. 1J shows an integrated assembly 150 including the integrated circuit and optical components such as an optical fiber 152 and a laser diode or a photodiode 154 on the same side of the substrate 102. In FIG. 1J, an electrical pad or UBM layer portion 156 is shown on the laser diode or photodiode 154, the electrical pad 156 in contact with the flow-stop layer portions 141 and the second conductive layer portion 149 in between the flow-stop layer portions 141. The electrical pads 156 are typically made of gold or capped with a layer of gold. The optical components such as the optical fiber 152 and the laser diode or a photodiode 154 are arranged into the respective dielectric cavities 116, 118 previously formed through the interconnect structure 104, the semiconductor layer

110 and the first insulating layer 108 in FIG. 1B. The optical fiber 152 is arranged in the first area of the support substrate 106 exposed by the first dielectric cavity 116 and the trench 120 and the laser diode or a photo diode 154 is arranged in the second area of the support substrate 106 exposed by the second dielectric cavity 118, the laser diode or the photo diode 154 in electrical contact with the electrical pad 156 in contact with the second conductive layer portion 149 and solder flow-stop layer portions 141 formed in FIG. 1G and FIG. 1I respectively.

[0031] A portion of the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 serves as a first alignment structure 162 for the subsequent placement of the laser diode or photo diode 154. A further portion of the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 serves as a second alignment structure 164 for the subsequent placement of the laser diode or photo diode 154. The combination of the UBM layer portion 134 deposited on the support substrate 106, the flow-stop layer portions 141, the second conductive layer portion 149 in between the flow-stop layer portions 141 and the electrical pad 156 provides for a third alignment structure 166 for the subsequent placement of the laser diode or photo diode 154. The first 162 and second 164 alignment structures may be termed as X/Y-axis stoppers and the third alignment structure 166 may be termed a Z-axis stopper.

[0032] FIGS. 2A to 2J shows a method of manufacturing an integrated assembly according to one embodiment of the present invention. The method as shown in FIGS. 2A to 2J is similar to the method as shown in FIGS. 1A to FIG. 1J with the difference in the patterning of the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 to provide for additional alignment structures for subsequent

placement of an optical component as shown in FIGs. 2B-1 and 2B-2. Fig. 2B-2 being a top view showing the design or arrangement of the X/Y axis stopper.

[0033] FIG. 2A is similar to FIG. 1A and shows an integrated assembly 150 including a substrate 102 and an interconnect structure 104 disposed above the substrate 102. The substrate 102 includes a silicon-on-insulator structure. In particular, the substrate 102 includes a support substrate 106, a first insulating layer 108 disposed above the support substrate 106 and a semiconductor layer 110 disposed above the first insulating layer 108. The interconnect structure 104 includes a metallization plane (not shown) and second insulating layer (not shown). The integrated assembly further includes a metallic pad 112 provided on the interconnect structure 104.

[0034] In one embodiment, the integrated assembly 150 may include an integrated circuit provided on the semiconductor layer 110. Optical passive structures may also be formed in the semiconductor layer 110. The optical passive structures include nano-tapered structures. Alignment keys may also be included in the integrated assembly 150 for alignment between the substrate 102 fabricated in a front end process and the interconnect structure 104 fabricated in a back end process.

[0035] In one embodiment, the interconnect structure 104 includes a stack layer of a plurality of metallization planes and second insulating layers, which may be termed as a multi-level metallization or dielectric stack.

[0036] In one embodiment, the support substrate 106 includes a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride. The first insulating layer 108 and second insulating layer respectively include a material selected from the group consisting of silicon oxide, a polymer and a dielectric

material. The semiconductor layer 110 includes a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium. The metallization plane includes Tungsten, Copper or Aluminum. The metallic pad 112 includes aluminium or any other combinations of metals like UBM.

[0037] In one embodiment, the thickness of the support substrate 106 is in the range of between about few hundred microns to full thickness of the substrate, depending on the wafer diameter. The thickness of the first insulating layer 108 can vary from sub-micron dimensions to several microns. The thickness of the semiconductor layer 110 is in the range of between tens of nanometers to about few microns. The thickness of the interconnect structure 104 is in the range of between few microns to tens of microns.

[0038] FIG. 2B-1 and FIG. 2B is similar to FIG. 1B with the exception that four dielectric cavities 116, 118, 158, 160 instead of two dielectric cavities 116, 118 are formed in the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 to expose four portions of the support substrate 106 by a suitable lithography process. The formation of a third dielectric cavity 158 and a fourth dielectric cavity 160 provide for two alignment structures (that is a first alignment structure 162, a second alignment structure 164) for the subsequent placement of the optical component. An example of the top view of the alignment patterns are illustrated in Figure 2B-2. The process of forming the dielectric cavities are as per that illustrated previously in FIG. 1B.

[0039] In FIG. 2C, like in FIG. 1C, a trench 120 is formed at the bottom of a first through hole 116 by a suitable lithography process. Another layer of photoresist (not shown) is deposited on the interconnect structure 104 and a portion of the support substrate 106. The photoresist layer is then patterned to form an opening thereby

exposing a portion of the support substrate 106 at the bottom of the first through hole 116 by suitable lithography techniques. The portion of the support substrate 106 not covered by the photoresist is being etched to form the trench 120 in the support substrate 106. The trench 120 may be used for subsequent optical fiber or lens placement. After forming the trench 120, the photoresist layer is removed or stripped away by a plasma resist strip and a wet clean process. This process in FIG. 2C may be termed the fiber cavity or guide slot lithography.

[0040] In this regard, any other suitable techniques or processes may also be used in order to provide greater flexibility with respect to forming the trench 120 in the support substrate 106. In one embodiment, suitable lithography processes include deep ultra-violet lithography, i-line lithography. Suitable etching process includes a deep reactive-ion etching (DRIE) process. The DRIE process is an anisotropic etch process used to create deep, steep-sided holes and trenches in substrates.

[0041] In an embodiment, a thin layer of dielectric (not shown) such as silicon nitride, silicon oxy-nitride, silicon oxide, silicon carbide in the range of about 50 to about 1000Å is deposited by plasma enhance chemical vapor deposition (PECVD) to improve the adhesion between a subsequently deposited under bump metallization (UBM) layer or UBM film stack with the underlying support substrate 106. The dielectric layer can be deposited as a single layer or a combination of two or more layers. The dielectric layer thus serves as an adhesion promoter between the support substrate and the deposited UBM metal or UBM film stack. The UBM layer or UBM film stack is composed of an adhesion layer like Titanium or Chromium, a solder diffusion barrier like Nickel or Platinum and finally a solder wetting layer like Gold or Copper.

[0042] In FIG. 2D, like in FIG. 1D, a dry resist film 122 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for UBM is transferred onto the dry resist film 122 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 122 is performed by a selective exposure to a radiation source, such as UV light. Then selective portions of the dry resist film 122 may be removed by a suitable developer solution, giving rise to three patterns 124, 126, 128 in the dry resist film 122. The three patterns 124, 126, 128 formed in the dry resist film 122 include a first pattern 124 which exposes a portion on the metallic pad 112, a second pattern 126 which exposes a portion of the interconnect structure 104 and a third pattern 128 which exposes a portion of the support substrate 106.

[0043] Next, a UBM layer or UBM film stack 129 is deposited over the dry resist film 122 and into the respective patterns 124, 126, 128 formed in the dry resist film 122 using an e-beam evaporator or sputtering system. The UBM layer portion 130 deposited on the metallic pad 112 may serve for a subsequent die attachment and wire-bonding, the UBM layer portion 132 deposited on the portion of the interconnect structure 104 may serve for a subsequent placement of a seal ring and the UBM layer portion 134 deposited on the portion of the support substrate 106 may serve for a subsequent placement of a laser diode. In one embodiment, the UBM film stack 129 is composed of a combination of 0.025 to 0.3 μm Titanium (Ti), 0.025 to 0.3 μm Platinum (Pt), 0.5 to 2 μm Gold (Au) multi-layer metal stack. The UBM film stack 129 can also be composed of other multi-layered metal stacks like for example 0.025 to 0.3 μm Chromium (Cr)/0.5-2 μm Gold (Au) and 0.025 to 0.3 μm Titanium (Ti)/0.025-0.3 μm Nickel (Ni)/0.5-2 μm Gold (Au).

[0044] In FIG. 2E, like in FIG. 1E, the dry resist film 122 and any unwanted UBM layer or UBM film stack 129 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 2D and FIG. 2E may be termed as dry film lithography process for lift-off metallization of UBM metal stack for a die attachment and wire-bonding, a seal ring, a laser diode. The process may also be termed as a contact or proximity alignment or projection lithography.

[0045] In FIG. 2F, like in FIG. 1F, another dry resist film 136 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable flow-stop pattern is transferred onto the dry resist film 136 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 136 is performed by a selective exposure to a radiation source, such as UV light. Then selective portions of the dry resist film 136 may be removed by a suitable developer solution, giving rise to two through holes 138 in the dry resist film 136. The two patterns 138 formed in the dry resist film 136 respectively expose two corresponding portions on the UBM layer portion 134 previously deposited on the portion of the support substrate 106.

[0046] Next, a flow-stop layer 140 is deposited over the dry resist film 136 and through the two patterns 138, onto the UBM layer portion 134 on the support substrate 106 using an e-beam evaporator or sputtering system. This provides for two flow-stop layer portions 141 positioned adjacent to each other on the UBM layer portion 134. In one embodiment, the material for the flow-stop layer 140 and the flow-stop layer portions is a material which does not react with a conductive material (for example solder) to be subsequently deposited in between the flow-stop layer portions 141. Some examples include metals such as Aluminium (Al), Nickel (Ni) and Platinum (Pt) and non-metals

such as dielectric or polymer. In one embodiment, the thickness of the flow-stop layer 140 is in the range of between about 0.5 μm to a few μm .

[0047] In FIG. 2G, like in FIG. 1G, the dry resist film 136 and any unwanted flow-stop layer 140 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 2F and FIG. 2G may be termed as dry film lithography process for lift-off metallization of flow-stop pattern. The process may also be termed as a contact or proximity alignment or projection lithography.

[0048] In FIG. 2H, like in FIG. 1H, a further dry resist film 142 is again laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for a conductive layer deposition is transferred onto the dry resist film 142 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 142 is performed by a selective exposure to a radiation source, such as UV light. Then selective portions of the dry resist film 142 may be removed by a suitable developer solution, giving rise to two patterns 144, 146 in the dry resist film 142. The two patterns 144, 146 includes a first pattern 144 which exposes the UBM layer portion 130 previously deposited on the metallic pad 112 and a second pattern 146 which exposes a combination of the UBM layer portion 134 previously deposited on the support substrate 106 and the flow-stop layer portions 141 deposited on the UBM layer portion 134.

[0049] Next, a conductive layer is deposited in an e-beam evaporator or sputtering system over the dry resist film 142 and through the two patterns 144, 146, thereby giving rise to a first conductive layer portion 148 onto the UBM layer portion 130 on the metallic pad 112 and a second conductive layer portion 149 on the UBM layer portion 134 on the support substrate 106, between the two flow-stop layer portions 141. The two

flow-stop layer portions 141 may serve as a boundary for the second conductive layer portion 149 and helps to prevent the second conductive layer portion 149 from flowing out of a designated area. The first conductive layer portion 148 and the second conductive layer portion 149 may be a solder layer.

[0050] In FIG. 2I, like in FIG. 1I, the dry resist film 142 and any unwanted conductive layer are removed by a suitable process, for example, a lift-off process. The processes in FIG. 2H and FIG. 2I may be termed as dry film lithography process to deposit a conductive layer for die attachment and electrical interconnection. The process may also be termed as a contact or proximity alignment or projection lithography.

[0051] FIG. 2J, like in FIG. 1J, shows an integrated assembly 150 including the integrated circuit and optical components such as an optical fiber 152 and a laser diode or a photodiode 154 on the same side of the substrate 102. In FIG. 2J, an electrical pad or UBM layer portion 156 is deposited on the laser diode or photodiode 154, the electrical pad 156 in contact with the flow-stop layer portions 141 and the second conductive layer portion 149 in between the flow-stop layer portions 141. The electrical pads 156 are typically made of gold or capped with a layer of gold. The optical components such as the optical fiber 152 and the laser diode or a photodiode 154 are arranged into the respective dielectric cavities 116, 118 previously formed through the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 in FIG. 2B. The optical fiber 152 is arranged in the first area of the support substrate 106 exposed by a first dielectric cavity 116 and the trench 120 and the laser diode or a photo diode 154 is arranged in the second area of the support substrate 106 exposed by a second dielectric cavity 118, the laser diode or the photo diode 154 in electrical contact with the electrical

pad 156 in contact with the second conductive layer portion 149 and flow-stop layer portions 141 formed in FIG. 2G and FIG. 2I respectively. The combination of the UBM layer portion 134 deposited on the support substrate 106, the flow-stop layer portions 141, the second conductive layer portion 149 in between the flow-stop layer portions 141 and the further electrical pad 156 provides for a third alignment structure 166 for the subsequent placement of the laser diode or photo diode 154. Therefore the first 162 and second 164 alignment structure may be termed as X-/ Y-axis stoppers and the third alignment structure 166 may be termed a Z-axis stopper as illustrated in Fig-2B-2.

[0052] FIGS. 3A to 3K shows a method of manufacturing an integrated assembly according to one embodiment of the present invention. The method as shown in FIGS. 3A to 3K is similar to the method as shown in FIGS. 1A to FIG. 1J with the difference in that the formation of the trench 120 in FIG. 1C has been moved to a step after the deposition of the conductive layer.

[0053] FIG. 3A shows an integrated assembly 150 including a substrate 102 and an interconnect structure 104 disposed above the substrate 102. The substrate 102 includes a silicon-on-insulator structure. In particular, the substrate 102 includes a support substrate 106, a first insulating layer 108 disposed above the support substrate 106 and a semiconductor layer 110 disposed above the first insulating layer 108. The interconnect structure 104 includes a metallization plane (not shown) and second insulating layer (not shown). The integrated assembly 150 further includes a metallic pad 112 provided on the interconnect structure 104.

[0054] In one embodiment, the integrated assembly 150 may include an integrated circuit provided on the semiconductor layer 110. Optical passive structures may also be

formed in the semiconductor layer 110. The optical passive structures include nano-tapered structures. Alignment keys may also be included in the integrated assembly for alignment between the substrate 102 fabricated in a front end process and the interconnect structure 104 fabricated in a back end process.

[0055] In one embodiment, the interconnect structure 104 includes a stack layer of a plurality of metallization planes and second insulating layers, which may be termed as a multi-level metallization or dielectric stack.

[0056] In one embodiment, the support substrate 106 includes a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride. The first insulating layer 108 and second insulating layer respectively include a material selected from the group consisting of silicon oxide, a polymer and a dielectric material. The semiconductor layer 110 includes a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium. The metallization plane includes Copper, Aluminum and Tungsten. The metallic pad 112 includes aluminium or any other combinations of metals like UBM.

[0057] In one embodiment, the thickness of the support substrate 106 is in the range of between about few hundred microns to full thickness of the substrate, depending on the wafer diameter. The thickness of the first insulating layer 108 can vary from sub-micron dimensions to several microns. The thickness of the semiconductor layer 110 is in the range of between tens of nanometers to about few microns. The thickness of the interconnect structure 104 is in the range of between few microns to tens of microns

[0058] In FIG. 3B, two dielectric cavities 116, 118 are formed in the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 to expose

two portions of the support substrate 106 by a suitable lithography process. First, a layer of photoresist 114 is deposited on the interconnect structure 104. The photoresist layer 114 is then patterned to form two openings or contact windows to expose two portions of the support substrate 106 by suitable lithography techniques. Portions of the interconnect structure 104, semiconductor layer 110 and the first insulating layer 108 not covered by the photoresist 114 are being etched to form two dielectric cavities 116, 118 to expose two portions of the support substrate 106. A first area of the support substrate 106 exposed by a first dielectric cavity 116 may be termed a reference contact window and a second area exposed by a second dielectric cavity 118 may be termed a laser diode area. After forming the two dielectric cavities 116, 118, the photoresist layer 114 is removed or stripped away by a plasma resist strip and a wet clean process. This process in FIG. 3B may be termed a contact window lithography.

[0059] In this regard, any other suitable techniques or processes may also be used in order to provide greater flexibility with respect to forming the dielectric cavities 116, 118. In one embodiment, suitable lithography processes include deep ultra-violet lithography, i-line lithography or broadband UV lithography by using conventionally coated positive or negative photoresist, laminated dry resist film, Spray coated resist and electroplated photoresist. Suitable etching process includes wet chemical etching and dry etching processes for example a deep reactive-ion etching (DRIE), Plasma Etching (PE) and Reactive Ion Etch (RIE) process.

[0060] In an embodiment, a thin layer of dielectric (not shown) such as silicon nitride, silicon oxy-nitride, silicon oxide, silicon carbide in the range of about 50A to about 1000A is deposited globally by plasma enhance chemical vapor deposition

(PECVD) after forming of the trench 120 to improve the adhesion of a subsequently deposited under bump metallization (UBM) layer or UBM film stack with the underlying support substrate 106. The dielectric layer can be deposited as a single layer or a combination of two or more layers. The dielectric layer thus serves as an adhesion promoter between the support substrate and the deposited UBM metal or UBM film stack. The UBM layer or UBM film stack is composed of an adhesion layer like Titanium or Chromium, a solder diffusion barrier like Nickel or Platinum and finally a solder wetting layer like Gold or Copper.

[0061] In FIG. 3C, a dry resist film 122 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for UBM is transferred onto the dry resist film 122 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 122 is performed by a selective exposure to a radiation source, such as UV light. Then selective portions of the dry resist film 122 may be removed by a suitable developer solution, giving rise to three patterns 124, 126, 128 in the dry resist film 122. The three patterns 124, 126, 128 formed in the dry resist film 122 include a first pattern 124 which exposes a portion on the metallic pad 112, a second pattern 126 which exposes a portion of the interconnect structure 104 and a third pattern 128 which exposes a portion of the support substrate 106.

[0062] Next, a UBM layer or UBM film stack 129 is evaporated over the dry resist film 122 and into the respective patterns 124, 126, 128 formed in the dry resist film 122 using an e-beam evaporator or sputtering system. The UBM layer portion 130 deposited on the metallic pad 112 may serve for a subsequent die attachment and wire-bonding, the UBM layer portion 132 deposited on the portion of the interconnect structure 104 may

serve for a subsequent placement of a seal ring and the UBM layer portion 134 deposited on the portion of the support substrate 106 may serve for a subsequent placement of a laser diode. In one embodiment, the UBM stack 129 is composed of a combination of 0.025 to 0.3 μm Titanium (Ti) , 0.025-0.3 μm Platinum (Pt) , 0.5-2 μm Gold (Au) multi-layer metal stack. The UBM can also be composed of other multi-layered metal stacks like for example: 0.025 to 0.3 μm Chromium (Cr)/0.5-2 μm Gold (Au) and 0.025 to 0.3 μm Titanium (Ti)/0.025-0.3 μm Nickel (Ni)/0.5-2 μm Gold (Au).

[0063] In FIG. 3D, the dry resist film 122 and any unwanted UBM layer or UBM stack 129 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 3C and FIG. 3D may be termed as dry film lithography process for lift-off metallization of UBM metal stack for a die attachment and wire-bonding, a seal ring, a laser diode. The process may also be termed as a contact or proximity alignment or projection lithography.

[0064] In FIG. 3E, another dry resist film 136 is laminated over the interconnect structure 104 using a dry-film laminator. A suitable flow-stop pattern is transferred onto the dry resist film 136 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 136 is performed by a selective exposure to a radiation source, such as light. Then selective portions of the dry resist film 136 may be etched away by a suitable developer solution, giving rise to two exposed patterns 138 in the dry resist film. The two exposed patterns 138 formed in the dry resist film 136 respectively expose two corresponding portions on the UBM layer portion 134 deposited on the portion of the support substrate 106.

[0065] Next, a flow-stop layer 140 is evaporated over the dry resist film 136 and through the two exposed patterns 138, onto the UBM layer portion 134 on the support substrate 106 using an e-beam evaporator. This provides for two flow-stop layer portions 141 positioned adjacent to each other on the UBM layer portion 134. In one embodiment, the material for the flow-stop layer 140 and the flow-stop layer portions 141 is a material which does not react with a conductive material (for example solder) to be subsequently deposited in between the flow-stop layer portions 141. Some examples include metals such as Aluminium (Al), Nickel (Ni) and Platinum (Pt) and non-metals such as dielectric or polymer. In one embodiment, the thickness of the flow-stop layer 140 is in the range of between about 0.5 μm to a few μm .

[0066] In FIG. 3F, the dry resist film 136 and any unwanted flow-stop layer 140 are removed by a suitable process, for example, a lift-off process. The processes in FIG. 3E and FIG. 3F may be termed as dry film lithography process for lift-off metallization of flow-stop pattern. The process may also be termed as a contact or proximity alignment or projection lithography.

[0067] In FIG. 3G, a further dry resist film 142 is again laminated over the interconnect structure 104 using a dry-film laminator. A suitable pattern for a conductive layer deposition is transferred onto the dry resist film 142 by a suitable lithography process. Essentially the transfer of the pattern to the dry resist film 142 is performed by a selective exposure to a radiation source, such as light. Then selective portions of the dry resist film 142 may be etched away by a suitable developer solution, giving rise to two patterns 144, 146 in the dry resist film 142. The two patterns 144, 146 include a first pattern 144 which exposes the UBM layer portion 130 previously deposited on the

metallic pad 112 and a second pattern 146 which exposes a combination of the UBM layer portion 134 previously deposited on the support substrate 106 and the flow-stop layer portions 141 deposited on the UBM layer portion 134.

[0068] Next, a conductive layer is evaporated over the dry resist film 142 and through the two patterns 144, 146, thereby giving rise to a first conductive layer portion 148 onto the UBM layer portion 130 on the metallic pad 112 and a second conductive layer portion 149 on the UBM layer portion 134 on the support substrate 106, between the two flow-stop layer portions 141 using an e-beam evaporator. The two flow-stop layer portions 141 may serve as a boundary for the second conductive layer portion 149 and helps to prevent the second conductive layer portion 149 from flowing out of a designated area. The first conductive layer 148 portion and the second conductive layer 149 portion may be a solder layer.

[0069] In FIG. 3H, the dry resist film 142 and any unwanted conductive layer are removed by a suitable process, for example, a lift-off process. The processes in FIG. 3G and FIG. 3H may be termed as dry film lithography process to deposit solder for die attachment and electrical interconnection. The process may also be termed as a contact or proximity alignment or projection lithography.

[0070] In FIG. 3I, a trench 120 is formed at the bottom of a first dielectric cavity 116 by a suitable lithography process. Another layer of photoresist 115 is deposited on the interconnect structure 104. The photoresist layer 115 is then patterned to form an opening 117 thereby exposing a portion of the support substrate 106 at the bottom of the first through hole 116 by suitable lithography techniques. The portion of the support substrate 106 not covered by the photoresist 115 is being etched to form the trench 120 in the

support substrate 106. The trench 120 may be used for subsequent optical fiber or lens placement.

[0071] In FIG. 3J, the photoresist layer 115 is removed or stripped away by a plasma resist strip and a wet clean process after forming the trench 120. This process in FIG. 3I and FIG. 3J may be termed the fiber cavity or guide slot lithography.

[0072] This embodiment allows the fiber cavity or guide slot patterns to be overlapped with the dielectric cavity patterns so that the fiber cavity patterns gets self-aligned with the overlapping edge of the dielectric cavity. This is possible due to very high etch selectivity to photoresist and dielectric material during the fiber cavity etching process.

[0073] In this regard, any other suitable techniques or processes may also be used in order to provide greater flexibility with respect to forming the trench 120 in the support substrate 106. In one embodiment, suitable lithography processes include deep ultra-violet lithography, i-line lithography or broadband UV lithography by using conventionally coated positive or negative photoresist, laminated dry resist film, Spray coated resist or electroplated photoresist. Suitable etching process includes a deep reactive-ion etching (DRIE) process. The DRIE process is an anisotropic etch process used to create deep, steep-sided holes and trenches in substrates.

[0074] FIG. 3K shows an integrated assembly 150 including the integrated circuit and optical components such as an optical fiber 152 and a laser diode or a photodiode 154 on the same side of the substrate 102. In FIG. 3K, an electrical pad or UBM layer portion 156 is deposited on laser diode or photodiode 154, the electrical pad 156 in contact with the flow-stop layer portions 141 and the second conductive layer 149 in between the flow-stop layer portions 141. The electrical pads 156 are typically made of gold or

capped with a layer of gold. The optical components such as the optical fiber 152 and the laser diode or photodiode 154 are arranged into the respective dielectric cavities 116, 118 previously formed through the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 in FIG. 3B. The optical fiber 152 is arranged in the first area of the support substrate 106 exposed by a first dielectric cavity 116 and the trench 120 and the laser diode or a photo diode 154 is arranged in the second area of the support substrate 106 exposed by a second dielectric cavity 118, the laser diode or the photo diode 154 in electrical contact with the electrical pad 156 in contact with the second conductive layer portion 149 and flow-stop layer portions 141 formed in FIG. 3F and FIG. 3H respectively.

[0075] A portion of the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 serves as a first alignment structure 162 for the subsequent placement of the laser diode or photo diode 154. A further portion of the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 serves as a second alignment structure 164 for the subsequent placement of the laser diode or photo diode 154. The combination of the UBM layer portion 134 deposited on the support substrate 106, the flow-stop layer portions 141, the second conductive layer portion 149 in between the flow-stop layer portions 141 and the electrical pad 156 provides for a third alignment structure 166 for the subsequent placement of the laser diode or photo diode 154. The first 162 and second 164 alignment structures may be termed as X/ Y-axis stoppers and the third alignment structure 166 may be termed a Z-axis stopper.

[0076] FIG. 4 shows a flowchart of a method of manufacturing an integrated assembly corresponding to FIGS. 1A to 1J and FIGS. 2A to 2J according to one

embodiment of the present invention. The method starts in step 402 with a starting substrate 102 and an interconnect structure 104 disposed above the substrate 102. The substrate 102 includes a support substrate 106, a first insulating layer 108 disposed above the support substrate 106 and a semiconductor layer 110 disposed above the first insulating layer 108. Next in step 404, dielectric cavities 116, 118 are formed in the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 by suitable lithography and etching processes. In step 406, a trench 120 is formed in the support substrate 106 to accommodate a subsequent placement of an optical component 152 by suitable lithography and etching processes. In step 407, a dielectric layer is deposited to improve the adhesion of subsequent deposited UBM layer with any surface in contact therewith. In step 408, a dry resist film 122 is laminated over the interconnect structure 104. A pattern for UBM metallization is transferred onto the dry resist film 122 and the dry resist film 122 is exposed and developed. Then an UBM layer or film stack 129 is deposited. In step 410, the dry resist film 122 and any unwanted UBM layer 129 are removed. In step 412, another dry resist film 136 is laminated over the interconnect structure 104. A pattern for flow-stop or solder-stop metallization is transferred onto the dry resist film 136 and the dry resist film 136 is exposed and developed. Then a flow-stop layer 140 is deposited. In step 414, the dry resist film 136 and any unwanted flow-stop layer 140 other than the flow-stop layer portions 141 as deposited on the UBM layer 134 is removed. In step 416, a further dry resist film 142 is laminated over the interconnect structure 104. A pattern for a conductive layer deposition is transferred onto the dry resist film 142 and the dry resist film 142 is exposed and developed. Then a conductive layer is deposited. In step 418, the dry resist film 142 and any unwanted conductive layer are

removed. Finally in step 420, self-aligned optical components 152, 154 are being attached. This flow may also be described as a DRIE first approach process as the deep silicon cavity is formed before the metallization processes.

[0077] FIG. 5 shows a flowchart of a method of manufacturing an integrated assembly corresponding to FIGS. 3A to 3K according to one embodiment of the present invention. The method starts in step 502 with a starting substrate 102 and an interconnect structure 104 disposed above the substrate 102. The substrate 102 includes a support substrate 106, a first insulating layer 108 disposed above the support substrate 106 and a semiconductor layer 110 disposed above the first insulating layer 108. Next in step 504, dielectric cavities 116, 118 are formed in the interconnect structure 104, the semiconductor layer 110 and the first insulating layer 108 by suitable lithography and etching processes. In step 505, a dielectric layer is deposited to improve the adhesion of a subsequent deposited UBM layer with any surface in contact therewith.. In step 506, a dry resist film 122 is laminated over the interconnect structure 104. A pattern for UBM metallization is transferred onto the dry resist film 122 and the dry resist film 122 is exposed and developed. Alternatively, Spin-coat or Spray-coat or Electroplate platable photo resist may also be coated, exposed and developed for deposition of the UBM layer or UBM film stack 129.

[0078] In step 508, the dry resist film 122 and any unwanted UBM layer 129 are removed. In step 510, another dry resist film 136 is laminated over the interconnect structure 104. A pattern for flow-stop or solder-stop metallization is transferred onto the dry resist film 136 and the dry resist film 136 is exposed and developed. Alternatively, Spin-coat or Spray-coat or Electroplate platable photo resist may also be coated, exposed

and developed for deposition of the solder flow-stop layer 140. In step 512, the dry resist film 136 and any unwanted flow-stop layer 140 other than the flow-stop layer portions 141 as deposited on the UBM layer 134 is removed. In step 514, a further dry resist film 142 is laminated over the interconnect structure 104. A pattern for a conductive layer deposition is transferred onto the dry resist film 142 and the dry resist film 142 is exposed and developed. Alternatively, Spin-coat or Spray-coat or electroplate platable photo resist may also be coated, exposed and developed for deposition of the conductive metal or solder.

[0079] In step 516, the dry resist film 142 and any unwanted conductive layer are removed. In step 518, a trench 120 is formed in the support substrate 106 to accommodate a subsequent placement of an optical component 152 by suitable lithography and etching processes. In step 520, the photoresist layer 114 is removed. Finally in step 522, self-aligned optical components 152, 154 are being attached. This flow may also be described as a DRIE last approach process.

[0080] FIG. 6 shows a top-view of an integrated assembly according to one embodiment of the present invention. The integrated assembly 150 includes a first dielectric cavity 116 formed through the interconnect structure 104, a trench 120 etched inside the support substrate 106, a second dielectric cavity 118 formed through the interconnect structure 104, an optical signal processing unit 168 and silicon waveguide 170 with tapered ends. The first dielectric cavity 116 and the trench 120 is configured to accommodate an optical fiber 152 and the second dielectric cavity 118 is configured to accommodate laser diode or photo diode 154. The optical signal processing unit 168 may

include a modulator and optical passive elements. The integrated assembly 150 as shown in FIG. 1J, FIG. 2J and FIG. 3K is a cross-sectional view along line A-A

[0081] In the following description, further aspects of embodiments of the present invention will be explained.

[0082] According to one embodiment of the present invention, an optical sub-assembly fabrication technology which integrates front-end semiconductor devices, complementary metal-oxide semiconductor (CMOS) compatible electro-optic modulator devices with optical components on a common silicon platform. The silicon platform which may also be called an integrated optical sub-assembly, also provides for very precise alignment of front-end CMOS devices and optical passives structures with the optical assembly structures and devices like lens, fiber and active devices like laser diode, photo-detector for example. The entire process of fabricating the integrated optical sub-assembly platform is a wafer level and production worthy process.

[0083] According to one embodiment of the present invention, a method of fabricating an integrated optical sub-assembly platform has been provided which provides for very precise alignment accuracies by leveraging semiconductor wafer fab processes. The non-standard metallization involving UBM and solder is integrated as back-end processes outside CMOS wafer fab in assembly or MEMS foundry.

[0084] According to one embodiment of the present invention, the method further incorporates certain special mechanical alignment structures which help in precisely positioning the laser diodes with respect to fiber, lens and other optical components.

[0085] According to one embodiment of the present invention, an optical sub-assembly fabrication technology has been provided which is divided into CMOS

compatible and wafer fab compatible front-end process and MEMS foundry compatible back-end process.

[0086] According to one embodiment of the present invention, a method of integrating preprocessed CMOS device structures with MEMS and optical components is provided.

[0087] According to one embodiment of the present invention, a method for realizing deep dielectric cavities with precise alignment with front-end device structures like transistors, optical detectors, nanotapered waveguides and modulator structures is provided.

[0088] According to one embodiment of the present invention, a method of forming deep silicon cavities inside the deep dielectric cavities which can be used for assembling MEMS and Optical components like fibers, optical and MEMS devices with precise alignment with front-end CMOS device structures is provided.

[0089] According to one embodiment of the present invention, a method of forming a wide range of metallization structures for optical, MEMS and electrical components assembly with high degree of alignment accuracy by using dry resist film based lift-off processing is provided.

[0090] According to one embodiment of the present invention, a method of using disparate metallization patterns over each other to serve as mechanical alignment structures, solder stop structures and electrical interconnect structures is provided.

[0091] According to one embodiment of the present invention, the substrate includes a silicon-on-insulator.

[0092] According to one embodiment of the present invention, the substrate includes a support substrate; a first insulating layer disposed above the support substrate; and a semiconductor layer disposed above the first insulating layer.

[0093] According to one embodiment of the present invention, the support substrate includes a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride.

[0094] According to one embodiment of the present invention, the first insulating layer includes a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.

[0095] According to one embodiment of the present invention, the semiconductor layer includes a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium.

[0096] According to one embodiment of the present invention, the integrated circuit is provided on the semiconductor layer.

[0097] According to one embodiment of the present invention, the integrated assembly further includes a metallic pad provided on the interconnect structure.

[0098] According to one embodiment of the present invention, the integrated assembly further includes a first metallic layer provided on the metallic pad.

[0099] According to one embodiment of the present invention, the integrated assembly further includes a first conductive layer provided on the first metallic layer.

[00100] According to one embodiment of the present invention, the first metallic layer is an under-bump metallization layer.

[00101] According to one embodiment of the present invention, the first conductive layer is solder.

[00102] According to one embodiment of the present invention, the integrated assembly further includes a second metallic layer provided on the interconnect structure.

[00103] According to one embodiment of the present invention, the second metallic layer is an under-bump metallization layer.

[00104] According to one embodiment of the present invention, the integrated assembly further includes a second dielectric cavity formed through the interconnect structure to accommodate a second optical component.

[00105] According to one embodiment of the present invention, the integrated assembly further includes a third metallic layer provided on the support substrate, within the second dielectric cavity.

[00106] According to one embodiment of the present invention, a thin layer of dielectric such as silicon nitride, silicon oxy-nitride, silicon oxide, silicon carbide is deposited by plasma enhance chemical vapor deposition to improve the adhesion of UBM metal and the deposited dielectric film with the underlying support substrate. The dielectric can be deposited as a single layer or a combination of two or more layers. The dielectric layer thus serves as an adhesion promoter between the support substrate and the third metallic layer over the support substrate.

[00107] According to one embodiment of the present invention, the integrated assembly further includes two flow-stop layer portions provided on the third metallic layer.

[00108] According to one embodiment of the present invention, the integrated assembly further includes a second conductive layer provided on the third metallic layer, within the two flow-stop layer portions.

[00109] According to one embodiment of the present invention, the integrated assembly further includes a fourth metallic layer provided on the second optical component for assembling on the second conductive layer between the two flow-stop layer portions.

[00110] According to one embodiment of the present invention, the fourth metallic layer in the second optical component is arranged in electrical contact with the second conductive layer.

[00111] According to one embodiment of the present invention, the third metallic layer is an under-bump metallization layer.

[00112] According to one embodiment of the present invention, each of the two flow-stop layer portions includes a material configured to stop the flow of the second conductive layer.

[00113] According to one embodiment of the present invention, the second conductive layer is solder.

[00114] According to one embodiment of the present invention, the fourth metallic layer is an under-bump metallization layer.

[00115] According to one embodiment of the present invention, the first optical component is an optical fiber or lens.

[00116] According to one embodiment of the present invention, the second optical component is a light emitting source, a detector, a laser diode or a photodetector.

[00117] According to one embodiment of the present invention, the integrated assembly further includes a trench formed in the support substrate to accommodate the first optical component.

[00118] According to one embodiment of the present invention, the trench is formed at the bottom of the first dielectric cavity.

[00119] According to one embodiment of the present invention, the integrated assembly further includes a first alignment structure disposed above the support substrate.

[00120] According to one embodiment of the present invention, the first alignment structure, also known as an X-Y alignment structure, is formed in the interconnect structure.

[00121] According to one embodiment of the present invention, the integrated assembly further includes a second alignment structure disposed above the support substrate.

[00122] According to one embodiment of the present invention, the second alignment structure, also known as an X-Y alignment structure, is formed in the interconnect structure.

[00123] According to one embodiment of the present invention, the third metallic layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer forms a third alignment structure also known as Z-axis alignment.

[00124] According to one embodiment of the present invention, the second optical component is provided within the first alignment structure, the second alignment structure and the third alignment structure.

[00125] According to one embodiment of the present invention, the interconnect structure further comprises a second insulating layer.

[00126] According to one embodiment of the present invention, the second insulating layer comprises a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.

[00127] According to one embodiment of the present invention, forming the integrated circuit on the substrate includes forming the integrated circuit on the semiconductor layer.

[00128] According to one embodiment of the present invention, the method further includes forming a metallic pad on the interconnect structure.

[00129] According to one embodiment of the present invention, the method further includes forming a first metallic layer on the metallic pad.

[00130] According to one embodiment of the present invention, the method further includes forming a first conductive layer on the first metallic layer.

[00131] According to one embodiment of the present invention, the method further includes forming a second metallic layer on the interconnect structure.

[00132] According to one embodiment of the present invention, the method further includes forming a second dielectric cavity through the interconnect structure to accommodate a second optical component.

[00133] According to one embodiment of the present invention, the method further includes forming a third metallic layer on the support substrate, within the second dielectric cavity.

[00134] According to one embodiment of the present invention, a thin layer of dielectric such as silicon nitride, silicon oxy-nitride, silicon oxide, silicon carbide is deposited by plasma enhance chemical vapor deposition to improve the adhesion of UBM metal and the deposited dielectric film with the underlying support substrate. The dielectric can be deposited as a single layer or a combination of two or more layers. The dielectric layer thus serves as an adhesion promoter between the support substrate and the third metallic layer over the support substrate.

[00135] According to one embodiment of the present invention, the method further includes forming two flow-stop layer portions on the third metallic layer.

[00136] According to one embodiment of the present invention, the method further includes forming a second conductive layer on the third metallic layer, within the two flow stop layer portions.

[00137] According to one embodiment of the present invention, the method further includes forming a fourth metallic layer provided on the second optical component for assembling on the second conductive layer between the two flow-stop layer portions.

[00138] According to one embodiment of the present invention, the method further includes arranging the second optical component in electrical contact with the second conductive layer.

[00139] According to one embodiment of the present invention, the method further includes forming a trench in the support substrate to accommodate the first optical component.

[00140] According to one embodiment of the present invention, forming the trench in the support substrate comprises forming the trench such that the trench is formed at the bottom of the first dielectric cavity.

[00141] According to one embodiment of the present invention, the method further includes forming a first alignment structure on or above the support substrate.

[00142] According to one embodiment of the present invention, forming the first alignment structure comprises forming the first alignment structure is formed in the interconnect structure.

[00143] According to one embodiment of the present invention, the method further includes forming a second alignment structure on or above the support substrate.

[00144] According to one embodiment of the present invention, forming the second alignment structure comprises forming the second alignment structure such that the second alignment structure is formed in the interconnect structure.

[00145] According to one embodiment of the present invention, forming the third metallic layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer portion comprises forming the third metallic layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer portion so as to form a third alignment structure.

[00146] According to one embodiment of the present invention, the method further includes providing the second optical component within the first alignment structure and the second alignment structure.

[00147] According to one embodiment of the present invention, forming the first metallic layer, the second metallic layer and the third metallic layer is performed in a common process.

[00148] According to one embodiment of the present invention, a thin layer of silicon nitride is deposited on silicon substrate to improve the adhesion of third metallic layer over the silicon substrate.

[00149] According to one embodiment of the present invention, the trench is formed at the bottom of the first dielectric cavity after formation of the first and second conductive layers.

[00150] According to one embodiment of the present invention the trench pattern is over-lapped with the dielectric cavity pattern so that the edge of the trench can be self-aligned with the edge of the dielectric cavity.

[00151] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

Claims

What is claimed is:

1. An integrated assembly comprising :
a substrate with an integrated circuit;
an interconnect structure disposed above the substrate, wherein the interconnect structure comprises a metallization plane;
a first dielectric cavity is formed through the interconnect structure and at least a part of the substrate to accommodate a first optical component;
wherein the integrated circuit and the first optical component are provided on the same side of the substrate.
2. The integrated assembly according to claim 1, wherein the substrate comprises a silicon-on-insulator.
3. The integrated assembly according to claim 1 or 2, wherein the substrate includes
a support substrate;
a first insulating layer disposed above the support substrate; and
a semiconductor layer disposed above the first insulating layer.
4. The integrated assembly according to claim 3, wherein the support substrate comprises a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride.
5. The integrated assembly according to claim 3 or 4, wherein the first insulating layer comprises a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.

6. The integrated assembly according to any one of claims 3 to 5, wherein the semiconductor layer comprises a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium.
7. The integrated assembly according to any one of claims 3 to 6, wherein the integrated circuit is provided on the semiconductor layer.
8. The integrated assembly according to any one of claims 1 to 7, further comprising a metallic pad provided on the interconnect structure.
9. The integrated assembly according to claim 8, further comprising a first metallic layer provided on the metallic pad.
10. The integrated assembly according to claim 9, further comprising a first conductive layer portion provided on the first metallic layer.
11. The integrated assembly according to claim 9 or 10, wherein the first metallic layer is an under-bump metallization layer.
12. The integrated assembly according to claim 10 or 11, wherein the first conductive layer portion is solder.
13. The integrated assembly according to any one of claims 1 to 12, further comprising a second metallic layer provided on the interconnect structure.
14. The integrated assembly according to claim 13, wherein the second metallic layer is an under-bump metallization layer.
15. The integrated assembly according to any one of claims 1 to 14, further comprising a second dielectric cavity formed through the interconnect structure to accommodate a second optical component.

16. The integrated assembly according to claim 15, further comprising a third metallic layer provided on the support substrate, within the second dielectric cavity.
17. The integrated assembly according to claim 16, further comprising two flow-stop layer portions provided on the third metallic layer.
18. The integrated assembly according to claim 17, further comprising a second conductive layer portion provided on the third metallic layer, within the two flow-stop layer portions.
19. The integrated assembly according to claim 18, further comprising a fourth metallic layer provided on the second optical component.
20. The integrated assembly according to claim 19, wherein the second optical component is arranged in electrical contact with the fourth metallic layer.
21. The integrated assembly according to any one of claims 16 to 20, wherein the third metallic layer is an under-bump metallization layer.
22. The integrated assembly according to any one of claims 17 to 21, wherein each of the two flow-stop layer portions includes a material configured to stop the flow of the second conductive layer.
23. The integrated assembly according to any one of claims 18 to 22, wherein the second conductive layer portion is solder.
24. The integrated assembly according to any one of claims 19 to 23, wherein the fourth metallic layer is an under-bump metallization layer.
25. The integrated assembly according to any one of claims 1 to 24, wherein the first optical component is an optical fiber or lens.

26. The integrated assembly according to any one of claims 15 to 25, wherein the second optical component is a light emitting source, a detector, a laser diode or a photodetector.
27. The integrated assembly according to any one of claims 3 to 26, further comprising a trench formed in the support substrate to accommodate the first optical component.
28. The integrated assembly according to claim 27, wherein the trench is formed at the bottom of the first dielectric cavity.
29. The integrated assembly according to any one of claims 3 to 28, further comprising a first alignment structure disposed above the support substrate.
30. The integrated assembly according to claim 29, wherein the first alignment structure is formed in the interconnect structure.
31. The integrated assembly according to any one of claims 3 to 30, further comprising a second alignment structure disposed above the support substrate.
32. The integrated assembly according to claim 31, wherein the second alignment structure is formed in the interconnect structure.
33. The integrated assembly according to any one of claims 16 to 32, wherein the third metallic layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer portion forms a third alignment structure.
34. The integrated assembly according to claim 33, wherein the second optical component is provided within the first alignment structure, the second alignment structure and the third alignment structure.

35. The integrated assembly according to any one of claims 1 to 34, wherein the interconnect structure further comprises a second insulating layer.
36. The integrated assembly according to claim 35, wherein the second insulating layer comprises a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.
37. A method of manufacturing an integrated assembly, the method comprising :
forming an integrated circuit on a substrate;
forming an interconnect structure on or above the substrate;
forming a first dielectric cavity through the interconnect structure and at least a part of the substrate to accommodate a first optical component; and
providing the integrated circuit and the first optical component on the same side of the substrate;
wherein the interconnect structure comprises a metallization plane.
38. The method according to claim 37, wherein the substrate comprises a silicon-on-insulator.
39. The method according to claim 37 or 38, wherein the substrate includes
a support substrate;
a first insulating layer disposed above the support substrate; and
a semiconductor layer disposed above the first insulating layer.
40. The method according to claim 39, wherein the support substrate comprises a material selected from the group consisting of silicon, sapphire, polysilicon, silicon oxide and silicon nitride.

41. The method according to claim 39 or 40, wherein the first insulating layer comprises a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.
42. The method according to any one of claims 39 to 41, wherein the semiconductor layer comprises a material selected from the group consisting of silicon, gallium arsenide and silicon-germanium.
43. The method according to any one of claims 39 to 42, wherein forming the integrated circuit on the substrate comprises forming the integrated circuit on the semiconductor layer.
44. The method according to any one of claims 37 to 43, further comprising forming a metallic pad on the interconnect structure.
45. The method according to claim 44, further comprising forming a first metallic layer on the metallic pad.
46. The method according to claim 45, further comprising forming a first conductive layer portion on the first metallic layer.
47. The method according to claim 45 or 46, wherein the first metallic layer is an under-bump metallization layer.
48. The method according to claim 46 or 47, wherein the first conductive layer portion is solder.
49. The method according to any one of claims 37 to 48, further comprising forming a second metallic layer on the interconnect structure.
50. The method according to claim 49, wherein the second metallic layer is an under-bump metallization layer.

51. The method according to any one of claims 37 to 50, further comprising forming a second dielectric cavity through the interconnect structure to accommodate a second optical component.
52. The method according to claim 51, further comprising forming a third metallic layer on the support substrate, within the second dielectric cavity.
53. The method according to claim 52, further comprising forming two flow-stop layer portions on the third metallic layer.
54. The method according to claim 53, further comprising forming a second conductive layer portion on the third metallic layer, within the flow stop layer.
55. The method according to claim 54, further comprising forming a fourth metallic layer on the second optical component.
56. The method according to claim 55, further comprising arranging the second optical component in electrical contact with the fourth conductive layer.
57. The method according to any one of claims 52 to 56, wherein the third metallic layer is an under-bump metallization layer.
58. The method according to any one of claims 53 to 57, wherein each of the two flow-stop layer portions include a material configured to stop the flow of the second conductive layer.
59. The method according to any one of claims 54 to 58, wherein the second conductive layer portion is solder.
60. The method according to any one of claims 55 to 59, wherein the fourth metallic layer is an under-bump metallization layer.

61. The method according to any one of claims 37 to 60, wherein the first optical component is an optical fiber or lens.
62. The method according to any one of claims 51 to 61, wherein the second optical component is a light emitting source, detector, laser diode or a photodetector.
63. The method according to any one of claims 39 to 62, further comprising forming a trench in the support substrate to accommodate the first optical component.
64. The method according to claim 63, wherein forming the trench in the support substrate comprises forming the trench such that the trench is formed at the bottom of the first dielectric cavity.
65. The method according to any one of claims 39 to 64, further comprising forming a first alignment structure on or above the support substrate.
66. The method according to claim 65, wherein forming the first alignment structure comprises forming the first alignment structure such that the first alignment structure is formed in the interconnect structure.
67. The method according to any one of claims 39 to 66, further comprising forming a second alignment structure on or above the support substrate.
68. The method according to claim 67, wherein forming the second alignment structure comprises forming the second alignment structure such that the second alignment structure is formed in the interconnect structure.
69. The method according to any one of claims 53 to 68, wherein forming the third metallic layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer portion comprises forming the third metallic

layer, the fourth metallic layer, the two flow-stop layer portions and the second conductive layer portion so as to form a third alignment structure.

70. The method according to claim 69, further comprising providing the second optical component within the first alignment structure, the second alignment structure and the third alignment structure.
71. The method according to any one of claims 37 to 70, wherein the interconnect structure further comprises a second insulating layer.
72. The method according to claim 71, wherein the second insulating layer comprises a material selected from the group consisting of silicon oxide, a polymer and a dielectric material.
73. The method according to any one of claims 45 to 72, wherein forming the first metallic layer, the second metallic layer and the third metallic layer is performed in a common process.

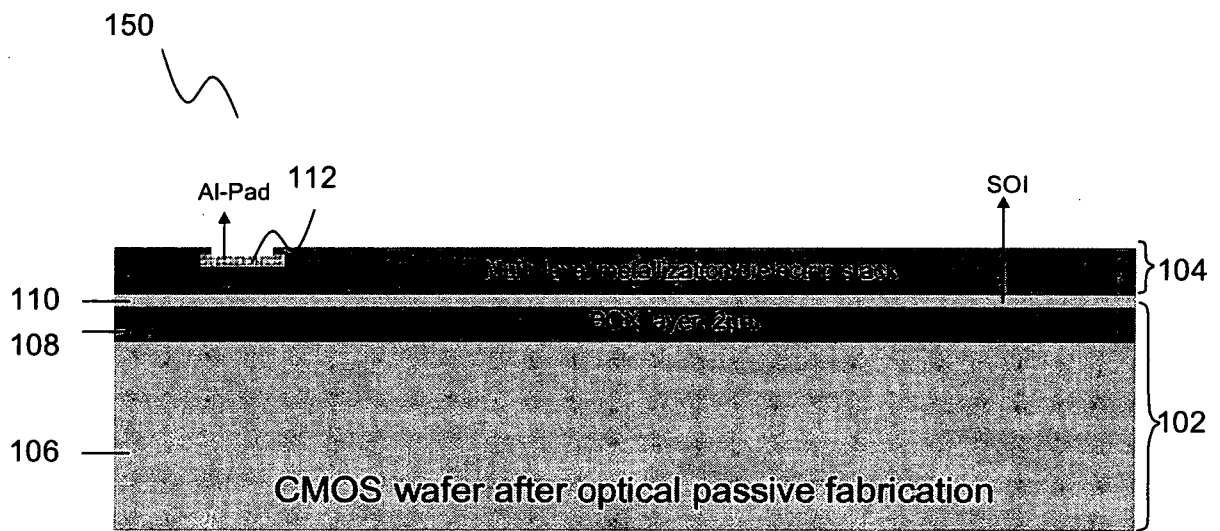


Figure 1A

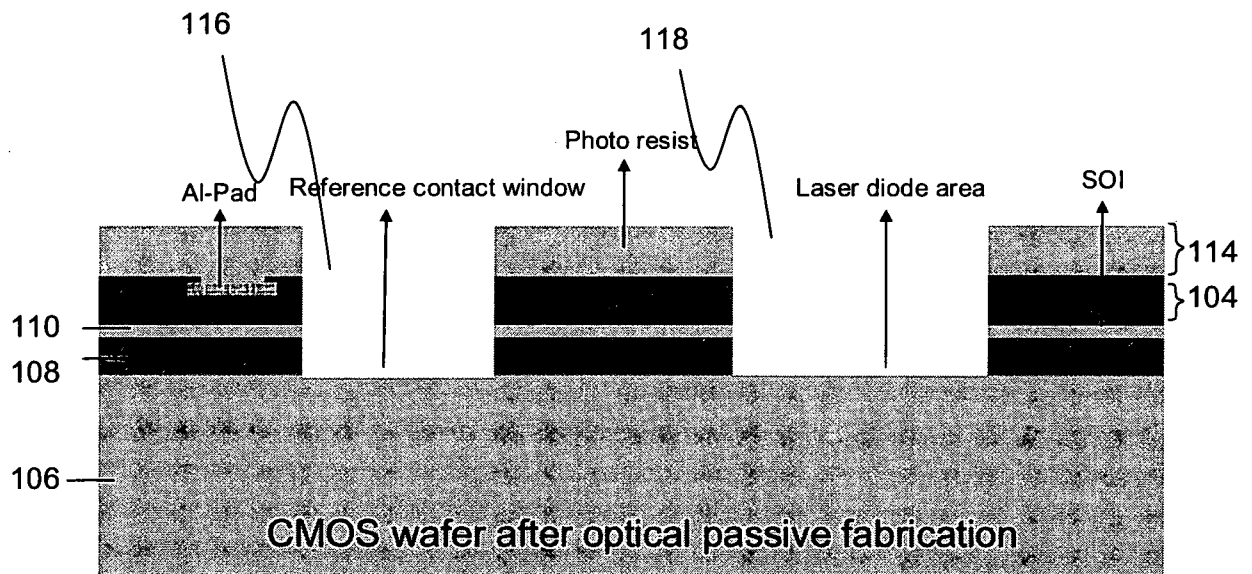


Figure 1B

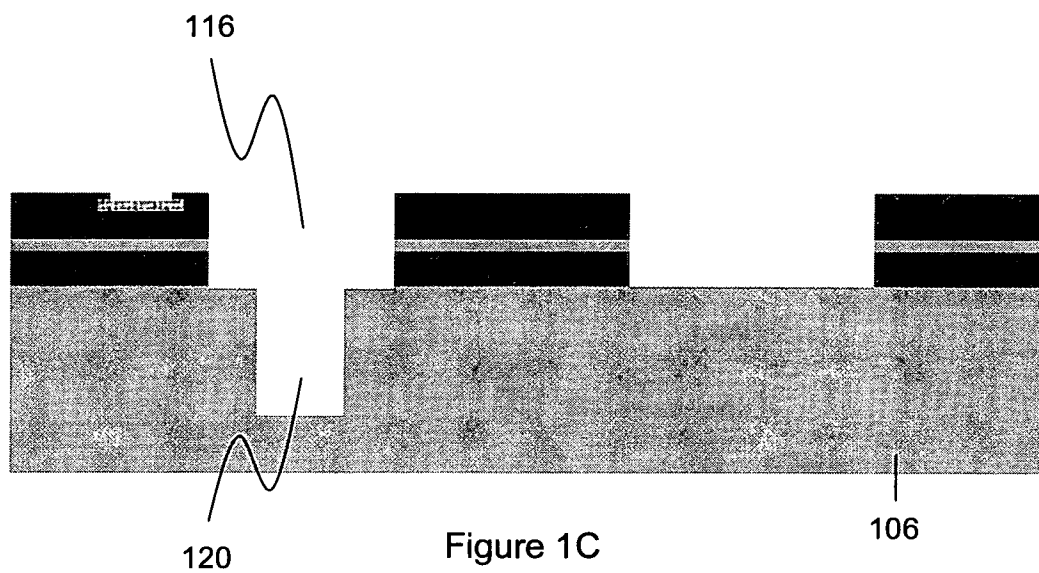


Figure 1C

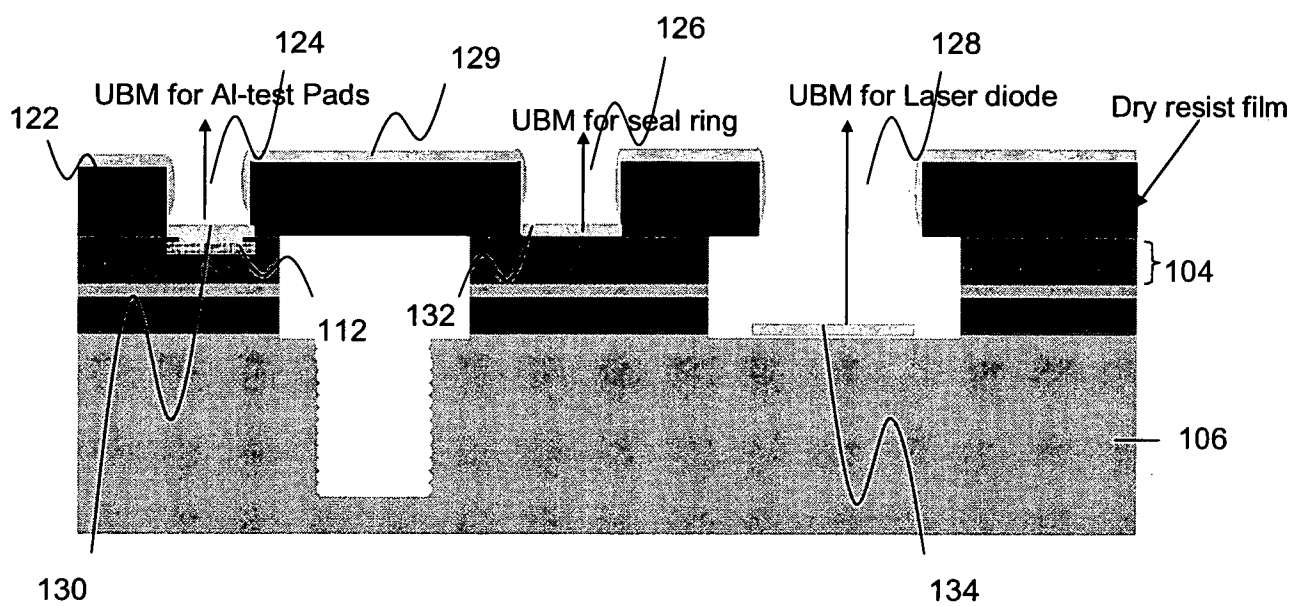


Figure 1D

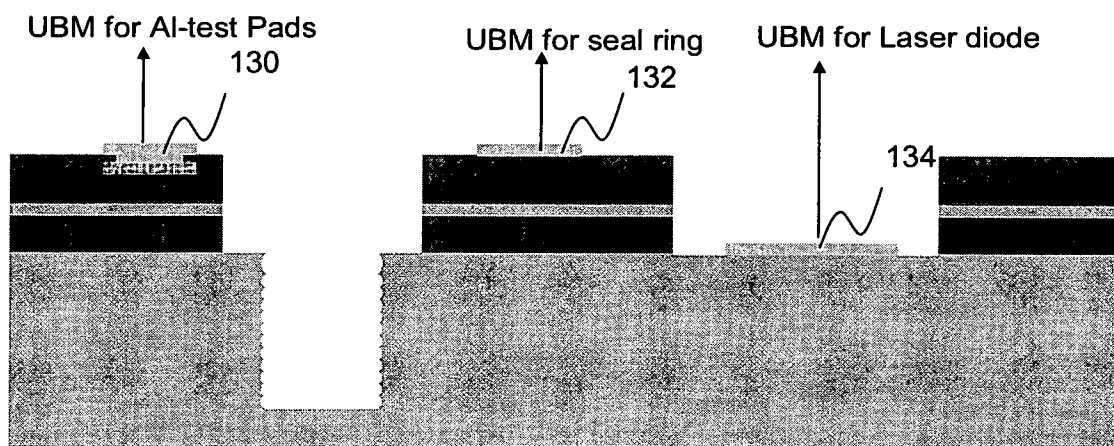


Figure 1E

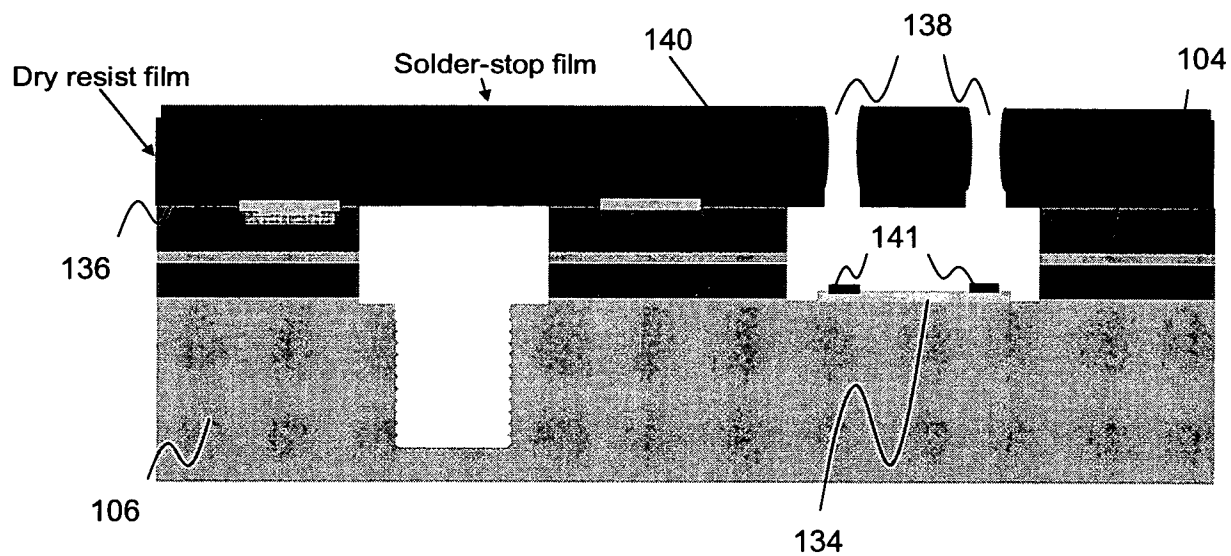


Figure 1F

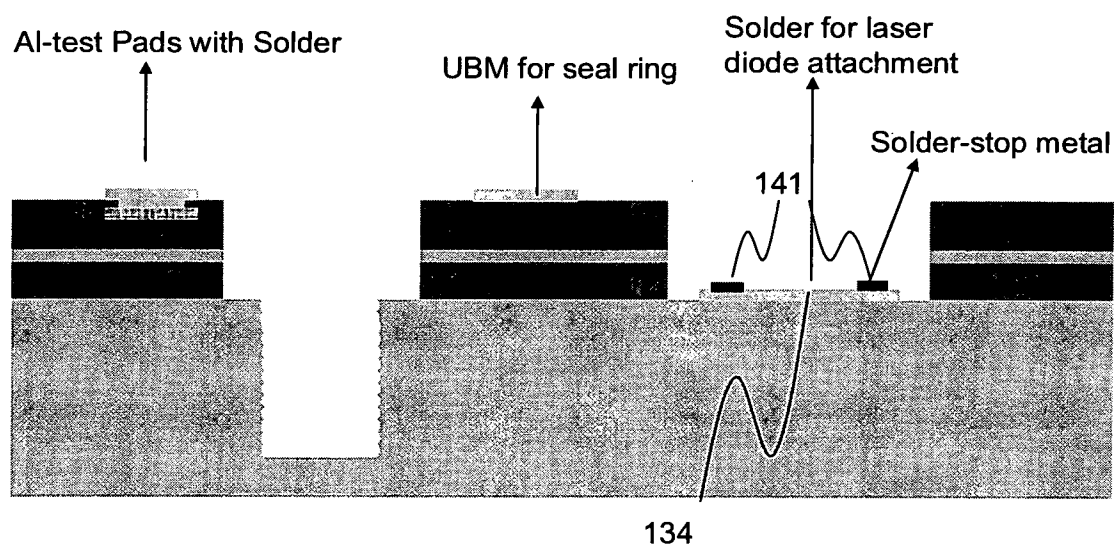


Figure 1G

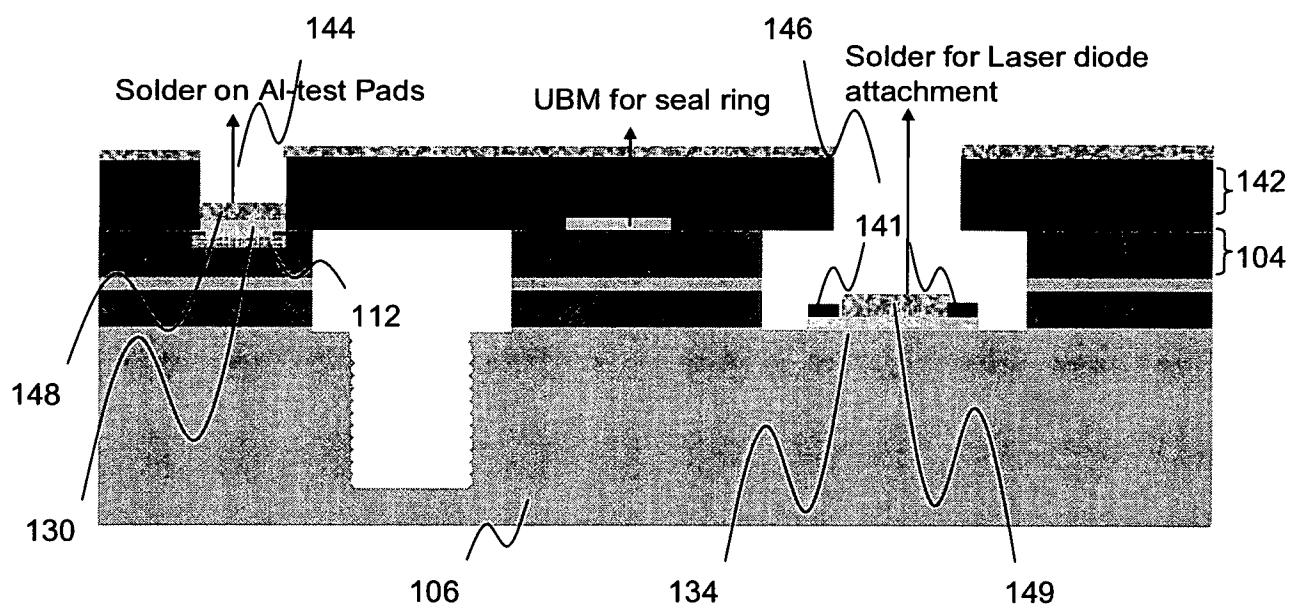


Figure 1H

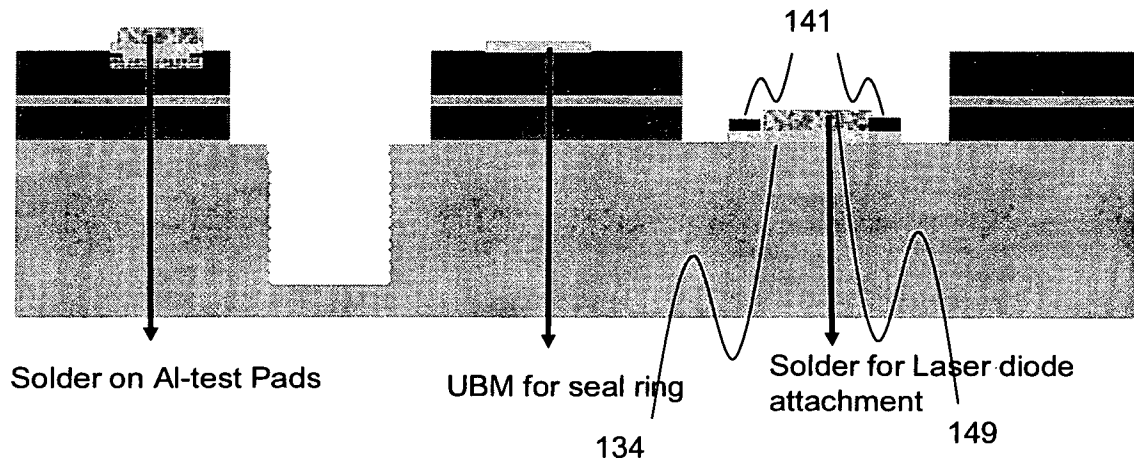


Figure 11

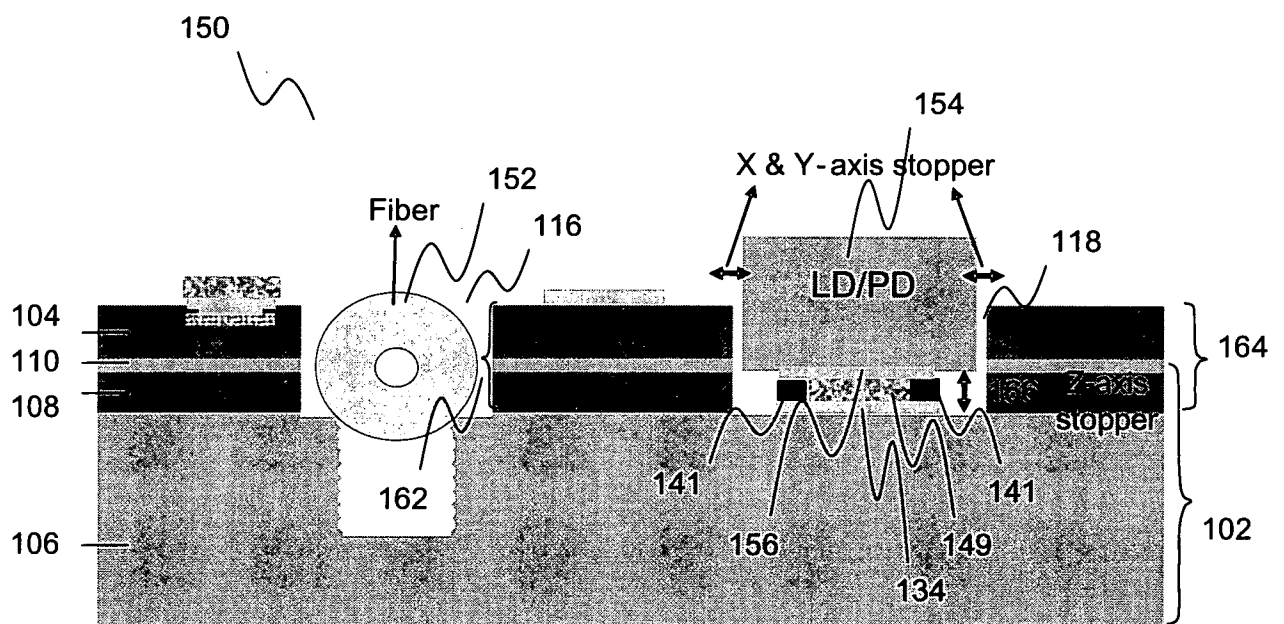


Figure 1J

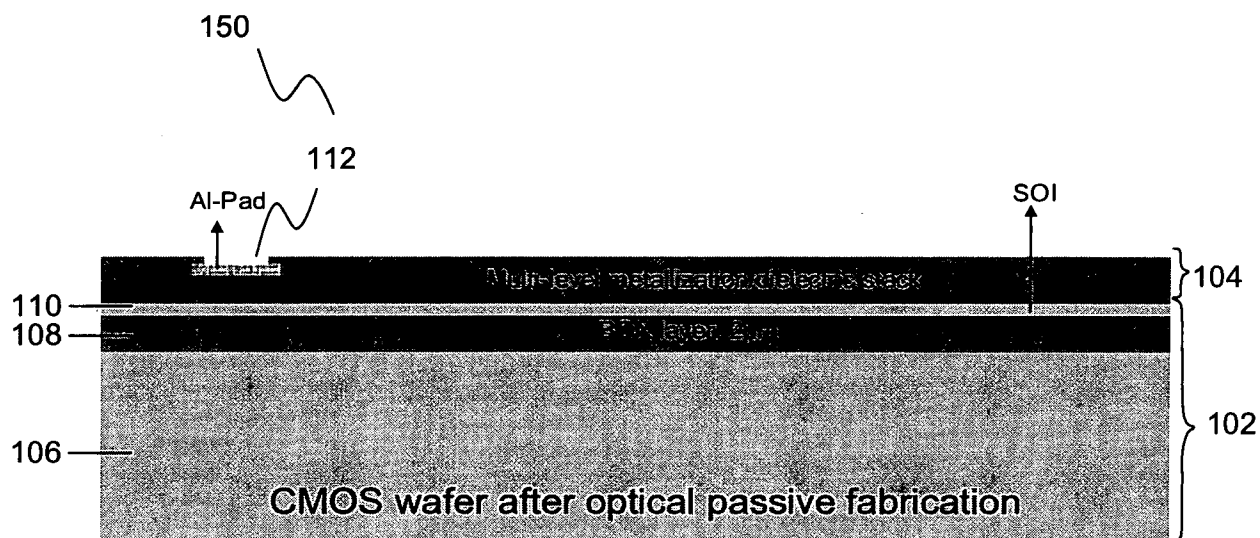


Figure 2A

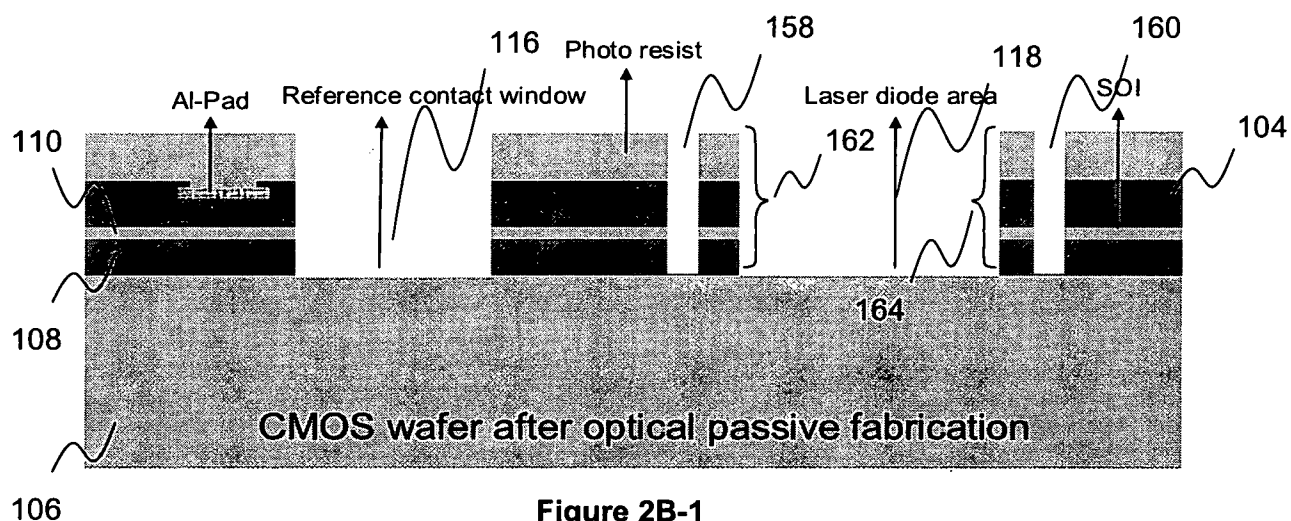


Figure 2B-1

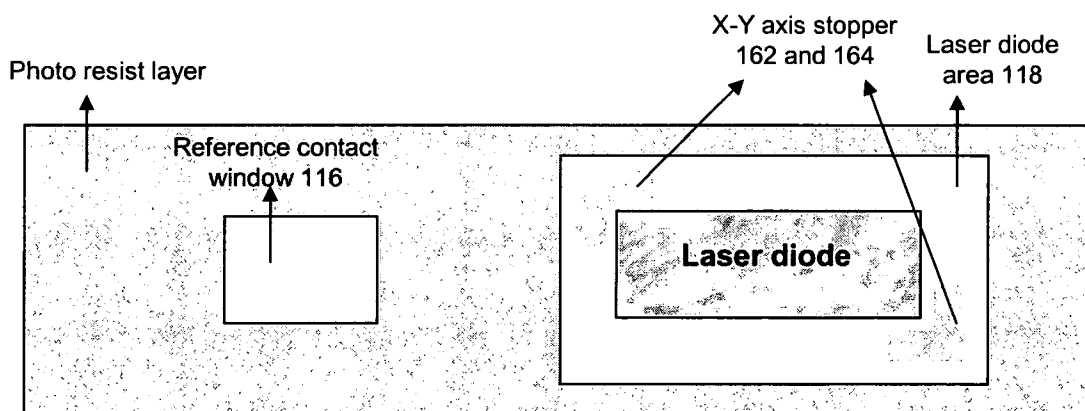


Figure 2B-2

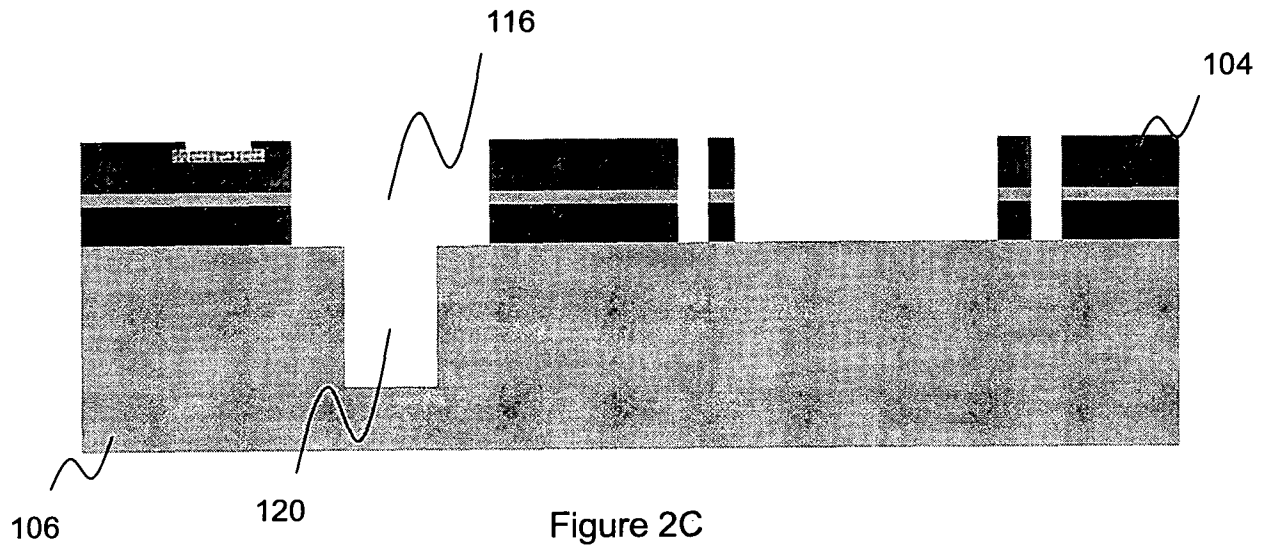


Figure 2C

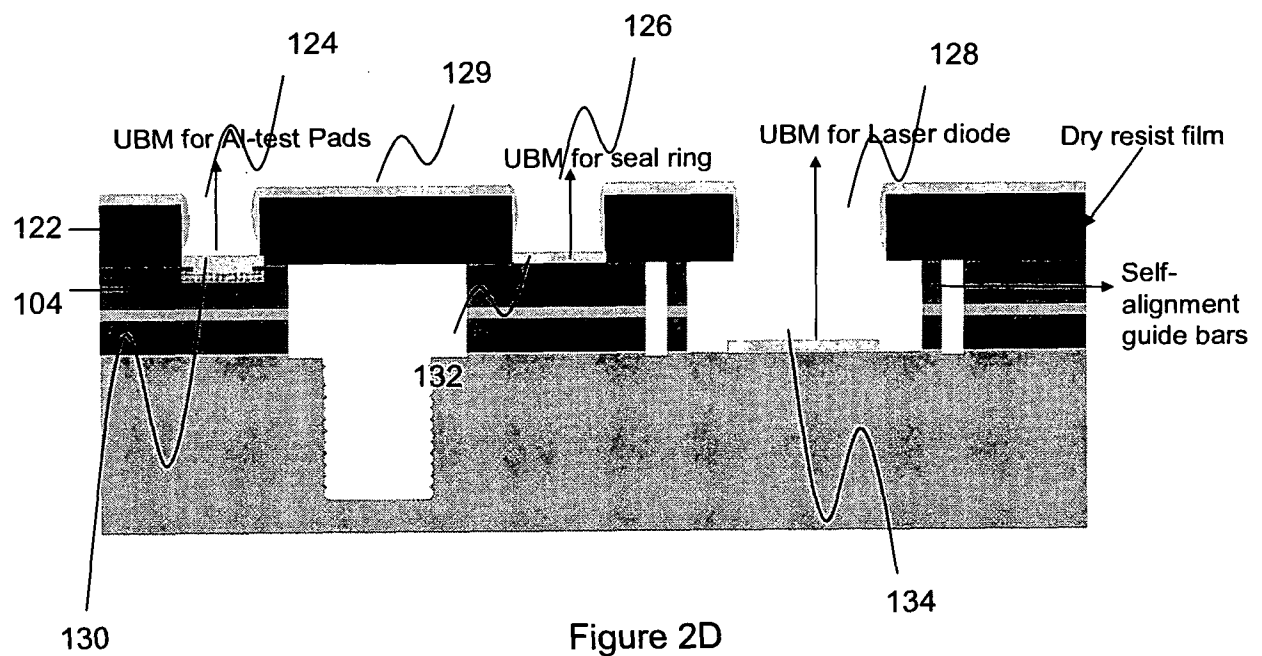


Figure 2D

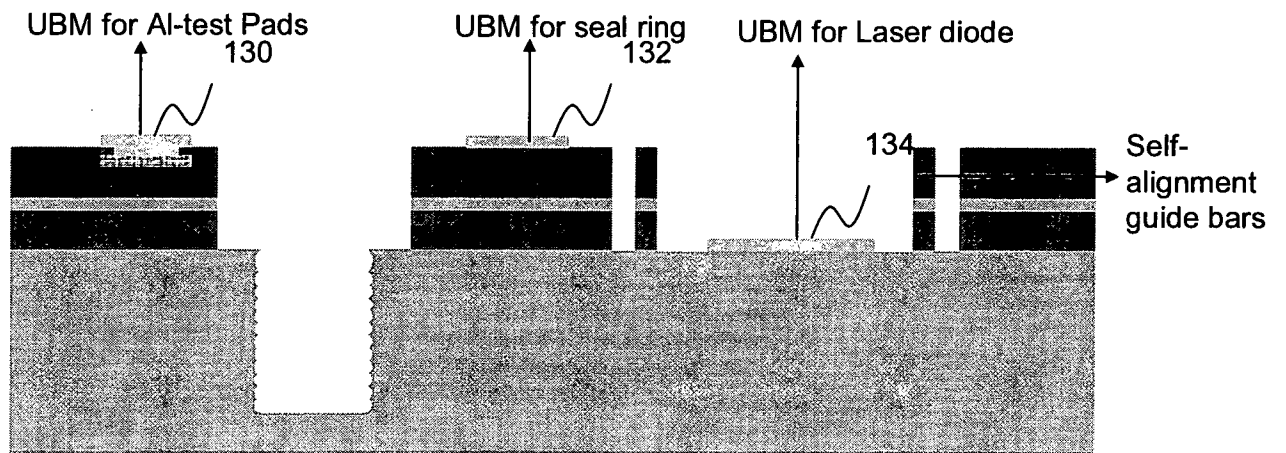


Figure 2E

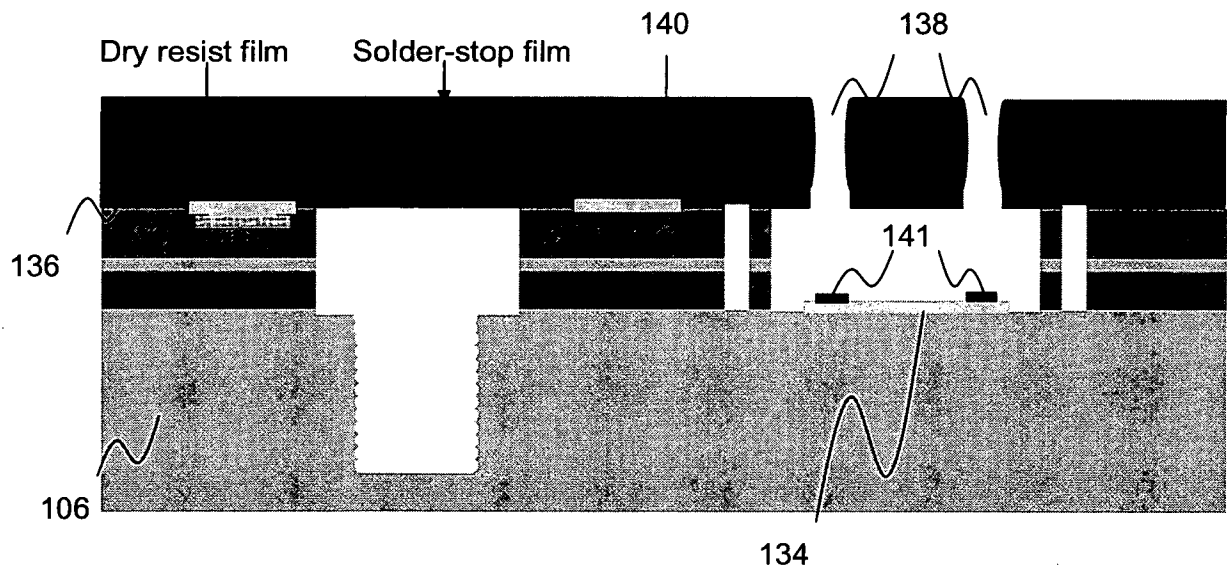


Figure 2F

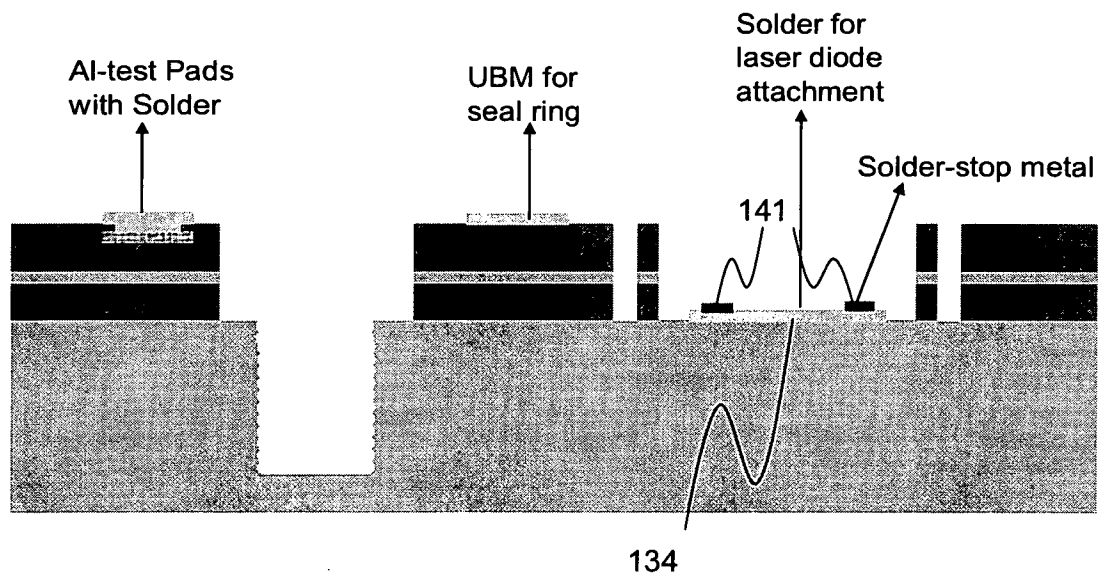


Figure 2G

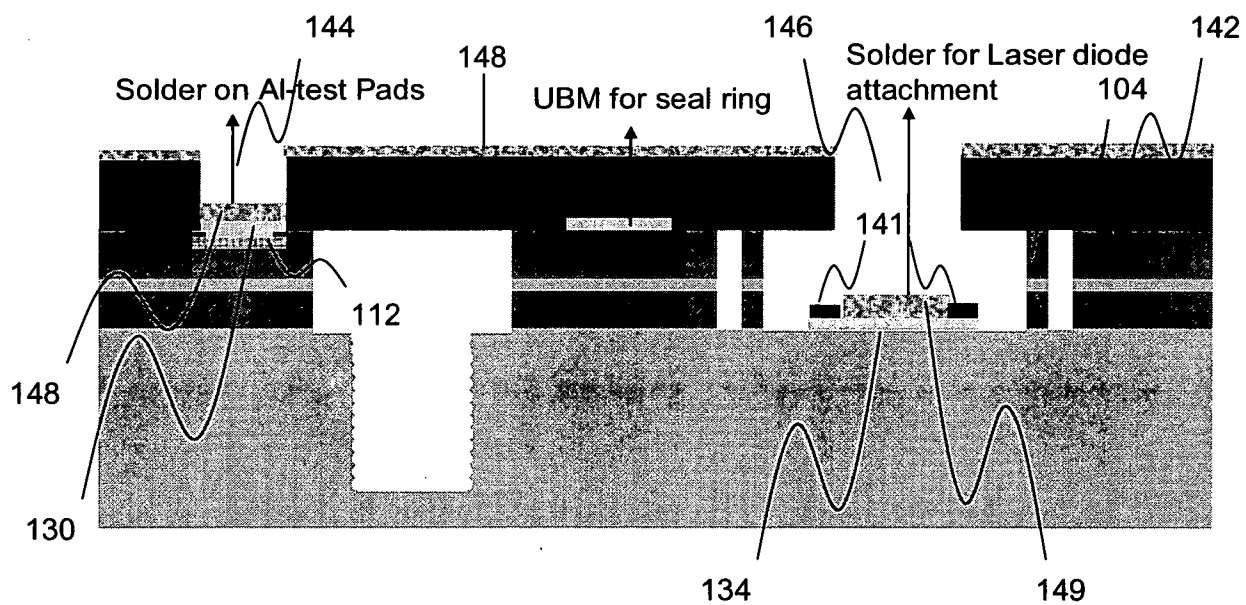


Figure 2H

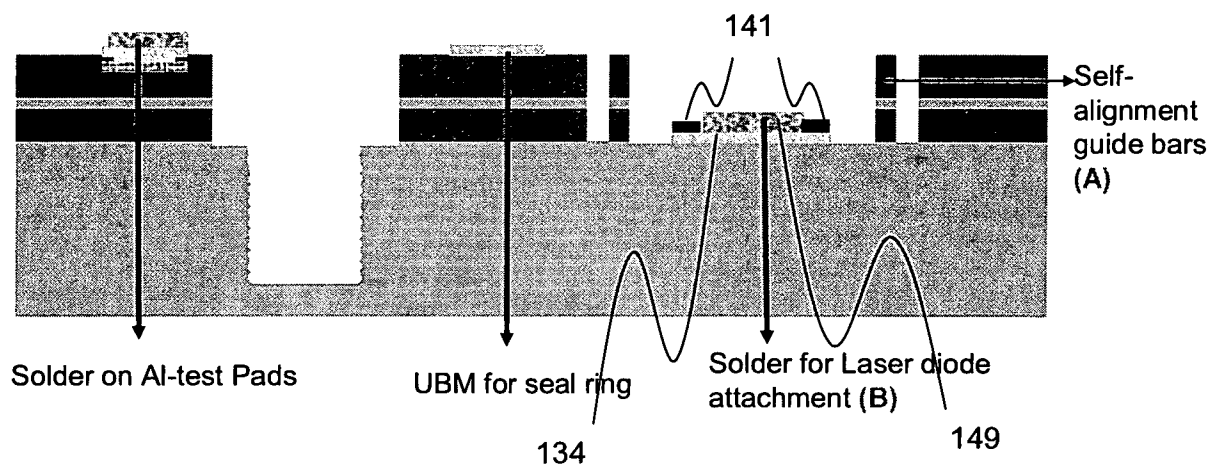


Figure 2I

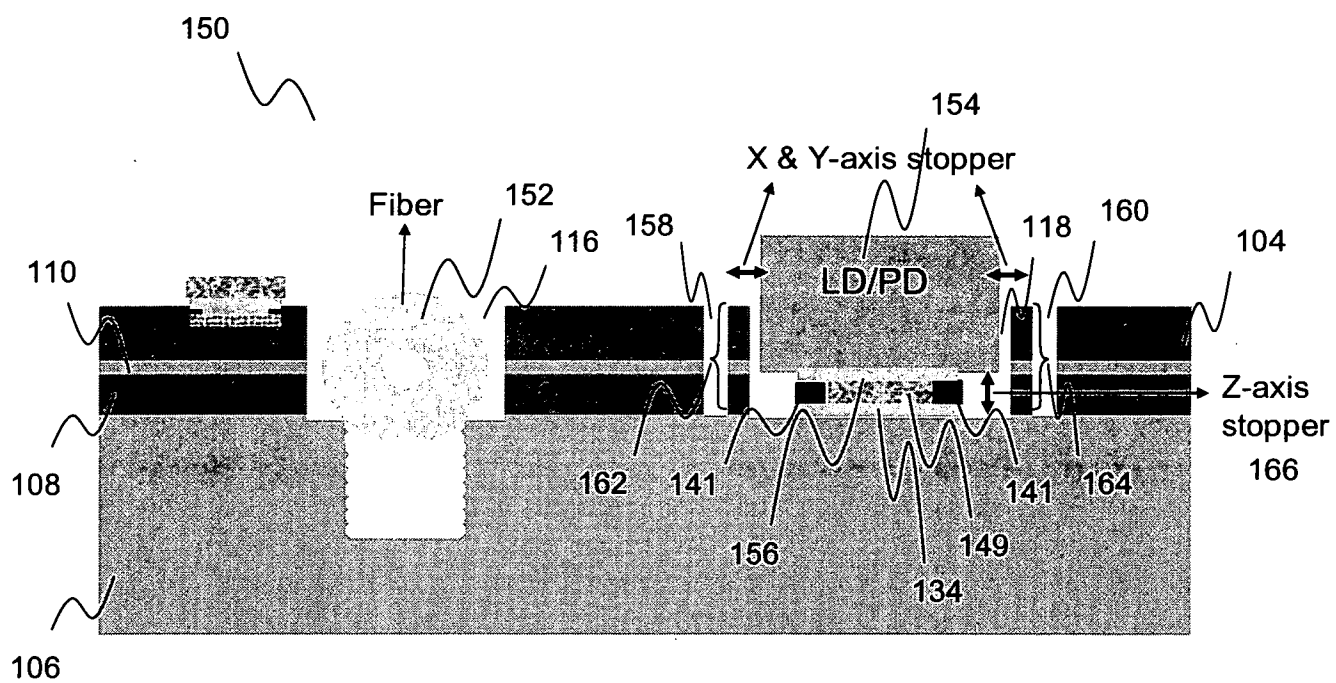


Figure 2J

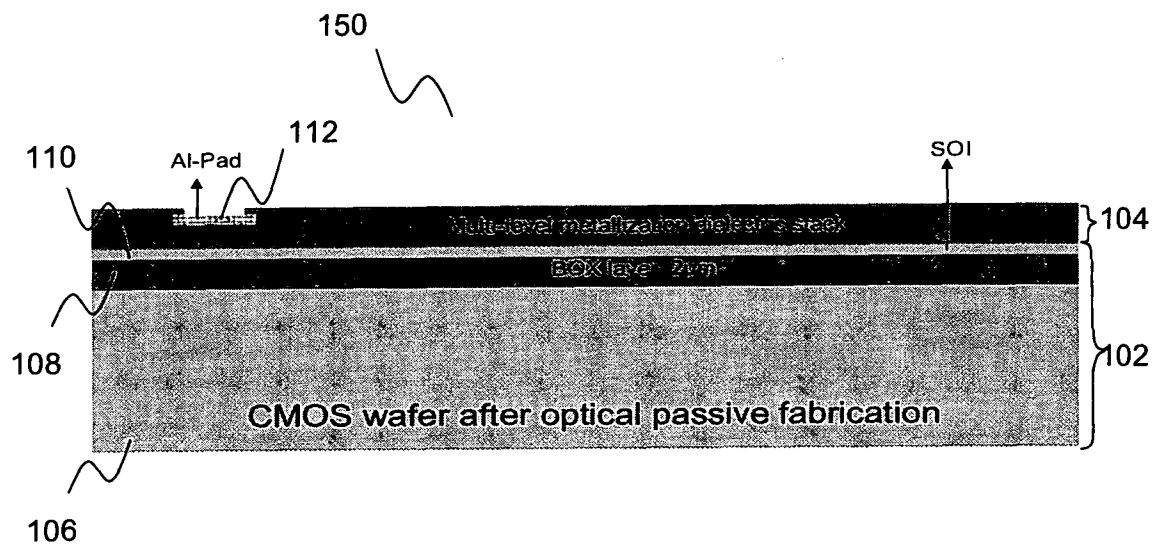


Figure 3A

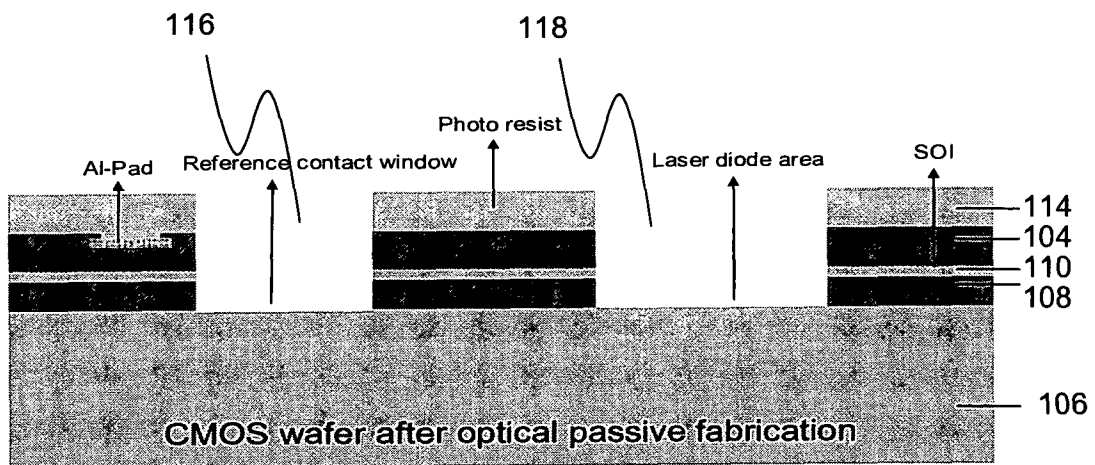


Figure 3B

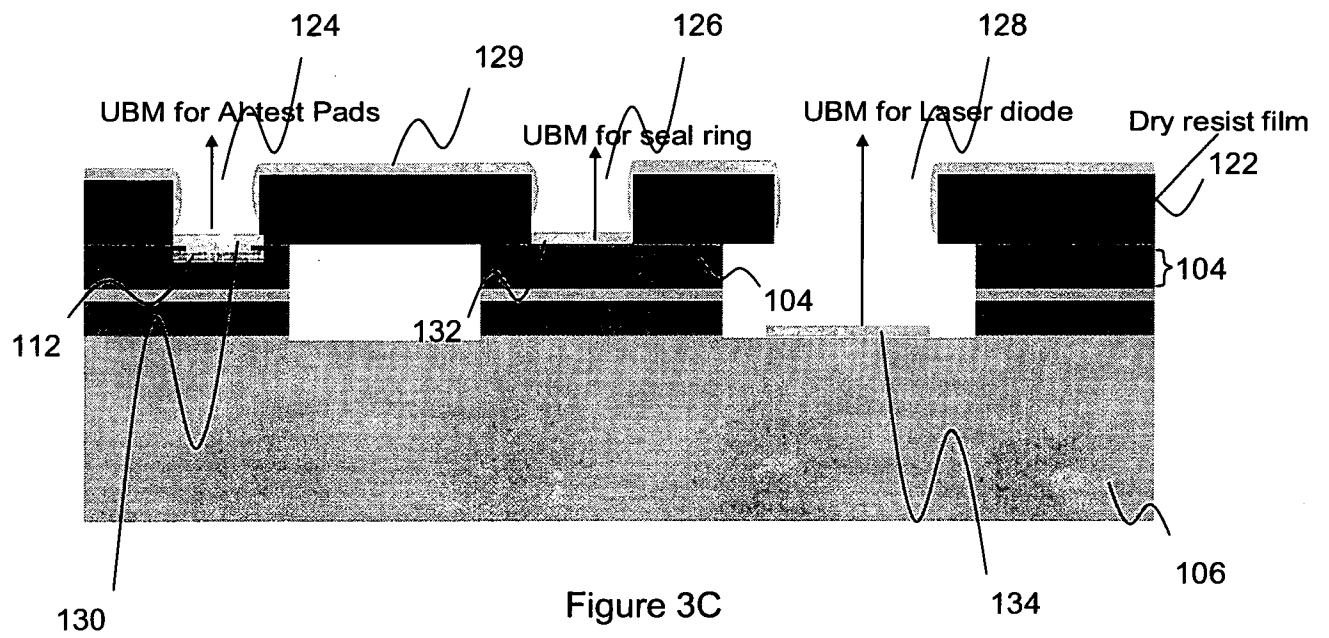


Figure 3C

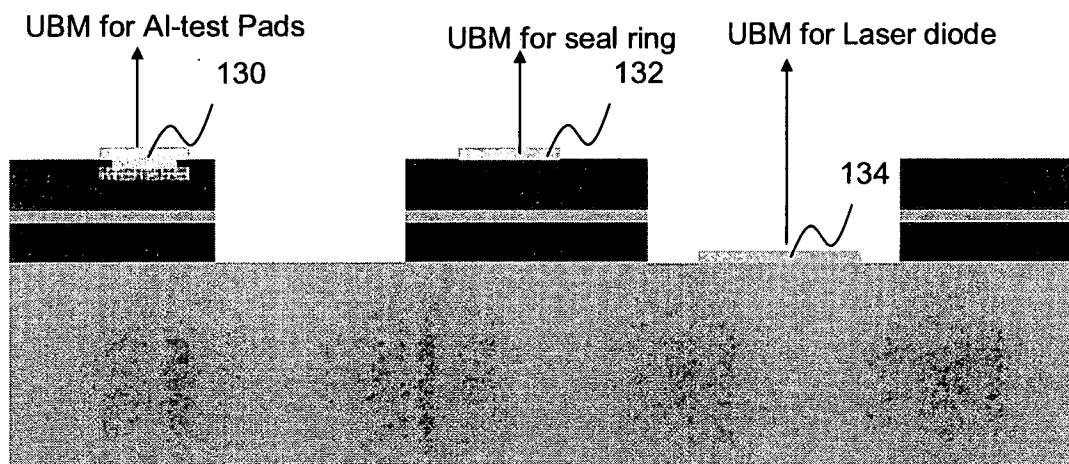


Figure 3D

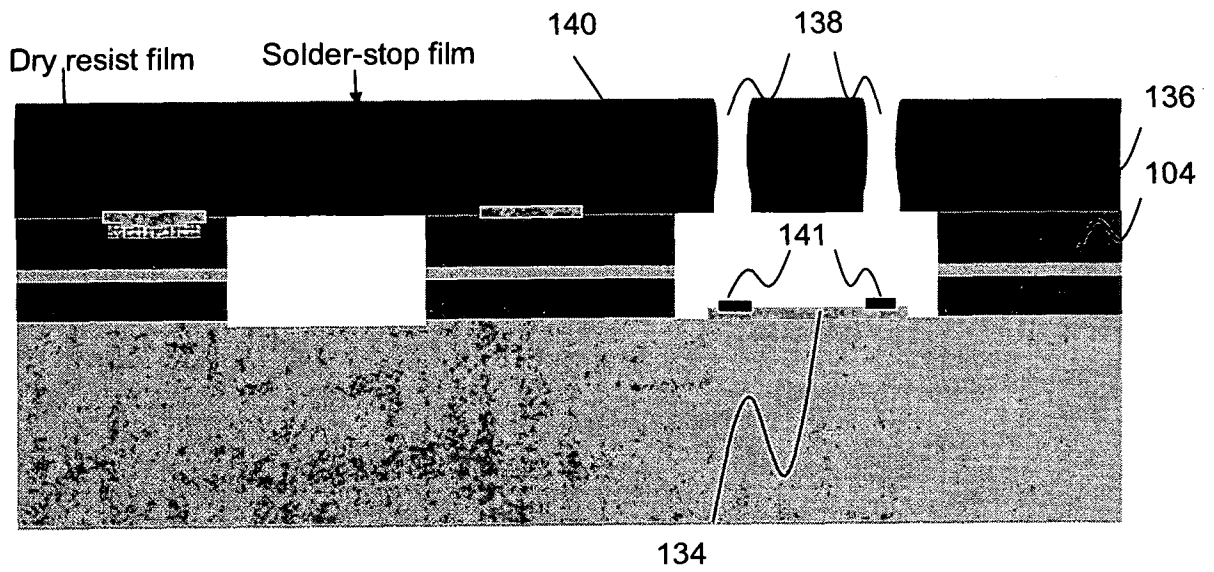


Figure 3E

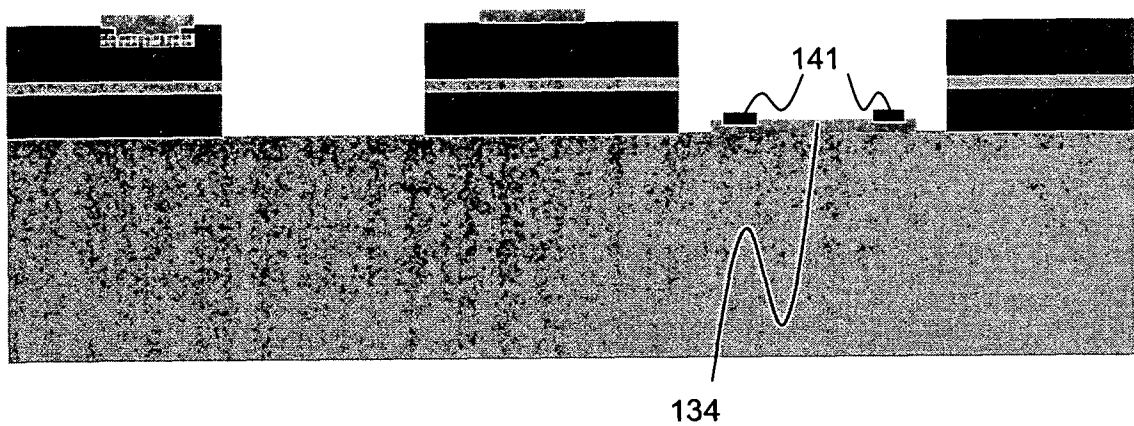


Figure 3F

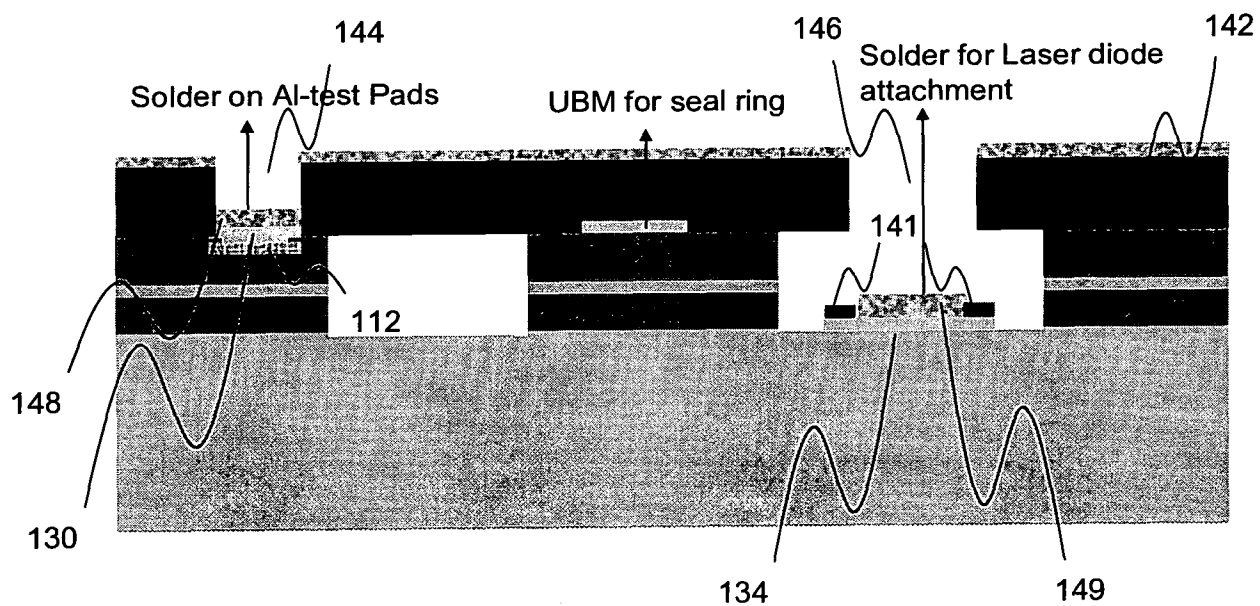


Figure 3G

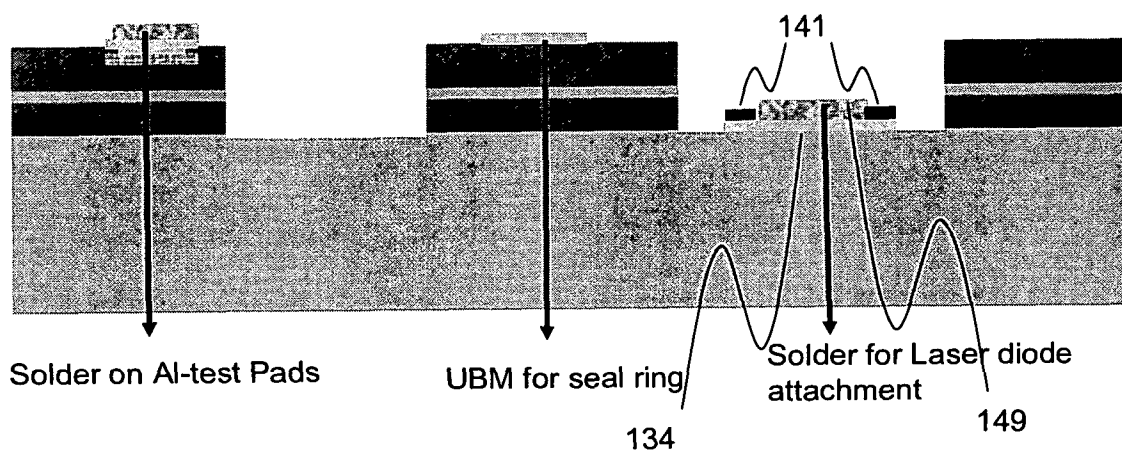


Figure 3H

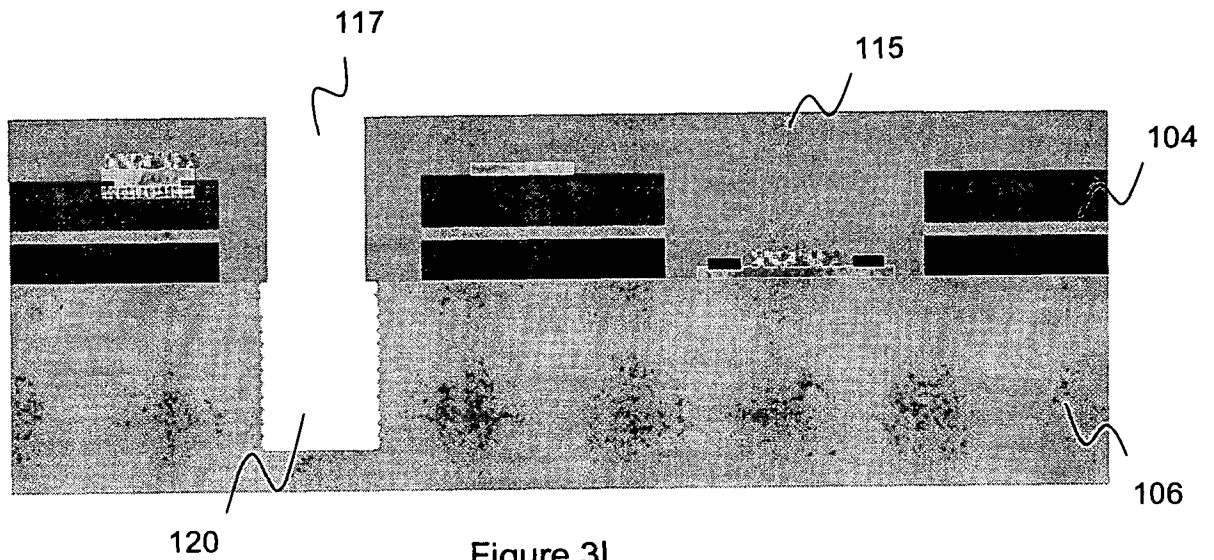


Figure 3I

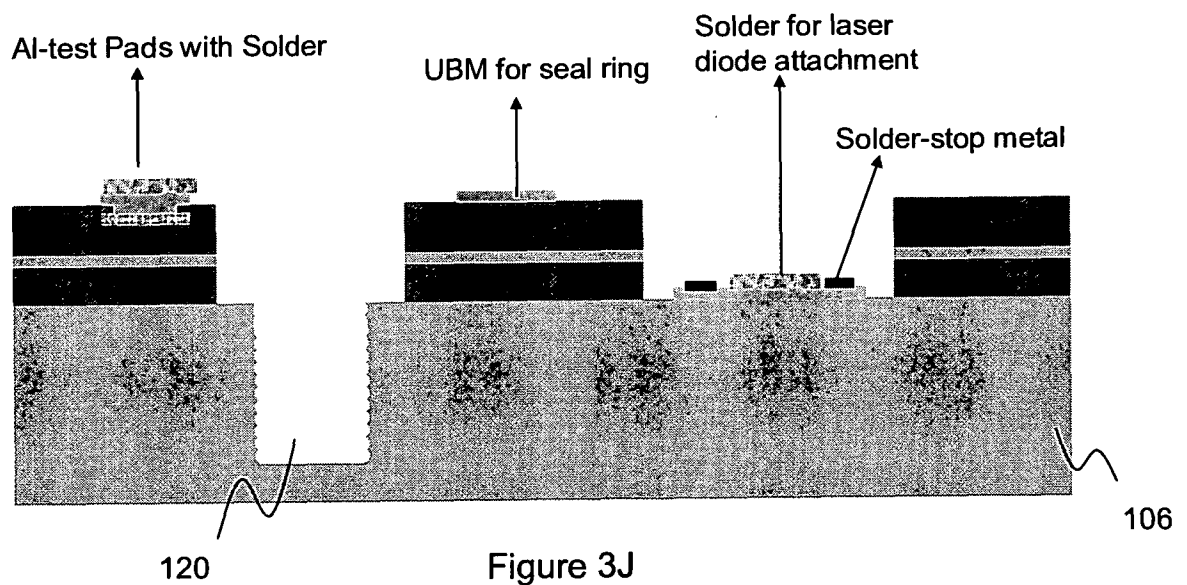


Figure 3J

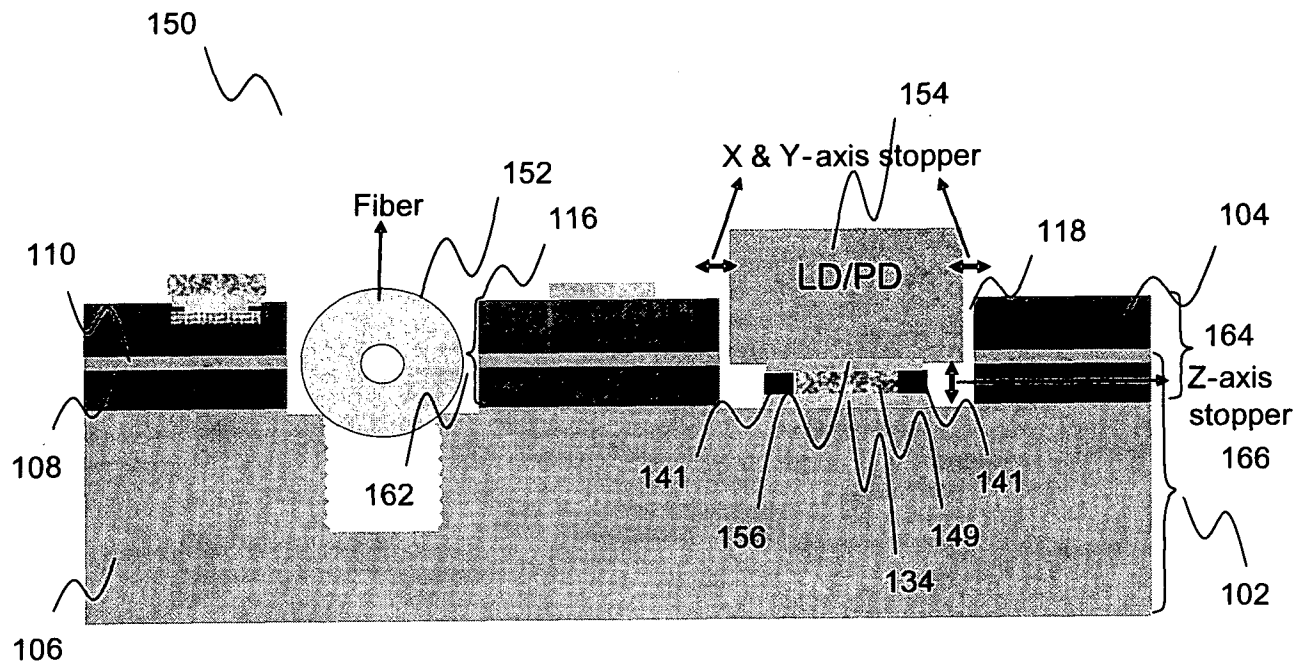


Figure 3K

Figure 4

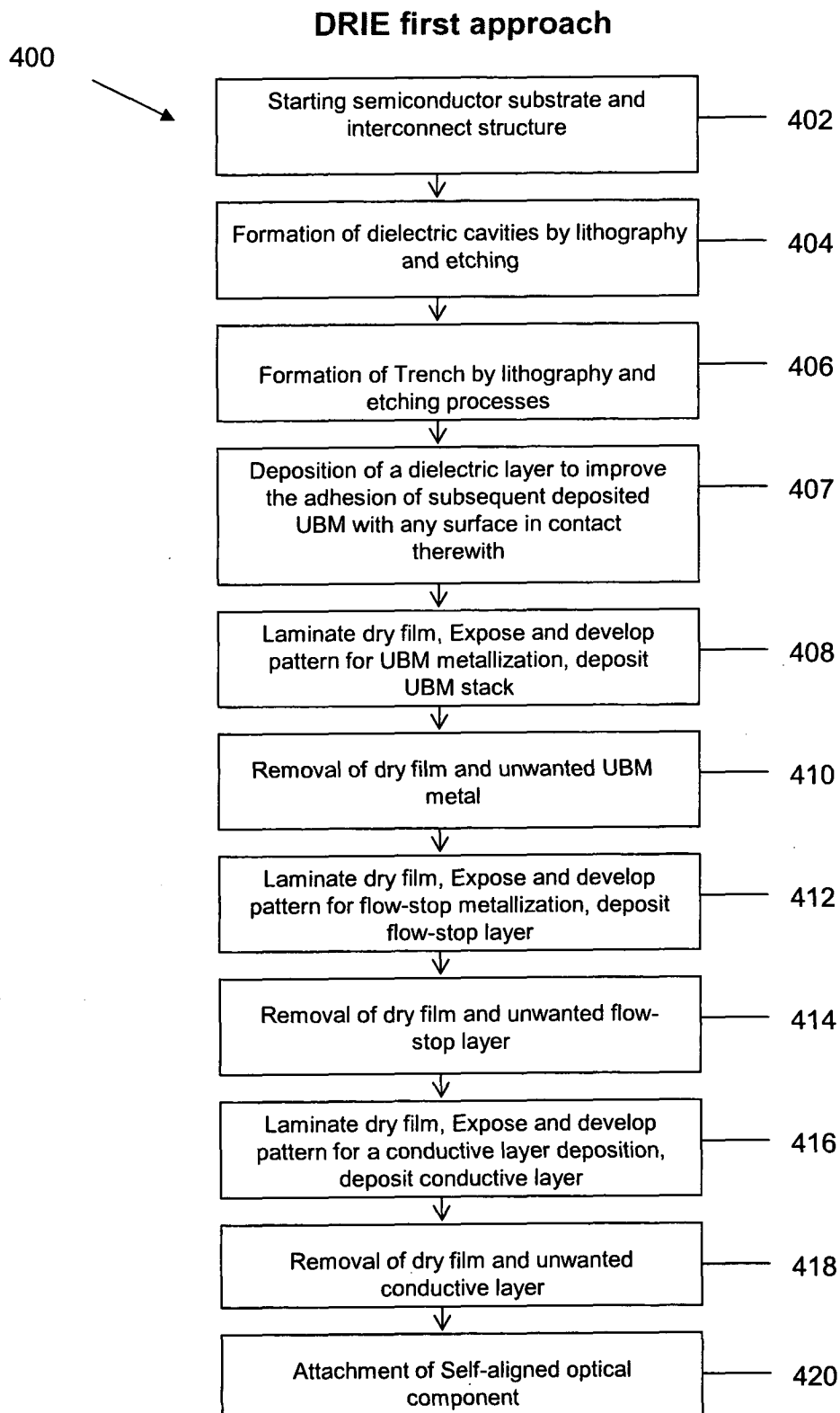


Figure 5

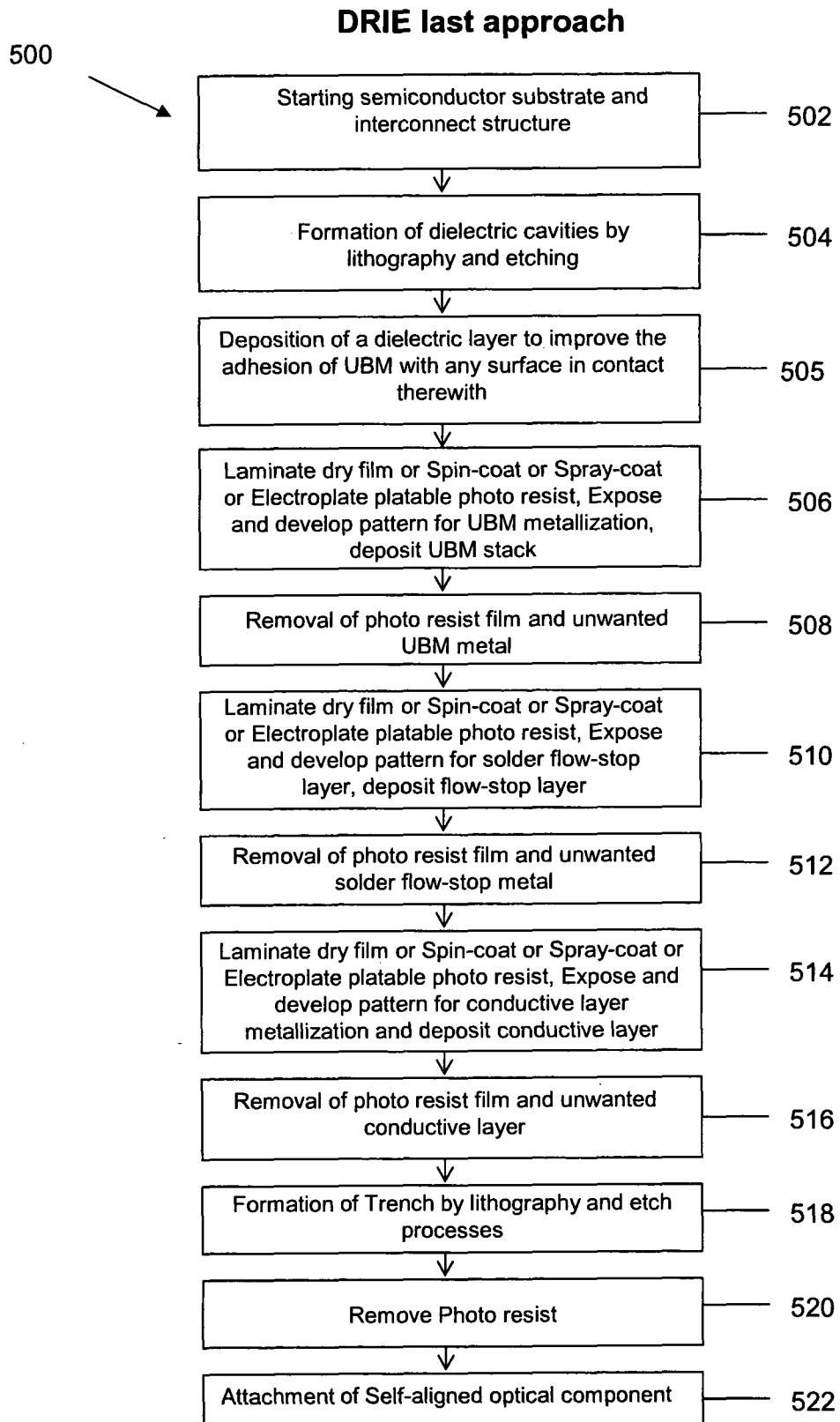
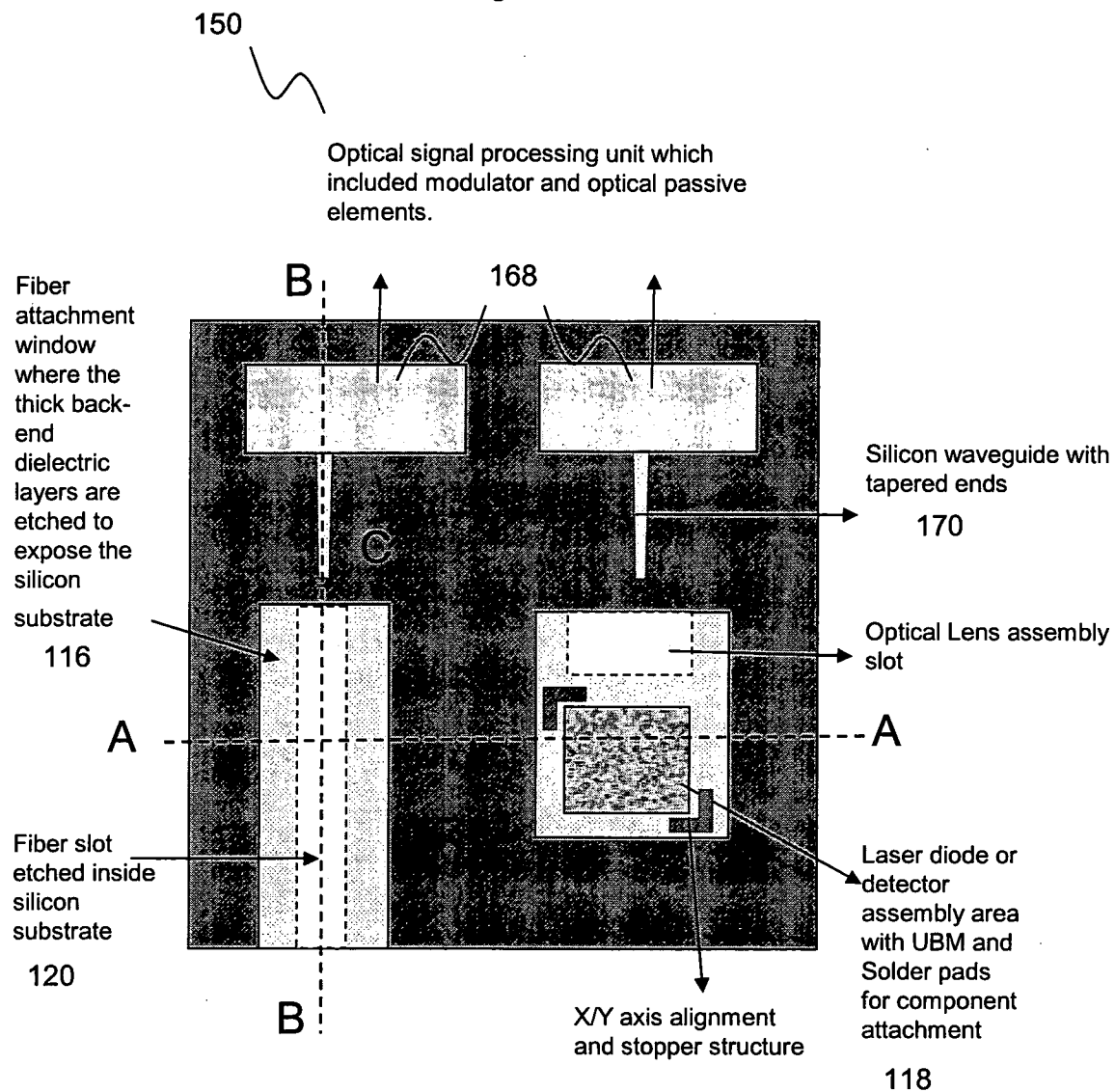


Figure 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000398

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

G02B 6/12 (2006.01)

H01L 27/14 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC: IPC H01L, G02B & Keywords: (substrate, wafer, base, silicon, SOI), (integrated circuit, IC, chip, die), (Inter connect, electrode, metallization, pad, dielectric stack, UBM), (cavity, hole, trench), (optical, fibre, diode, lens, laser or wave guide), (optical signal, optical processing, modulator)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0207016 A1 (PATEL ET AL.) 21 October 2004 Paragraphs 0041, 0046 and 0047, Figs. 3-5	1-15, 26-27, 29-32, 34-51, 61-62, 65-68 and 70-72
X	US 2006/0177173 A1 (SHASTRI ET AL.) 10 August 2006 Paragraphs 0026-0027, Figs. 5-6	1-6, 8-15, 26-27, 35- 42, 44-51, 61-62 and 71-72
A	WO 2007/082059 A2 (SIOPTICAL INC.) 19 July 2007	

☒ Further documents are listed in the continuation of Box C

☒ See patent family annex

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 10 November 2008	Date of mailing of the international search report 21 NOV 2008
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustalia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer JAYATI RAY AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3654

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000398

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6387720 B1 (MISHELOFF ET AL.) 14 May 2002	
A	US 2002/0196998 A1 (STEINBERG ET AL.) 26 December 2002	
A	US 2005/0201683 A1 (GHIRON ET AL.) 15 September 2005	
A	WO 2008/038921 A1 (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 3 April 2008	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2008/000398

This annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report				Patent Family Member			
US	2004207016	CA	2520972	CN	1784781	EP	1625615
		KR	20060003046	US	6968110	US	7118682
		US	2004240822	US	2005236619	US	2007000862
		WO	2004088396	WO	2004095112		
US	2006177173	CN	101128761	WO	2006084237		
WO	2007082059	CA	2636930	US	7415184	US	2007274630
US	6387720	CN	1371483	EP	1218788	WO	0144842
US	2002196998	US	6839474				
US	2005201683	CA	2555573	EP	1714174	KR	20060124721
		US	7013067	WO	2005077110		
WO	2008038921	NONE					
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.							
END OF ANNEX							