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(54) Title: SYSTEM AND METHODS OF SUBPIXEL RENDERING IMPLEMENTED ON DISPLAY PANELS

(57) Abstract: Various embodiments of a display system are disclosed. One embodiment comprises a panel having a set of drivers connected to a subpixel rendering circuit in which the number of data lines going to the drivers is less than the different number of color data sets generated by the subpixel rendering circuit. In another embodiment, the driver circuits and/or the subpixel rendering circuit are constructed on the panel, using the panel's thin film transistors.

**SYSTEM AND METHODS OF SUBPIXEL RENDERING IMPLEMENTED ON DISPLAY  
PANELS**

**BACKGROUND**

[01] In commonly owned United States Patent Application Serial No. 09/916,232 (“the ‘232 application” – herein incorporated by reference) entitled “ARRANGEMENT OF COLOR PIXELS FOR FULL COLOR IMAGING DEVICES WITH SIMPLIFIED ADDRESSING” as well as in commonly owned U.S. Patent Application No. 10/278,353 (“the ‘353 application” – herein incorporated by reference), entitled “IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH INCREASED MODULATION TRANSFER FUNCTION RESPONSE,” filed on October 22, 2002, and in commonly owned U.S. Patent Application No. 10/278,352 (“the ‘352 application” – herein incorporated by reference) entitled “IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH SPLIT BLUE SUBPIXELS,” filed on October 22, 2002, novel subpixel arrangements are therein disclosed for improving the cost/performance curves for image display devices.

[02] These subpixel arrangements achieve better cost/performance curves than traditional RGB striping systems -- particularly when coupled with subpixel rendering means and methods further disclosed in those applications and in commonly owned United States Patent Application Serial Number 10/051,612 (“the ‘612 application” – herein incorporated by reference) entitled “CONVERSION OF RGB PIXEL FORMAT DATA TO PENTILE MATRIX SUB-PIXEL DATA FORMAT”; and in commonly owned United States Patent Application Serial Number 10/150,355 (“the ‘355 application” – herein incorporated by reference) entitled “METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH GAMMA ADJUSTMENT”; and in commonly owned United States Patent Application Serial No. 10/215,843 (“the ‘843 application” – herein incorporated by reference) entitled “METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH ADAPTIVE FILTERING”.

[03] These novel subpixel arrangements and systems and methods of performing subpixel rendering thereon cuts across nearly every technology base for creating a display. In particular, liquid crystal displays (LCDs) are particularly well suited to these novel arrangements and methods – as the above mentioned technology sharply improves display performance by increasing or holding the same resolution and MTF with a reducing the number of pixel elements when compared with RGB stripe systems. Thus, manufacturing yields for high resolution LCD displays should improve utilizing this novel technology.

[04] It is known in the art of LCD display manufacturing to migrate row and column drivers – traditionally found on an IC driver circuit external to the active matrix display – onto the display itself. In polysilicon (e.g. low temperature poly silicon (LTPS)) active matrix displays, amorphous silicon active matrix displays or generally active matrix displays made with CdSe or other semiconductor

materials, additional thin film transistors (TFTs) are created onto the display itself that serve as driving circuitry for the display – thereby lowering the cost of the combined driver/display system. Figure 1A depicts a current conventional display system 100 that comprises a display panel 102 having row (104) and column (106) drivers comprising TFTs manufactured onto the panel. Separately, an integrated circuit (108a) – typically an application specific integrated circuit (ASIC) or field programmable gate array (FPGA) – accepts data input and may provide both timing or clocking of the data and outputting of the data and timing or clock signals to the panel.

[05] As for driver circuitry, it would be advantageous to leverage the cost savings of utilizing some processing capability of the TFTs on the panel to provide subpixel rendering processing (SPR) directly on the panel.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[06] The accompanying drawings, which are incorporated in, and constitute a part of this specification illustrate various implementations and embodiments disclosed herein.

[07] Figure 1A shows a conventional polysilicon or amorphous silicon LCD display system with row and column drivers integrated onto the panel.

[08] Figure 1B shows a polysilicon or amorphous silicon LCD display system with row and column drivers integrated onto a panel that includes external subpixel rendering that might be required for new pixel layouts.

[09] Figure 2 depicts one embodiment of a high level block diagram of the present invention with subpixel rendering processing circuitry constructed onto the panel.

[010] Figure 3 depicts another embodiment of a high level block diagram of the present invention.

[011] Figure 4A is one embodiment of the integrated SPR circuitry onto a display panel where the panel comprising a subpixel layout with at least one column having alternating color data.

[012] Figure 4B is an embodiment of a driver circuit suitable to drive data lines where there is alternating color data thereon.

[013] Figure 5A is another embodiment of the integrated SPR circuitry onto a display panel where the panel comprising a subpixel layout with at least one column having alternating color data.

[014] Figure 5B is another embodiment of the integrated SPR circuitry onto a display panel where the panel comprising a subpixel layout with at least one column having alternating color data.

[015] Figure 5C is an embodiment of a driver circuit suitable to drive data lines in Figure 5B.

[016] Figure 6A is yet another embodiment of the integrated SPR circuitry onto a display panel where the panel comprising a subpixel layout with at least one column having alternating color data.

[017] Figure 6B is an embodiment of the integrated SPR circuitry showing the multiplexing of two data channels.

[018] Figure 7 is yet another embodiment of the integrated SPR circuitry onto a display panel where the panel comprising another subpixel layout with at least one column having alternating color data.

[019] Figure 8 is yet embodiment of the integrated SPR circuitry onto a display panel where the panel comprising the subpixel layout of Figure 7.

### **DETAILED DESCRIPTION**

[020] Reference will now be made in detail to implementations and embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[021] Figure 1B depicts one embodiment of a system that might include SPR on a separate chip (108b). Such SPR might be provided to drive panels having new subpixel arrangements as detailed in several applications noted above and herein incorporated by reference.

[022] Figure 2 is one embodiment of a high level block diagram made in accordance with the principles of the present invention. Display system 200 comprises a display panel 202 – which further comprises row drivers 204 and a combined column driver and SPR circuitry 206 integrated into the panel using additional TFTs. The SPR function may include gamma pipeline (the ‘355 application), remapping filters (the ‘612 application), adaptive filtering (the ‘843 application), and clock frequency translator function. Tcon 208 provides timing control for the panel.

[023] Figure 3 is another embodiment of a high level block diagram of a suitable system. In this system, the SPR and column drivers are split into multiple units 206A, 206B (etc. for as many other units, as is suitable). The units effectively break the panel into blocks so that the required speed of the incoming data needing to be rendered on the display is matched against the performance of the display.

[024] Figure 4A is one embodiment of the integrated SPR circuitry onto a display panel where the panel comprising a subpixel layout as described in the ‘353 application. Panel 400 comprises an eight subpixel repeat pattern in which the green subpixels 402 are twice as numerous as, the blue 406 and red subpixels 404. Although shown as the same size in Figure 4A, the green subpixels 402 can be narrower than the blue 406 and red subpixels 404, as disclosed in the ‘353 application. Driver circuitry 408 is coupled to the column data lines of the panel. As can be seen, every other column lines of subpixels comprises alternating red and blue subpixels. As such, one embodiment of a driver circuit 410 for such a R/B line is shown in Figure 4B. Driver 410 accepts two data paths for the red and blue data input. Mux 426 accepts this red/blue data and, depending on which data is being clocked in, sends appropriate red and blue data to latch 420. Data is transferred to memory 422 during the interval

between lines of data. D/A converter 424 does the appropriate conversion of data to a format suitable for driving individual pixels in a column. Driver 412 for the green data would not require a MUX.

[025] As is the case in Figure 4A, if the subpixels of the panel have different widths and/or dimensions, it may be advantageous to construct the driver TFT for the bigger subpixels larger than those driving subpixels of smaller size and dimensioning. The driver TFT is larger because it must supply higher currents to drive the larger capacitance of the larger pixels.

[026] The red, green and blue SPR data is accomplished by SPR circuitry 421. It will be appreciated that SPR circuitry 421 could be constructed either on the panel similar to the driver circuitry 408, or could reside in a chip connected to the panel. SPR circuitry 421 further comprises red (424), green (426), and blue (428) SPR circuitry that would implement the various subpixel rendering methods - in accordance with the various patent applications incorporated herein, or any of the known subpixel rendering routines.

[027] Figure 4B shows the driver architecture in a typical panel with integrated drivers. Data from SPR blocks are transferred to individual circuit blocks. In the case of green, the data is transferred directly to latch 420. Red and blue data are transferred to MUX 426 at half the clock frequency of green data. MUX 426 selects one of the data paths depending on which row is being addressed by row driver block. After the MUX, the data flow is the same for red, green, and blue data. It passes down to latch 420 then to memory 422 and out from D/A 424.

[028] Figure 5A is another embodiment of the integrated SPR circuitry onto a display panel. In this embodiment, there is one data path on which all R,G, and B data is transmitting. Data from red, green and blue SPR are being selected by data selector (or MUX) 502 so that for one line being rendered, the data is read out as GRGBGRGB and the next line is read out as GBGRGBGR and repeated. The data frequency could be 1.5 times higher than the incoming frequency, but the number of data paths is cut from three lines to one line.

[029] Figure 5B shows an alternative data flow where data from the three separate SPR blocks are transmitted on three separate data paths. As shown, the incoming data frequency into the SPR circuitry is at a certain frequency ( $f_c$ ). In one embodiment, the data frequency out of the green SPR could be clocked at the same frequency,  $f_c$ , while data frequency out of the red and blue SPR could be clocked at half that frequency,  $f_c/2$ .

[030] Figure 5C shows a suitable driver circuit which would service both the green and the red/blue columns. Driver 504 might comprise latch 506, memory 508 and D/A 510 elements. In all cases, the data from the SPR block is transmitted in digital or analog form to a latch (digital) or sample and hold circuit (analog) during one display line time. In the case of digital data, the number of parallel lines, indicated by the slash mark, is equal to the resolution of the panel. For example, a 6 bit panel (64

levels) will have 6 parallel lines. Before the next line of data is present (retrace time), the data is transferred to a second memory 508 (for green data). For red and blue data, this data is sent to a MUX/Memory component 512, that would select the appropriate red or blue data and store it into memory. MUX/Memory 512 could be implemented as one component or separately. During the next line time, the data is transferred to the column lines directly (for analog) or through a digital to analog (D/A) converter. While the data is transferred to the column lines of the display, new data is read into the latches 506.

[031] Figure 6A is yet another embodiment of the integrated SPR circuitry onto a display panel. In this embodiment, data selector 502 inputs red and blue data from the respective SPR units and outputs the appropriate data for proper rendering to the panel. In this case, there would be no need for a different driver circuit 604 for green, red/blue subpixel columns. It will be appreciated that, like the SPR circuitry, data selector 502 could be constructed onto the panel itself, or reside off panel in a suitable chip. Figure 6B shows the details of the data selector 502 implemented as a MUX circuit 602. The clock frequency of red/blue data is equal to green data after the MUX, but there are only two data paths to the column driver circuits.

[032] Figure 7 is yet another embodiment of the integrated SPR circuitry onto a display panel. In this embodiment, the display panel 702 comprises another unique subpixel arrangement as described in the '232 application. In this case, blue data is passed down an entire column, while the red/green data alternate down a next column. Thus, the SPR circuitry for Figure 7 might parallel the circuitry shown in Figure 5A, except the roles of blue and green data are different. In one embodiment, the data clock, running at a frequency,  $f_c$ , is input into the R, G, and B SPR circuitry. The data that is output might run at  $f_c/2$ , which is then input into data selector 502. The output of data selector 502 might run at  $3f_c/2$ , which in turn is input into the driver circuits. Thus, while the number of data lines have been reduced from three lines down to one line, the data clock rate going to the panel is 50% higher than running into the SPR. This tradeoff might be important for smaller displays where the dot clock can be run slower.

[033] Similarly, Figure 8 would be the parallel of Figure 6, except the roles of blue and green data are different. In this case, the number of data lines to the panel are two line, as opposed to three lines. Data selector 802 would switch red and green data appropriately according to the row being written. It should be appreciated that the principles of these embodiments apply to any display whereby at least one column alternates between two or more colors and that the scope of the present invention contemplates application of such principles.

[034] Although the foregoing embodiments have been described as having particular advantage with certain parts of the driver and/or SPR processing circuitry as being implemented on the panel itself with its TFTs, the same circuitry and architecture could be implemented off the panel entirely. The advantage would still remain in reducing the number of data lines going into the panel itself with the

application of the data selector circuit as described.

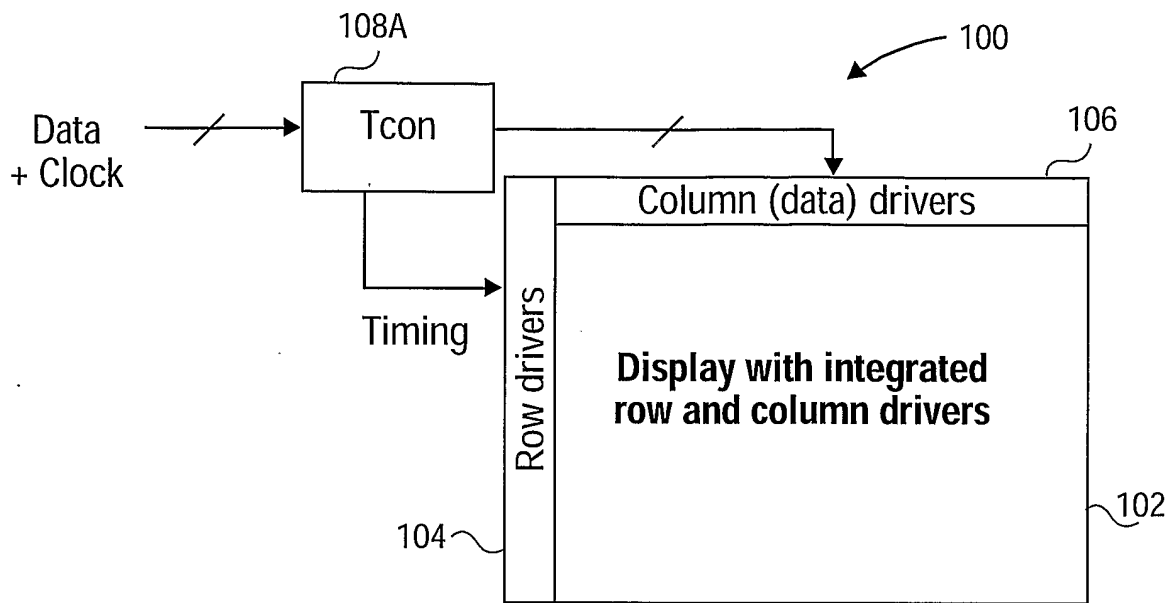
[035] While the invention has been described with reference to exemplary embodiments, it will be understood that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

CLAIMS

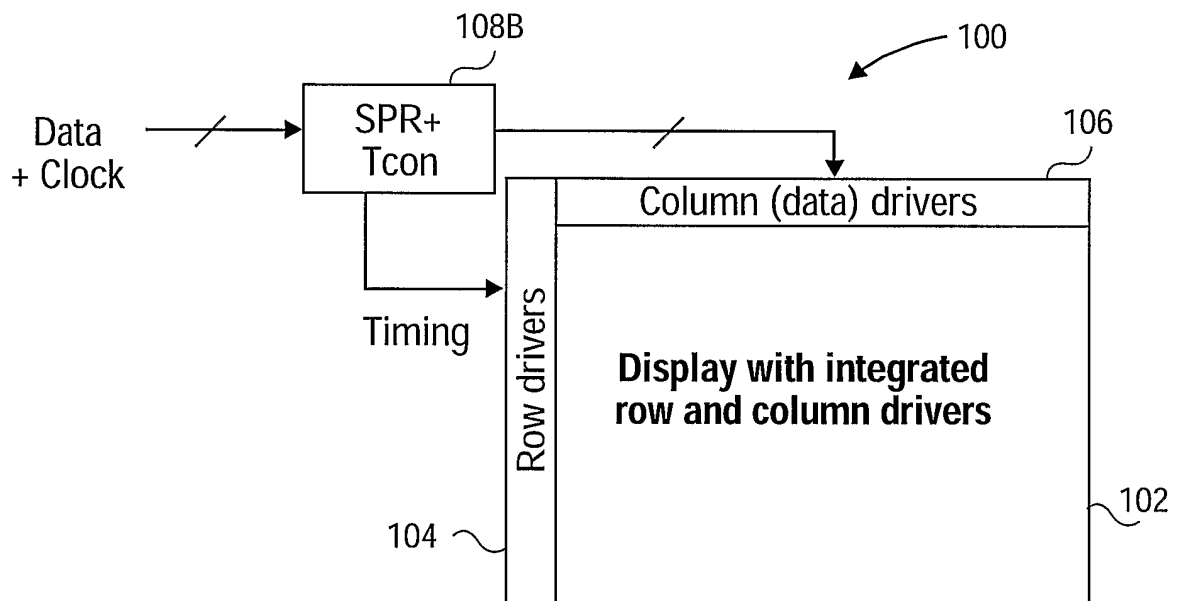
What is claimed is:

1. A display system comprising: a panel, said panel comprising a repeating subpixel grouping, each subpixel comprising one of a group, said group comprising a first color subpixel, a second color subpixel and a third color subpixel; said subpixel grouping comprising a plurality of columns wherein at least one said column further comprising an alternating pattern of subpixels of said first color and subpixels of said second color, said subpixel grouping further comprising at least one said column of subpixels of said third color; a set of drivers coupled to said columns of subpixels; a subpixel rendering circuit coupled to said drivers, said subpixel rendering circuit to output first color data, second color data, and third color data to said first color subpixels, said second color subpixels, and said third color subpixels respectively; and wherein said first color data, said second color data, and said third color data are for output to said set of drivers with less than three data lines.
2. The display system as recited in Claim 1 wherein said system further comprises: a data selector to input said first color data and said second color data on a first input data line and a second input data line respectively; and wherein said data selector is to output a serial stream of first color data and second color data on a first output data line.
3. The display system as recited in Claim 1 wherein said system further comprises: a data selector to input said first color data, said second color data, and said third color data on a first input data line, a second input data line, and a third input data line respectively; and wherein said data selector is to output a serial stream of first color data, second color data, and third color data on a first output data line.
4. The display system as recited in Claim 1 wherein said panel comprises a liquid crystal display panel and said drivers are constructed on said panel with said panel's thin film transistors.
5. The display system as recited in Claim 1 wherein said panel comprises a liquid crystal display panel and drivers and said subpixel rendering circuit are constructed on said panel with said panel's thin film transistors.

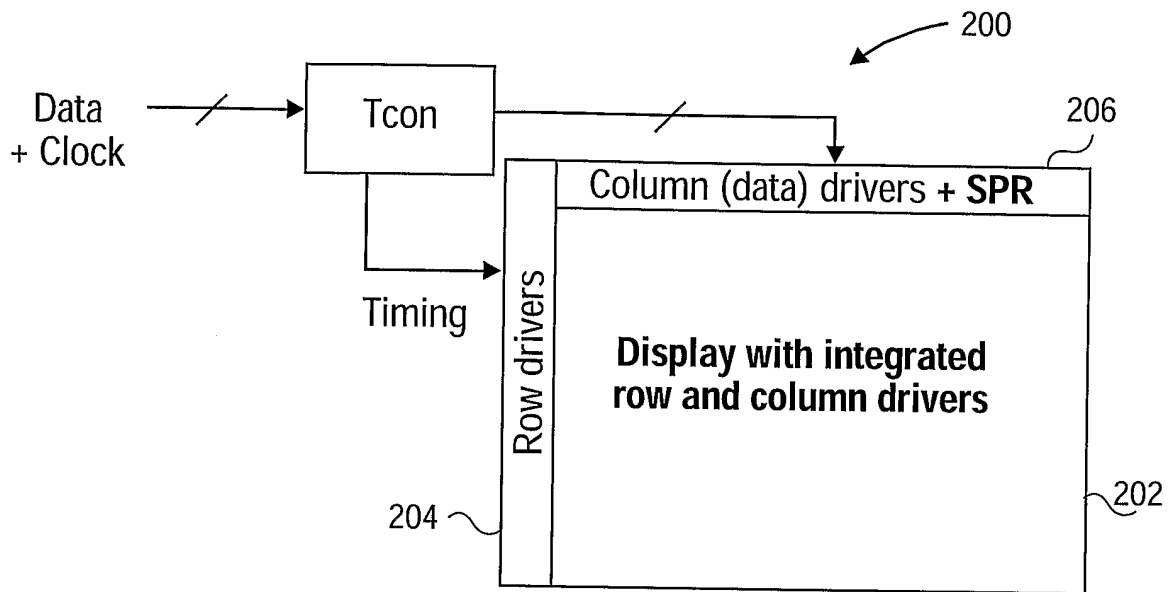




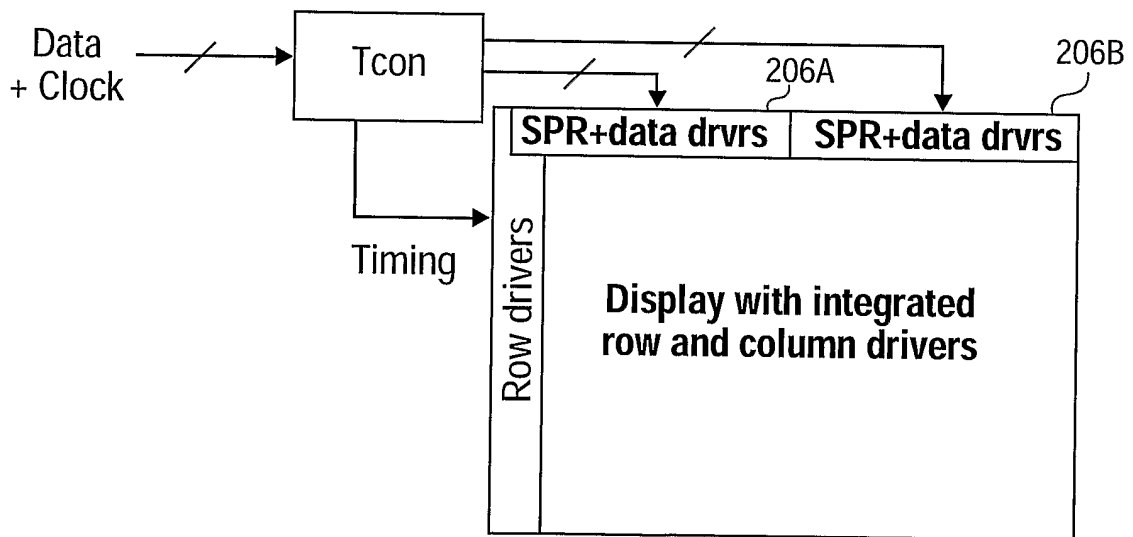
**FIG. 1A**  
(PRIOR ART)



**FIG. 1B**

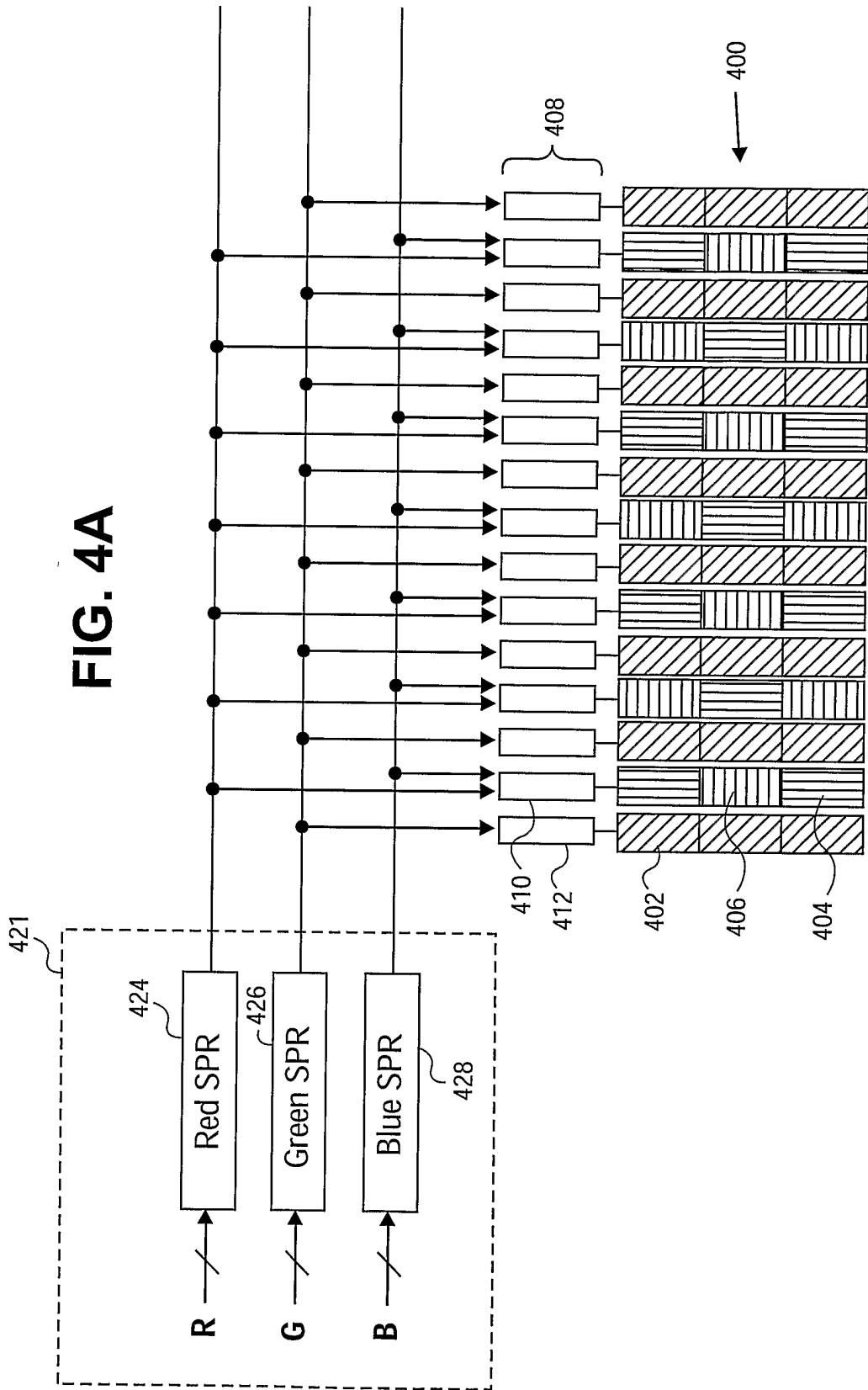


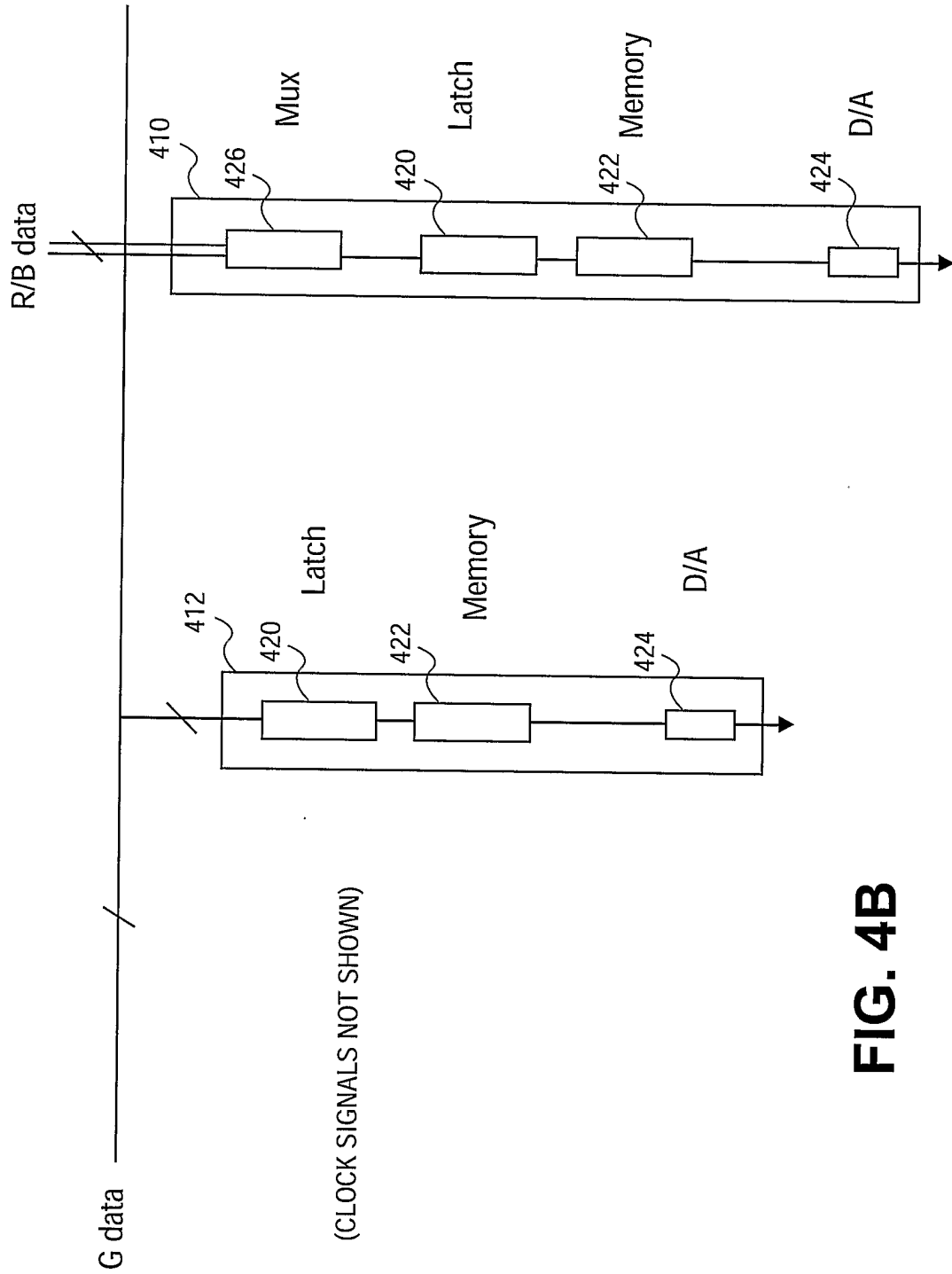
**FIG. 2**



**FIG. 3**

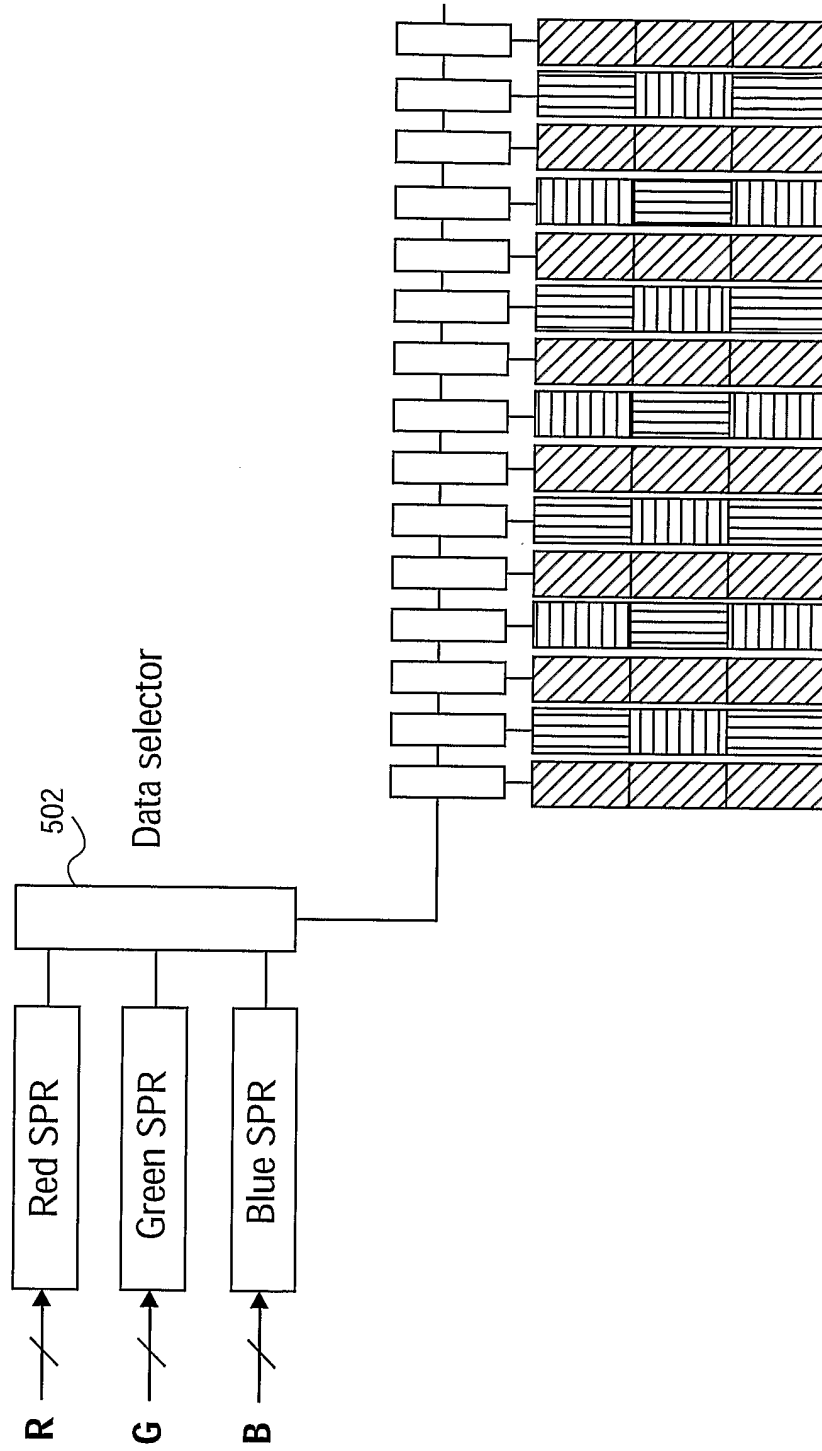
FIG. 4A

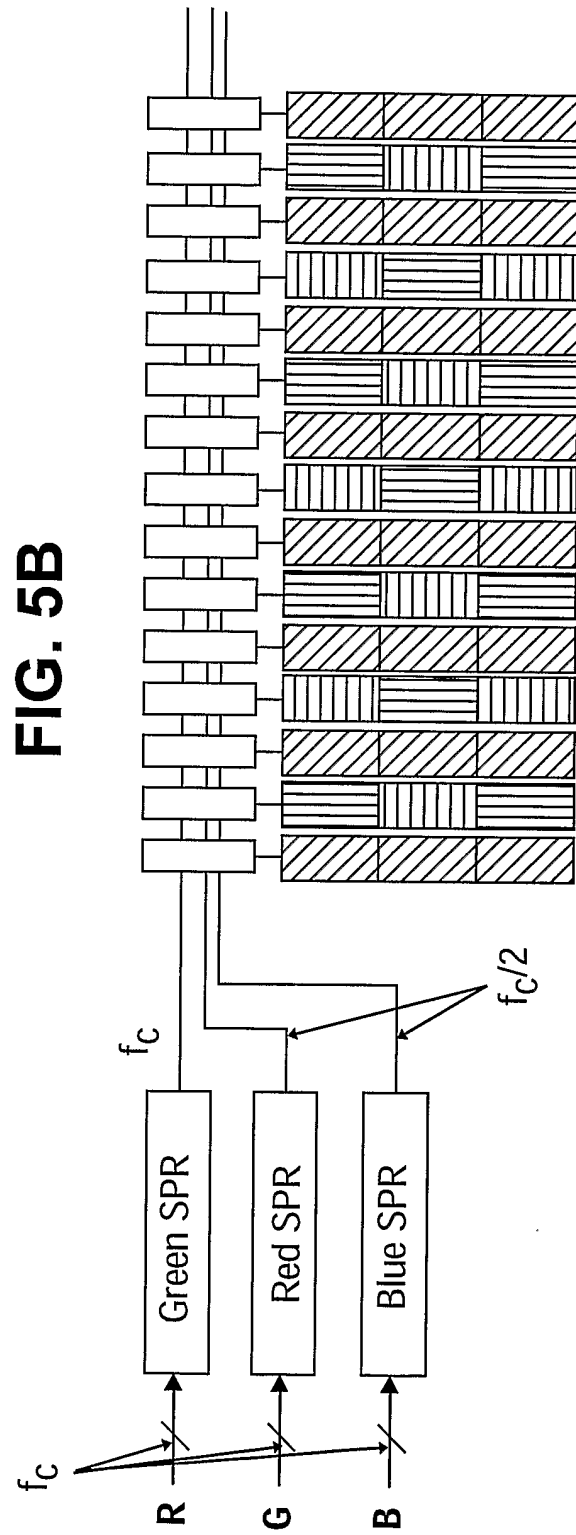




**FIG. 4B**

FIG. 5A





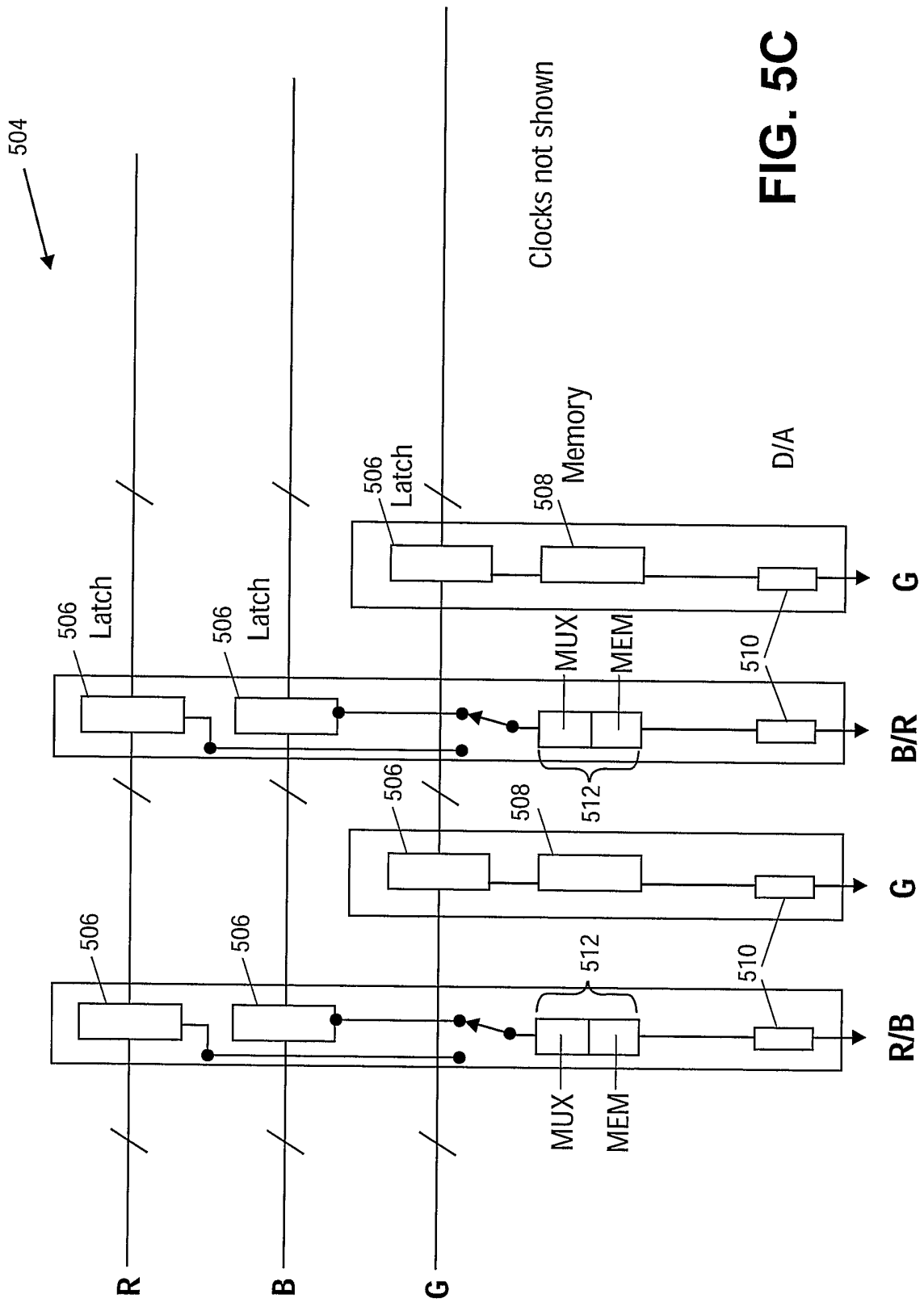


FIG. 5C

FIG. 6A

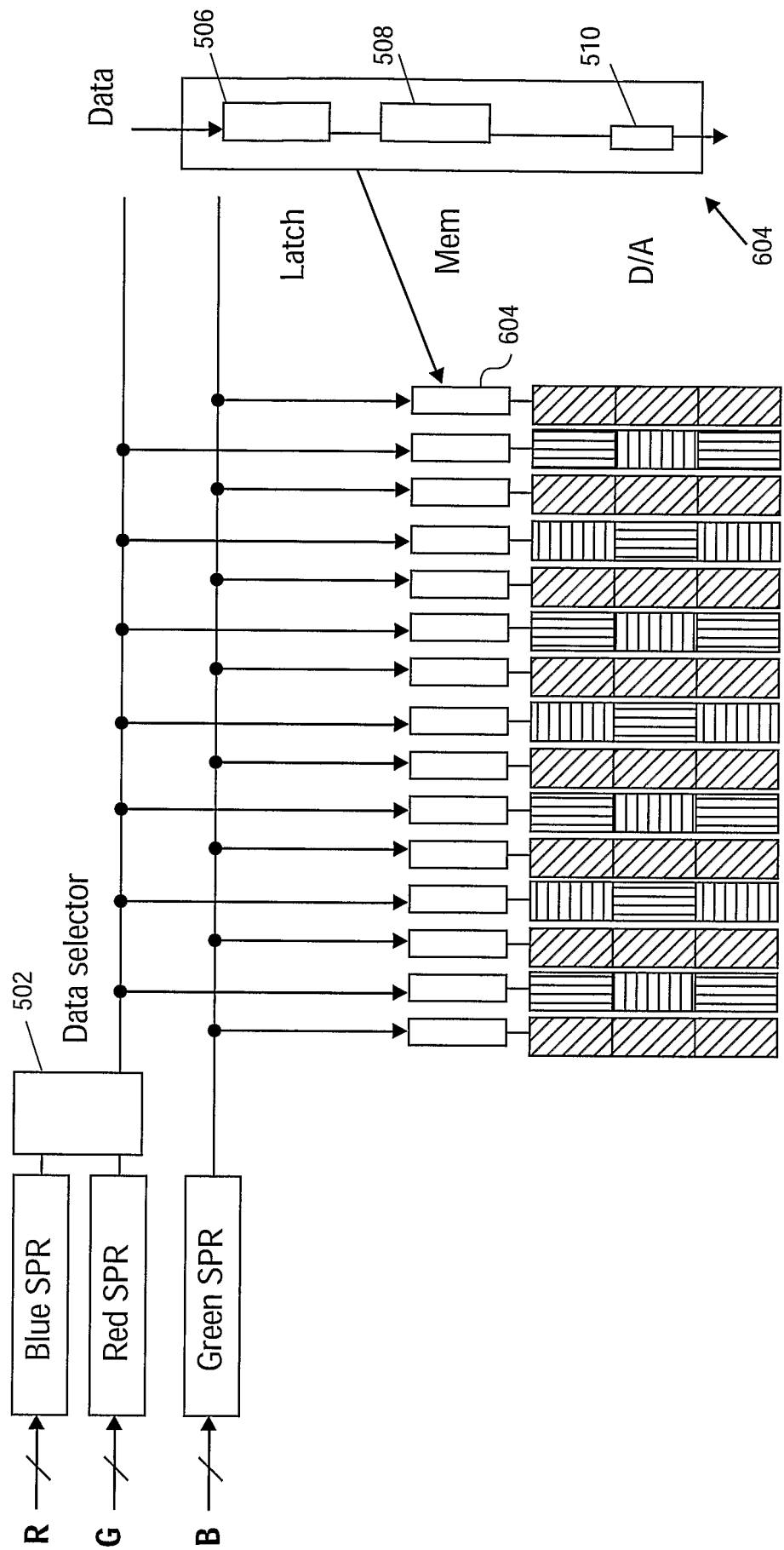




FIG. 6B

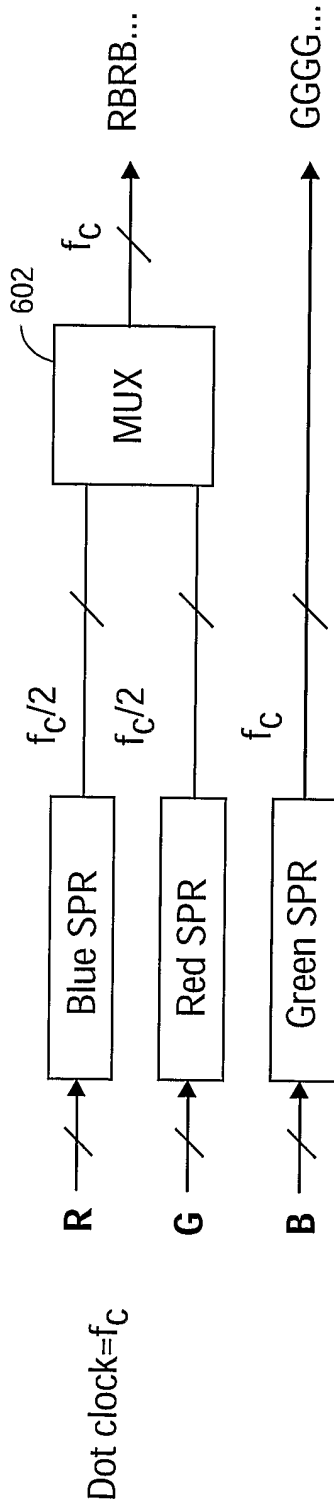


FIG. 7

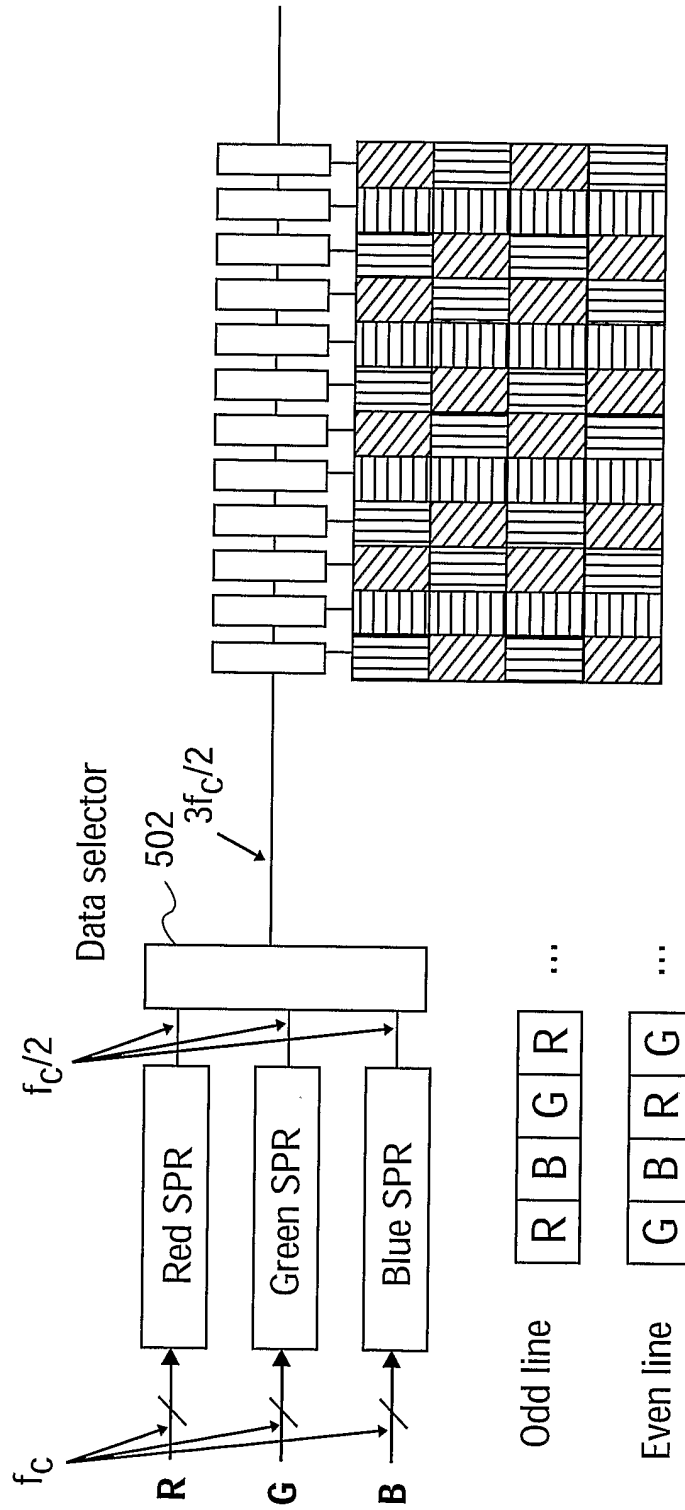


FIG. 8

