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(54) Title: HIGH TEMPERATURE THERMOPLASTIC SUBSTRATE HAVING A VACUUM DEPOSITED SOLDERABLE ELECTRICAL CIRCUIT PATTERN AND METHOD OF MANUFACTURE

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![Diagram of a high temperature thermoplastic substrate with solderable electrical circuit pattern](image-url)

(57) Abstract

To manufacture an electrical circuit pattern on the surface (102A) of a high temperature thermoplastic (such as polyetherimide) substrate (102), the substrate is prepared by creating a reactive surface suitable for bonding an electrical conductor (104) to the surface of the substrate. There are two methods of surface preparation. In the wet method, the substrate is boiled in hydrogen peroxide, while in the dry method, the substrate is sputter etched in an argon or argon-oxygen atmosphere. A base layer (106) of nickel, chromium or nickel-chromium is then vacuum deposited over the reactive surface of the substrate. Next, a solderable layer (108) of copper is vacuum deposited over the base layer. An electrical circuit pattern is then formed from the base and solderable layers using photolithographic techniques.
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HIGH TEMPERATURE THERMOPLASTIC
SUBSTRATE HAVING A VACUUM
DEPOSITED SOLDERABLE ELECTRICAL
CIRCUIT PATTERN AND METHOD OF MANUFACTURE

BACKGROUND of the INVENTION

This invention pertains to printed circuits, and more particularly to a manufacturing process for producing printed circuits on high temperature thermoplastic substrates by vacuum deposition.

There are a number of thermoplastic materials that can be molded or otherwise formed into shapes of printed circuit substrates. To be a suitable material for a printed circuit substrate, however, the material must be able to withstand the temperatures that result from soldering. When ordinary tin/lead solders are used, the substrate must be able to withstand temperatures in the region of 200°-230°C. If low temperature solders are used, however, the substrate needs to withstand slightly lower temperatures in the region of 170°-200°C. Accordingly, the term "high temperature
thermoplastic" will be used throughout the specification to indicate thermoplastic materials that have a heat deflection temperature of 170°C or greater, as determined by the American Society of Testing and Materials (ASTM) standard test No. D648. Such materials include polyetherimide (PEI), polysulfone, polyethersulfone, polyamideimide, polyarylsulfone, polyarylate, polyetheretherketone, polybutyleneterephthalate, and blended combinations thereof.

In the past, some of these high temperature thermoplastic materials have been used as printed circuit substrates. There are two basic methods that have been used to affix an electrical circuit pattern to the surface of such a substrate. In the foil bonding method, a conductive foil is adhesively bonded to the substrate and an electrical circuit is formed from the foil by selective chemical etching. In the plating method, the electrical circuit pattern is selectively plated on the surface of the substrate by an electroless plating process. Unfortunately, there are disadvantages to both methods. In the foil bonding method, the surface of the substrate must be substantially flat and connections from one side of the substrate to the other via "through-holes" cannot be formed with this technique. Thus, if conductive through-holes are required on a foil bonded substrate, an additional plating process must also be included. In the electroless plating method, the primary disadvantage is time, which is typically on the order of several hours to plate-up an electrical circuit pattern of useable thickness.

Vacuum deposition of conductive materials has been previously used to form electrical circuit patterns on certain substrate materials, in
particular, ceramic materials. Vacuum deposition has also been used to deposit certain materials over high temperature thermoplastics, for example, dichroic materials have been vacuum deposited over PEI to form reflectors for surgical lamps. Since vacuum deposition lacks the aforementioned disadvantages of the foil bonding and plating processes, it appears to be ideal for affixing solderable electrical circuit patterns to the surface of high temperature thermoplastic substrates. Unfortunately, when solderable materials are vacuum deposited onto unprepared high temperature thermoplastic substrates, the bond strength between the substrate and the solderable layer is so low that the vacuum deposited material simply peels away from the surface of the substrate when the substrate is exposed to soldering temperatures.

**SUMMARY of the INVENTION**

Briefly, the invention is a process for vacuum depositing a solderable electrical conductor onto the surface of a high temperature thermoplastic substrate. In the process, the surface of a high temperature thermoplastic substrate is first prepared by creating a reactive surface suitable for bonding a solderable electrical conductor to the substrate. Then, a solderable electrical conductor is vacuum deposited onto the reactive surface of the substrate.

**BRIEF DESCRIPTION of the DRAWINGS**

Figs. 1A-1C are edge views of an electrical circuit being manufactured by the present process which illustrate the structure that results at various stages of the manufacturing process; more specifically:
Fig. 1A illustrates a thermoplastic substrate wherein a solderable electrical conductor has been vacuum deposited onto a reactive surface of the substrate.

Fig. 1B illustrates the substrate after a photoresist layer has been applied over the solderable electrical conductor, and windows have been opened up in the photoresist layer into which additional conductive layers are plated.

Fig. 1C illustrates the substrate after the photoresist layers have been removed, such that only a solderable electrical circuit pattern remains affixed to the reactive surface of the substrate.

DESCRIPTION of the PREFERRED EMBODIMENT

Surface Preparation

To vacuum deposit a solderable conductor onto the surface of a high temperature thermoplastic substrate, the surface of the substrate must be properly prepared. There are two methods of surface preparation: a wet and a dry process. In both the wet and dry processes, the substrate is first cleaned in a detergent solution such as Alkanox™.

In the wet process, the substrate is placed in boiling peroxide for approximately 15 minutes. Although hydrogen peroxide is preferred, other peroxides may also be suitable such as peroxides of sodium, potassium, calcium, magnesium, beryllium, barium, lithium or strontium. The substrate is then removed from the peroxide, rinsed in dionized water and dried at 150°C for approximately 1 hour. In the dry process, the substrate is rinsed in dionized water, dried at 130°C for approximately 4 hours and then sputter etched in an argon or argon/oxygen atmosphere for 1 minute at 500 Watts. Following
either process, the substrate may be plasma cleaned, preferably in an oxygen environment for 10 minutes at 500 Watts. The result of either the wet or dry process is the creation of a reactive surface (102A) suitable for bonding a solderable electrical conductor to the substrate.

Conductor Deposition

After plasma cleaning, a solderable electrical conductor 104 is vacuum deposited onto the reactive surface 102A of the substrate 102, as illustrated in Fig. 1A. Solderable electrical conductor 104 includes two layers, a base layer 106 and a solderable layer 108. Base layer 106, which is sometimes referred to as a "glue" layer, is vacuum deposited onto the reactive surface 102A of substrate 102 to a thickness of 700-1000 Angstroms. Base layer 106 is preferably an 80/20 nickel-chrome alloy, although nickel or chromium are also suitable. Vacuum deposition can be accomplished by sputtering or evaporation, though sputtering is preferred. Next, solderable layer 108 is vacuum deposited over base layer 106 to a thickness of approximately 4000 Angstroms. Solderable layer 108 is preferably copper, although other solderable metals may also be suitable.

This process results in a high temperature thermoplastic substrate having a modified surface onto which a solderable electrical conductor is vacuum deposited. Irrespective of the soldering technique, vapor phase reflow, infra-red, hot gas, conduction or otherwise, this electrical conductor can withstand repeated exposure to soldering temperatures without peeling away from the substrate. The present process is not only suitable for depositing a conductor on flat surfaces, but can also be used with substrates
having irregular or non-planar surfaces. This process can also be used to form conductors on both sides of a substrate, and conductive through-holes can easily be made by starting with a blank substrate with holes.

Circuit Formation

The preferred process for forming an electrical circuit pattern from this vacuum deposited conductor is described below, although other photolithographic techniques may also be used. To form an electrical circuit pattern from solderable conductive layer 104, a photoresist layer 110 is first applied over conductive layer 104, as illustrated in Figure 1B. By pattern exposing and developing the resist, a window 110A is opened up at a location where a conductive runner is desired. Next, copper or other solderable metal is electroplated over vacuum deposited copper layer 104 in window 110A. Plated copper layer 112 is typically plated to a thickness of 2.5 to 50 microns. A thin layer of gold 114 or other noble metal is then electroplated over plated copper layer 112.

Next, the remaining photoresist is stripped away using a conventional photoresist stripper and the vacuum deposited copper layer 108, except the areas that underlie electroplated copper layer 112, is etched away using a solution of dilute nitric acid. Finally, base layer 106, except the areas that underlie electroplated copper layer 112, are etched away using dilute hydrochloric acid. The resulting electrical circuit is then rinsed and dried.
An electrical circuit manufactured by this technique is easily distinguished from a similar circuit manufactured by the foil bonding or plating processes. Even to the naked eye, one skilled in the art can easily determine the process that was used to apply the conductors. In particular, the plating process produces a rough textured surface while vacuum deposition produces a smoother surface. Obviously, an analysis of the cross-sections of two circuits, one manufactured by the present process and the other by one of the prior art techniques, would easily reveal the process used to manufacture the circuit since the present process includes a conductive base layer (106) and the other processes do not. Presumptively, an analysis of the surfaces of substrates manufactured by these different processes would also reveal a difference in their chemistries.
We claim as our invention:

1. A process for vacuum depositing a solderable electrical conductor onto the surface of a high temperature thermoplastic substrate, comprising the steps of:
   preparing the surface of a high temperature thermoplastic substrate by creating a reactive surface suitable for bonding a solderable electrical conductor to said substrate; and
   vacuum depositing a solderable electrical conductor onto said reactive surface of said substrate.
2. The process of claim 1, wherein the step of preparing the surface of a high temperature thermoplastic substrate includes placing said substrate in a solution of peroxide.

3. The process of claim 2, wherein said solution of peroxide is hydrogen peroxide.

4. The process of claim 2, wherein the step of vacuum depositing a solderable electrical conductor includes the steps of:
   vacuum depositing a base layer onto said reactive surface of said substrate; and
   vacuum depositing a solderable layer over said base layer.

5. The process of claim 4, wherein said base layer comprises nickel, chromium or nickel-chromium.

6. The process of claim 4, wherein said high temperature thermoplastic substrate comprises polyetherimide, polysulfone, polyethersulfone, polyamideimide, polyarylsulfone, polyarylate, polyetheretherketone, or blends thereof.

7. The process of claim 1, wherein the step of preparing the surface of a high temperature thermoplastic substrate includes sputter etching said surface of said substrate.

8. The process of claim 8, wherein said substrate is sputter etched in an argon or argon-oxygen atmosphere.
9. The process of claim 7, wherein the step of vacuum depositing a solderable electrical conductor includes the steps of:
   vacuum depositing a base layer onto said reactive surface of said substrate; and
   vacuum depositing a solderable layer over said base layer.

10. The process of claim 9, wherein said base layer comprises nickel, chromium or nickel-chromium.

11. The process of claim 9, wherein said high temperature thermoplastic substrate comprises polyetherimide, polysulfone, polyethersulfone, polyamideimide, polyarylsulfone, polyarylate, polyetheretherketone, polybutyleneterephthalate, or blends thereof.

12. The process of claim 1, wherein the step of vacuum depositing a solderable electrical conductor includes the steps of:
   vacuum depositing a base layer onto said reactive surface of said substrate; and
   vacuum depositing a solderable layer over said base layer.

13. The process of claim 12, wherein said base layer comprises nickel, chromium or nickel-chromium.

14. The process of claim 12, wherein said high temperature thermoplastic substrate comprises polyetherimide, polysulfone, polyethersulfone, polyamideimide, polyarylsulfone, polyarylate, polyetheretherketone, polybutyleneterephthalate, or blends thereof.
15. An electrical circuit, comprising in combination:

- a high temperature thermoplastic substrate having a reactive surface suitable for bonding a solderable conductor to said substrate; and
- a solderable electrical conductor vacuum deposited on said surface of said substrate.
16. The electrical circuit of claim 15 wherein said electrical conductor includes a base layer vacuum deposited on said reactive surface of said substrate and a solderable layer vacuum deposited over said base layer.

17. The electrical circuit of claim 16, wherein said base layer includes nickel, chromium or nickel-chromium.
# INTERNATIONAL SEARCH REPORT

**International Application No.** PCT/US88/03920

### I. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both National Classification and IPC:

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### II. FIELDS SEARCHED

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<td>428/418,425.8,458,460-463,473.5,474.4,475.5,476.3,**</td>
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

### III. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>X</td>
<td>US, A, 4,604,168, (Liu), 05 August 1986, (05.08.86), (See Abstract and Col. 2, lines 3-25 and 46-63)</td>
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<td>Y</td>
<td>US, A, 4,269,137, (Johnson), 26 May 1981, (26.05.81), (See Col. 4, lines 9-43)</td>
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<td>US, A, 4,064,030, (Nakai), 20 December 1977, (20.12.77), (See Col. 1, lines 46-68 and Col. 4, lines 12-20)</td>
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* Special categories of cited documents: *A* document defining the general state of the art which is not considered to be of particular relevance. *E* earlier document but published on or after the international filing date. *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified). *O* document referring to an oral disclosure, use, exhibition or other means. *P* document published prior to the international filing date but later than the priority date claimed. *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention. *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step. *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to the person skilled in the art. *A* document member of the same patent family.

### IV. CERTIFICATION

Date of the Actual Completion of the International Search: 11 January 1989

Date of Mailing of this International Search Report: 10 APR 1989

International Searching Authority: ISA/US

Signature of Authorized Officer: Aaron Weijschuck
FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

**476.6, 476.9; 428/480, 500, 524, 626

V. □ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. □ Claim numbers \______, because they relate to subject matter \______ not required to be searched by this Authority, namely:

2. □ Claim numbers \______, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out \______, specifically:

3. □ Claim numbers \______, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. □ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This International Searching Authority found multiple inventions in this international application as follows:

1. □ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. □ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. □ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. □ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest
□ The additional search fees were accompanied by applicant's protest.
□ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (supplemental sheet) (Rev. 11-87)