(51) International Patent Classification ³ :		(11) International Publication Number: WO 82/ 03957
H03K 13/02	A1	(43) International Publication Date: 11 November 1982 (11.11.82)

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(54) Title: DIGITAL TO ANALOG CONVERTER
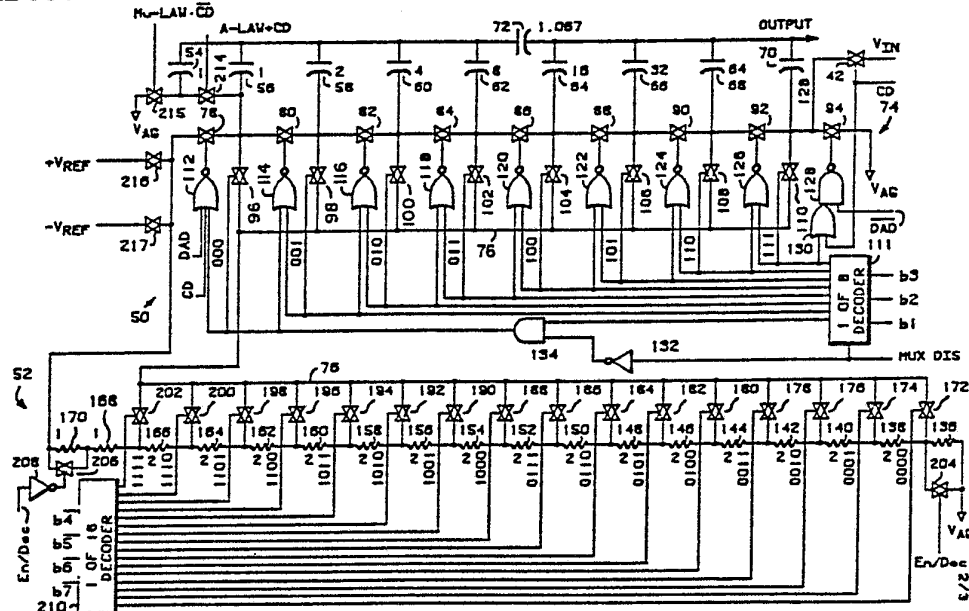
(57) Abstract

An operational amplifier (18) capable of selectively performing a variety of circuit functions. A single operational amplifier (18) utilizes switched capacitors (24, 32 and 36) for sampling and holding an input signal V_{IN}, for establishing a low frequency pole, for applying the sample to an output capacitance (47 and 48) to charge the capacitance and for comparing the input signal V_{IN} with a reference V_{AG}. The multi-function circuit (12) provides a large savings in circuit area and permits versatility of circuit applications. One embodiment of the invention is to utilize a companding DAC (14) having a capacitor array which may be used as the output capacitance (47 and 48) of the operational amplifier circuit (12). The DAC provided utilizes an R ladder DAC (52) coupled directly to a C DAC (50) and has a switching structure that is simpler than comparable prior art circuits. The DAC (14) is asynchronous and has programmable A- and Mu-225 law PCM conversion capability. Coupled directly to the C DAC (50) is an operational amplifier receive filter circuit (16) which utilizes the C DAC (50) as an input capacitor thereby eliminating the need for a buffer amplifier and allowing the DAC (14) to be used for both analog to digital and digital to analog conversion.

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DIGITAL TO ANALOG CONVERTER

CROSS REFERENCE TO RELATED APPLICATIONS

Related subject matter can be found in the following

5   copending applications, each of which is assigned to the
assignee hereof:

1.   Application Serial Number (SC-81153), entitled
"A MULTIPLE FUNCTION OPERATIONAL AMPLIFIER CIRCUIT", filed
simultaneously herewith by Robert Noble Allgood, Stephen

10   Harlow Kelley, Richard Walter Ulmer and Henry Wurzburg.

2.   Application Serial Number (SC-81155), entitled
"A CAPACITIVE DAC TO SWITCHED CAPACITOR FILTER INTERFACE
CIRCUIT", filed simultaneously herewith by Stephen Harlow
Kelley and Richard Walter Ulmer.

15   BACKGROUND OF THE INVENTION

1.   Field of the Invention

This invention relates generally to digital to analog
converters and more particularly to companded digital to
analog converters having programmable MU- or A-law capabi-

20   lity.

2.   Description of the Prior Art

Companding (compression/expansion) digital to analog
converters are commonly used in pulse code modulation
(PCM) to encode voice signals into an eight bit binary

25   code utilizing either the Mu-255 or A-law conversion.
Previously, such companding digitial to analog converters
have utilized two binary-weighted capacitor arrays wherein
one array was used for step bit encoding and the other
array was used for chord bit encoding as discussed by Paul

30   R. Gray, David A. Hodges, John P. Tsividis and Jacob
Chacko, Jr. in an article entitled "Companded Pulse-Code
Modulation Voice Coder Using Monolithic Weighted Capacitor
Arrays", in the IEEE Journal of Solid State Circuits,
December, 1975, pp. 497-499. A unity gain buffer amplifier

35   connected the two capacitor arrays, and three transmission
gates were required for switching each capacitor in the

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chord array to one of three bus lines. The physical
arrangement of the switching structure required tunneling
in order to fabricate an integrated circuit. Furthermore,
the associated logic circuitry required the use of a
5 sequencer and was complex.

    Several variations of companding digital to analog
converters have been used. Single capacitor arrays were
utilized for both the step and chord determinations. Con-
verter circuits with a single array of capacitors have the
10 distinct advantage of having capacitor ratios of 128:1
which are the source of error since precise large capaci-
tor ratios are difficult to obtain. A circuit using a
switched resistor ladder for the step bit determination
and a capacitor array for the chord bit determination was
15 discussed by J.T. Caves, C.H. Chan, S.O. Rosenbaum, L.P.
Sellars and J.B. Terry in an article entitled "A PCM Voice
Coder with On-Chip Filters", in the IEEE Journal of Solid
State Circuits, February 1979, pp. 65-67. By using the
resistor array to convert the step bits, the unity gain
20 buffer amplifier was eliminated and only a single refer-
ence voltage was required, but this and all other compara-
ble circuits continue to have all the previously mentioned
disadvantages.

25   SUMMARY OF THE INVENTION
    It is an object of the present invention to provide a
digital to analog converter adaptable for PCM companding
law which requires less decoding logic and is easier to
implement in integrated circuit form than similar circuits
30 of the prior art.

    Another object of this invention is to provide a new
and improved companding digital to analog converter having
programmable A- or Mu- companding law capability and which
utilizes a switched capacitor array in the conversion of
35 chord bits to an analog signal and a switched resistor

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ladder in the conversion of step bits to an analog sig-
nal.

Yet another object of this invention is to provide a
digital to analog converter which is adaptable for uses
5   other than companding law decoding and which utilizes
fewer components and less integrated circuit die area than
similar circuits of the prior art.

According to a preferred form of the invention, there
is provided a digital to analog converter having a resis-
10 tor ladder portion and a capacitor ladder portion. The
capacitor ladder portion decodes a digital signal which
defines the chord bits of a companded PCM word and the
capacitors are binarily weighted to provide a nonlinear
analog output. Two reference voltages are required and a
15 ladder of logic gates switch the capacitors between the
two reference voltages and a ladder of logic gates couple
a selected resistor ladder voltage to the capacitor array
portion and the output in response to the step bit digital
signal. One-half bit correction is provided by the switch-
20 ing of an additional resistor, and an additional switched
capacitor allows selection of A- or Mu- law operation. The
above and other objects, features and advantages of the
present invention will be more clearly understood from the
following detailed description taken in conjunction with
25 the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram illustrating one
preferred embodiment of the invention.
30   Figure 2 is a schematic diagram illustrating one
preferred embodiment of the digital to analog converter.

Figure 3 is a graphic timing diagram for the schema-
tic embodiment shown in Figures 1 and 2.

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DESCRIPTION OF THE PREFERRED EMBODIMENT

Shown in Figure 1, is a combined filter and
coder/decoder (codec) circuit 10 constructed in accordance
with the preferred embodiment of this invention. The
5   filter-codec circuit 10 is comprised generally of a switched
capacitor multiple function operational amplifier portion
12, a ladder switched capacitive digital to analog converter
(DAC) portion 14, and a receive filter portion 16 which
interfaces with the DAC portion 14. The circuit 10 is
10   capable of receiving and storing an analog signal, V_{IN},
while simultaneously filtering the signal. The signal
V_{IN} may be transferred to the DAC portion 14 and
converted to a digital output by utilizing the operational
amplifier portion 12 as a comparator. An analog to digital
15   (A/D) conversion may be interrupted at any time and the DAC
portion 14 discharged and utilized to perform a digital to
analog (D/A) conversion. After a D/A conversion has been
made, the A/D conversion may be resumed. Thus the circuit
10 is particularly useful for PCM voice encoding and
20   decoding because the two functions may be asynchronous.

In the preferred form, operational amplifier portion 12
has an operational amplifier 18 with its non-inverting and
inverting inputs connected to a reference voltage, say
analog ground V_{AG}, via switches 20 and 22, respectively.
25   A first plate of feedback capacitor 24 is connected to the
inverting input of the operational amplifier 18 via a switch
26 and a second plate of the capacitor 24 is connected to
the output of the operational amplifier 18 via a switch 28.
An input capacitor 32 provides AC coupling of an input
30   signal V_{IN} to the inverting input of the operational
amplifier 18 via the switch 26 and the passband gain K of
the operational amplifier portion 12 is approximately equal
to the ratio of capacitors 32 and 24.

In the preferred embodiment, all the switches are
35   conventional CMOS transmission gates which are constructed

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to be enabled or closed when a clock signal, applied to the
control inputs thereof by a clock generator 30, is in a high
state, and disabled or open when the clock signal is in a
low state. Thus, for example, when the switch 20 is enabled
5   by signal A, switches 26 and 28 are enabled by signal B, and
switch 22 is disabled by signal C, the operational amplifier
portion 12 is connected to sample the input signal V_{IN}
onto the feedback capacitor 24.

A switch 34 connects the first plate of feedback
10   capacitor 24 to a first plate of a switched capacitor 36,
and a switch 38 connects the second plate of the feedback
capacitor 24 to the first plate of the switched capacitor
36. The second plate of the switched capacitor 36 is
connected to the reference V_{AG}. The switches 34 and 38
15   are controlled by signals E and D, respectively, and
alternately switch the capacitor 36 from the inverting input
to the output of the operational amplifier 18. The value of
the capacitor 36 determines, in part, the location of a high
pass pole of the operational amplifier portion 12 of the
20   circuit 10, permitting the filtering of the input signal
V_{IN} while it is being sampled onto the feedback
capacitor 24.

In the preferred embodiment, the DAC portion 14 has a
first input terminal which is selectively coupled to a first
25   reference voltage, $\pm V_{ref}$, via a switch 40; a second
input terminal which is selectively coupled to the output of
the operational amplifier portion 12 or a second reference
voltage, V_{AG}, via switches 42 and 43, respectively; and
an output terminal selectively coupled to the second
30   reference voltage, V_{AG}, the non-inverting input of the
operational amplifier 18 or the input of the receive filter
portion 16 via switches 44, 45 and 46, respectively. In
general, the DAC portion 14 can be represented as an
unswitched capacitor 47 and a switched capacitor 48. In the
35   illustrated form, the first plates of the capacitors 47 and

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48 may be selectively coupled via a DAC switch 49 to form
the effective first plate of the DAC portion 14, while the
second plates thereof are coupled together to form the
second plate of the DAC portion 14.

5   In operation, switches 40, 42, 43, 44, 45, 46 and 49
are controlled by signals H, F, F, G, C, I and H,
respectively. For example, the input sample KV_{IN} can be
transferred onto the DAC portion 14 as it is being sampled
onto the feedback capacitor 24, if, as shown in Figure 3,

10   the signals F and G are simultaneously in the high state and
the signal H is in the low state. Thus, another function of
the operational amplifier portion 12 is to charge the DAC
portion 14 to the input sample KV_{IN} preparatory to
converting the analog input signal into a digital signal.

15   If it may be necessary for the DAC portion 14 to be charged
from the feedback capacitor 24 relatively long after a
sample is placed thereon, switches 26 and 28 should be
compensated switches to isolate the charged capacitor 24 and
prevent parasitic leakage paths from leaking part of the

20   sampled charge off of the feedback capacitor 24. In
addition, it should be recognized that the offset voltage of
the operational amplifier 18 will be charged onto the DAC
portion 14 along with the input signal sample.

         When the switch 22 is enabled by signal C, the

25   operational amplifier 18 may be reconfigured as a comparator
for use in an A/D conversion. For example, if switches 43
and 45 are enabled via signals F and C, respectively, while
switches 42 and 44 are disabled via signals F and G,
respectively, then the voltage transferred onto DAC portion

30   14 by the operational amplifier portion 12 will be
translated relative to the second reference voltage V_{AG}.
Of course, the stored offset voltage will also be translated
by the switching action, but will now appear as an error of
opposite polarity. By switching the inverting input of the

35   operational amplifier 18 from the feedback capacitor 24 to

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the second reference voltage V_{AG} and the non-inverting
input from the second reference V_{AG} to the output
terminal of the DAC portion 14, the operational amplifier 18
will be connected as a comparator and will provide an output
5   indicative of the difference between the voltages on the
inputs thereof. Note that the offset voltage stored on the
DAC portion 14 is now present as a bias on the non-inverting
input of the operational amplifier so that the offset
voltage of the operational amplifier 18 will be
10   automatically cancelled.

      If, before an A/D conversion has been completed, it is
desired to perform a D/A conversion, the DAC portion 14 can
be discharged and used to perform the D/A conversion. For
example, switches 42 and 44 may be enabled by signals F and
15   G, respectively, to discharge the DAC 14. Thereafter,
switches 40 and 49 may be enabled by signals B and H,
respectively, to charge the DAC portion 14 to a percentage
of the first reference $\pm V_{ref}$ representing the analog
equivalent of a digital input which is being converted.
20   After the D/A conversion is completed, the input sample
KV_{IN} may again be charged onto the DAC portion 14 as
previously detailed and the A/D conversion restarted where
it was interrupted.

      In the illustrated embodiment, one operational
25   amplifier 18 has been used for a variety of circuit
functions. In the preferred embodiment, the operational
amplifier portion 12 may be conveniently fabricated as a
monolithic integrated circuit which requires no external
components to perform each of the described circuit
30   functions.

      Shown in Figure 2 is a preferred form of the DAC
portion 14 of Figure 1. In the illustrated form, the DAC
portion 14 is comprised of two DAC sections, a capacitive or
C DAC section 50 and a resistive or R DAC section 52. DACs
35   of this form are commonly called stacked DACS and find

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frequent application in pulse code modulation (PCM) to make
use of companding (compression/expansion) which permits an
8-bit binary code to cover a greater dynamic range than
otherwise possible. Two internationally known companded

5   codes are the Mu-255 compression law and the segmented
A-law. In both laws, samples of an analog speech signal are
mapped using an 8-bit PCM code into sixteen chords, with
each chord comprising sixteen equal steps. In the Mu-255
law, the step intervals in each chord precisely double in

10   size away from the origin of the input-output curve. The
same is also true for the A-law, except that the first two
chords on each side of the origin have the same step size.
Both laws contain 256 quantization levels which are bounded
by 255 decision levels. The format of the 8-bit companded

15   PCM word is for the first bit to indicate the sign of the
voice signal, the second through fourth bits are chord bits
which, with the sign bit, indicate which one of the sixteen
chords the signal is in, and the fifth through eighth bits
are step bits which indicate which one of the sixteen steps

20   the signal corresponds to.
         In the illustrated embodiment, the C DAC section 50
includes a unit capacitor 54 and eight rank ordered
capacitors 56 through 70 which are effectively binarily
weighted by the ratio 2^n, where n equals 0-7 for

25   capacitors 56-70, respectively. The capacitors 54-70 each
have a first and a second plate, with the second plates
being coupled to the output terminal of the DAC portion 14.
         In the illustrated embodiment, a dividing capacitor 72
is interposed between the second plates of capacitors 54-62

30   and the second plates of capacitors 64-70, to reduce the
physical size of the capacitors 64-70 relative to capacitors
54-62 and eliminate problems associated with large ratios
which tend to be imprecise. Stated another way, the
dividing capacitor 72 is used to divide the effective value

35   of the capacitors 54-62 as seen by the capacitors 64-70.

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Thus, although the weighted value of each capacitor
is as shown in Figure 2, the actual unit values of the
capacitors 54-70 are, in the preferred form, respectively 1,
1, 2, 4, 8, 1, 2, 4 and 8. However, the capacitors 54-62

5   contribute a total unit value of only 1 at the output due to
the dividing capacitor 72, while the capacitors 64-70
contribute a total unit value of 15 units at the output. It
should be noted that the embodiment shown is only exemplary
and other values may be substituted. In order to make the

10   impedance of the capacitors 54-62 in series with capacitor
72 equal to 1 unit at the output terminal of the DAC portion
14 and allow the capacitors 54-62 to have unit weights
totaling 16, the weighted value of the capacitor 72 is found
by solving the following for X, the weighted value:

15                      $1/16 + 1/X = 1$
              or, $X = 16/15 = 1.067$ unit
         The capacitive DAC section 50 also includes a C ladder
switching network 74 for selectively coupling the first
plates of the capacitors 54-70 to the first reference

20   voltage $\pm V_{ref}$, the second reference voltage V_{AG},
or a step voltage developed by the R DAC section 52 on a
common rail 76. In the preferred form, the C ladder
switching network 74 comprises C rail switches 78 through
94, with the switch 78 being connected between the first

25   reference voltage $\pm V_{ref}$ and the first plate of the
capacitor 54, and the switch 94 being connected between the
second reference voltage V_{AG} and the first plate of the
capacitor 68. The switches 80 through 92 are connected
between the first plates of respective, successively ordered

30   pairs of the capacitors 56-70. The C ladder switching
network 74 further includes C rung switches 96-110, coupled
between the first plates of the capacitors 56-70,
respectively, and the common rail 76. Each of the C rail
switches 78-94 and the C rung switches 96-110 has a rank

35   order corresponding to the rank of the associated capacitors

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56-70.

The C ladder switching network 74 is controlled by a C
logic circuit which includes a one-of-eight, C decoder 111
having digital inputs b1, b2, and b3 which receive
corresponding chord input code bits of the PCM word, and
eight rank ordered C rung outputs, each of which provides a
C rung enable signal to a respective one of the ranked C
rung switches 96-110. For example, the C rung output
corresponding to a chord input code of 000 is connected to
the C rung switch 96. Thus, for any one particular chord
input code, a respective one of the C rung enable signals
will be provided to enable the associated one of the C rung
switchs 96-110, and all the other C rung switches 96-110
will be disabled.

The C logic circuit also includes rank ordered gates
112 through 128 which provide C rail disable signals to
selectively disable respective C rail switches 78-94. In
the illustrated form, the gates 114-126 are two-input NOR
gates which have the inputs thereof coupled to respective
adjacent pairs of the C rung outputs beginning from the
lowest rank (chord input codes 000 and 001) to the highest
rank (chord input codes 110 and 111). Gate 112 is a
three-input NOR which has a first input thereof coupled to
the lowest ranked C rung output (chord input code 000), a
second input thereof coupled to a Charge DAC or CD disable
signal for selectively decoupling the first plates of the
capacitors 54-70 from the first and second reference
voltages, and a third input thereof coupled to a D/A
Discharge or DAD disable signal for selectively discharging
the DAC capacitors 54-70 in preparation for a digital to
analog conversion. The gate 128 is a two-input NAND having
a first input thereof coupled to the inverse of the DAD
disable signal and the second input thereof coupled to the
output of a gate 130. The gate 130 is preferably a
two-input OR having a first input thereof coupled to the

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highest ordered C rung output (chord input code 111) and a
second input thereof coupled to the CD disable signal.

In this configuration, the C rail disable outputs from
the gates 112-128 determine which of the first plates of the
5   capacitors 56-70 are connected to one another and to the
reference voltages $\pm V_{ref}$ and V_{AG}. Assuming that
the CD disable signal is in a high state, the gate 112
disables the C rail switch 78 to decouple the first plates
of the capacitors 56-70 from the first reference voltage,
10   $\pm V_{ref}$, and the gates 128 and 130 cooperate to disable
the C rail switch 94 to decouple the first plates of the
capacitors 56-70 from the second reference voltage V_{AG}.
If, as shown in Figure 3, the CD disable signal is also
coupled to the control input of the switch 42 as signal F,
15   switch 42 will then couple the input signal sample onto the
first plates of the capacitors 56-70. On the other hand if
the DAD disable signal is in the high state, the gate 112
disables C rail switch 78 to decouple the first plates of
the capacitors 56-70 from the first reference voltage
20   $\pm V_{ref}$, and gate 128 enables C rail switch 94 to couple
the first plates of the capacitors 56-70 to the second
reference voltage V_{AG}.

In the illustrated embodiment, the C decoder 111 may be
selectively disabled via a Mux disable signal whenever it is
25   necessary to charge or discharge the capacitors 54-70. In
the preferred embodiment, the C decoder 111 will respond to
a Mux disable signal in the high state by providing an
enable signal on the lowest C rung output only.
Simultaneously, an inverter 132 disables a gate 134
30   interposed in the lowest C rung output between the gates 112
and 114 and switch 96, and the C decoder 111, to prevent the
enable signal from otherwise enabling the C rung switch 96.
Preferably, the gate 134 is a two-input AND having a first
input connected to the lowest ranked C rung output and a
35   second input connected to the output of the inverter 132,

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the input of the latter being coupled to receive the Mux
disable signal.

In the illustrated embodiment, the R DAC section 52
includes a voltage divider for developing on each of a rank
5   ordered plurality of step nodes a step voltage between the
first reference voltage $\pm V_{ref}$ and the second reference
voltage V_{AG}. In the preferred form, the voltage divider
comprises a plurality of resistors 136 through 170 connected
in series between the first reference voltage $\pm V_{ref}$
10 and the second reference voltage V_{AG}, with the resistors
136, 168 and 170 having a relative value of one unit each
and the resistors 138 through 166 having a relative value of
two units each. In this configuration, predetermined step
voltages having absolute values spaced between $\pm V_{ref}$
15 and V_{AG} are developed on the step nodes between each
pair of resistors 136-170.

The R DAC section 52 also includes an R ladder
switching network for coupling a selected one of the step
nodes to the common rail 76. In particular, a plurality of
20 rank ordered R rung switches 172 through 202 couple
respective step nodes to the common rail 76. In the
preferred form, switches 204 and 206 are coupled in parallel
with resistors 136 and 170, respectively, to selectively
short one of the resistors 136 and 170 in response to an
25 Encode/Decode or En/Dec signal for reasons made clear
hereinafter.

The R ladder switching network is controlled by a
one-of-sixteen, R decoder 210 having digital inputs b4, b5,
b6 and b7 corresponding to the step input code bits of the
30 PCM word, and sixteen R rung outputs for providing enable
signals to respective R rung switches 172 through 202. For
example, the R rung output corresponding to a step input
code of 0000 is connected to the R rung switch 172, and the
R rung output corresponding to a step input code of 1111 is
35 connected to the R rung switch 202. Thus for any one

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particular step input code, a respective one of the R rung
enable signals will be provided to enable the associated one
of the R rung switches 172-202. In response to the R rung
enable signal, the particular R rung switch 172-202 will

5   couple a respective step node to the common rail 76. Thus,
each step voltage developed across the R DAC section 52 may
be selectively connected to the C DAC section 50 via the
common rail 76.

To obtain a programmable A- and Mu-255 law capability,

10   the DAC portion 14 utilizes the coding capacitor 54 which
has a first plate connected to a first code switch 214. The
first code switch 214 couples the first plate of the coding
capacitor 54 to the first plate of the lowest ranked
capacitor 56. A second plate of the coding capacitor 54 is

15   connected to the second plate of the capacitor 56. A second
code switch 215 is connected between the second reference
voltage V_{AG} and the first plate of the coding capacitor
54. The first code switch 214 is enabled when either an
A-law PCM conversion signal or a CD enable signal is applied

20   to its control input terminal in a high state. The second
code switch 215 is enabled whenever both a Mu-law PCM
conversion signal and the complement of the CD enable signal
are applied in a high state to its control input terminal.
Whenever the first code switch 214 is enabled, the second

25   code switch 215 is disabled and the DAC portion 48 provides
A-law PCM conversion. Thus, the coding capacitor 54 is
always connected in parallel with the capacitor 56 when the
C DAC section 50 is being charged. When A-law conversion is
desired, the capacitor 54 is allowed to remain in parallel

30   with the capacitor 56, so that the combination of the
capacitors 54 and 56 provides a capacitance of two units.
However, when Mu-255 law conversion is desired, the first
plate of the coding capacitor 54 is connected to the second
reference voltage V_{AG} and disconnected from the first

35   plate of the capacitor 56. This removes one unit of

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capacitance from the C DAC section 50 to provide one-half
the A-law chord size in chord 000. Thus, the step size at
the origin is one-half as large in Mu-law as the step size
at the origin in A-law.

5   Since the polarity of the input sample KV_{IN} may be
above or below the second reference voltage V_{AG}, the DAC
portion 14 must be able to compare the sample on the C DAC
50 to both the positive and the negative forms of the first
reference voltage $\pm V_{ref}$. In the preferred embodiment,

10   reference voltage generators (not shown) generate the
required first reference voltages $+V_{ref}$ and
$-V_{ref}$. As shown in Figure 2, the appropriate one of
the positive and negative first reference voltages may be
selectively coupled to the C DAC 50 and R DAC 52 via

15   switches 216 and 217, respectively, as described
hereinafter.

          Referring again to Figure 1, the first stage of the
receive filter portion 16 comprises an operational amplifier
220, a feedback capacitor 218, and a switched capacitor 222

20   having a first plate connected to the reference V_{AG} and
a second plate which is alternately connected to the
non-inverting input of the operational amplifier 220, via a
switch 224, and the output of the operational amplifier 220,
via a switch 226, in response to a control signal J and the

25   inverse thereof, to simulate a feedback resistance. In the
preferred embodiment, the receive filter portion 16 includes
additional filter stages with appropriate feedback paths
(not shown) for performing the desired filter functions. By
selectively coupling the charge of the DAC portion 14

30   directly to the input of the receive filter 16 via switch
46, the need for an intermediate buffer amplifier is totally
eliminated. In this configuration, parasitic capacitance
errors normally associated with the use of a buffer
amplifier to couple the output of the DAC portion 14 to the

35   receive filter portion 16 are eliminated since the output

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terminal of the DAC portion 14 will always settle to the
second reference voltage V_{AG}. The elimination of the
buffer amplifier also conserves power and circuit area.

The international standard sampling rate for PCM voice
5   encoding is 8 kHz or one frame every 125 usec. In the
preferred embodiment, each frame is divided into sixteen
equal conversion segments, and is synchronized to a Tx Sync
signal. To illustrate the cooperation of the operational
amplifier portion 12 and the DAC portion 14, reference will
10   now be made to Figure 3 which illustrates one frame in which
two D/A conversions are _asynchronously_ performed in the
course of one A/D conversion. Of course, the example shown
in Figure 3 is representative of only one of many ways the
circuit 10 is capable of performing.

15   In general, an A/D conversion is performed by sampling
the analog input signal V_{IN}, and storing an input sample
$-KV_{IN}$ onto the feedback capacitor 24. The input sample
is then transferred onto the first plates of the capacitors
54-70 of the DAC portion 14, and translated onto the second
20   plates thereof to reinvert the sample. The polarity of the
translated sample is then determined relative to the second
reference voltage V_{AG}. A binary search is then
performed, using a conventional successive approximation
register or SAR (not shown), to converge to the digital code
25   which, when converted using the DAC portion 14, will
effectively cancel the sample charge on the second plates of
the capacitors 54-70, and force the voltage on the output
terminal of the DAC portion 14 to the second reference
voltage V_{AG}. Recall that when the DAC portion 14 is
30   being charged to the input sample voltage, the switch 214 is
enabled and the switch 215 is disabled, adding the one unit
of capacitance of the capacitor 54 to the 255 units of
capacitance of the capacitors 56-70 for a total C DAC 50
capacitance of 256 units. Since the R DAC 52 is capable of
35   applying any one of the sixteen step voltages to any one of

the capacitors 54-70 via the step node 76, the DAC portion
14 effectively divides the voltage difference between the
first reference voltage $\pm V_{ref}$ and the second reference
voltage V_{AG} into 256(units of capacitance)*16(step
5   voltages) or 4096 segments. However, the DAC portion 14 is
actually able to generate only 8(chords)*16(steps) or 128 of
these segments, due to the increasing step and chord size
inherent in companding.

In the process of encoding, the analog input sample is
10   compared against a set of decision levels corresponding to
the segments the DAC portion 14 can generate with the R DAC
52 configured to provide step voltages which are multiples
of the first reference voltage $V_{ref}/16$. In the
preferred embodiment, the R DAC 52 is so configured by the
15   En/Dec signal, which enables switch 204 and disables switch
206. However, it is well known that this technique of
encoding results in a quantizing error in the range of 0 to
-1.

In the example shown in Figure 3, it will be assumed
20   that the DAC portion 14 is operating according to the Mu-255
companding law. In this mode, the first plate of capacitor
54 is coupled via switch 215 to the second reference voltage
V_{AG} during the conversion, so that only 255 units of
capacitance can be switched to each of the 16 step voltages
25   for a total of only 4080 segments. Thus, the effective
range of the DAC portion 14 is limited to
$(4080/4096) * \pm V_{ref}$.

During the first segment, the analog input signal
V_{IN} is sampled, and the instantaneous value stored on
30   the feedback capacitor 24 as $-KV_{IN}$, where $-K$ is the gain
of the operational amplifier 18. For the purposes of this
explanation, it will be assumed that the input sample
$-KV_{IN}$, stored on the feedback capacitor 24, has a value
of $-340/4096$ of the first reference voltage $+V_{ref}$.
35   Simultaneously, the input sample is transferred to the first

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plates of the capacitors 54-70 of the C DAC circuit 50 via
the gate 42 which is enabled by the signal CD. After the
input sample has been stored on the C DAC 50, the sample is
translated relative to the second reference voltage V_{AG}

5   by coupling the second plates of capacitors 54-70 to the
non-inverting input of operational amplifier 18 and the
first plates of capacitors 54-70 to the second reference
voltage V_{AG}. The polarity of the sample can now be
determined by configuring the operational amplifier 18 as a

10   comparator to compare the translated sample to the second
reference voltage V_{AG}. For the example given, the
output of the operational amplifier 18 will be positive,
indicating that the input sample KV_{IN} was positive when
sampled. The result of the comparison is then stored as a

15   positive sign bit in the SAR, and used to select the
negative one of the first reference voltages $\pm V_{ref}$ by
disabling switch 216 and enabling switch 217.

       During the second segment, the SAR forces the next most
significant bit or b1 to a 1, making a mid-range chord input

20   code 100 to the C decoder 111 and the low-range step input
code 0000 to the R decoder 210. In response to the chord
input code of 100, the C decoder 111 and gates 112-130
disable switches 86 and 88, and enable switches 78-84 and
90-94, to couple the first plates of capacitors 56-62 to the

25   first reference voltage $-V_{ref}$ and the first plates of
capacitors 66-70 to the second reference voltage V_{AG}.
The C decoder 111 and gates 112-130 also disable switches
96-102 and 106-110, and enable switch 104 to couple the
first plate of capacitor 64 to the step node 76. In

30   response to the step input code of 0000, the R decoder 210
disables switches 174-202 and enables switch 172, to couple
the step node 76 to the second reference voltage V_{AG}.
The resulting sharing on the second plates of the capacitors
54-70 of the charge representing the stored sample, develops

35   a voltage on the second plates of the capacitors 54-70, and

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applied to the non-inverting input of the operational
amplifier 18, which is still in the comparator
configuration.

Since the charge due to the switching of the first
5   plates of capacitors 56-62 to the first reference voltage
$-V_{ref}$ is not sufficient to cancel all of the sample
charge on the second plates of all of the capacitors 54-70,
the voltage on the second plates will still be above the
second reference voltage V_{AG}. The output of the
10   operational amplifier 18 will therefore be positive,
resulting in a code of 1 being stored in the b1 position of
the SAR.

In the hypothetical example shown, an Rx Sync signal is
received during the third segment, indicating that the A/D
15   conversion sequence must be interrupted to perform a D/A
conversion. Thus, during the fourth segment, the DAC
capacitors 54-70 are initially discharged, since the input
sample $-KV_{IN}$ is still being held on the feedback
capacitor 24. Assume, for example, that a digital input
20   code 00101100 has been received. Since the sign bit b0 is
0, the desired analog output signal must be negative. If
the receive filter portion 16 has an odd number of inversion
stages therein, as in the preferred embodiment, then the
positive one of the first reference voltages $+V_{ref}$
25   must be selected by enabling switch 216 and disabling switch
217. After discharge, the C decoder 111 responds to the
chord input code of 010 by enabling switches 78-80, 86-94
and 100, and disabling switches 82 and 84. Simultaneously,
the R decoder 210 responds to the step input code of 1100 by
30   enabling switch 196 and disabling 172-194 and 198-202.
Thus, the first plates of capacitors 56 and 58 are coupled
to the first reference voltage $+V_{ref}$, the first plate
of capacitor 60 is coupled to the step node 76, and the
first plates of capacitors 62-70 and 54 are coupled to the

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second reference voltage V_{AG}. For the example given,
the step voltage developed by the R DAC 52 on step node 76
will be $(25/32)*V_{ref}$. The charge on the output
terminal of the DAC portion 14 resulting from the selective

5   switching of the first plates of the capacitors 56-60 is
coupled to the receive filter portion 16 via switch 46 under
control of control signal I. It can be shown, using charge
redistribution principles, that this charge is proportional
to $[(98/4096)*(+V_{ref})]$, with the proportionality

10   constant being related to the Thevinin equivalent total
capacitance of the array of capacitors 54-70 as seen from
the output terminal of the DAC portion 14.

In the preferred embodiment, the capacitors 54-70
function as the input capacitance of the first stage of the

15   receive filter portion 16, and determine in part the gain of
this stage. In order to reduce the gain required of the
first stage of the receive filter portion 16 while
increasing the dynamic range of the filter portion 16, the
D/A conversion is performed twice in consecutive segments in

20   order to couple a sufficient amount of charge into the
receive filter portion 16. An unexpected advantage accruing
from interfacing the DAC portion 14 to the receive filter
portion 16 in this manner is the automatic correction of the
$(\sin x)/x$ distortion normally associated with flat-top or

25   zero order hold sampling of an analog signal. For a more
detailed description of this problem, reference may be made
to the copending Application Serial Number 138,969, filed 10
April 1980 by Stephen H. Kelley and Henry Wurzburg and
assigned to the assignee of the present invention.

30   It is possible to minimize the quantizing error
resulting from the original A/D conversion, by performing a
half bit correction during the D/A conversion. To
accomplish the correction, the R DAC 52 should be configured
to provide the step voltages as odd multiples of the second

35   reference voltage $V_{AG}/32$. In the preferred embodiment,

the R DAC 52 is so configured by the En/Dec signal which
enables switch 206 and disables switch 204. The correction
effectively raises or upshifts the R ladder by one-half LSB
in a digital to analog conversion, to compensate for the
5   relative lowering or downshifting of the R ladder by
one-half LSB in an analog to digital conversion, resulting
in a shifting of the quantizing error to the range of $\pm 1/2$.

By the end of the fifth segment, the converted analog
signal has been coupled into the receive filter 16 and
10   charged onto the filter feedback capacitor 218. At the
start of the sixth period, the analog to digital conversion
is resumed where it was interrupted, by charging the input
sample $-KV_{IN}$ back onto the DAC capacitors 54-70 from the
feedback capacitor 24. At the end of the sixth segment, the
15   input signal sample is again translated onto the second
plates of capacitors 54-70, as described above.

During the seventh segment, the SAR, which has remained
at the value established by the end of the second segment,
forces the next most significant digital input bit b2, i.e
20   the second chord input bit, to a 1. In response to the
resulting chord input code of 110, the C decoder 111 and
gates 112-130 disable switches 90 and 92, and enable
switches 78-88 and 94, to couple the first plates of
capacitors 56-66 to the first reference voltage $-V_{ref}$
25   and the first plate of capacitor 70 to the second reference
voltage V_{AG}. The C decoder 111 and gates 112-130 also
disable switches 96-106 and 110, and enable switch 108, to
couple the first plate of capacitor 68 to the step node 76.
In response to the step input code of 0000, the R decoder
30   210 disables switches 174-202 and enables switch 172 and
204, to couple the step node 76 to the second reference
voltage V_{AG}. The resulting sharing on the second plates
of the capacitors 54-70 of the charge representing the
stored sample, develops a voltage on the second plates of
35   the capacitors 54-70, which is applied to the non-inverting

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input of the operational amplifier 18, the latter being
still in the comparator configuration.

Since the charge due to the switching of the first
30   plates of capacitors 56-66 to the first reference voltage
$-V_{ref}$ is now more than sufficient to cancel all of the
sample charge on the second plates of all of the capacitors
54-70, the voltage on the second plates will be below the
second reference voltage V_{AG}. The output of the
operational amplifier 18 will therefore be negative,
resulting in a code of 0 being stored in the b2 position of
the SAR.

During the eighth segment, the SAR forces the next most
5   significant digital input bit b3, i.e the third chord input
bit, to a 1. In response to the resulting chord input code
of 101, the C decoder 111 and gates 112-130 disable switches
88 and 90, and enable switches 78-86 and 92-94, to couple
the first plates of capacitors 56-64 to the first reference
10   voltage $-V_{ref}$ and the first plate of capacitors 68-70
to the second reference voltage V_{AG}. The C decoder 111
and gates 112-130 also disable switches 96-104 and 108-110,
and enable switch 106, to couple the first plate of
capacitor 66 to the step node 76. In response to the step
15   input code of 0000, the R decoder 210 disables switches
174-202 and enables switch 172 and 204, to couple the step
node 76 to the second reference voltage V_{AG}. The
resulting sharing on the second plates of the capacitors
54-70 of the charge representing the stored sample, develops
20   a voltage on the second plates of the capacitors 54-70,
which is applied to the non-inverting input of the
operational amplifier 18, the latter being still in the
comparator configuration.

Since the charge due to the switching of the first
25   plates of capacitors 56-64 to the first reference voltage
$-V_{ref}$ is still more than sufficient to cancel all of
the sample charge on the second plates of all of the

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capacitors 54-70, the voltage on the second plates will be
again be below the second reference voltage V_{AG}. The
output of the operational amplifier 18 will therefore be
negative, resulting in a code of 0 being stored in the b3
5   position of the SAR. Thus, by the end of the eighth
segment, the chord input portion of the SAR contains 100,
indicating that the amplitude of the input signal sample is
within chord 4.

        During the ninth segment, the SAR forces the next most
10   significant digital input bit b4, i.e the first step input
bit, to a 1. In response to the chord input code of 100,
the C decoder 111 and gates 112-130 disable switches 86-88,
and enable switches 78-84 and 90-94, to couple the first
plates of capacitors 56-62 to the first reference voltage
15      $-V_{ref}$ and the first plate of capacitors 66-70 to the
second reference voltage V_{AG}. The C decoder 111 and
gates 112-130 also disable switches 96-102 and 106-110, and
enable switch 104, to couple the first plate of capacitor 64
to the step node 76. In response to the step input code of
20   1000, the R decoder 210 disables switches 172-186 and
190-202, and enables switch 188, to couple
$(16/32)*V_{ref}$ to the first plate of capacitor 64 via
step node 76. The resulting sharing on the second plates of
the capacitors 54-70 of the charge representing the stored
25   sample, develops a voltage on the second plates of the
capacitors 54-70, which is applied to the non-inverting
input of the operational amplifier 18, the latter being
still in the comparator configuration.

        Since the charge due to the switching of the first
30   plates of capacitors 56-62 to the first reference voltage
$-V_{ref}$ and the first plate of the capacitor 64 to
$(16/32)*V_{ref}$ is still more than sufficient to cancel
all of the sample charge on the second plates of all of the
capacitors 54-70, the voltage on the second plates will
35   again be below the second reference voltage V_{AG}. The

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output of the operational amplifier 18 will therefore be
negative, resulting in a code of 0 being stored in the b4
position of the SAR. In a similar manner, each of the
remaining digital input bits b5, b6 and b7, corresponding to
5   the remaining step input bits are determined in the tenth,
eleventh and twelfth segments, respectively. Thus, by the
end of the twelfth segment, the chord input portion of the
SAR contains 100 and the step input portion of the SAR
contains 0110, indicating that the amplitude of the input
10   signal V_{IN}, when sampled, was within step 6 of chord 4.

        Any time after the A/D conversion has been completed,
the contents of the SAR can be transferred into an
appropriate holding register (not shown) for subsequent use
or transmission. In the preferred embodiment, the transfer
15   is accomplished during the segment following determination
of digital code bit b7. The SAR is then cleared to all
zeros so as to be ready for the next A/D conversion cycle.

        During the thirteenth segment, a second Rx Sync signal
is received. In response, the circuit 10 operates as
20   described above to perform the requested digital to analog
conversion during the fourteenth and fifteenth segments.
When neither an analog to digital or a digital to analog
conversion is occurring, the circuit may enter an idle mode,
as in the thirteenth and sixteenth segments. Depending upon
25   the relative timing of the Tx and Rx Sync signals, each
frame may have from 0 to 4 idle mode segments.

        Although the operation of the circuit 10 has been
illustrated using the exemplary timing diagram of Figure 3,
it will be clear that the ability of the circuit 10 to
30   perform two D/A conversions and one A/D conversion during a
single frame assures asynchronous operation in voice
applications. In fact, it can be shown that the circuit 10
will perform satisfactorily even if the Tx Sync signal
occurs a few segments early, provided that the previous A/D
35   conversion has been completed.

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While the invention has been described in the context
of a preferred embodiment, it will be apparent to those
skilled in the art that the present invention may be
modified in numerous ways and may assume many embodiments
5 other than that specifically set out and described above.
Accordingly, it is intended by the appended claims to cover
all modifications of the invention which fall within the
true spirit and scope of the invention.

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CLAIMS ·

1. A converter for providing an analog output signal cor-
responding to a digital input code, comprising:

      voltage divider means for providing a step voltage
          selected between first and second reference volt-
5   ages in response to the digital input code, com-
          prising:

      resistance means coupled between the first and second
          reference voltages, for developing on each of a
          plurality of step nodes a predetermined step volt-
10   age between the first and second reference volt-
          ages; and

      R ladder switching means coupled between the resis-
          tance means and a common rail, for coupling, in
          response to the digital input code, a selected one
15   of the step nodes to the common rail; and

      charge redistribution means coupled to the common
          rail, for providing the analog output signal as a
          function of the step voltage on the common rail and
          the digital input code, comprising:

20   capacitance means comprising a rank ordered plurality
          of capacitors having respective first plates and
          interconnected second plates, for developing·the
          analog output signal on the second plates as a
          function of the voltages coupled to the first
25   plates; and

      C ladder switching means coupled to the first and
          second reference voltages, the common rail and each
          of the first plates of the capacitors, for coup-
          ling, in response to the digital input code, the
30   step voltage on the common rail to the first plate
          of a selected one of the capacitors, the first ref-
          erence voltage to the first plates of each of the
          capacitors of lower rank than the selected one of
          the capacitors, and the second reference voltage to
35   the first plates of each of the capacitors of high-
          er rank than the selected one of the capacitors.

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2. The converter of claim 1 wherein the C ladder switch-
ing means comprise:

      a C rung switching network comprising a rank ordered
          plurality of C rung switching elements, each
5   coupled between the first plate of a respective
          one of the capacitors and the common rail, for
          coupling a respective one of the first plates to
          the common rail in response to a respective C
          rung enable signal; and
10   a C rail switching network comprising a rank ordered
          plurality of C rail switching elements, the
          first of which is coupled between the first ref-
          erence voltage and the first plate of the capa-
          citor of lowest rank, the last of which is
15   coupled between the second reference voltage and
          the first plate of the capacitor of highest
          rank, and the balance of which are coupled
          between the first plates of respective, succes-
          sively ordered pairs of the capacitors, for
20   decoupling, in response to a rail disable sig-
          nal, the first plate of the selected one of the
          capacitors from the first plate of the capaci-
          tors of lower and higher rank; and·
      C ladder logic means coupled to the C rung and C rail
25   switching network, for providing, in response to
          the digital input code, said C rung enable sig-
          nal and said C rung disable signal.

3. The converter of claim 2 wherein the capacitors com-
prising the capacitance means are binarily weighted, with
30 the ordering thereof from lowest rank to highest rank
being in accordance with said binary weighting.

4. The converter of claim 3 wherein the C ladder logic
means comprise:

      C decoder means having a rank ordered plurality of C
35   rung outputs coupled to respective ones of the C

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run switching elements, for providing the C rung
enable signal on a particular one of the C rung
outputs in response to each digital input code;
and

5   C rail logic means comprising a rank ordered plurali-
ty of gates, the first of which has an input
coupled to the lowest ranked C rung output and
an output coupled to the first C rail switching
element, the last of which has an input coupled

10   to the highest ranked, C rung output and an out-
put coupled to the last C rail switching ele-
ment, and the balance of which have inputs
coupled to respective adjacent pairs of the C
rung outputs, beginning from lowest rank to

15   highest rank, and an output coupled to a respec-
tive one of the ranked C rail switching elements
in response to the C rung enable signal on a
particular one of the C rung outputs.

5.   The converter of claim 3 wherein the R ladder switch-
20   ing means comprise:

an R rung switching network comprising a rank ordered
plurality of R rung switching elements, each
coupled between a respective one of the step
nodes and the common rail; and

25   R logic means coupled to the R rung switching network
for providing an R rung enable signal to a par-
ticular one of the R rung switching elements in
response to the digital input code.

6.   The converter of claim 5 wherein the R logic means
30   comprise:

R decoder means comprising a rank ordered plurality
of R rung output coupled to respective ones of
the R rung switching elements, for providing the
R run enable signal on a particular one of the R

35   rung outputs in response to each digital input
code.

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7.   The converter of claim 6 wherein the first and last C rail switching elements are responsive to a second disable signal, for decoupling the first plates of the capacitance means from both of the reference voltages, and responsive

5   to a third disable signal, for decoupling the first plates from the first reference voltage and coupling the first plates to the second reference voltage.

8.   The converter of claim 7 further comprising input switching means, for coupling an analog input voltage to

10   the first plates of the capacitance means in response to the second disable signal.

9.   The converter of claim 4 further comprising a dividing capacitor interposed between the second plates of the capacitors of less than predetermined rank order and the

15   second plates of the capacitors of at least the predetermined rank order.

10.   The circuit of claim 8 further comprising:

       positive reference voltage means, for providing a
              positive reference voltage greater than the

20   second reference voltage;

       negative reference voltage means, for providing a
              negative reference less than the second refer-
              ence voltage; and

       reference switching means, for providing a particular

25   one of the positive and negative reference
              voltages as the first reference voltage in
              response to the digital input code.

AMENDED CLAIMS
(received by the International Bureau on 10 September 1982 (10.09.82))

1. (Amended) In a converter for providing an analog
output signal corresponding to a digital input code,
comprising:

   voltage divider means for providing a step voltage
      selected between first and second reference
      voltages in response to the digital input code,
      comprising:

   resistance means coupled between the first and
      second reference voltages, for developing on each
      of a rank ordered plurality of step nodes a
      predetermined step voltage between the first and
      second reference voltages; and

   R ladder switching means coupled between the
      resistance means and a common rail, for coupling,
      in response to the digital input code, a selected
      one of the step nodes to the common rail; and

   charge redistribution means coupled to the common
      rail, for providing the analog output signal as a
      function of the step voltage on the common rail
      and the digital input code, comprising:
      capacitance means comprising a rank ordered
      plurality of capacitors having respective first
      plates and interconnected second plates, for
      developing the analog output signal on the second
      plates as a function of the voltages coupled to
      the first plates, characterised by:

   C ladder switching means having a rank ordered
      plurality of C rung switching elements and a rank
      ordered plurality of C rail switching elements
      coupled to the first and second reference
      voltages, the common rail and each of the first
      plates of the capacitors, for coupling, in
      response to the digital input code, the step

voltage on the common rail to the first plate of a selected one of the capacitors, the first reference voltage to the first plates of each of the capacitors of lower rank than the selected one of the capacitors, and the second reference voltage to the first plates of each of the capacitors of higher rank than the selected one of the capacitors.

2. (Amended) A converter for providing an analog output
   signal corresponding to a digital input code,
   comprising:

       voltage divider means for providing a step voltage
           selected between the first and second reference
           voltages in response to the digital input code,
           comprising:

               resistance means coupled between the first and
               second reference voltages, for developing on
               each of a plurality of step nodes a
               predetermined step voltage between the first
               and second reference voltages;

           R ladder switching means coupled between the
               resistance means and a common rail, for
               coupling, in response to the digital code, a
               selected one of the step nodes to the common
               rail; and

       charge redistribution means coupled to the common
           rail, for providing the analog output signal as
           a function of the step voltage on the common
           rail and the digital input code, characterized
           by:

           capacitance means comprising a rank ordered
               plurality of capacitors having respective first
               plates and interconnected second plates, for
               developing the analog output signal on the
               second plates as a function of the voltages
               coupled to the first plates;

           a C rung switching network comprising a rank
               ordered plurality of C rung switching elements,
               each coupled between the first plate of a
               respective one of the capacitors and the common
               rail, for coupling a respective one of the
               first plates to the common rail in response to
               a respective C rung enable signal;

           a C rail switching network comprising a rank

ordered plurality of C rail switching elements,
the first of which is coupled between the first
reference voltage and the first plate of the
capacitor of lowest rank, the last of which is
coupled between the second reference voltage
and the first plate of the capacitor of highest
rank, and the balance of which are coupled
between the first plates of respective,
successively ordered pairs of the capacitors,
for decoupling, in response to a rail disable
signal, the first plate of the selected one of
the capacitors of lower and higher rank; and

C ladder logic means coupled to the C rung and C
rail switching networks, for providing, in
response to the digital input code, said C rung
enable signal and said C rail disable signal.

3. (Amended) The converter of claim 2 wherein the
capacitors comprising the capacitance means are
characterized by being binarily weighted, with the
ordering thereof from lowest rank to highest rank being
in accordance with said binary weighting.

4. (Amended) The converter of claim 3 wherein the C ladder
logic means are characterized by:

C decoder means having a rank ordered plurality of C
rung outputs coupled to respective ones of the C

rung switching elements, for providing the C rung
enable signal on a particular one of the C rung
outputs in response to each digital input code;
and

C rail logic means comprising a rank ordered
plurality of gates, the first of which has an
input coupled to the lowest ranked C rung output
and an output coupled to the first C rail
switching element, the last of which has an input
coupled to the highest ranked C rung output and
an output coupled to the last C rail switching
element, and the balance of which have inputs
coupled to respective adjacent pairs of the C
rung outputs, beginning from lowest rank to
highest rank, and an output coupled to a
respective one of the ranked C rail switching ·
elements in response to the C rung enable signal
on a particular one of the C rung outputs.

5.   (Amended) The converter of claim 2 wherein the R ladder
     switching means are characterized by:
          an R rung switching network comprising a rank
          ordered plurality of R rung switching elements,
          each coupled between a respective one of the step
          nodes and the common rail; and
     R logic means coupled to the R rung switching
          network for providing an R rung enable signal to
          a particular one of the R rung switching elements
          in response to the digital input code.

6.   (Amended) The converter of claim 5 wherein the R logic
     means are characterized by:
          R decoder means comprising a rank ordered plurality
          of R rung output coupled to respective ones of
          the R rung switching elements, for providing the

R rung enable signal on a particular one of the R
rung outputs in response to each digital input
code.

7.   (Amended) The converter of claim 6 wherein the first
     and last C rail switching elements are responsive to a
     second disable signal, for decoupling the first plates
     of the capacitance means from both the first and second
     reference voltages, and responsive to a third disable
     signal, for decoupling the first plates of the
     capacitance means from the first reference voltage and
     coupling the first plates of the capacitance means to
     the second reference voltage.

8.   (Amended) The converter of claim 7 further
     characterised by switching means, for coupling an
     analog input voltage to the first plates of the
     capacitance means in response to the second disable
     signal.

9.   (Amended) The converter of claim 4 further comprising a
     dividing capacitor interposed between the second plates
     of the capacitors of less than a predetermined rank
     order and the second plates of the capacitors of at
     least the predetermined rank order.

10. (Amended) The circuit of claim 8 further characterized
     by:
          positive reference voltage means, for providing a
               positive reference voltage greater than the
               second reference voltage; and
          negative reference voltage means, for providing a
               negative reference less than the second reference
               voltage; and
          reference switching means, for providing a
               particular one of the positive and negative
               reference voltage in response to the digital
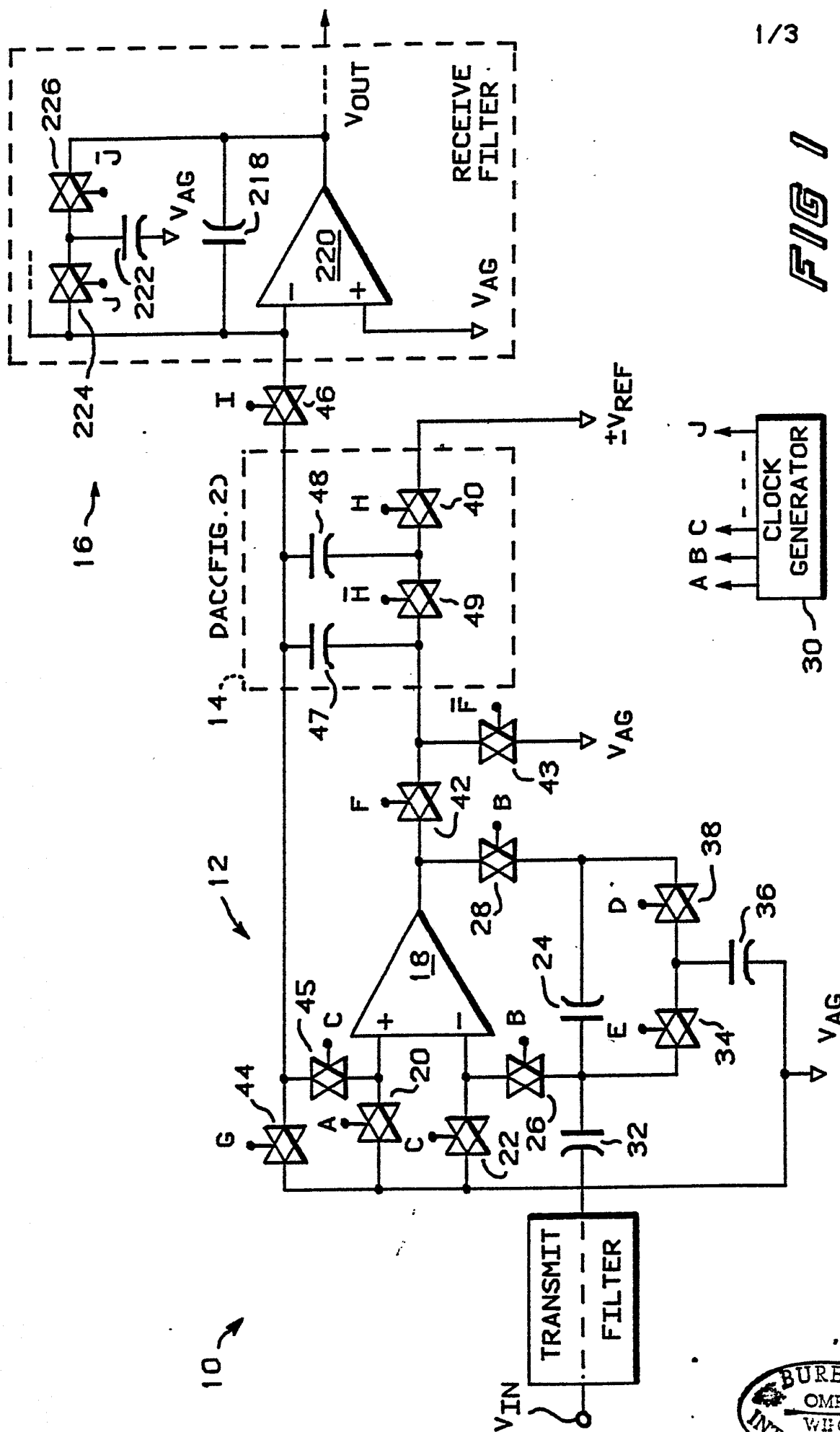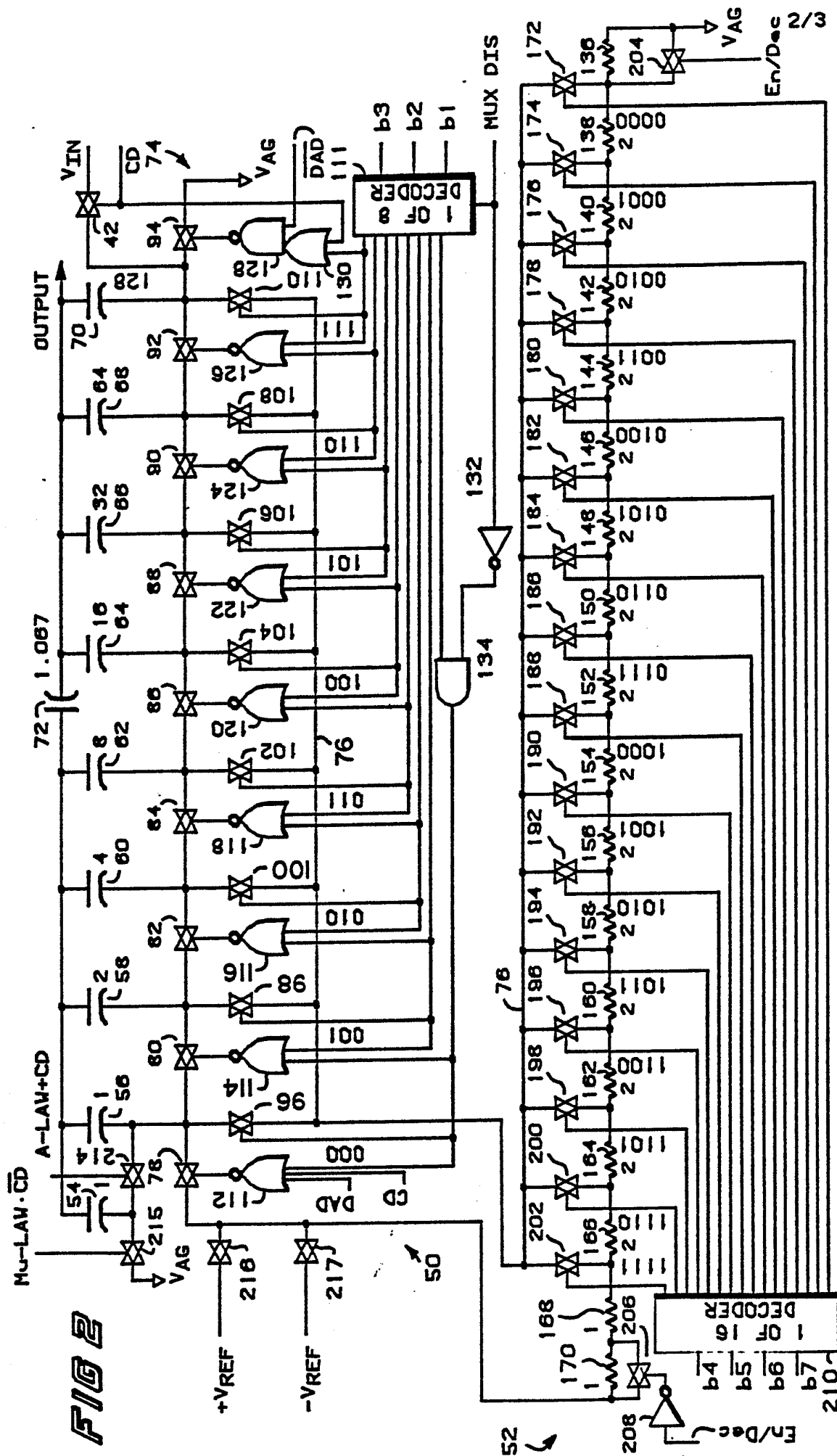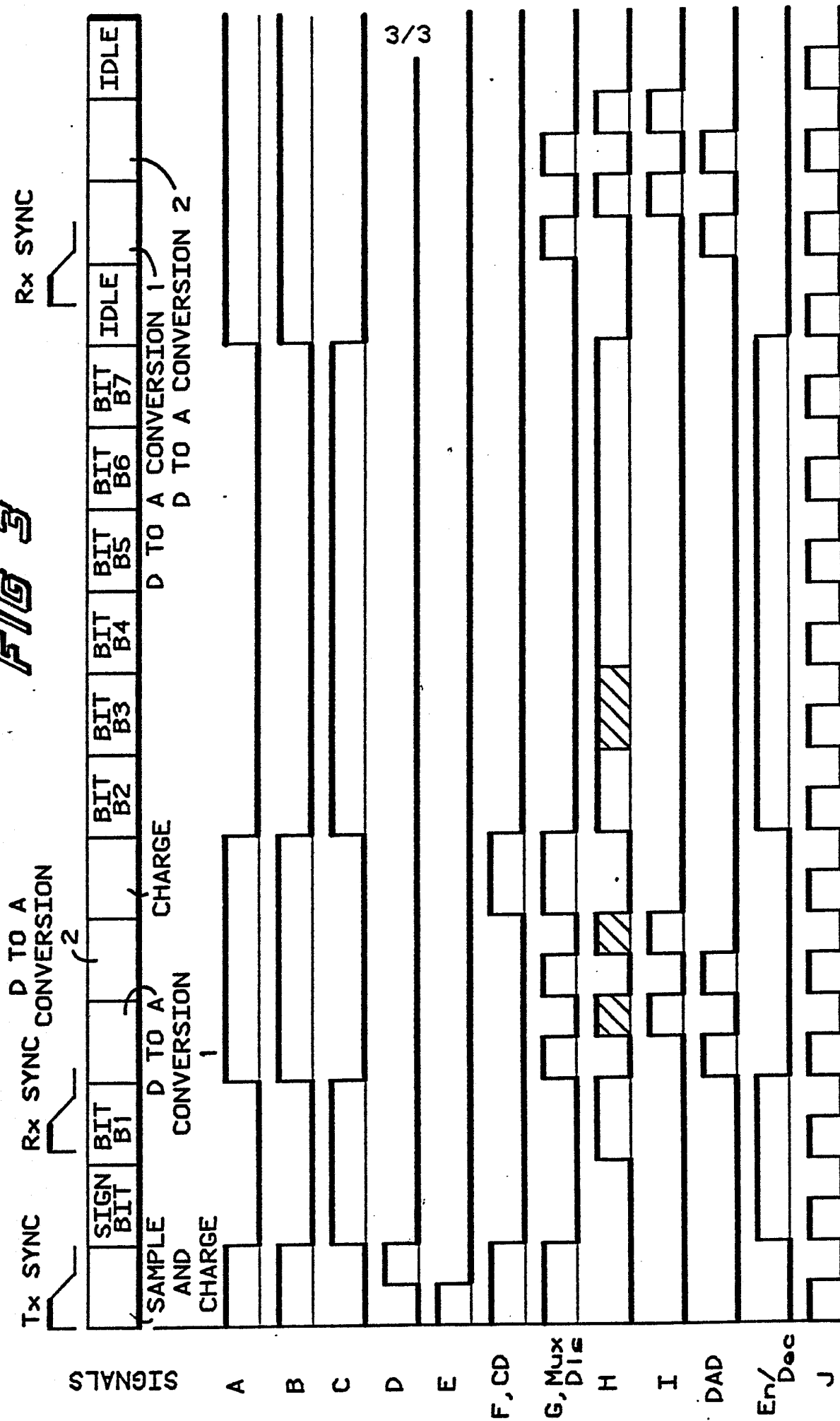   input code.

BUREAU
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FIG 1

FIG 2

FIG 3

FIG 3

INTERNATIONAL SEARCH REPORT

International Application No **PCT/US 8 2 / 0 0 5 1 5**

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. CL3 H03k 13/02
US. CL. 340/347 DA

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	340/347DA 340/347AD 340/347C

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [*]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	N IEEE Journal of Solid State Circuits Vol. SC-14 No. 6 Published December 1979 Pages 961-969 Yusuf Haque et al Note Fig. 2,	1
X	N IEEE Journal of Solid-State Circuits Vol. SC-14 No. 1 Published Feb. 1979 Pg. 65-73 J,T, Caves et al	1

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
July 13, 1982	**29 JUL 1982**
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/UB	Charles D. Miller