United States Patent [19]

Rosenthal

[11] **3,781,848**

[45] **Dec. 25, 1973**

[54] **DISPLAY SYSTEM**

[75] Inventor: **Jerome A. Rosenthal,** Brighton, N.Y.

[73] Assignee: **Xerox Corporation,** Stamford, Conn.

[22] Filed: **Dec. 28, 1971**

[21] Appl. No.: **212,934**

[52] **U.S. Cl.** ..... **340/324 A,** 315/18

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** ..... 340/324 A

[56] **References Cited**

UNITED STATES PATENTS

3,540,032	11/1970	Criscimagna et al.	340/324 A
3,696,388	10/1972	Eichelberger	340/324 A
3,329,948	7/1967	Halsted	340/324 A
3,325,802	6/1967	Bacon	340/324 A
3,537,098	10/1970	Nielsen et al.	340/324 A

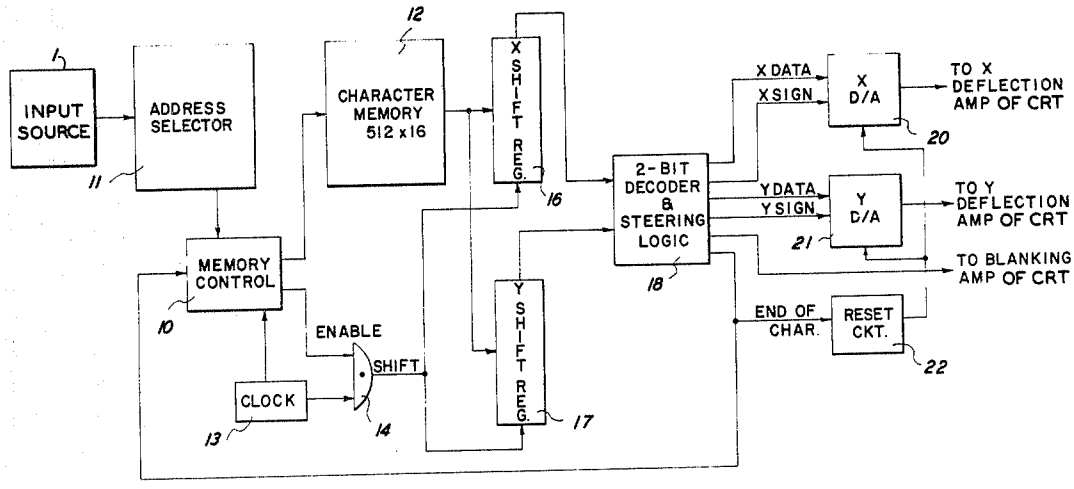
Primary Examiner—David L. Trafton

Attorney—James J. Ralabate et al.

[57] **ABSTRACT**

Apparatus for generating characters or symbols by deflecting the electron beam of a cathode ray tube with signals derived from a read only character memory. The character memory provides an output under the influence of memory control. This output is loaded into registers and then fed as a bit stream to a decoder. The decoder interprets the bit stream and sends X and Y increments and control signals to digital to analog converters which generate strokes to form the desired characters on the screen of the cathode ray tube.

4 Claims, 2 Drawing Figures



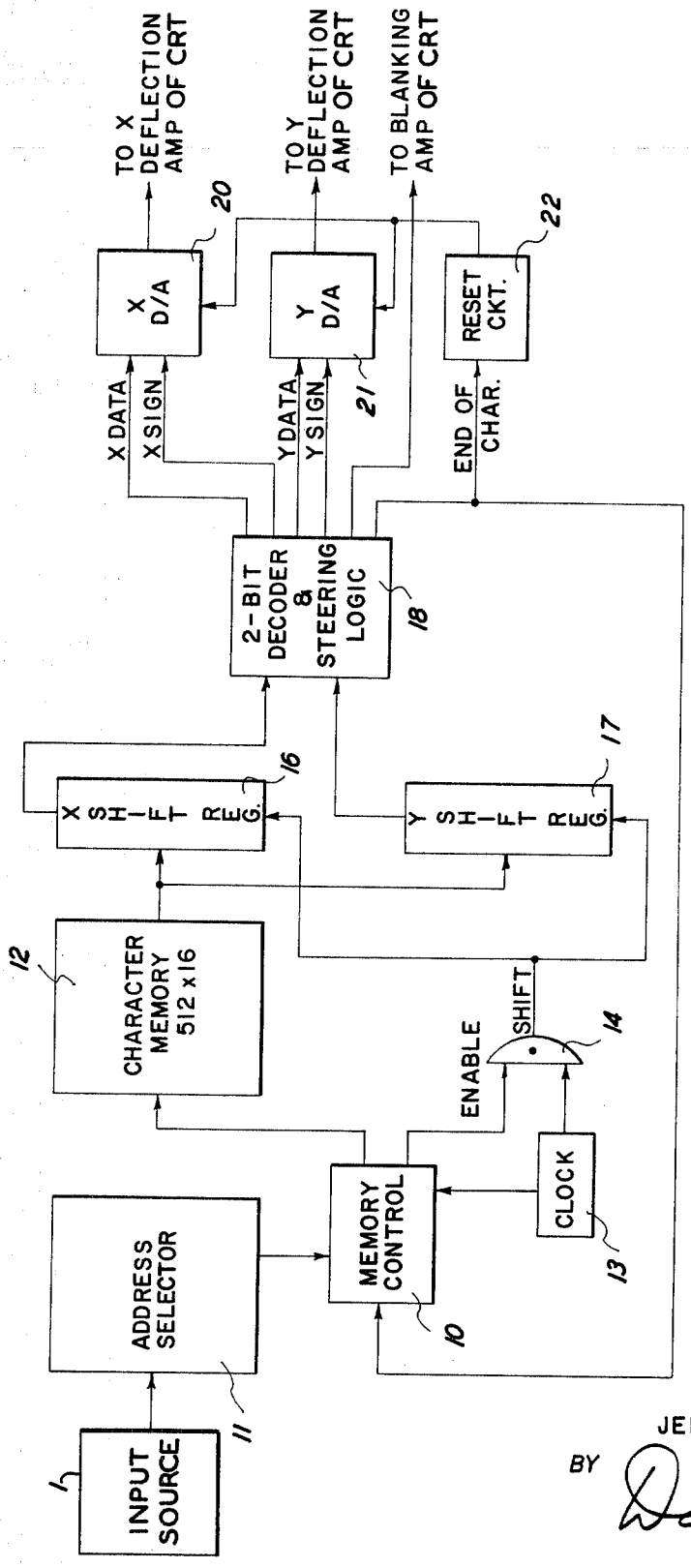
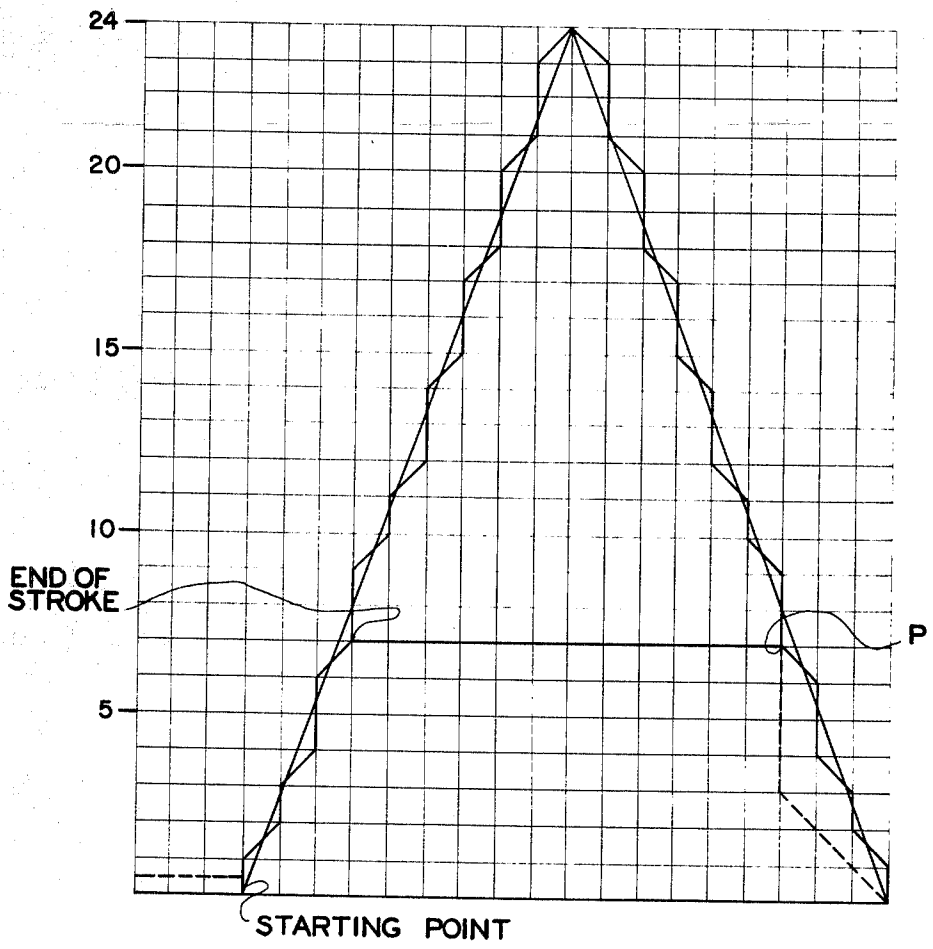


FIG. 1

INVENTOR
JEROME A. ROSENTHAL

BY

ATTORNEY



F1	F2	F3	F4	F5	F6	F7	F8
1 1 1 0 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 1							
0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1							

F9	F10	F11	F12	F13	F14	F15	F16
0 1 1 1 0 0 1 0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 0							
0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0							

F17	F18	F19	F20	F21	F22	F23
1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0						
1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1						

EXAMPLE OF CHARACTER CODING

FIG. 2

DISPLAY SYSTEM

This invention relates to character generating apparatus. More particularly, this invention relates to an electronic character generator in which the electron beam of a cathode ray tube is deflected in order to form characters or symbols on the tube screen.

BACKGROUND OF THE INVENTION

With the advent of the computer and other rapid data transmission devices, there has come a need for systems which can effectively and speedily display the intelligence from these sources. Improvements in electromechanical printers have substantially increased speed. However, because of the problems of mechanical inertia, electromechanical printers soon reach a practical upper limit speed. To fill the need for fast responding display devices a number of electronic devices have been proposed. Among these is the character generator apparatus employing a cathode ray tube that may employ matrix, bit stream or stroke character encoding. A comparison of matrix, bit stream and stroke character encoding would show that each has certain advantages regarding such factors as memory size, ease of coding, character quality, exposure efficiency and circuit complexity. Matrix encoding systems have the disadvantages of poor exposure efficiency while requiring a large memory. However, matrix encoding has the advantages of coding ease and simple circuit configurations with moderate character quality. Stroke encoding systems have the disadvantage of difficult coding and complex circuit configuration. Nevertheless, stroke encoding systems do have the advantages of good character quality and exposure efficiency with small memory requirements. Lastly, the advantages of bit stream character encoding systems fall roughly between that of matrix and stroke systems in that memory size and circuit complexity are moderate whereas coding, character quality and exposure efficiency are good. This invention incorporates the advantages of ease of coding and circuit simplicity of the matrix character encoding system as well as the advantages of good character quality and exposure efficiency of the stroke character encoding system. In short, this invention employs a bit stream encoding system modified to incorporate the advantages of both the matrix and stroke character encoding systems.

Character generation by means of a cathode ray tube has the objective of displaying line traces on the face of the tube or screen. The line traces may represent vectors, alphanumeric characters or symbols. To provide such a display, the electron beam of the cathode ray tube is deflected from point to point along a predetermined path. To deflect the electron beam along the predetermined path, it is necesssry at each point of direction change in the path to apply the proper deflection signals to the horizontal (X-axis) and vertical (Y-axis) deflection circuits of the cathode ray tube to move the electron beam to the next point of direction change. In digitally operated display systems, these deflection signals are stored in the character memory and applied to the input circuits of the cathode ray tube at timed intervals. Digitally operated systems of the past required a great deal of programming and calculations of values of deflection signals in order to drive the electron beam across the tube screen. In addition, depending on the number and type of symbols to be generated,

digital storage and logic circuits were generally quite numerous. Also the deflection control circuits of these prior art display systems had the disadvantages of requiring precision components as well as being difficult to control.

In these prior art systems a multiplicity of current sources such as transistors and balancing resistors are utilized in order to generate line segments of characters. Since individual transistors inherently have different operating characteristics, compensating circuitry is required to offset their differing characteristics. The effects of drift and the difficulty of maintaining equal character stroke intensity are also disadvantages frequently encountered in these systems. These deficiencies of prior art systems served not only to increase the complexity of the scanning control but also to increase the expense of the display apparatus.

Accordingly, it is an object of this invention to provide an improved and inexpensive character generating apparatus.

It is another object of this invention to provide a character generating apparatus requiring less current sources for generating character strokes.

It is a further object of this invention to provide a character generating apparatus wherein all the character strokes are confined to a grid simplifying the coding of stroke signals.

It is a further object of this invention to provide a character generating apparatus wherein the electron beam of the cathode ray tube is automatically deflected to trace a symbol or character by a data bit stream input to circuits which control tube deflection.

SUMMARY OF THE INVENTION

In accordance with principles illustrative of this invention, a cathode ray tube is advantageously provided for character generation. Stroke generators activate the deflection circuits of the cathode ray tube by delivering fixed voltage pulses to current sources which in turn charge capacitors. The strokes are coded as binary bit streams for the X and Y axes. A binary "1" bit causes a fixed amount of charge to be deposited or removed from the capacitor associated with appropriate coordinates of X and Y. A binary "0" bit causes no change in the quantity of charge. The entire bit stream for constructing the character is stored in read only memory. The bit stream is read out of memory and stored in shift registers by memory control and then feed to decoder and steering logic. The decoder and steering logic interprets the bit streams and directs the X and Y incremental bit streams along with bits representing the signs of X and Y to the X and Y digital to analog converters. The decoder and steering logic also generates the signals for controlling beam blanking and end of character. The end of character signal is fed to a reset circuit which provides means for positioning the characters in the character areas as well as resetting the digital to analog converters in preparation for the generation of a new character. The blanking signal is applied directly to the blanking amplifier of the cathode ray tube. The outputs from the X and Y digital to analog converters are applied directly to the X and Y deflection amplifiers. The invention also provides means in the decoder and steering logic for distributing the "0" and "1" bits within the stream so that digitization error is minimized.

DESCRIPTION OF THE DRAWING

The foregoing will be more readily understood upon a reading of the following description in conjunction with the drawing in which:

FIG. 1 is a block schematic diagram of an illustra-tive embodiment incorporating the principles of the present invention; and

FIG. 2 shows a sample character and its code.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1 there is depicted a block schematic diagram of an illustrative embodiment incorporating the principles of this invention. All of the circuitry to implement this embodiment is well known to one of ordinary skill in the art and no detailed description thereof will be given. Six binary bits of information from an input source **1**, such as a computer, data keyboard, magnetic tape, etc., are fed into address selector **11**. The six binary bits are character selection bits and may be in ASCII, EBCDIC or other standardized code. In address selector **11** the six bit binary code is translated into a nine bit binary code designating the starting address for each character in character memory **12**. This translation may be done by any of various well known prior art techniques. Memory control **10** controls the transmission of the translated address to character memory **12**. It is to be noted that any codes specified herein are intended to be illustrative and not limiting, since it will occur to those skilled in the art that other codes could be used depending upon the number of characters or symbols desired and the amount of storage available.

Character memory **12** illustratively is organized into 16-bit words. These words are each subdivided into an eight-bit word for the X coordinate and an eight-bit word for the Y coordinate. Information for controlling the generation of a character is stored as a block of contiguous words, the aforementioned translated address defining the first word of the block.

Upon the selection of a character, a **16**-bit word is provided at the output of character memory **12**. The two eight-bit words within the 16-bit word contain the respective X and Y incremental pulse trains as well as control bits such as blanking, unblanking, X and Y sign, and end of character. From character memory **12** one eight-bit word for the X coordinate is loaded in parallel into the X shift register **16** and one eight-bit word for the Y coordinate is loaded in parallel into the Y shift register **17**. Both the X and Y eight-bit words are stored in their respective registers **16** and **17** until directed by memory control **10**, clock **13** and gate **14** to send a serial bit stream to two-bit decoder and steering logic **18**. Decoder and steering logic **18** interprets the bit stream and directs the X and Y incremental bit streams to X and Y digital to analog converters **20** and **21**, respectively. In X and Y digital to analog converters **20** and **21**, the binary bits are integrated by current sources which in turn charge or discharge capacitors and are converted into electron beam strokes for the cathode ray tube having direction and amplitude.

The strokes are coded as binary bit streams for the X and Y axes. A binary "1" bit causes a fixed amount of charge to be deposited or removed from the capacitor associated with the appropriate X and Y coordinates. A binary "0" bit causes no change in the quantity of charge on the capacitor. Decoder and steering logic **18** also generates sign X, sign Y, blanking and end of character pulses. For example, a stroke which has an X increment of four and a Y increment of two requires a bit stream of:

1111
1001,

the upper line being the bit stream for the X increment and the lower line for the Y increment. For each stroke, the X and Y "1" bits are placed in the stream to cause minimum digitization error. This is accomplished by arranging the bit stream so that it most accurately approximates the actual character shape as shown in FIG. 2 and discussed more fully hereinafter.

In order to control the bit stream, it is necessary to insert control information into the bit stream. When there is a change in X sign, Y sign, blanking, or to indicate end of character, control bits are sent along in the bit stream. Provision is made to insert three bits of control information into the X bit stream and three bits of information into the Y bit stream. The first control bits in each stream are a code which signifies that the next two bits in the stream are control information. In one implementation of the invention, the control code is "0,0" this "0,0" combination not being permitted to occur in the X and Y increment bit streams. The second two bits of the control information indicate X sign and Y sign. The third two bits indicate blank, unblank or end of character. Some examples of control bits in this implementation are:

011
000

X positive, Y negative, beam unblanked,

000
000

X negative, Y negative, beam blanked,

000
001

end of character.

The stroke from X and Y digital to analog converters **20** and **21** are applied directly to the X and Y deflection amplifiers of the cathode ray tube (not shown). An end of character signal from decoder **18** is applied directly to reset circuit **22** which positions the character in sequence on the cathode ray tube and also resets the capacitors in X and Y digital to analog converters **20** and **21** in preparation for the start of a new character. Finally, a blanking signal from decoder **18** is applied directly to the blanking amplifier of the cathode ray tube (not shown).

A sample character and its code are shown in FIG. **2**. In order to code this character, using a character height of 24 units, 170 bits of memory is required. Recalling that the top line represents an X increment bit stream and the line below it represents a Y increment bit stream, the character A is formed on the grid as described hereinafter. For the sake of illustration the bit streams have been blocked into frames numbering 1–23. In frame **1** it is seen that it takes six bits to move the electron beam to the starting point of the letter A. The first two 0,0 code bits of frame **2** indicate that four control bits are to follow. The two 1, 1 bits indicate sign X positive and sign Y positive. The next 1,0 bits represent beam unblanked. Frames **3–8** initiate the strokes to form the first leg of the letter A moving upward. At the end of frame **8** a change of direction is required. Therefore, frame **9** contains control bits indicating X

positive, Y negative and beam unblanked. Frames **10–15** initiate the strokes to form the second leg of the letter A moving downward. At the end of frame **15** change of direction as well as blanking is required. Control bits in frame **16** provide for a negative X increment, a positive Y increment and beam blanked. Frames **17** and **18** provide bits to move the blanked beam up to point P. At this time frame **19** contains control bits for a negative X increment, a negative Y increment, and beam unblanked. The crossbar is formed by the bits in frames **20–22.** Frame **23** contains end of character bits which prepares the system for formation of a new character of symbol.

As can be seen from FIG. **2** the resultant character is generated in continuous line segments of substantially equal stroke lengths on the grid. This permits characters having substantially constant intensity. Moreover, the characters are formed at high speed and have good character definition independent of character size and location.

It will be apparent to those skilled in the art that the present invention may be used generally in display systems and is not limited to the embodiment described. Numerous other variations, modifications and adaptations of the present invention will be apparent to those skilled in the art, and such as come within the spirit and scope of the appended claims are considered to be embraced by the present invention.

What is claimed is:

1. Character generating apparatus for controlling the horizontal and vertical deflection circuits of a cathode ray tube to move an electron beam across the screen of the cathode ray tube to display a character thereon, said apparatus comprising

memory means including addressable storage locations for storing indicia representing characters, said indicia including horizontal and vertical deflection increment information,

means for receiving a character code defining a character to be displayed and translating said received code into a memory means address corresponding to the character defined by the received character code,

means responsive to said memory means address for retrieving from said memory means the indicia representing said defined character,

horizontal and vertical deflection increment shift register means,

means for loading the horizontal and vertical deflection increment information of said retrieved indicia in parallel fashion into the respective shift register means,

means for serially shifting said horizontal and vertical deflection increment information of said retrieved indicia out of the respective shift register means as respective bit streams for the horizontal and vertical deflection circuits of said cathode ray tube,

a single horizontal converter and a single vertical converter for converting the respective bit streams into stroke signals for application to the respective deflection circuits, and

logic means responsive to said bit streams for controlling the deflection circuits of said cathode ray tube in accordance with the stroke signals to display said defined character on the screen of said cathode ray tube.

2. The apparatus of claim **1** wherein said logic means includes means for recognizing control signals in said bit streams indicating direction of travel for said electron beam and blanking of said electron beam, and responsive to said control signals for controlling said deflection circuits in accordance with said control signals.

3. The apparatus of claim **2** wherein said logic means further comprises means for recognizing an end of character control signal in said bit streams for resetting said deflection circuits so as to position said electron beam for the display of another character.

4. Character generating apparatus comprising

a cathode ray tube having X and Y axis deflection control circuits for controlling the movement of the electron beam of the cathode ray tube across the screen of said cathode ray tube,

address selector means for receiving a character code from a data source and transforming said character code into an address code,

character memory means responsive to said address code for each character in memory for furnishing two words which contain control bits and respective X and Y incremental pulse train bits,

shift register means for receiving said two words and for converting each of said words into a bit stream,

decoder and steering logic means for interpreting said control bits in said bit streams,

a single X digital to analog converter and a single Y digital to analog converter responsive to said decoder and steering logic means for converting the respective X and Y incremental pulse train bits in said bit streams into character stroke signals, and

X and Y deflection amplifiers responsive to said character stroke signals for deflecting the electron beam on the screen of said cathode ray tube to form characters thereon.

* * * * *