



(51) International Patent Classification:

H03M 1/56 (2006.01) *H03M 1/06* (2006.01)
H04N 5/357 (2011.01) *H03M 1/12* (2006.01)

(21) International Application Number:

PCT/EP2018/068953

(22) International Filing Date:

12 July 2018 (12.07.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

17183983.0 31 July 2017 (31.07.2017) EP

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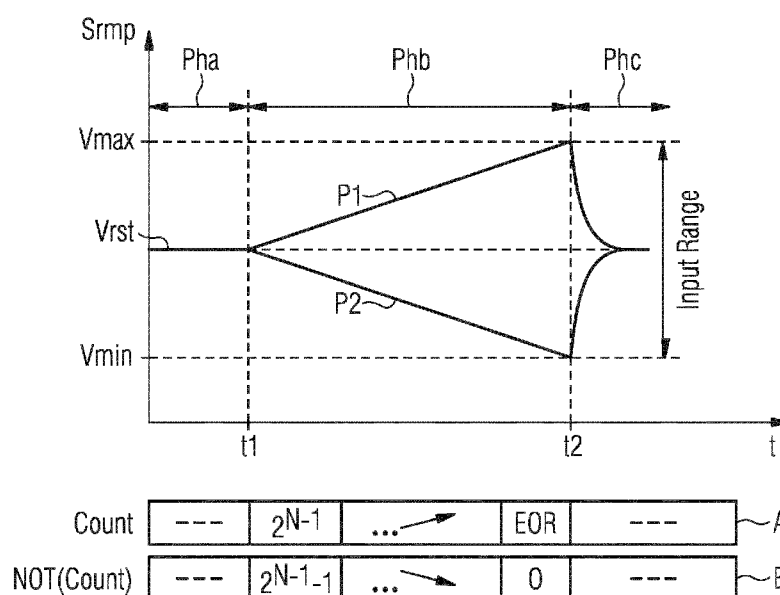
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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) Title: ANALOG-TO-DIGITAL CONVERTER CIRCUIT AND METHOD FOR ANALOG-TO-DIGITAL CONVERSION

FIG 1



(57) **Abstract:** In an embodiment an analog-to-digital converter circuit has an input (20) for receiving at least a first analog signal level (Sin), a ramp generator (RG) adapted to provide a ramp signal (Srmp) having a constant and adjustable starting level (Vrst) which splits into a first section (P1) which is rising and a second section (P2) which is falling concurrently to the first section's (P1) rising, wherein the starting level (Vrst) lies within an input range of the analog-to-digital converter circuit, a comparison unit (CMP) which is coupled by its first input to the input (20) of the analog-to-digital converter circuit and is coupled by its second input in a switchable manner to the ramp generator (RG), a counter (CNT) which is coupled to a control unit (CTL), and the control unit (CTL) which is coupled to an output of the comparison unit (CMP), wherein the control (CTL) unit is prepared to enable the counter (CNT) depending on a comparison of the ramp signal (Srmp) with the first analog signal level (Sin) and to determine a digital value (Dv) as a function of a count



SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

Description

ANALOG-TO-DIGITAL CONVERTER CIRCUIT AND METHOD FOR ANALOG-TO-DIGITAL CONVERSION

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The disclosure is directed to an analog-to-digital converter circuit and a method for analog-to-digital conversion.

10 The field of this disclosure concerns analog-to-digital converters, ADCs, especially, ADCs using a ramp signal for the conversion. Such converters are called ramp ADCs.

ADCs are widely used in image sensors, for example image sensors implemented in complementary metal-oxide-
15 semiconductor, CMOS, technology. One known type of ADC in image sensors is a ramp ADC which is generally employed in CMOS image sensors due to its compact size and simplicity, allowing to easily perform multiple conversions in parallel. Image sensors comprise an array of unit elements, called
20 pixels. The array of pixels is exposed to radiation during an exposure period and, subsequently, the signal value of each pixel is read from the array.

Pixel signals are analog signals. An ADC is provided to
25 convert the analog pixel signal into a digital value. The ADCs are a major building block in image sensors and are often the bottleneck in the readout block of the image sensor in terms of frame rate, dynamic range and power consumption. Various arrangements have been proposed where analog-to-
30 digital conversion is performed in parallel for analog signal values read from columns of an array. To avoid various column-to-column non-uniformities, all column ADCs share the same ramp voltage or ramp signal generated by a ramp

generator. This helps to increase the speed at which the pixel array can be read. Therefore, these ADCs are typically used in a column of pixels for the conversion of a full row of pixels within a single conversion cycle.

5

One problem with existing ramp ADCs is their slow conversion time, i.e. long conversion cycle. The conversion cycle generally refers to the time needed for an ADC to provide a digital output equivalent to an analog input. A conversion
10 with the resolution of N bits performed by a state of the art converter typically requires 2^N clock cycles of the clock used within the converter.

Each time a conversion is performed, the ramp signal used in
15 state of the art ADCs must be reset to a well-defined value, corresponding to one of the limits of an ADC's input swing. With the ever increasing speed of the ramp ADCs, this ramp-reset time is becoming an important fraction of the total conversion time. Furthermore, as the trend in imaging is
20 towards higher resolution, dead time caused by the ramp reset becomes even larger as the ramp generator's load increases proportionally to the number of columns of the array.

When choosing an ADC, there is always a trade-off between
25 factors such as resolution, speed and accuracy. For CMOS image sensors, an accurate ADC is mandatory, otherwise the added error will increase the overall image noise. Removing accuracy from the equation, the need for a compromise between speed and resolution still remains and, consequently, an
30 equilibrium between frame rate and color depth. Other factors such as area and power consumption can also be important.

Due to the accuracy requirement, a state of the art ADC typically used in CMOS image sensors usually performs slow conversions. Presently, one of the big challenges for CMOS image sensors design is the improvement of conversion time in order to achieve more frames per second or higher resolutions without neglecting accuracy.

It is therefore an object of the present disclosure to provide an analog-to-digital converter circuit and a method for analog to digital conversion with improved conversion speed. Additional objects are to improve speed-resolution ratio and reduce power consumption during reset of an ADC while allowing for flexible signal dependent steepness.

The objects are achieved by the subject-matter of the independent claims. Embodiments and developments are defined in the dependent claims.

The definitions as described above also apply to the following description unless stated otherwise.

In one embodiment an analog-to-digital converter circuit has an input for receiving at least a first analog signal level, a ramp generator, a comparison unit, a counter and a control unit. The ramp generator is adapted to provide a ramp signal. The ramp signal has a constant and adjustable starting level which splits into a first section which is rising, and a second section which is falling concurrently to the first section's rising. The starting level of the ramp signal lies within an input range of the analog-to-digital converter circuit. The comparison unit is coupled by its first input to the input of the analog-to-digital converter circuit and is further coupled by its second input in a switchable manner to

the ramp generator. The counter is coupled to the control unit. The control unit is coupled to an output of the comparison unit. The control unit is prepared to enable the counter depending on a comparison of the ramp signal with at least the first analog signal level and to determine a digital value as a function of a count of the counter reached at an intersection point of the ramp signal with at least the first analog signal level.

10 The comparison unit is configured to compare the ramp signal with the first analog signal level and to provide therefrom a comparison output to the control unit. The control unit activates the counter depending on said comparison output and determines the digital value which corresponds to the first
15 analog signal level as a function of the count of the counter which has been reached at the intersection point of the ramp signal with the at least first analog signal level.

By means of the special shape of the ramp signal generated by the ramp generator, the time needed for a conversion of the first analog signal level into the digital value is greatly reduced. When compared with state of the art ramp ADCs, the digital value is determined and provided in half time but with the same resolution. Conversion speed is greatly
20 improved.

Due to its shape the presently defined ramp signal having a constant and adjustable starting level which splits or forks into the first and the second sections, said ramp signal may also be denoted as a dual slope ramp with common reset. First
30 and second sections represent the dual slope, while the starting level is called the common reset.

The first analog signal level comprises for instance a pixel signal of an image sensor.

5 The count reached by the counter is represented by a number between zero and two to the power of N minus 1 denoted 2^N-1 , wherein N refers to a resolution of the ADC circuit generally given in bits.

10 The intersection point of the ramp signal with the at least first analog signal level refers to the point where the ramp signal, especially either its first section or its second section, reaches the level of the first analog signal level.

15 In a development, the counter is configured to count in one direction only starting from the middle of its predefined digital scale.

The predefined digital scale of the counter represents a digital output scale of the ADC circuit. The digital scale is predefined by the resolution which is to be achieved by the ADC circuit. If the resolution amounts to N bits, the digital scale ranges from zero to 2^N-1 . Due to the counter's configuration to start counting from the middle of the predefined digital scale, the counter only needs to count
20 half the scale amounting to 2 to the power of N-1 counts or codes instead of 2 to the power of N codes amounting to the full scale as of state of the art ramp ADCs. The other half of the scale is covered by a logical correlation within the defined ADC circuit.

30

In other words, the ADC circuit generates the ramp signal with two simultaneous slopes, i.e. the first section and the second section, which are moving away from a common point,

denoted the constant and adjustable starting level on the analog domain. The starting level may also be denoted as the reset point. Said starting level is located within the input range of the ADC circuit, for example, for a fully linear scale at the middle of the ADC input range. By this, each section of the ramp signal covers half of the input range and due to the concurrency of first and second section, the input range of the ADC circuit is fully covered in half the time when compared with a state of the art single slope ramp ADC known to those skilled in the art. First and second sections of the ramp signal correlate with a first and a second half of the digital output scale. Consequently, the time needed for a conversion, i.e. for determining the digital output value is reduced to half the time.

The counter is configured to either count upwards starting from the middle of the predefined digital scale by increasing the count. Alternatively, the counter is configured to count downwards starting from the middle of the predefined digital scale by decreasing the count.

In a further development, the control unit is adapted to control operation of the analog-to-digital converter circuit during a conversion cycle comprising a ramp selection phase, a counting phase and a reset phase.

The control unit controls the operation of the ADC circuit by means of at least one control signal which controls the ramp generator, the comparison unit and the counter, respectively, and switchable connections within the ADC circuit. A switchable connection refers to a connection between two components of a circuit which is realized by a switch. A

switch is implemented by a transistor or a transmission gate, for example.

In a development, the control unit comprises a configuration unit and an inversion unit. The configuration unit is adapted to provide a configuration signal depending on a comparison of the constant and adjustable starting level of the ramp signal with at least the first analog signal level during the ramp selection phase. The inversion unit is coupled in a switchable manner to at least one output of the counter and during the counting phase is prepared to provide the count directly or in its inverted form depending on the configuration signal.

During the ramp selection phase of a conversion cycle the ramp signal assumes its constant and adjustable starting level. During said phase the configuration unit provides the configuration signal depending on the comparison of the starting level of the ramp signal with the first analog signal level. The configuration signal therefore reflects the result of a rough comparison between the first analog signal level at the input of the ADC circuit and the starting level of the ramp signal. By means of the configuration signal, either the first section or the second section of the ramp signal is used in a comparison in the subsequent counting phase. The counter is enabled as soon as the ramp signal splits into the first and the second section. This marks the beginning of the counting phase. By means of the configuration signal the provided count is directly used in the determination of the digital output value or the count is inverted and used in its inverted form to determine the digital output value.

The configuration unit is prepared to provide the configuration signal once in a conversion cycle, i.e. during the ramp selection phase.

- 5 The configuration signal represents an example of the control signal generated by the control unit. In the case that the counter is configured to count upwards and the first section of the ramp is used in a comparison, the count is used directly as the digital value. In the case that the counter
10 is configured to count upwards and the second section is used in the comparison, the count is used in its inverted form.

In a development, the ramp generator comprises a first capacitor, a second capacitor, a first current generating
15 unit and a second current generating unit. The first capacitor is coupled in a switchable manner under control of the control unit to an output of the first current generating unit and the second capacitor is coupled in a switchable manner under control of the control unit to an output of the
20 second current generating unit. The first capacitor is connected in a switchable manner under control of the control unit to the second capacitor. The first current generating unit is configured to provide a positive charging current having an adjustable level at its output in order to generate
25 the first section of the ramp signal in cooperation with the first capacitor. The second current generating unit is configured to provide a negative charging current having an adjustable level at its output in order to generate the second section of the ramp signal in cooperation with the
30 second capacitor.

The first current generating unit generates the positive charging current with an adjustable level. The positive

charging current is provided to the first capacitor and under control of the control unit the first section of the ramp signal is thus generated. The second current generating unit generates the negative charging current with an adjustable
5 level which is provided to the second capacitor. Thus, under the control of the control unit the second section of the ramp signal is generated.

10 In an example implementation capacitance values of first and second capacitances are adapted to each other.

In an example, first and second current generating units are implemented by means of at least one current source and current mirrors. Alternatively, first and second current
15 generating units are realized by voltage integrators.

In a development, the ramp generator further comprises a buffer component with an output for providing a reset signal having a constant and adjustable level. The output of the
20 buffer component is connected in a switchable manner under control of the control unit to the first and to the second capacitor in order to generate the starting level of the ramp signal during the reset phase and the ramp selection phase.

25 During the reset phase, the ramp signal is reset to its constant starting level. For this purpose, first and second capacitors are directly connected so that a charge transfer occurs between both capacitors until an equilibrium point. Next, the buffer component is connected to a connection point
30 between first and second capacitor, in order to ensure that said connection point assumes the starting level of the ramp signal. The level of the reset signal provided by the buffer component is adjusted to the starting level of the ramp

signal. The buffer component ensures that the starting level of the ramp signal does not oscillate between different conversion cycles.

5 The described way of resetting the ramp signal to its constant starting level achieves a reduction in power consumption when compared with a state of the art single slope ramp ADC. As a single slope ramp increases from the lowest to the highest value of the input range of an ADC,
10 during reset of the ramp it is necessary to discharge the ramp to the lowest value for performing the next conversion. For this purpose usually strong buffers are needed causing considerable current consumption, especially during a ramp reset. In the proposed ADC circuit, using the ramp signal
15 with first and second sections, the reset can be partially performed by transferring charge between first and second capacitors, also called ramp capacitors, such that the current consumption peak is much smaller than in state of the art single slope ADCs.

20

As both sections of the ramp signal, i.e. first section and second section, start from a common point, there is no risk of discontinuities occurring during conversion. In an example implementation the starting level of the ramp signal is
25 adjusted to the middle of the input range of the ADC circuit and first and second sections are generated with substantially the same slope. Reset of the ramp signal in this case can be called a self-reset. Since the first and second section of the ramp signal are generated by charging
30 or discharging the first or the second capacitor and as the slope of both sections is symmetrical, both sections are at the same distance from the starting level of the ramp signal at the end of a counting phase.

By optimizing the reset of the ramp signal as described above, time for resetting is saved when compared to state of the art ADCs. Consequently, a conversion cycle is shorter.

5

In one embodiment an image sensor has a pixel array and at least one ADC circuit as defined above. The ADC circuit is employed in a column parallel topology.

10 The pixel array may have one pixel or one times K pixels or L times K pixels. The pixels are arranged in columns. In the column parallel topology the ramp signal is shared by all columns while several analog-to-digital conversions are completed simultaneously.

15

Due to improvement in conversion speed achieved with the specified ADC circuit, the image sensor is enabled to realize a higher frame rate.

20 In one embodiment a method for analog to digital conversion comprises the following steps:

- receiving at least a first analog signal level,
- generating a ramp signal having a constant and adjustable starting level which splits into a first section which is rising and a second section which is falling concurrently to
25 the first section's rising, wherein the starting level lies within an input range of the analog-to-digital converter circuit,
- comparing at least the first analog signal level with the
30 ramp signal,
- enabling a counting in function of the comparing of the ramp signal with the at least first analog signal level, and

- determining a digital value as a function of a count reached at an intersection point of the ramp signal with at least the first analog signal level.

- 5 By employing the ramp signal defined above in the analog-to-digital conversion, an improvement on conversion speed/resolution ratio is achieved. The method allows to increase the frame rate of an image sensor without losing resolution or it allows to increase resolution without
10 compromising frame rate.

The method described herein is implemented by means of the ADC circuit described above in one example implementation.

- 15 In a development the conversion is performed during a conversion cycle which comprises a ramp selection phase, a counting phase, and a reset phase.

- In a further development, during the reset phase the ramp
20 signal assumes its constant and adjustable starting level. During the ramp selection phase the at least first analog signal level is compared to the starting level of the ramp signal and a configuration signal is generated accordingly for selecting the first or the second section of the ramp
25 signal in the subsequent counting phase. During the counting phase the ramp signal splits into the first and the second section. One of the first section and the second section is used for comparing at least the first analog signal level with the ramp signal depending on the configuration signal
30 generated during the precedent ramp selection phase.

During one conversion cycle, the digital value corresponding to the first analog signal level is determined. For this

purpose, in the ramp selection phase the first analog signal is roughly compared to the starting level of the ramp signal in order to decide which of the sections, either the first or the second section, to be generated during the subsequent counting phase is to be used for the comparison during the counting phase. For example, if the first analog signal level lies above the constant starting level of the ramp signal, the first section shall be used during the counting phase. If the analog signal level lies below the starting level of the ramp signal, the second section of the ramp signal shall be used in the subsequent counting phase. The configuration signal is generated to indicate this selection. No matter which one of the first or the second section of the ramp signal is used, both sections are generated during the counting phase. Only one of said sections of the ramp signal is used in the counting phase for the comparison with the first analog signal level as indicated by the configuration signal. The counting phase ends as soon as the first section of the ramp signal reaches the highest level of the ADC's input range and the second section reaches the lowest level of the ADC's input range. In the subsequent reset phase, the ramp signal is reset to its starting level.

Power consumption and time spent during the reset phase is greatly reduced when compared to state of the art ramp analog-to-digital conversions due to the fact that at the end of the counting phase both sections of the ramp signal are at a similar distance from the starting level and only have to be reset to said starting level.

In a development depending on the configuration signal generated during the ramp selection phase, either the count reached at an intersection point of the ramp signal with at

least the first analog signal is determined as the digital value, or an inverted form of the count reached at an intersection point of the ramp signal with at least the first analog signal level is determined as the digital value.

5

In a development the counting starts from the middle of the predefined digital scale and is effected by counting upwards until the highest value of the digital scale or by counting downwards until the lowest value of the digital scale.

10

As detailed above, the counting is effected in one direction only.

In a development the generation of the ramp signal is effected such that the starting level of the ramp signal is adjusted to the middle of the input range of the ADC circuit and the first section's rising is mirror-symmetric to the second section's falling. Therein the starting level represents the axis of symmetry.

20

In this development the first and second sections have substantially the same gradient or slope.

In an alternative development the generation of the ramp signal is effected such that the first section is rising according to a first adjustable gradient and the second section is falling according to a second adjustable gradient.

25

According to said alternative development, the ramp signal has two different slopes when splitting from the starting level. The steepness or gradient of the first and second sections is adjusted, for example depending on the level of the first analog signal level. Thereby, a flexible signal-

30

dependent steepness of the ramp signal is enabled. In this way, the influence of photon shot noise is mitigated.

The text below explains the proposed ADC circuit and
5 corresponding method in detail using exemplary embodiments with reference to the drawings. Components and circuit elements that are functionally identical or have the identical effect bear identical reference numbers. In so far as circuit parts or components correspond to one another in
10 function, a description of them will not be repeated in each of the following figures.

Figure 1 shows an embodiment example of a ramp signal as proposed to be used in the proposed ADC circuit;
15

Figure 2 shows an embodiment example of an ADC circuit as proposed;

Figure 3 shows timing diagram examples for the ADC circuit as of Figure 2;
20

Figure 4 shows a first example of an analog-to-digital conversion as proposed;

25 Figure 5 shows a second example of an analog-to-digital conversion as proposed;

Figure 6 shows a comparison with a state of the art ADC;

30 Figure 7 shows another comparison with a state of the art ADC;

Figure 8 shows an example of a ramp signal to be used in the proposed ADC circuit;

Figures 9A, 9B and 9C each show different shapes of ramp
5 signals to be used in the proposed ADC circuit;

Figure 10 shows a correlated double-sampling conversion using the proposed ADC converter and method.

10 Figure 1 shows an embodiment example of a ramp signal as proposed to be used in the proposed ADC circuit. The ramp signal S_{rmp} is depicted in relation to time t . A full conversion cycle of the ramp signal S_{rmp} is illustrated having a ramp selection phase Pha , a counting phase Phb , and
15 a reset phase Phc . During the ramp selection phase Pha the ramp signal S_{rmp} is at its constant start level V_{rst} . At point-in-time t_1 the counting phase Phb starts and the ramp signal S_{rmp} splits into a first section $P1$ and a second section $P2$. It can be discerned that the first section $P1$ is
20 rising, while the second section $P2$ is falling. At a point-in-time t_2 the first section $P1$ of the ramp signal S_{rmp} has reached a maximum level V_{max} , while the second section $P2$ of the ramp signal S_{rmp} has reached a minimum level V_{min} . The region between the minimum level V_{min} and the maximum level
25 V_{max} represents an input range of the ADC circuit which is based on the depicted ramp signal S_{rmp} . At point-in-time t_2 the reset phase Phc starts in which the first section $P1$ and the second section $P2$ of the ramp S_{rmp} resume the constant starting level V_{rst} .

30

The ramp signal S_{rmp} is implemented, for example, by a voltage. Consequently, the starting level V_{rst} , the minimum

level V_{min} and the maximum level V_{max} each represent a voltage level.

After the ramp signal S_{rmp} has reached its starting level

5 V_{rst} in the reset phase Phc , the next conversion cycle can be started with the next ramp selection phase Pha .

Beneath the illustration of the ramp signal S_{rmp} Figure 1 shows counts of a counter of the proposed ADC circuit.

10 Therein, counts corresponding to the first section $P1$ are presented in line A and inverted counts denoted "NOT (Count)" of the counter corresponding to the second section $P2$ are presented in line B. As explained above, the ADC circuit has a resolution of N bits. The total scale of the counter
15 consequently ranges from zero to the highest code denoted "end of range" or "EOR", here $2^N - 1$. As defined above, the counter starts at the middle of its digital scale, i.e. at count $2^{(N-1)}$, which corresponds to the analog starting level V_{rst} of the ramp signal S_{rmp} . For the rising section $P1$ the
20 counts are increased until the highest code EOR at point-in-time t_2 . The inverted counts on line B corresponding to the falling section $P2$ of the ramp signal S_{rmp} are determined by a logical NOT operation to the counts of line A, as the counter is configured to count upwards.

25

From analyzing the digital scale of the counter employed in the ADC circuit, it can be seen that the first and the last code are correlated by the logical NOT operation or inversion. The same correlation exists between the second and
30 the penultimate code, between the third and the third-last code and so on, until the middle of the scale, as illustrated in Table 1.

First Half of Scale			Second Half of Scale	
Decimal	Binary		Binary	Decimal
0	0000 0000 0000	Logical NOT ↔	1111 1111 1111	4095 (2^N-1 =EOR)
1	0000 0000 0001		1111 1111 1110	4094
2	0000 0000 0010		1111 1111 1101	4093
...	...		...	...
2046	0111 1111 1110		1000 0000 0001	2049
2047	0111 1111 1111		1000 0000 0000	2048 (2^{N-1})

Table 1

By employing the ramp signal S_{rmp} as depicted in Figure 1, the logical correlation from Table 1 is transposed to the analog domain of the analog input signal and the analog ramp signal S_{rmp} .

Figure 2 shows an embodiment example of an analog-to-digital converter circuit as proposed. The ADC circuit comprises an input 20 for receiving at least a first analog signal level S_{in} . The ADC circuit further comprises a ramp generator RG which is adapted to provide the ramp signal S_{rmp} , a comparison unit CMP, a counter CNT and a control unit CTL. The first analog signal level S_{in} is provided to a first input of the comparison unit CMP. A second input of the comparison unit CMP is coupled in a switchable manner to an output of the ramp generator RG for receiving the ramp signal S_{rmp} . One output of the comparison unit CMP is coupled to the control unit CTL. At the output of the comparison unit CMP a comparison signal S_{cm} is provided which is a function of a comparison between the analog signal level S_{in} and the ramp signal S_{rmp} .

In the depicted example the comparison unit CMP is implemented by an operational amplifier having the output at which the comparison signal S_{cm} is provided and an inverted

output at which an inverted comparison signal $\overline{\text{Scm}}$ is provided.

The counter CNT is coupled to the control unit CTL and is
5 enabled by a charging signal Sch. The control unit CTL
comprises a configuration unit FF and an inversion unit INV.
The configuration unit FF is configured to provide a
configuration signal Sdc depending on a comparison of the
constant and adjustable starting level Vrst of the ramp
10 signal Srmp with the first analog signal level Sin during the
ramp selection phase. The inversion unit INV is coupled in a
switchable manner to at least one output of the counter CNT
and is prepared to provide the count directly or in its
inverted form depending on the configuration signal Sdc
15 during the counting phase.

In the depicted example the configuration unit FF is realized
by a flip-flop, especially by a D-flip-flop. The D-input of
the configuration unit FF receives the comparison signal Scm.
20 A clock input of the configuration unit FF receives an enable
signal Sen. At a Q output of the configuration unit FF the
configuration signal Sdc is provided as described above.

In this example the inversion unit INV is realized by a full
25 bridge comprising switches SW45, SW46, SW47 and SW48.
Switches SW45 and SW47 are each controlled by the
configuration signal Sdc. Switches Sw46 and Sw48 are
controlled by the configuration signal Sdc in its inverted
form as indicated by empty circuits next to respective
30 control inputs of said switches signifying a logical
inversion or NOT operation of the provided configuration
signal Sdc. The full bridge of the inversion unit INV
receives the count Ct and the inverted count NCt from the

counter CNT at its inputs. Depending on the configuration signal Sdc and the corresponding configuration of the switches, the count Ct or the inverted count NCT is provided as digital value Dv at an output of the inversion unit INV.

- 5 Optionally, the inversion unit INV has a second output for providing an inverted digital value NDv which corresponds to the digital value Dv in its inverted form.

- In the depicted example the control unit CTL further
10 comprises a processing subunit PRC. The processing subunit PRC is connected in a switchable manner to the outputs of the comparison unit CMP, i.e. switch SW43 which is controlled by the configuration signal Sdc connects the positive output of the comparison unit CMP to the processing subunit PRC, while
15 switch SW44 which is controlled by the inverted configuration signal Sdc connects the negative output of the comparison unit CMP to the processing subunit PRC. The processing subunit PRC is further connected to the output of the inversion unit INV at which the digital value Dv is provided.
20 Optionally, the processing subunit PRC is further connected to the second output of the inversion unit INV at which the inverted digital value NDv is provided. The processing subunit PRC has a storage for storing the determined digital value Dv in each conversion cycle. Storing of the digital
25 value Dv is enabled by the comparison signal Scm.

- The ramp generator RG comprises a first capacitor C1, a second capacitor C2, a first current generating unit CGU1 and a second current generating unit CGU2. An output of the first
30 current generating unit CGU1 is coupled by means of switch SW31 to a first terminal of the first capacitor C1. A second terminal of the first capacitor C1 is coupled to a reference potential terminal 10. The first current generating unit CGU1

is configured to provide a positive charging current I_1 to the first capacitor C_1 . An output of the second current generating unit CGU2 is coupled by switch SW32 to a first terminal of the second capacitor C_2 . A second terminal of the second capacitor C_2 is connected to the reference potential terminal 10. The second current generating unit CGU2 is configured to provide a negative charging current I_2 at its output. The first terminal of the first capacitor C_1 is coupled to the first terminal of the second capacitor C_2 by means of switches SW11 and SW12 which are operated concurrently under control of an equalize signal Seq provided by the control unit CTL.

The second current generating unit CGU2 comprises a current source CS for providing a reference current I_{ref} and a current mirror. The current source CS is coupled to a supply potential terminal 11 providing, for example, supply potential VDD and to an input of the current mirror. Instead of potential VDD another potential which enables the intended reference current I_{ref} can be used as known to those skilled in the art. An output of the current mirror forms an output of the second current generating unit CGU2. The first current generating unit CGU1 also comprises a current mirror. An input of the first current generating unit CGU1 is coupled to the second current generating unit CGU2. It receives an input current which is a function of the reference current I_{ref} . An output of the current mirror forms an output of the first current generating unit CGU1. The current mirror of the first current generating unit CGU1 is realized, for example by PMOS transistors as depicted in Figure 2. The current mirror of the second current generating unit CGU2 is implemented for example by NMOS transistors as depicted in Figure 2. A level of the positive charging current I_1 can therefore be adjusted

by adjusting the level of the reference current I_{ref} and a ratio realized by means of the current mirror of the first current generating unit CGU1. A level of the negative charging current I_2 can be adjusted by means of adjusting the level of the reference current I_{ref} and the ratio of the current mirror of the second current generating unit CGU2. The positive charging current I_1 is provided to the first terminal of the first capacitor C_1 by means of switch SW31 which is controlled by the charging signal S_{ch} provided by the control unit CTL. The negative charging current I_2 is provided to the first terminal of the second capacitor C_2 by means of a switch SW32 which is controlled by the charging signal S_{ch} .

The ramp generator RG additionally comprises a buffer component BUF. The buffer component BUF has an input for receiving a ramp reset level V_{rr} and an output for providing a reset signal S_{rst} as a function of the ramp reset level V_{rr} . In the depicted example the buffer component BUF is realized by an operational amplifier configured in unity feedback. The output of the buffer component BUF is coupled by means of switch SW2 to the first terminals of first and second capacitors C_1 , C_2 . Switch SW2 is controlled by a ramp reset signal S_{rr} which is provided by the control unit CTL.

A connection point between the output of the first current generating unit CGU1 and the first terminal of the first capacitor C_1 forms a first output of the ramp generator RG. A connection point between the output of the second current generating unit CGU2 and the first terminal of the second capacitor C_2 forms a second output of the ramp generator RG. The first output is coupled by means of switch SW41 to the second input of the comparison unit CMP. The second output of

the ramp generator RG is coupled by means of switch SW42 to the second input of the comparison unit CMP. Switch SW42 is controlled by the configuration signal Sdc, while switch SW41 is controlled by the configuration signal Sdc in its inverted form, such that either switch SW42 or switch SW41 is closed.

At the first output of the ramp generator RG, the first section P1 of the ramp signal Srmp is provided due to the charging of the first capacitor C1 by the positive charging current I1. At the second output of the ramp generator RG, the second section P2 of the ramp signal Srmp is provided due to the discharging of the second capacitor C2 by means of the negative charging current I2. Under control of the configuration signal Sdc either the first section P1 or the second section P2 of the ramp signal Srmp is supplied to the second input of the comparison unit CMP during the counting phase.

Detailed functioning of the circuit depicted in Figure 2 is described with reference to Figure 3.

In the case that the proposed ADC circuit of Figure 2 is used in an image sensor in a column parallel topology, the ramp generator RG and the counter CNT are shared between all the columns of a pixel array within the image sensor. Each column needs a separate comparison unit CMP and a separate control unit CTL.

The control unit CTL has means for generating the equalize signal Seq, the enable signal Sen, the charging signal Sch, and the ramp reset signal Srr. Generation of said control signals is implemented, for example in the processing subunit PRC.

Figure 3 shows timing diagram examples for the ADC circuit as of Figure 2. From top to bottom, different signals are depicted with relation to time t . First, the ramp signal S_{rmp} is shown with the constant starting level V_{rst} and first and second sections $P1$, $P2$. The first analog signal level S_{in} is presented beneath the ramp signal S_{rmp} . The next line shows the configuration signal S_{dc} below which the equalize signal S_{eq} is depicted. The next line shows the ramp reset signal S_{rr} followed by the charging signal S_{ch} . The bottom line shows the enable signal S_{en} .

As indicated at the top one and a half conversion cycles are shown wherein each conversion cycle has a reset phase Phc , a ramp selection phase Pha and a counting phase Phb . A conversion cycle either begins or ends with the reset phase Phc . In the depicted example a conversion cycle begins with a reset phase Phc . During the first conversion cycle the analog signal level S_{in} lies below the starting level V_{rst} of the ramp signal S_{rmp} . The signals below the time line are digital signals, in particular binary signals, having two logical levels.

In a first part of the reset phase Phc of the first conversion cycle, switches $SW11$ and $SW12$ are closed by means of the equalize signal S_{eq} . Charge is transferred from the first capacitor $C1$ to the second capacitor $C2$ until an equilibrium point is reached. As soon as the ramp reset signal S_{rr} goes to a logical high at point-in-time t_a switch $SW2$ is closed and the output of the buffer component BUF is connected to the connection point between first and second capacitors $C1$, $C2$. By this, the ramp signal S_{rmp} is forced to assume its starting level V_{rst} . By this, the offset between

first and second capacitor C1 and C2 is removed and the starting level Vrst of the ramp signal is maintained unchanged between different conversion cycles. At point-in-time tb the equalize signal Seq and the ramp reset signal Srr go back to logical low and switches SW11, SW12 and SW2 are opened. The ramp selection phase Pha starts. During this phase, the enable signal Sen goes to logical high such that the comparison unit CMP and the configuration unit FF are activated. One of the switches SW41 or SW42 is closed from a previous conversion cycle, thereby connecting either the potential at the first terminal of the first capacitor C1 or the potential at the first terminal of the second capacitor C2 to the second input of the comparison unit CMP. Both potentials are at the same level during the ramp selection phase Pha. Consequently, the starting level Vrst of the ramp signal Srm is compared with the first analog signal level Sin. As the level of the first analog signal the level Sin is below the starting level Vrst, the positive output of the comparison unit CMP goes to high which is reflected and stored at output Q of the flip-flop of the configuration unit FF. Consequently, the configuration signal Sdc goes to high which closes switch SW32 to provide the second section P2 to the second input of the comparison unit CMP. Furthermore, by means of the configuration signal Sdc switch SW44 is closed connecting the negative output of the comparison unit CMP to the control input of the processing subunit PRC. Within the inversion unit INV by means of the configuration signal Sdc switches SW45 and SW47 are closed such that the inverted count NCT of counter CNT is provided as the digital value Dv. This means that although counter CNT is prepared to only count upwards from the middle of the digital scale, decreasing counts are provided as the count.

Shortly after the configuration of the switches by means of the configuration signal Sdc is completed, at point-in-time t1 the charging signal Sch goes to logical high which closes switches SW31 and SW32 for providing the positive charging current I1 to the first capacitor C1 and the negative charging current I2 to the second capacitor C2. At point-in-time t1 the ramp signal Srm consequently splits into the first section P1 and second section P2. At t1 the counting phase Phb starts and the counter CNT is activated.

As can be seen during the counting phase Phb of the first conversion cycle, both sections P1, P2 of the ramp signal Srm are generated concurrently, while just the second section P2 is supplied to the comparison unit CMP. At point-in-time t1' the second section P2 of the ramp signal Srm crosses the level of the first analog signal at level Sin. This changes the output of the comparison unit which enables storage of the digital value Dv reflecting the count Ct reached at point-in-time t1' within the processing subunit PRC. First and second sections P1, P2 of the ramp signal Srm are generated until the end of the counting phase Phb when the maximum and the minimum level of the input range are reached at point-in-time t2.

At point-in-time t2 the next conversion cycle starts with a reset phase Phc in which the ramp signal Srm is reset to its constant starting level Vrst.

Shortly before the end of the counting phase Phb the enable signal Sen assumes a logical zero which deactivates the comparison unit CMP and the configuration unit FF. At point-in-time t2 the charging signal Sch goes to zero which

disconnects first and second current generating units CGU1, CGU2 from first and second capacitors C1, C2.

5 In the generation of the enable signal Sen response time of the comparison unit CMP is taken into account. In the example of Figure 3 the starting level Vrst of the ramp signal Srmp coincides with the middle of the input range ranging from the maximum level Vmax to the minimum level Vmin. First and second sections P1, P2 are generated mirror-symmetric with
10 respect to the starting level Vrst.

In an optimization when the ADC circuit is used in an image sensor in a column parallel topology, in order to keep the loads associated with each ramp independent from the input
15 signal level a dummy comparator or a dummy input stage is additionally used in the circuit of Figure 2. The unused section of the ramp signal is connected in this case to the dummy comparator for performance and linearity improvement.

20 The value of the starting level Vrst, the level of the reference current Iref and the end of the range of the digital scale of the counter are selected in consistency with the desired input range to be achieved by the ADC circuit.

25 In an alternative implementation of the ADC circuit the current source CS and the current mirrors of the first and the second current generating unit CGU1, CGU2 are replaced by respective voltage integrators. The remaining circuitry is consequently adapted as known to those skilled in the art.

30

Figure 4 shows a first example of an analog-to-digital conversion as proposed. In this example the ramp signal Srmp and the first analog signal level Sin are shown in relation

to time t . Beneath the signal diagram corresponding counts are depicted. In this example the first analog signal level is higher than the starting level V_{rst} of the ramp signal S_{rmp} . Accordingly, in the ramp selection phase Pha it is
5 determined to use the first section $P1$ of the ramp signal S_{rmp} in the subsequent counting phase Phb . During the counting phase Phb the counter counts upwards until the intersection point between the first section $P1$ of the ramp signal S_{rmp} and the first analog signal level S_{in} at point-
10 in-time $t1'$. At this point-in-time, the counter has reached a count of 2952 which is provided as the digital value Dv of the conversion cycle.

Figure 5 shows a second example of a conversion as proposed.
15 Figure 5 coincides with the conversion of Figure 4 with the exception that the first analog signal level S_{in} in this example is below the starting level V_{rst} of the ramp signal S_{rmp} . Therefore, in the ramp selection phase Pha it is determined to use the second section $P2$ of the ramp signal
20 S_{rmp} in the subsequent counting phase Phb . Consequently, the count 2952 reached at point-in-time $t1'$ where the second section $P2$ of the ramp signal S_{rmp} crosses the first analog signal level S_{in} is used in its inverted form. Accordingly, the digital value Dv determined during the depicted
25 conversion cycle amounts to 1143.

Figure 6 shows a comparison between a state-of-the-art single slope ramp ADC and the proposed ADC circuit using a dual slope ramp. In the upper part of Figure 6 a timing diagram
30 corresponding to a state-of-the-art single slope ramp ADC is depicted, while in the bottom of Figure 6 the timing of the proposed ADC circuit is shown. In both cases a first analog signal level S_{in} corresponding to a reference level of a

pixel and subsequently a second analog signal level S_{in2} are converted in two consecutive conversion cycles CC1, CC2.

The upper diagram shows the course of a state-of-the-art
5 single-slope ramp signal S_r with a reset level V_r and the course of the first analog signal level S_{in} , as well as the course of the second analog signal level S_{in2} . It can be seen that in the first conversion cycle CC1 a first amount of time T_{REF} is needed for conversion of the first analog signal
10 level S_{in} . Subsequently, the amount of time R_{REF} is spent on resetting the ramp S_r back to its reset level. In the second conversion cycle CC2 an amount of time T_{SIG} is needed for conversion of the second analog signal level S_{in2} . Subsequently, an amount of time R_{SIG} is spent on resetting
15 the ramp S_r back to its reset level.

The diagram below shows the course of the newly proposed ramp signal S_{rmp} having the starting level V_{rst} and the course of first and second analog signal levels S_{in} , S_{in2} . It can be
20 seen that in the first conversion cycle CC1 only half the amount of time T_{SIG} is spent in converting the first analog signal level S_{in} . Subsequently the ramp signal S_{rmp} is reset to its starting level V_{rst} in the amount of time R_{REF} . In the second conversion cycle CC2 for conversion of the second
25 analog signal level S_{in2} again half the amount of time T_{SIG} is spent. Subsequently, the ramp signal S_{rmp} is reset to its starting level V_{rst} .

The comparison between the upper diagram and the lower
30 diagram reveals that the amount of time T_S is saved, which is depicted in the lower diagram by the hatched section. The proposed ADC converter and corresponding method for conversion therefore achieve an improvement with respect to

conversion time when compared to state-of-the-art single-slope ADCs.

Figure 7 shows another comparison between a state-of-the-art ADC and the proposed ADC circuit. Conversion time is depicted in relation to quantization levels. Line a) represents the speed resolution ratio of a state of the art ADC, while line b) represents the speed resolution ratio of the proposed ADC circuit.

For providing a resolution of N bits or N quantization levels, the state-of-the-art ADC needs the amount of time T. For providing the same resolution of quantization levels or bits, the proposed ADC circuit only needs half the amount of time T. Furthermore, if the proposed ADC circuit is given the full amount of time T for a conversion cycle, a resolution of two times N is achieved as can be seen from line b). The improvement of speed resolution ratio is clearly visible from Figure 7.

Figure 8 shows an example of a ramp signal to be used in the proposed ADC circuit. In contrast to the fully linear scale used for the ramp signals, for instance of Figure 5 described above, where the same absolute value of current is provided to the first and the second capacitors for generating symmetrical slopes, Figure 8 is based on a dual step approach. This means that different absolute values of positive and negative charging currents are provided to the first and second capacitors for generating non-symmetrical slopes P1, P2 representing first and second section P1, P2 of the ramp signal S_{rmp} . The rate of charge in the first section P1 differs from the rate of discharge in the the second section P2 as indicated by the values "Y" and "2Y" reflecting

the difference in gradient between first and second section P1, P2. Consequently, light-dependent slopes are achieved by the two sections P1, P2. In detail, for low light, the first section P1 with the smaller gradient is provided, while for
5 high light the second section P2 with the higher gradient is generated. This allows to mitigate photon shot noise. The starting level V_{rst} provides a threshold for step changing. In other words, by adjusting the starting level V_{rst} , the level on the analog input range from which a step size of the
10 ADC circuit is increased or decreased can be controlled.

Figures 9A, 9B and 9C each show a different shape of the ramp signal to be used with the proposed ADC circuit, e.g. as of Figure 2. In each case the course of the ramp signal S_{rmp} is
15 depicted with relation to time t . Each of the depicted shapes is based on a multi-step approach, meaning that different absolute values of positive and negative charging currents are provided to first and second capacitors for generating non-symmetrical first and second sections P1, P2 of the ramp
20 signal S_{rmp} with an additional change of charge and discharge rate during a conversion cycle. The starting level V_{rst} and the count provide the thresholds for step variation.

In order to realize the shapes of the ramp signals S_{rmp}
25 depicted in Figures 8A, 8B, 9A, 9B and 9C, it is necessary to adapt first and second current generating units as of Figure 2. For example, the current mirrors of said current generating units shall be implemented with more branches and a corresponding logic to control these branches as known to
30 those skilled in the art.

Figure 10 shows a correlated double-sampling conversion using the proposed ADC converter. The course of the ramp signal

Srmp, the first and the second analog signal levels Sin, Sin2 are depicted in relation to time t. The first analog signal level Sin in this case again represents a reset or dark level of a pixel, while the second analog signal level Sin2 represents the signal level of said pixel. Here, both values are converted in one conversion cycle. The second analog signal level Sin2 is converted as described above. A corresponding digital value Dv2 is determined at count 2952 which is reached at the intersection point of the first section P1 of the ramp signal Srmp with the second analog signal level Sin2. The counter continues counting until the intersection point of the second section P2 of the ramp signal Srmp with the first analog signal level Sin. The inverted count 25, representing the digital value Dv, is stored and the counter is stopped. Consequently, a new end of range EOR' is achieved shown in line A. This refers to a new input range from a new maximum level Vmax2 to the first analog signal level Sin.

In order to implement the described correlated double-sampling in one conversion cycle, it is necessary to adapt the implementation of the comparison unit as of Figure 2 by adding a second comparator for comparing the second analog signal level Sin2 to the ramp signal Srmp. Furthermore, the counter has to be implemented as a local counter.

Although, the effective input range is limited to the new input range as indicated in Figure 10, and some codes at the bottom and at the top of the scale will be missed, it is assumed that the reset level of a pixel is the lowest possible value, so that the lost codes have no significant impact on the dynamic range. Furthermore, in this case the codes which are missed at the top of the scale can be

minimized with an efficient gain configuration and adequate starting level V_{rst} of the ramp signal S_{rmp} . Consequently, the correlated double-sampling conversion can be simplified to a subtraction between the digital value $Dv2$ and the first
5 digital value Dv in the digital domain.

It is to be understood that any feature described in relation to any one embodiment may be used alone, or in combination with other features described, and may also be used in
10 combination with one or more features of any other of the embodiments, or any combination of any other of the embodiments unless described as alternative. Furthermore, equivalents and modifications not described above may also be employed without departing from the scope of the ADC circuit
15 and corresponding method which are defined in the accompanying claims.

Reference list

	P1, P2	first, second section
	Srmp	ramp signal
5	Sin	first analog signal level
	Sdc	configuration signal
	Vrst	starting level
	Pha, Phb, Phc	phase
	t	time
10	CTL	control unit
	CMP	comparison unit
	CNT	counter
	BUF	buffer component
	CGU1, CGU2	current generating unit
15	RG	ramp generator
	PRC	processing subunit
	FF	configuration unit
	INV	inversion unit
	C1, C2	capacitor
20	I1, I2	charging current
	SW11, SW12, SW2	switch
	SW31, SW32	switch
	SW41, SW42, SW43, SW44	switch
	SW45, SW46, SW47	switch
25	10, 11, 20	terminal
	A, B, a), b)	line
	t1, t1', t2	point-in-time
	Scm	comparison signal
	$\overline{\text{Scm}}$	inverted comparison signal
30	Srst	reset signal
	Srr	ramp reset signal
	Sch	charging signal
	Seq	equalize signal

	Sen	enable signal
	Vrr	ramp reset level
	Iref	reference current
	CS	current source
5	Ct	count
	NCt	inverted count
	Dv, DV2	digital value
	NDv	inverted digital value
	Sr	single-slope ramp signal
10	CC1, CC2	conversion cycle
	TREF, RREF, TSIG, RSIG, TS, T	amount of time
	Vmin, Vmax, Vmax2	level

Claims

1. An analog-to-digital converter circuit having

- an input (20) for receiving at least a first analog
5 signal level (Sin),
- a ramp generator (RG) adapted to provide a ramp signal (Srmp) having a constant and adjustable starting level (Vrst) which splits into a first section (P1) which is rising and a second section (P2) which is falling concurrently to the
10 first section's (P1) rising, wherein the starting level (Vrst) lies within an input range of the analog-to-digital converter circuit,
- a comparison unit (CMP) which is coupled by its first input to the input (20) of the analog-to-digital converter
15 circuit and is coupled by its second input in a switchable manner to the ramp generator (RG),
- a counter (CNT) which is coupled to a control unit (CTL), and
- the control unit (CTL) which is coupled to an output of
20 the comparison unit (CMP),

wherein the control (CTL) unit is prepared to enable the counter (CNT) depending on a comparison of the ramp signal (Srmp) with at least the first analog signal level (Sin) and to determine a digital value (Dv) as a function of a count
25 (Ct) of the counter (CNT) reached at an intersection point of the ramp signal (Vramp) with at least the first analog signal level (Sin).

2. The analog-to-digital converter circuit according to claim
30 1,

wherein the counter (CNT) is configured to count in one direction only starting from the middle of its predefined digital scale.

3. The analog-to-digital converter circuit according to claim 1 or 2,

wherein the control unit (CTL) is adapted to control

5 operation of the analog-to-digital converter circuit during a conversion cycle (CC1, CC2) comprising a ramp selection phase (Pha), a counting phase (Phb), and a reset phase (Phc).

10 4. The analog-to-digital converter circuit according to claim 3,

wherein the control unit (CTL) comprises a configuration unit (FF) and an inversion unit (INV), wherein the configuration unit (FF) is adapted to provide a configuration signal (Sdc) depending on a comparison of the constant and adjustable

15 starting level (Vrst) of the ramp signal (Srmp) with at least the first analog signal level (Sin) during the ramp selection phase, and

wherein the inversion unit (INV) is coupled in a switchable manner to at least one output of the counter (CNT) and during
20 the counting phase is prepared to provide the count (Ct) directly or in its inverted form depending on the configuration signal (Sdc).

25 5. The analog-to-digital converter circuit according to one of claims 1 to 4,

wherein the ramp generator (RG) comprises a first capacitor (C1), a second capacitor (C2), a first current generating unit (CGU1) and a second current generating unit (CGU2),

wherein the first capacitor (C1) is coupled in a switchable
30 manner under control of the control unit (CTL) to an output of the first current generating unit (CGU1) and the second capacitor (C2) is coupled in a switchable manner under control of the control unit (CTL) to an output of the second

current generating unit (CGU2), and wherein the first capacitor (C1) is connected in a switchable manner under control of the control unit (CTL) to the second capacitor (C2),

5 wherein the first current generating unit (CGU1) is configured to provide a positive charging current (I1) having an adjustable level at its output in order to generate the first section (P1) of the ramp signal (Srmp) in cooperation with the first capacitor (C1),

10 wherein the second current generating unit (CGU2) is configured to provide a negative charging current (I2) having an adjustable level at its output in order to generate the second section (P2) of the ramp signal (Srmp) in cooperation with the second capacitor (C2).

15

6. The analog-to-digital converter circuit according to claim 5,

wherein the ramp generator (RG) further comprises a buffer component (BUF) with an output for providing a reset signal (Srst) having a constant and adjustable level, the output of the buffer component (BUF) being connected in a switchable manner under control of the control unit (CTL) to the first and the second capacitor (C1, C2) in order to generate the starting level of the ramp signal (Srmp) during the reset phase and the ramp selection phase.

20

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7. An image sensor having a pixel array and at least one analog-to-digital converter circuit according to one of claims 1 to 6 in a column parallel topology.

8. A method for analog-to-digital conversion comprising the following steps:

- receiving at least a first analog signal level (Sin),

- generating a ramp signal (Srmp) having a constant and adjustable starting level (Vrst) which splits into a first section (P1) which is rising and a second section (P2) which is falling concurrently to the first section's (P1) rising,
5 wherein the starting level (Vrst) lies within an input range of an analog-to-digital converter circuit,
- comparing at least the first analog signal level (Sin) with the ramp signal (Srmp),
- enabling a counting in function of the comparing of the
10 ramp signal (Sramp) with at least the first analog signal level (Sin), and
- determining a digital value (Dv) as a function of a count (Ct) reached at an intersection point of the ramp signal (Sramp) with at least the first analog signal level
15 (Sin).

9. The method for analog-to-digital conversion according to claim 8,
wherein the conversion is performed during a conversion cycle
20 which comprises a ramp selection phase (Pha), a counting phase (Phb), and a reset phase (Phc).

10. The method for analog-to-digital conversion according to claim 9,
25 wherein during the reset phase (Phc) the ramp signal (Srmp) assumes its constant and adjustable starting level (Vrst), wherein during the ramp selection phase (Pha) the at least first analog signal level (Sin) is compared to the starting level (Vrst) of the ramp signal (Srmp) and a configuration
30 signal (Sdc) is generated accordingly for selecting the first or the second section (P1, P2) of the ramp signal (Srmp) in the subsequent counting phase, and

wherein during the counting phase (Phb) the ramp signal (Srmp) splits into the first and the second section (P1, P2), wherein one of the first and the second section (P1, P2) is used for comparing at least the first analog signal level (Sin) with the ramp signal (Srmp) depending on the configuration signal (Sdc) generated during the precedent ramp selection phase (Pha).

11. The method for analog-to-digital conversion according to claim 10, wherein depending on the configuration signal (Sdc) generated during the ramp selection phase (Pha) either the count (Ct) reached at the intersection point of the ramp signal (Vramp) with at least the first analog signal level (Sin) is determined as the digital value (Dv), or an inverted form of the count (Ct) reached at the intersection point of the ramp signal (Vramp) with at least the first analog signal level (Sin) is determined as the digital value (Dv).

12. The method for analog-to-digital conversion according to one of claims 8 to 11, wherein the counting starts from the middle of the predefined digital scale and is effected by counting upwards until the highest value of the digital scale or by counting downwards until the lowest value of the digital scale.

13. The method for analog-to-digital conversion according to one of claims 8 to 12, wherein the generating the ramp signal (Srmp) is effected such that the starting level (Vrst) of the ramp signal (Srmp) is adjusted to the middle of the input range of the analog-to-digital converter circuit and the first section's (P1) rising is mirror symmetric to the second section's (P2)

falling, wherein the starting level (Vrst) represents the axis of symmetry.

14. The method for analog-to-digital conversion according to
5 one of claims 8 to 12,
wherein the generating the ramp signal (Srmp) is effected
such that the first section (P1) is rising according to a
first adjustable gradient and that the second section (P2) is
falling according to a second adjustable gradient.

FIG 1

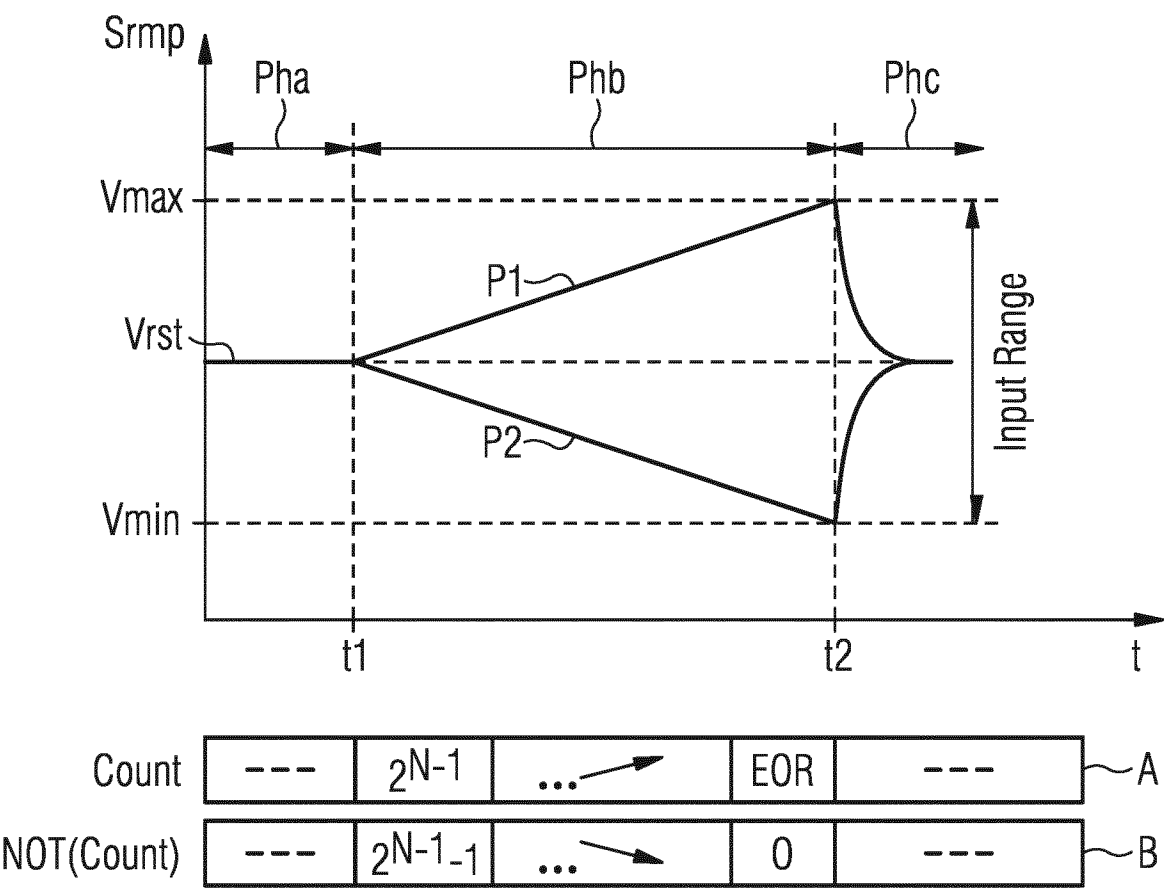


FIG 2

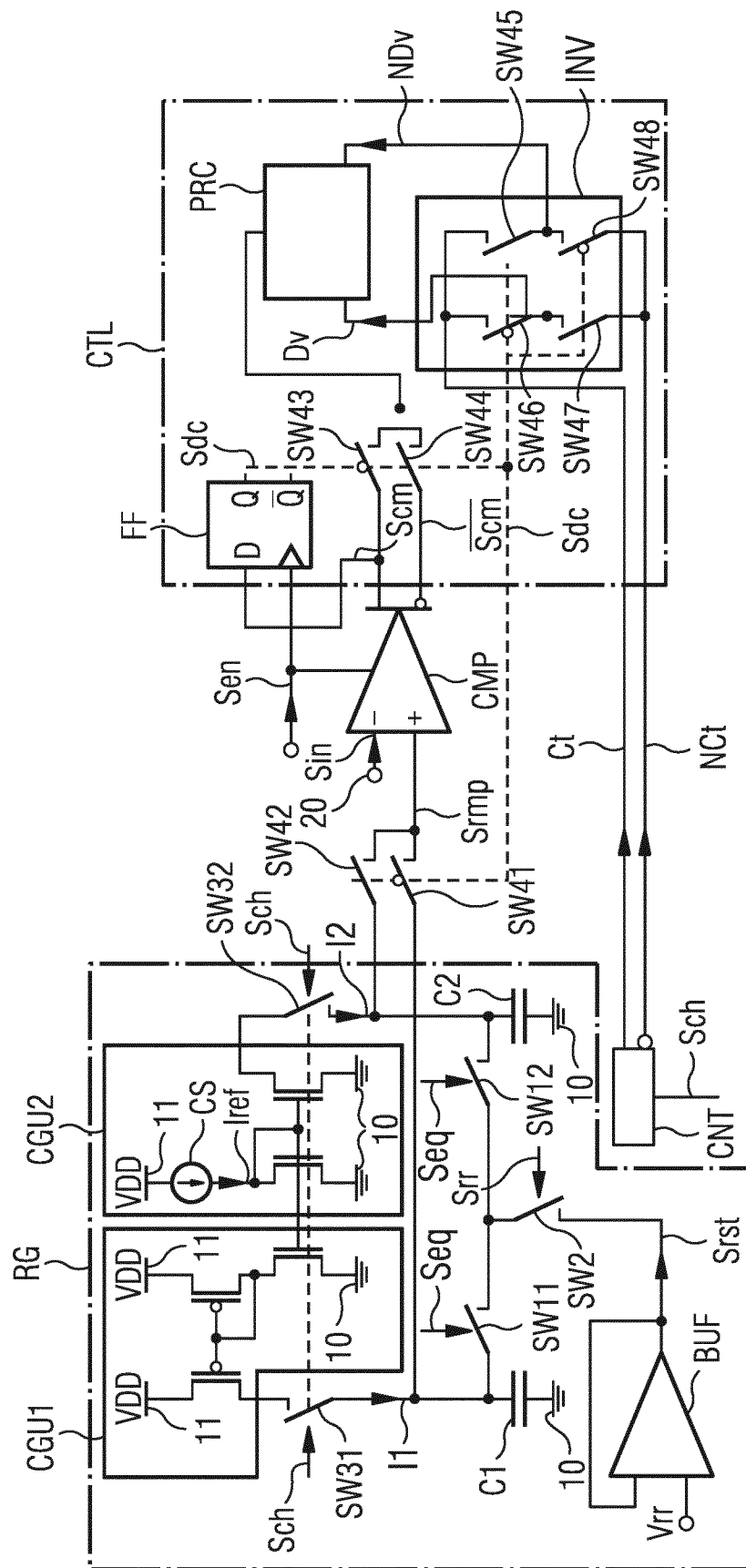


FIG 3

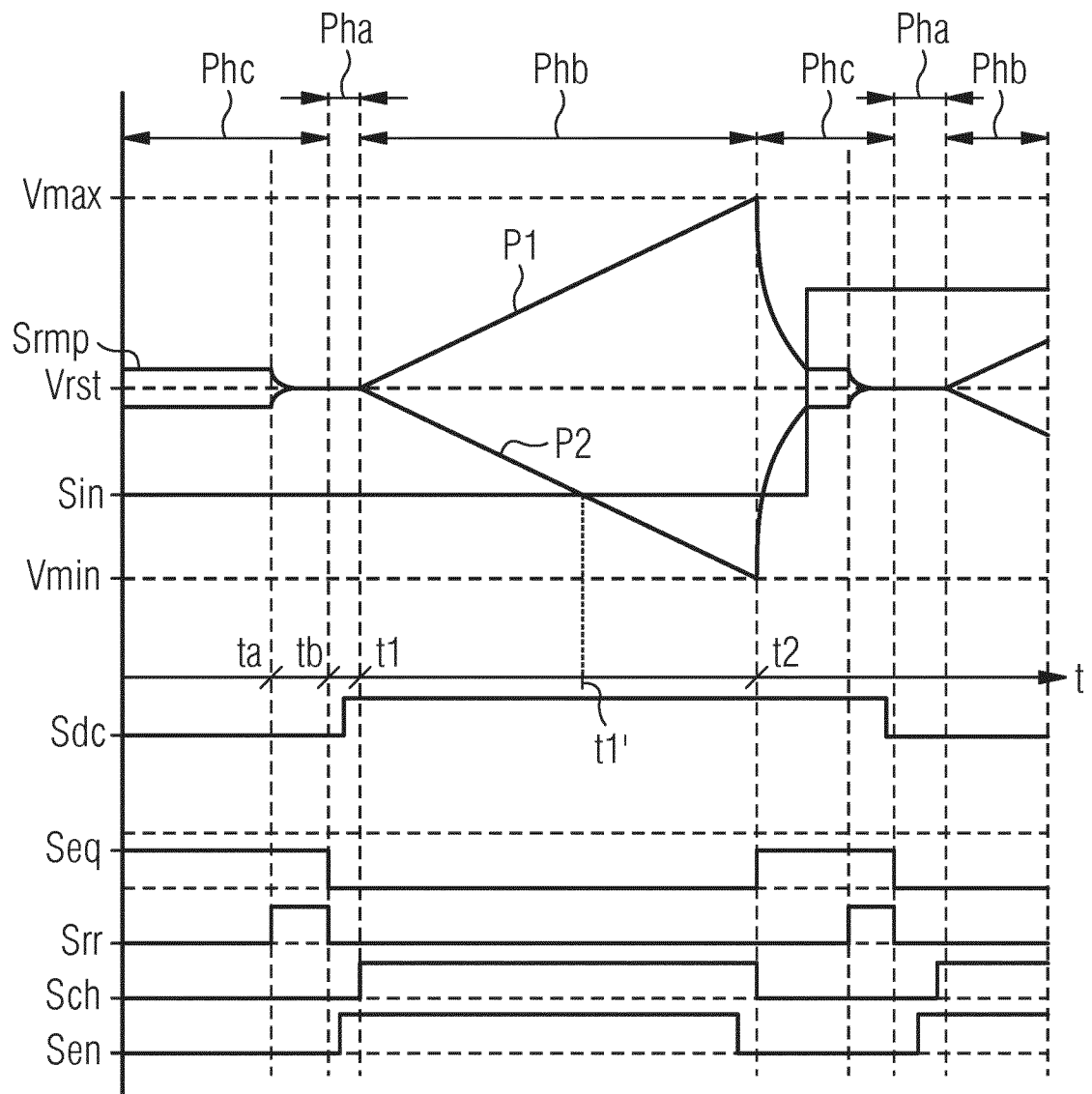


FIG 4

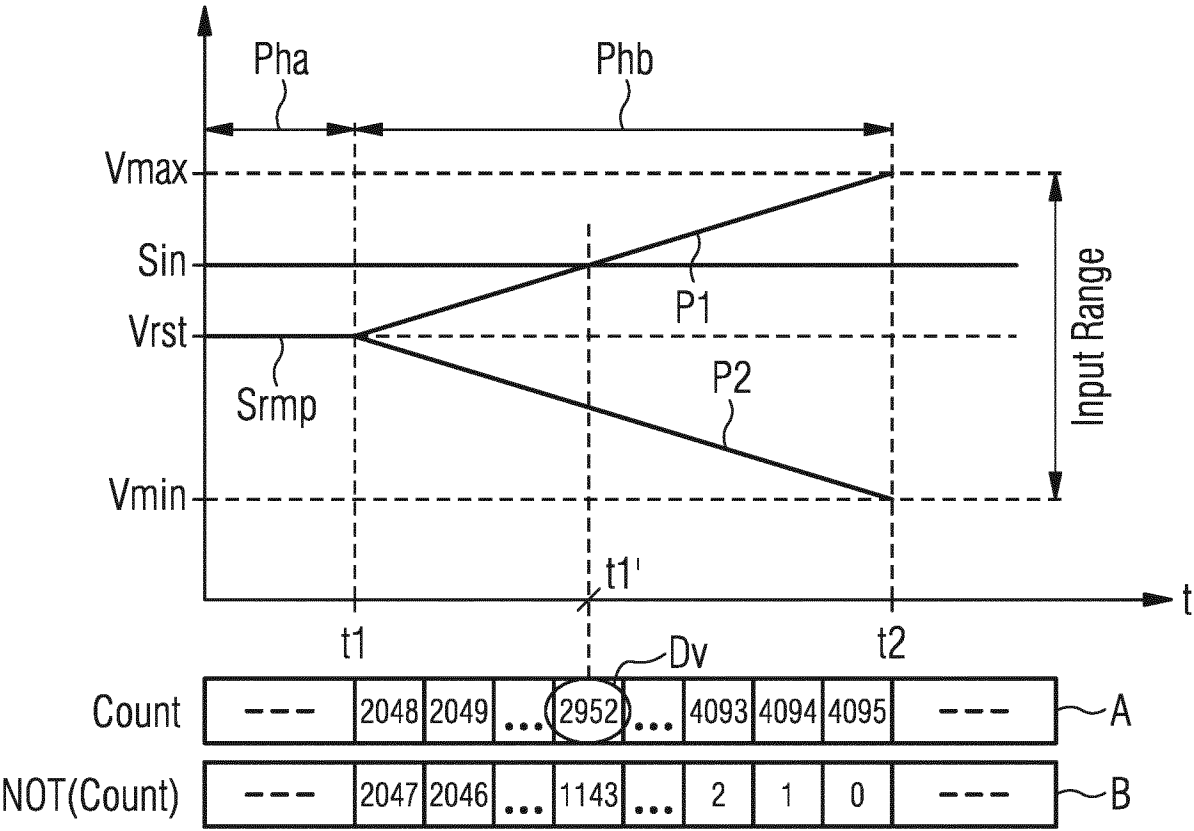


FIG 5

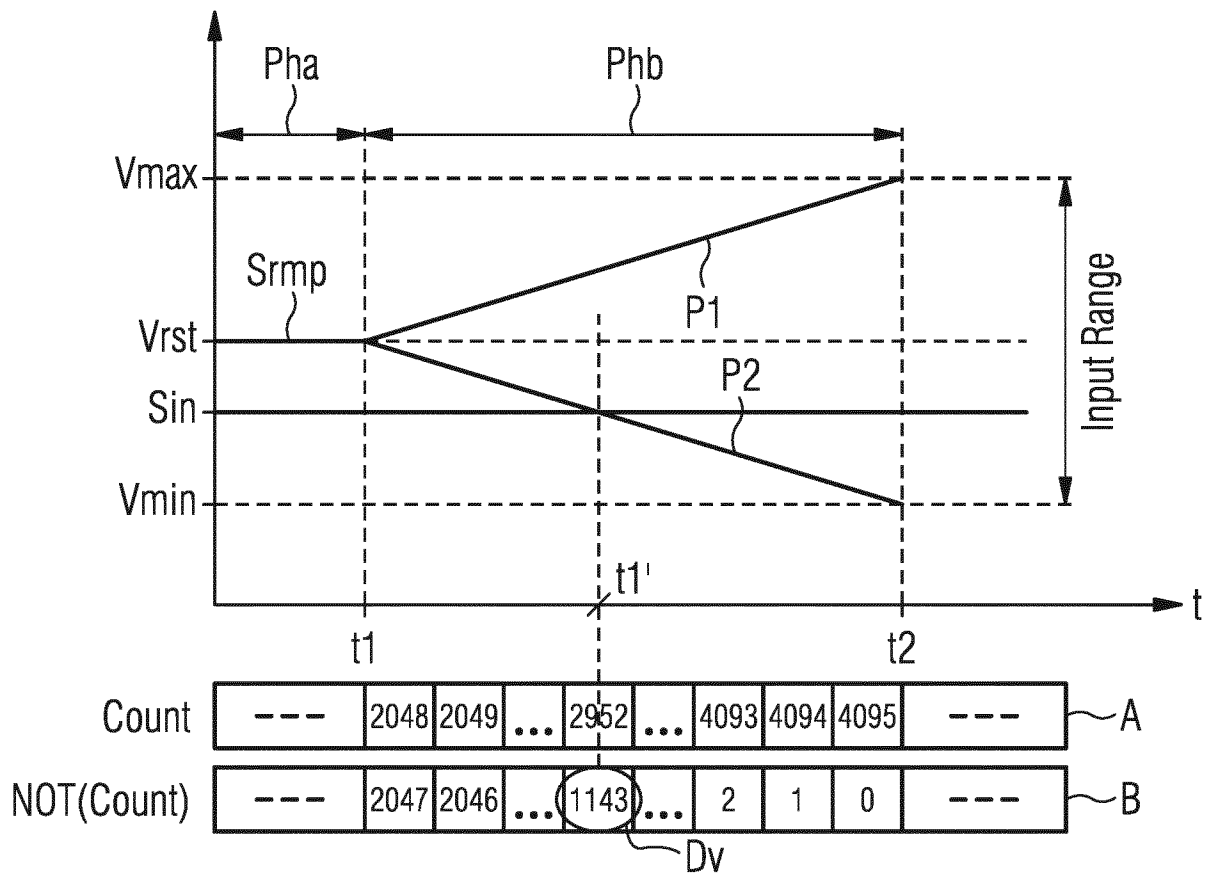


FIG 6

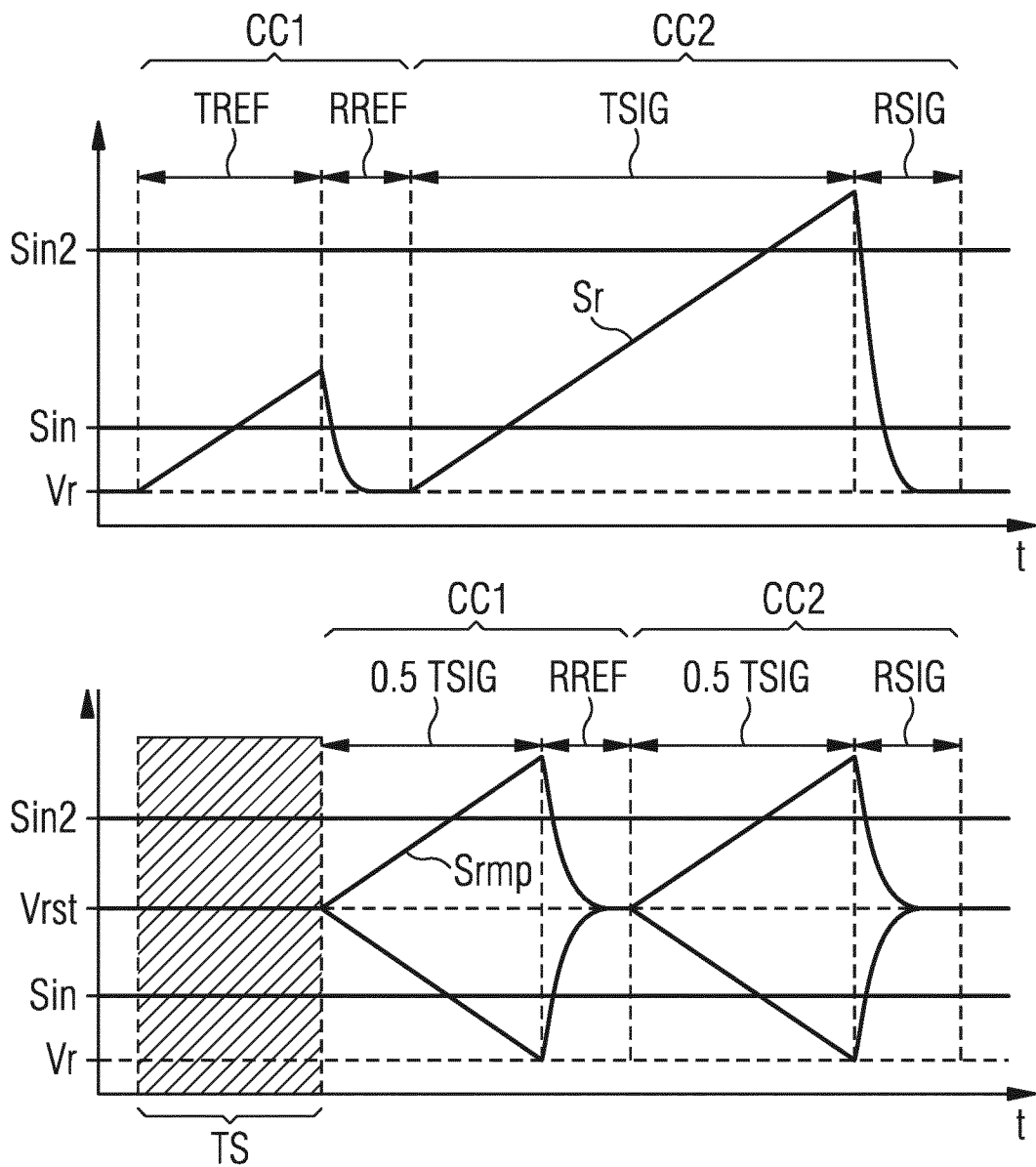


FIG 7

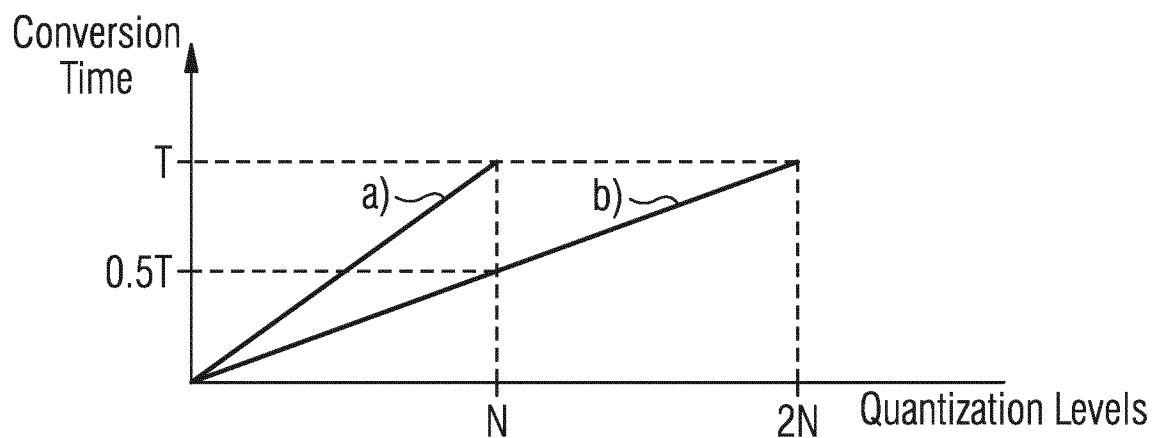


FIG 8

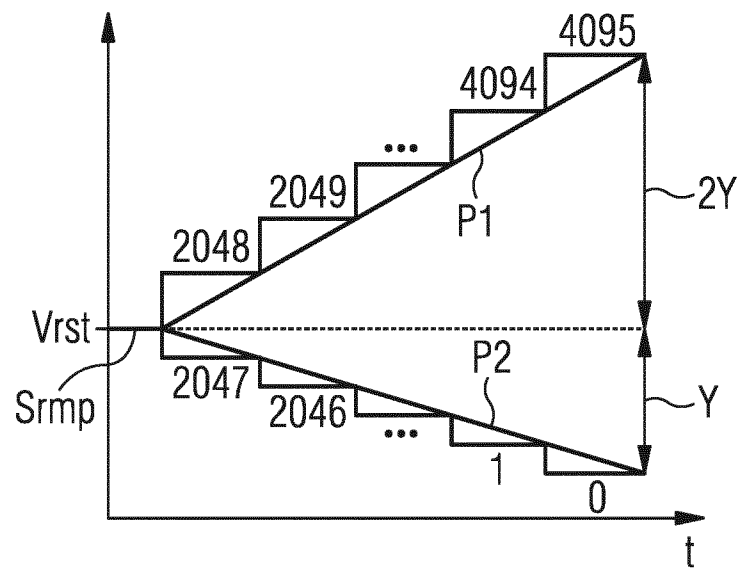


FIG 9A

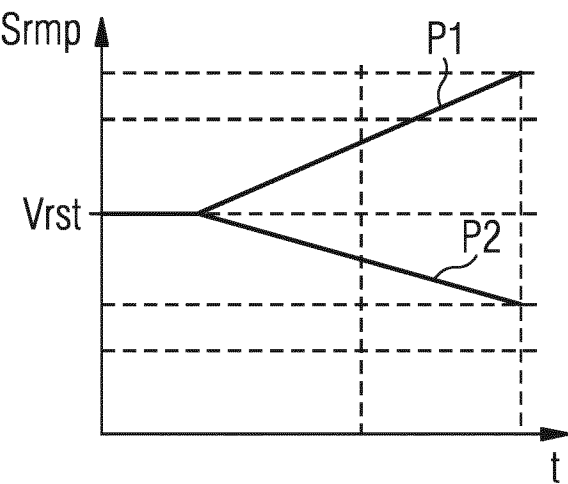


FIG 9B

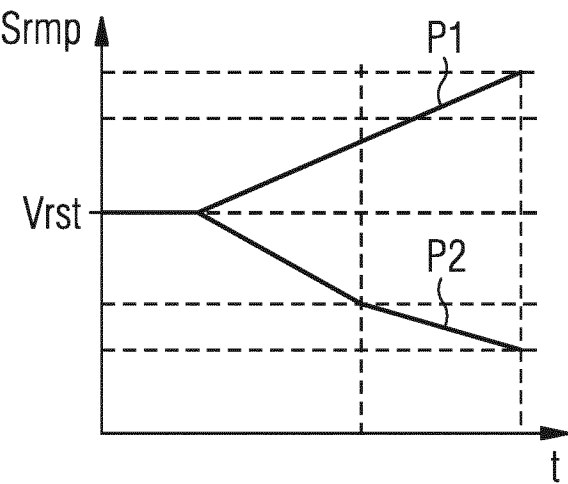


FIG 9C

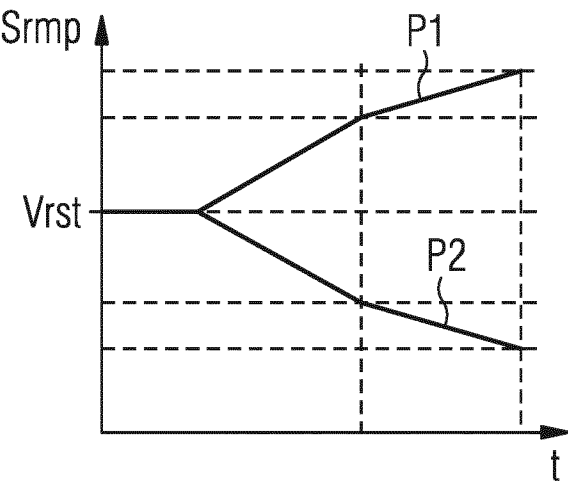
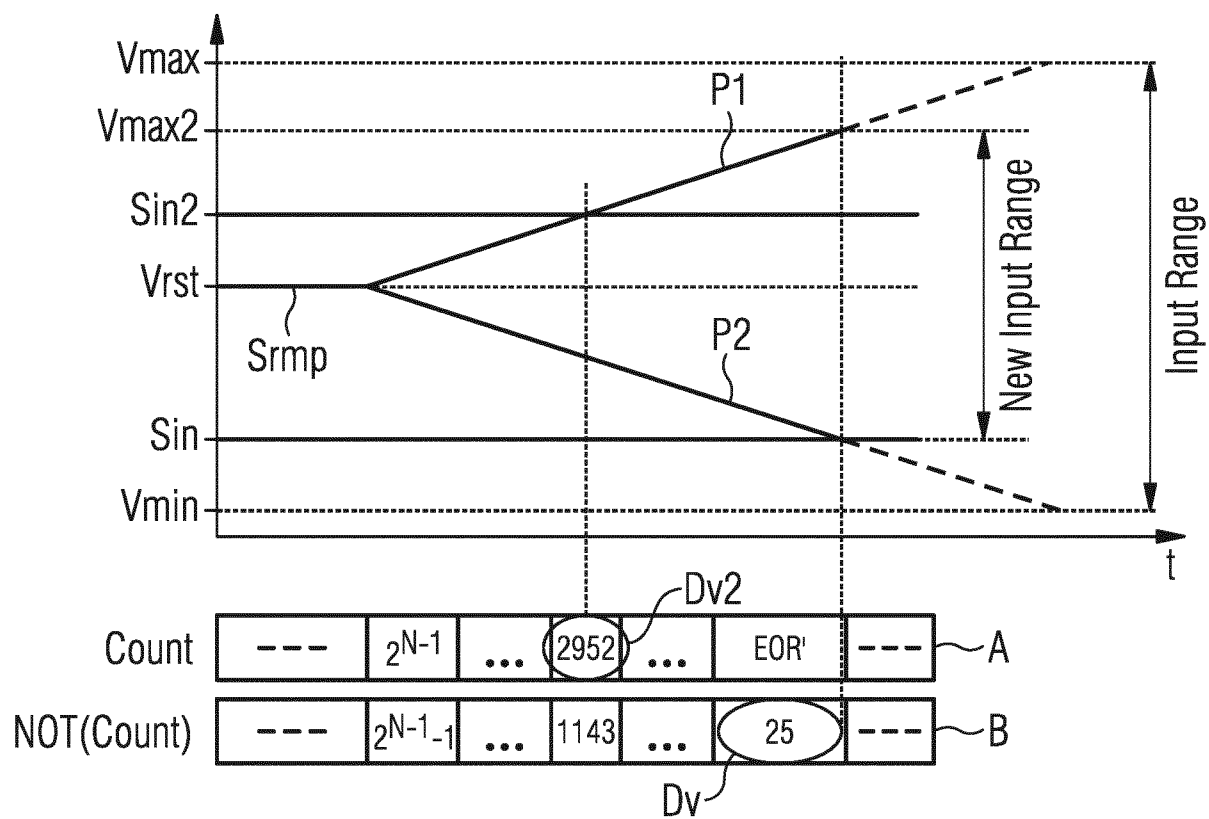


FIG 10



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/068953

A. CLASSIFICATION OF SUBJECT MATTER INV. H03M1/56 H04N5/357 H03M1/06 ADD. H03M1/12		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H03M H04N		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/042859 A1 (LEE JUNG HO [KR] ET AL) 12 February 2015 (2015-02-12) paragraphs [0098] - [0108]; figures 5,6,7a,8 paragraph [0071] paragraph [0084] paragraph [0048] paragraph [0072]	1-14
A	----- US 2015/138413 A1 (SATO MAKI [JP]) 21 May 2015 (2015-05-21) paragraph [0107]; figure 9	5,6
A	----- GB 2 421 374 A (MICRON TECHNOLOGY INC [US]) 21 June 2006 (2006-06-21) figure 11 -----	5,6
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 14 September 2018		Date of mailing of the international search report 20/09/2018
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Galardi, Leonardo

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2018/068953

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