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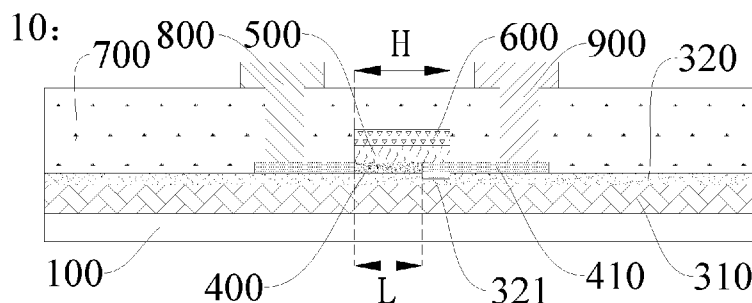


FIG. 3

- (57) Abstract:** A thin film transistor (10) may include a substrate (100); a buffer layer (300) on a surface of the substrate (100); an active layer (400) on a surface of the buffer layer (300) opposite from the substrate (100); a gate insulating layer (500) on a surface of the active layer (400) opposite from the substrate (100), and a gate (600) on a surface of the gate insulating layer (500) opposite from the substrate (100). A width of the active layer (400) may be smaller than a width of the gate (600), and an orthographic projection of the gate (600) on the substrate (100) may cover an orthographic projection of the active layer (400) on the substrate (100).

1 **THIN FILM TRANSISTOR, FABRICATING METHOD THEREOF,**
2 **DISPLAY SUBSTRATE AND DISPLAY APPARATUS**

3
4 **CROSS-REFERENCE TO RELATED APPLICATIONS**

5 **[0001]** This application claims benefit of the filing date of Chinese Patent Application
6 No. 201811588559.5 filed on December 25, 2018, the disclosure of which is hereby
7 incorporated in its entirety by reference.

8 **TECHNICAL FIELD**

9 **[0002]** The present disclosure relates to display technologies, and in particular, to a
10 thin film transistor, a method for fabricating the same, a display substrate, and a
11 display apparatus.

12 **BACKGROUND**

13 **[0003]** The present display panels include liquid crystal display (LCD) panels and
14 organic light-emitting diode display (OLED) panels. Thin film transistors (TFTs) are
15 core components in a display panel and are arranged in an array in the display panel
16 as switch devices of pixel units of the display panel. In a conventional thin film
17 transistor, the width of the active layer is equal to the width of the gate. Because the
18 width of the active layer is relatively long, the thin film transistor has a small on-state
19 current. To reduce the width of the gate directly, however, is more likely to lead to
20 disconnections.

21 **BRIEF SUMMARY**

22 **[0004]** One embodiment of the present disclosure is a thin film transistor. The thin
23 film transistor may include a substrate; a buffer layer on a surface of the substrate; an
24 active layer on a surface of the buffer layer opposite from the substrate; a gate
25 insulating layer on a surface of the active layer opposite from the substrate, and a gate
26 on a surface of the gate insulating layer opposite from the substrate; wherein a width
27 of the active layer may be smaller than a width of the gate, and an orthographic
28 projection of the gate on the substrate covers an orthographic projection of the active
29 layer on the substrate.

1 [0005] Optionally, a conducting layer may be provided at two sides of the active layer
2 respectively and an orthographic projection of the conducting layer on the substrate
3 partially overlaps the orthographic projection of the gate on the substrate.

4 [0006] Optionally, the buffer layer may include: a first sub-buffer layer on the
5 substrate, and a material forming the first sub-buffer layer contains carriers; and a
6 second sub-buffer layer on a surface of the first sub-buffer layer opposite from the
7 substrate, the second sub-buffer layer comprising at least a thin region, wherein the
8 orthographic projection of the conducting layer covers an orthographic projection of
9 the thin region on the substrate, and the orthographic projection of the thin region at
10 least has an overlapping area with the orthographic projection of the gate on the
11 substrate.

12 [0007] Optionally, a groove may be provided on a surface of the second sub-buffer
13 layer opposite from the first sub-buffer layer, and a part of the second sub-buffer layer
14 under a bottom of the groove constitutes the thin region.

15 [0008] Optionally, a groove may be provided on a surface of the second sub-buffer
16 layer facing the first sub-buffer layer, and a part of the second sub-buffer layer on a
17 top of the groove constitutes the thin region.

18 [0009] Optionally, a thickness of the thin region may be less than or equal to about
19 100 nm.

20 [0010] Optionally, a material forming the first sub-buffer layer may include silicon
21 nitride.

22 [0011] Optionally, a material forming the second sub-buffer layer may include silicon
23 dioxide.

24 [0012] Optionally, a material forming the active layer may include amorphous indium
25 gallium zinc oxide.

26 [0013] Optionally, a width of the active layer may be within a range of about 1 μm to
27 about 3 μm .

28 [0014] Optionally, the thin film transistor may further include a light shielding layer
29 between the substrate and the buffer layer, wherein an orthographic projection of the
30 light shielding layer on the substrate covers the orthographic projection of the active

1 layer on the substrate, and an area of the orthographic projection of the light shielding
2 layer on the substrate is smaller than an area of the orthographic projection of the gate
3 on the substrate.

4 **[0015]** Another embodiment of the present disclosure is a method of fabricating a thin
5 film transistor. The method may include: providing a substrate; forming a buffer layer
6 on a surface of the substrate; forming an active layer on a surface of the buffer layer
7 opposite from the substrate; and forming a gate insulating layer and a gate
8 sequentially on a surface of the active layer opposite from the substrate, wherein a
9 width of the active layer is smaller than a width of the gate, and an orthographic
10 projection of the gate on the substrate covers an orthographic of the active layer on
11 the substrate.

12 **[0016]** Optionally, forming the buffer layer on the surface of the substrate may
13 include: forming a first sub-buffer layer on the surface of the substrate, wherein a
14 material forming the first sub-buffer layer contains carriers; and forming a second
15 sub-buffer layer having at least a thin region on a surface of the first sub-buffer
16 opposite from the substrate.

17 **[0017]** Optionally, forming the active layer on the surface of the buffer layer opposite
18 from substrate and forming the gate insulating layer and the gate may include:
19 forming a semiconductor layer on a surface of the second sub-buffer layer opposite
20 from the substrate; annealing the semiconductor layer to enable the carriers in the first
21 sub-buffer layer to enter the semiconductor layer through the thin region of the second
22 sub-buffer layer; forming an insulating layer and a metal layer on surfaces of the
23 second sub-buffer layer and the semiconductor layer opposite from the substrate;
24 patterning the metal layer and the insulating layer by one-time patterning process to
25 form the gate and the gate insulating layer respectively; and performing a conducting
26 treatment to a part of the semiconductor layer that is not covered by the gate
27 insulating layer and the gate, thereby obtaining the active layer and the conducting
28 layer.

29 **[0018]** Optionally, forming the second sub-buffer layer having at least a thin region
30 may include forming the second sub-buffer layer on a surface of the first sub-buffer
31 opposite from the substrate; and forming a groove on a surface of the second sub-

1 buffer layer opposite from the substrate, wherein a part of the second sub-buffer layer
2 under a bottom of the groove constitutes the thin region.

3 **[0019]** Optionally, forming the second sub-buffer layer having the thin region may
4 include: forming the second sub-buffer layer on a surface of the first sub-buffer
5 opposite from the substrate; and forming a groove on a surface of the second sub-
6 buffer layer facing the substrate, wherein a part of the second sub-buffer layer on a
7 top of the groove constitutes the thin region.

8 **[0020]** Optionally, the method, before forming the buffer layer on the surface of the
9 substrate, may further include: forming a light shielding layer on the surface of the
10 substrate, wherein an orthographic projection of the light shielding layer on the
11 substrate covers an orthographic projection of the active layer on the substrate, and an
12 area of the orthographic projection of the light shielding layer on the substrate is less
13 than an area of the orthographic projection of the gate on the substrate.

14 **[0021]** Another embodiment of the present disclosure is a display substrate. The
15 display substrate may include the thin film transistor.

16 **[0022]** Another embodiment of the present disclosure is a display apparatus. The
17 display apparatus may include the display substrate.

18 **BRIEF DESCRIPTION OF THE DRAWINGS**

19 **[0023]** In order to more clearly illustrate the technical solutions of the embodiments
20 of the present disclosure, the drawings of the embodiments will be briefly described
21 below. It is obvious that the drawings in the following description relate only to some
22 embodiments of the present disclosure, and are not to limit the disclosure:

23 **[0024]** FIG. 1 shows a schematic cross-sectional view of a conventional thin film
24 transistor in the related art;

25 **[0025]** FIG. 2 shows a schematic cross-sectional view of a thin film transistor
26 according to one embodiment of the present disclosure;

27 **[0026]** FIG. 3 shows a schematic cross-sectional view of a thin film transistor
28 according to one embodiment of the present disclosure;

29 **[0027]** FIG. 4 shows a schematic cross-sectional view of a thin film transistor
30 according to one embodiment of the present disclosure;

1 [0028] FIG. 5 shows a schematic cross-sectional view of a thin film transistor
2 according to one embodiment of the present disclosure;

3 [0029] FIG. 6 shows a schematic cross-sectional view of a thin film transistor
4 according to one embodiment of the present disclosure;

5 [0030] FIG. 7 shows a schematic cross-sectional view of a thin film transistor
6 according to one embodiment of the present disclosure;

7 [0031] FIG. 8 is a flow chart showing a method of fabricating a thin film transistor
8 according to one embodiment of the present disclosure;

9 [0032] FIGS. 9a-9d show schematic views of a method for fabricating a thin film
10 transistor according to one embodiment of the present disclosure;

11 [0033] FIG. 10 is a flow chart showing a method for fabricating a thin film transistor
12 according to one embodiment of the present disclosure;

13 [0034] FIGS. 11a-11h show schematic views of a method for fabricating a thin film
14 transistor according to one embodiment of the present disclosure;

15 [0035] FIG. 12 is a flow chart showing a method for fabricating a thin film transistor
16 according to one embodiment of the present disclosure; and

17 [0036] FIGS. 13a and 13b show schematic views of a method for fabricating a thin
18 film transistor according to one embodiment of the present disclosure.

19 **DETAILED DESCRIPTION**

20 [0037] In order to make the objects, technical solutions and advantages of the
21 embodiments of the present disclosure clearer, the technical solutions of the
22 embodiments of the present disclosure will be clearly and completely described below
23 in conjunction with the drawings of the embodiments of the present disclosure. It is
24 apparent that the described embodiments are part of the embodiments of the present
25 disclosure, and not all of the embodiments. All other embodiments obtained by a
26 person of ordinary skill in the art based on the described embodiments of the present
27 disclosure without departing from the scope of the disclosure are within the scope of
28 the disclosure.

29 [0038] Unless otherwise defined, the technical terms or scientific terms used herein
30 should be understood in the ordinary sense as understood by those of ordinary skill in

1 the art to which the disclosure pertains. The words “first,” “second,” and similar terms
2 used in the present disclosure do not denote any order, quantity, or importance, but
3 are used to distinguish different components. Similarly, “including” or “comprising”
4 and the like means that the element or object appear in front of the word cover the
5 elements or objects and their equivalents listed after the word, and the other elements
6 or objects are not excluded.

7 **[0039]** A numerical value modified by “about” herein means that the numeric value
8 can vary by 10% thereof.

9 **[0040]** In the related art, referring to FIG. 1, a thin film transistor 10 includes a light
10 shielding layer 200, a buffer layer, an active layer 400, a gate insulating layer 500, a
11 gate 600, an interlayer insulating layer 700, a source 800, and a drain 900, which are
12 sequentially formed on a substrate 100. The buffer layer is disposed on a side of the
13 light shielding layer 200 opposite from the substrate 100, and the buffer layer includes
14 a first sub-buffer layer 310 and a second sub-buffer layer 320. A conducting treatment
15 is performed on two sides of the active layer 400 after formation of the gate 600 and
16 the gate insulating layer 500. As such, the width L of the active layer is equal to the
17 width H of the gate 600. The thin film transistor 10 thus fabricated has a long width L
18 of the active layer, so that the on-state current is small. To reduce the width of the
19 gate 500 directly is more likely to cause disconnections.

20 **[0041]** One embodiment of the present disclosure provides a thin film transistor. In
21 one embodiment, referring to FIG. 2, the thin film transistor 10 includes a substrate
22 100, a buffer layer 300 on the substrate 100, an active layer 400 on a surface of the
23 buffer layer 300 opposite from the substrate, a gate insulating layer 500 on a surface
24 of the active layer 400 opposite from the substrate, and a gate 600 on a surface of the
25 gate insulating layer 500 opposite from the substrate. The orthographic projection of
26 the gate 600 on the substrate 100 overlaps with the orthographic projection of the gate
27 insulating layer 500 on the substrate 100. The width L of the active layer 400 of the
28 thin film transistor 10 is smaller than the width H of the gate 600, and the
29 orthographic projection of the gate 600 on the substrate 100 covers the orthographic
30 projection of the active layer 400 on the substrate 100. Thus, the width L of the active
31 layer 400 of the thin film transistor 10 is not limited by the width H of the gate 600, so
32 that the width of the active layer 400 can be made relatively small. As such, the on-

1 state current of the thin film transistor 10 can be significantly increased. Furthermore,
2 the process is simple, easy to implement, and easy for industrial production.

3 **[0042]** According to one embodiment of the present disclosure, it should be
4 understood for those skilled in the art as referring to the FIG. 2 that the thin film
5 transistor further includes an interlayer insulating layer 700, a source 800, and a drain
6 900. The positional relationships between the interlayer insulating layer 700, the
7 source 800, the drain 900 and other structures are the same or similar as the positional
8 relationships between the interlayer insulating layer, the source, the drain and other
9 structures in the conventional thin film transistor, and are not repeated herein. It
10 should be understood by those skilled in the art that the "width of the active layer"
11 herein has the same meaning as the "channel length" generally referred to in the field
12 of semiconductors, that is, the distance that the current flows along the active layer
13 between the source and the drain after the thin film transistor is turned on. The width
14 of the gate or other structure is defined as the length of the gate or the other structures
15 measured at the same direction as the width of the active layer, that is, the direction
16 the current flows along the active layer between the source and the drain.

17 **[0043]** In one embodiment, referring to FIG. 2, the thin film transistor 10 is provided
18 with a conducting layer 410 at both sides of the active layer 400. The orthographic
19 projection of the conducting layer 410 overlaps the orthographic projection of the gate
20 on the substrate 100. Therefore, the width L of the active layer 400 of the thin film
21 transistor 10 is not limited by the width H of the gate 600, so that the width of the
22 active layer 400 can be made relatively small, and the on-state current can be
23 significantly increased in the thin film transistor 10. Furthermore, the process is
24 simple, easy to implement, and easy for industrial production.

25 **[0044]** According to one embodiment of the present disclosure, the material forming
26 the active layer 400 may be made of amorphous indium gallium zinc oxide. As a
27 result, the material is widely available and easy to obtain, low in cost, and easy to
28 implement in the manufacturing process.

29 **[0045]** In one embodiment, the width of the active layer 400 may be about 1 μm to
30 about 3 μm . In some embodiments, the width of the active layer 400 may be 1 μm , 2
31 μm or 3 μm . The width of the active layer 400 can be made small as long as that this

1 may not cause the disconnection of the gate, so that the on-state current can be
2 significantly increased in the thin film transistor 10.

3 **[0046]** In one embodiment, referring to FIGS. 3-6, the buffer layer 300 further
4 includes a first sub-buffer layer 310 on a surface of the substrate 100, and a second
5 sub-buffer layer 320 on a surface of the first sub-buffer layer 310 opposite from the
6 substrate 100. The material forming the first sub-buffer layer 310 contains carriers.
7 The material forming the first sub-buffer layer 310 may be silicon nitride (SiN_x) and
8 the material forming the second sub-buffer layer 320 may be silicon dioxide (SiO_2).
9 Thus, those materials are widely available, easy to obtain and have low cost.

10 **[0047]** According to some embodiments of the present disclosure, referring to FIGS.
11 3-6, the second sub-buffer layer 320 includes a thin region 321. The orthographic
12 projection of the conducting layer 410 on the substrate 100 covers the orthographic
13 projection of the thin region 321 on the substrate 100. The orthographic projection of
14 the thin region 321 on the substrate 100 at least partially overlaps with the
15 orthographic projection of the gate 600 on the substrate 100. Therefore, the width L of
16 the active layer 400 of the thin film transistor 10 is not limited by the width H of the
17 gate 600. Optionally, the implementation is described as follows.

18 **[0048]** In one embodiment, the active layer 400 and the conducting layer 410 are
19 obtained by first forming a semiconductor layer on the entire surface of the second
20 sub-buffer layer 320, and then by performing a conducting treatment to parts of the
21 semiconductor layer.

22 **[0049]** In one embodiment, the material forming the second sub-buffer layer 320 may
23 be made of silicon dioxide and the material forming the first sub-buffer layer 310 may
24 be made of silicon nitride. The silicon nitride material may contain a large number of
25 carriers, for example, hydrogen ions and the like. The second sub-buffer layer 320 of
26 the thin film transistor 10 is provided with a thin region 321. During the fabrication of
27 the thin film transistor 10, a process may be applied so that the carriers in the material
28 forming the second sub-buffer layer 320 can flow into the semiconductor layer
29 through the thin region 321 on the second sub-buffer layer 320, thereby performing a
30 conducting treatment to a part of the semiconductor layer where the carriers enter.
31 Conventional processes such as ion doping can also be applied in the subsequent
32 process to perform a conducting treatment on other part of the semiconductor layer,

1 thereby forming the conducting layer 410 and the active layer 400. Thus, it allows the
2 width L of the active layer 400 not to be limited by the width H of the gate 600 and
3 the width of the active layer 400 can be made smaller. As a result, the on-state current
4 can be significantly increased, and the process is simple, easy to implement, and easy
5 for industrial production.

6 **[0050]** In one embodiment, the thickness of the thin region 321 in a direction
7 perpendicular to the substrate may be greater than 0 and less than or equal to 100 nm.
8 In some embodiments of the present disclosure, the thickness of the thin region may
9 be 1 nm, 2 nm, 5 nm, 10 nm, 20 nm, 50 nm, 80 nm, or 100 nm. When the thickness of
10 the thin region 321 is in a proper range, the carriers described above may more easily
11 move through the thin region 321 of the second sub-buffer layer 320, and at the same
12 time the carriers are prevented from moving through the second sub-buffer layer 320
13 in the non-thin regions. Therefore, the thin film transistor can operate normally. Thus,
14 the width L of the active layer 400 of the thin film transistor 10 is not limited by the
15 width H of the gate 600. The width of the active layer 400 can be made relatively
16 small and the on-state current can be significantly increased.

17 **[0051]** In one embodiment, the orthographic projection of the thin region 321 on the
18 substrate 100 may at least partially overlap with the orthographic projection of the
19 gate 600 on the substrate 100. That is, a thin region may also be provided in a part of
20 the second sub-buffer layer 320 whose orthographic projection on the substrate does
21 not overlap with the orthographic projection of the gate 600 on the substrate 100, as
22 shown in FIG. 4. Because the thin region 321 on the second sub-buffer layer 320
23 extends to a region that does not overlap the orthographic projection of the gate 600
24 on the substrate 100, the conducting treatment can be applied to a larger region of the
25 semiconductor layer. This would help preventing disconnection of the conducting
26 layer 410 in the subsequent fabrication process, which otherwise may result in the
27 inoperable thin film transistor 10, and allowing the width L of the active layer 400 of
28 the thin film transistor 10 not to be limited by the width H of the gate 600. The width
29 of the active layer 400 can be made relatively small, thereby significantly increasing
30 the on-state current. Furthermore, the process is simple, easy to implement, and easy
31 for industrial production.

1 **[0052]** In one embodiment, a plurality of thin regions 321 may be provided. For
2 example, the second sub-buffer layer 320 at both sides of the gate 600 may have thin
3 regions 321, as shown in FIG. 5. A plurality of thin regions 321 may further allow the
4 width L of the active layer 400 of the thin film transistor 10 not to be limited by the
5 width H of the gate 600. The width of the active layer 400 can be made smaller, and
6 the on-state current can be further increased.

7 **[0053]** In one embodiment, there is no particular restriction on the position of the thin
8 region 321. The thin region 321 may be formed by thinning a surface of the second
9 sub-buffer layer 320 opposite from the substrate 100, or by thinning a surface of the
10 second sub-buffer layer 320 facing the substrate 100, or by thinning both surfaces of
11 the second sub-buffer layer 320 opposite from the substrate 100 and facing the
12 substrate 100. In some embodiments of the present disclosure, a groove is formed on a
13 surface of the second sub-buffer layer 320 opposite from the first sub-buffer layer 310,
14 and the thin region 321 is the region under the bottom of the groove of the second
15 sub-buffer 320 with reference to FIGS. 3-5. In one embodiment, a groove may be
16 formed on the surface of the second sub-buffer layer 320 facing the first sub-buffer
17 layer 310, and the thin region 321 is the region on the top of the groove of the second
18 sub-buffer 320 with reference to FIG. 6. Both types of thin regions 321 as mentioned
19 above may further allow the width L of the active layer 400 of the thin film transistor
20 10 not to be limited by the width H of the gate 600. The width of the active layer 400
21 can be made smaller, and further less than the width of the gate 600 of the thin film
22 transistor 10. The on-state current is further increased. Compared with the thin region
23 321 in FIG. 6, the thin region 321 in FIGS. 3-5 may require a process, which is simple,
24 easier to implement and easier for industrial production.

25 **[0054]** In one embodiment, referring to FIG. 7, the thin film transistor 10 further
26 includes a light shielding layer 200 between the substrate 100 and the buffer layer 300.
27 The orthographic projection of the light shielding layer on the substrate 100 covers
28 the orthographic projection of the active layer 400 on the substrate 100. The area of
29 the orthographic projection of the light-shielding layer 200 on the substrate 100 is less
30 than that of the gate 600 on the substrate 100. Therefore, because the width L of the
31 active layer 400 of the thin film transistor 10 is not limited by the width H of the gate
32 600, the width of the active layer 400 can be made smaller. The light shielding layer

200 of the thin film transistor 10 may only cover the active layer 400. The area of the orthographic projection of the light shielding layer on the substrate 100 may be less than the area of the orthographic projection of the gate 600 on the substrate 100.

[0055] Another embodiment of the present disclosure provides a method for making a thin-film transistor. According to one embodiment of the present disclosure, referring to FIGS. 8 and 9a to 9d, the method comprises the following steps:

[0056] Step S10 includes forming a buffer layer 300 on a surface of a substrate 100 with reference to FIG. 9a.

[0057] In one embodiment, a process for forming the buffer layer 300 on the surface of the substrate 100 may employ vacuum evaporation, chemical vapor deposition, spin coating, or inkjet printing. The process parameters used in vacuum evaporation, chemical vapor deposition, spin coating, or inkjet printing may be conventional process parameters in those processes and are not repeated herein. As such, the fabrication process is simple, easy to implement, and easy for industrial production.

[0058] Step S20 includes forming an active layer 400 on a surface of the buffer layer 300 opposite from the substrate 100 with reference to FIG. 9b.

[0059] In one embodiment, a process for forming an active layer 400 on the surface of the buffer layer 300 opposite from the substrate 100 may employ vacuum evaporation, chemical vapor deposition, spin coating, and inkjet printing. The conventional process parameters used in vacuum evaporation, chemical vapor deposition, spin coating, and inkjet printing are not repeated herein. As such, the fabrication process is simple, easy to implement, and easy for industrial production.

[0060] Step S30 includes forming a gate insulating layer 500 and a gate 600 sequentially on a surface of the active layer 400 opposite from the substrate 100. The orthographic projection of the gate 600 on the substrate 100 overlaps with the orthographic projection of the gate insulating layer 500 on the substrate 100 and the width L of the active layer 400 of the thin film transistor 10 is smaller than the width H of the gate. The orthographic projection of the gate 600 on the substrate 100 covers the orthographic projection of the active layer 400 on the substrate 100, as shown in FIG. 9c.

1 **[0061]** In one embodiment, a process of forming the gate insulating layer 500 on the
2 surface of the active layer 400 opposite from the substrate 100 may employ vacuum
3 evaporation, chemical vapor deposition, spin coating, and inkjet printing. The
4 conventional process parameters used in these techniques are not repeated herein. The
5 fabrication process is simple, easy to implement, and easy for industrial production.

6 **[0062]** In one embodiment, a process of forming the gate 600 on the substrate may
7 employ vacuum evaporation, chemical vapor deposition, spin coating, and inkjet
8 printing. The conventional process parameters used in these techniques are not
9 repeated herein. The fabrication process is simple, easy to implement, and easy for
10 industrial production.

11 **[0063]** Step S40 includes forming an interlayer insulating layer 700, a source 800, and
12 a drain 900, as shown in FIG. 9d.

13 **[0064]** In one embodiment, processes for forming the interlayer insulating layer 700,
14 the source 800, and the drain 900 are all conventional. The process parameters are
15 also conventional process parameters, and they are not repeated herein.

16 **[0065]** In one embodiment, with reference to FIGS. 10 and 11a to 11h, the method
17 further includes the following steps:

18 **[0066]** With reference to FIG. 11a, step S100 includes forming a first sub-buffer layer
19 310 on a surface of the substrate 100, wherein the material forming the first sub-
20 buffer layer 310 contains carriers.

21 **[0067]** In one embodiment, the process of forming the first sub-buffer layer 310 on
22 the surface of the substrate 100 may employ vacuum evaporation, chemical vapor
23 deposition, spin coating, and inkjet printing. The conventional process parameters are
24 used in these techniques, and they are not repeated herein. The fabrication process is
25 simple, easy to implement, and easy for industrial production.

26 **[0068]** Step S200 includes forming a second sub-buffer layer 320 having a thin region
27 321 on a surface of the first sub-buffer layer 310 opposite from the substrate 100, as
28 shown in FIG. 11b.

29 **[0069]** In one embodiment, a process of forming the second sub-buffer layer 320
30 having the thin region 321 on the surface of the first sub-buffer layer 310 opposite

1 from the substrate 100 may employ vacuum evaporation, chemical vapor deposition,
2 spin coating, and inkjet printing. The conventional process parameters are used in
3 these techniques and they are not repeated herein. The fabrication process is simple,
4 easy to implement, and easy for industrial production.

5 **[0070]** In some embodiments of the present disclosure, forming the second sub-buffer
6 layer 320 includes forming a second sub-buffer layer 320 on the first sub-buffer layer
7 310, and forming a groove on a surface of the second sub-buffer layer 320 opposite
8 from the substrate 100, wherein the thin region 321 is the region under the bottom of
9 the groove of the second sub-buffer layer 320. Therefore, the process is simple, easy
10 to implement, and easier for industrial production. The process allows the width L of
11 the active layer 400 of the thin film transistor 10 not to be limited by the width H of
12 the gate 600. The width of the active layer 400 can be made relatively small, thereby
13 further reducing the width of the active layer 400 and thus increasing the on-state
14 current.

15 **[0071]** Step S300 includes forming a semiconductor layer 399 on a surface of the
16 second sub-buffer layer 320 opposite from the substrate 100 (see FIG. 11c for a
17 schematic structural view).

18 **[0072]** In one embodiment, the processes of forming the active layer 400 on a surface
19 of the second sub-buffer layer 320 opposite from the substrate and forming the
20 conducting layer 410 at both sides of the active layer 400 may employ vacuum
21 evaporation, chemical vapor deposition, spin coating, and inkjet printing. The
22 conventional process parameters are used in these techniques, and they are not
23 repeated herein. The conducting layer 410 may be formed by performing a conducting
24 treatment on the semiconductor layer. The conducting treatment may be an annealing
25 process at a high temperature, which makes carriers in the second sub-buffer layer
26 320 flowing into the semiconductor layer, thereby forming the conducting layer 410.
27 The fabrication process is simple, easy to implement, and easy for industrial
28 production.

29 **[0073]** Step S400 includes annealing the semiconductor layer 399 so that the carriers
30 in the first sub-buffer layer 310 enter into the semiconductor layer 399 through the
31 thin region 321 of the second sub-buffer layer 320, as shown in FIG. 11d.

1 [0074] In one embodiment, the annealing treatment is performed at a high
2 temperature such that carriers (e.g., hydrogen ions) in the material forming the first
3 sub-buffer layer 310 enter into the semiconductor layer 399 through the thin region
4 321 of the second sub-buffer layer 320, thereby making a part of the semiconductor
5 layer 399 to be conductive, which is the structure 5 in FIGS. 11d to 11f. Because the
6 thickness of the thin region 321 is in a certain range, no excessive carriers may enter
7 into the semiconductor layer 399 to make the whole semiconductor layer to be
8 conductive that may affect the performance of the thin film transistor.

9 [0075] In one embodiment, the thin region 321 with the range of the thickness
10 described above may be used to prevent carriers from continuously entering into the
11 semiconductor layer 399 in the subsequent fabrication processes, thereby preventing
12 the whole semiconductor layer 399 from becoming conductive. The temperature of
13 the annealing treatment is generally 360 to 400 °C. When the thickness of the thinner
14 region 321 is in the range described above, only at the temperature as previously
15 mentioned can be achieved that the carriers enter into the semiconductor layer 399,
16 thereby preventing the semiconductor layer 399 from becoming overly conductive.
17 Therefore, the width of the active layer of the thin film transistor is not limited by the
18 width of the gate and the width of the active layer can be made relatively small. The
19 on-state current can be significantly increased and also the performance in other
20 aspects is better.

21 [0076] Step S500 includes forming an insulating layer and a conductive layer 599
22 sequentially on surfaces of the second sub-buffer layer 320 and the semiconductor
23 layer 399 opposite from the substrate 100 with reference to FIG. 11e.

24 [0077] In one embodiment, the process of forming an insulating layer 499 on the
25 surfaces of the semiconductor layer 399 opposite from the substrate 100 may employ
26 vacuum evaporation, chemical vapor deposition, spin coating, and inkjet printing. The
27 process parameters used in these techniques are all conventional, and they are not
28 repeated herein. The fabrication process is simple, easy to implement, and easy for
29 industrial production.

30 [0078] In one embodiment, the process of forming a conductive layer 599 may
31 include vacuum evaporation, chemical vapor deposition, rotary coating, and inkjet
32 printing. The conventional process parameters used in these techniques are all

1 conventional, and they are not repeated herein. The fabrication process is simple, easy
2 to implement, and easy for industrial production.

3 **[0079]** Step S600 includes patterning the conductive layer 599 and the insulating
4 layer 499 by one patterning process to form the gate insulating layer 500 and the gate
5 600, as shown in FIG. 11f.

6 **[0080]** In one embodiment, the patterning process includes coating a layer of
7 photoresist on a surface of the conductive layer 599 opposite from the first sub-buffer
8 layer 310, then followed by exposing, developing, dry etching, photoresist peeling
9 and so on, thereby forming the gate insulating layer 500 and the gate 600. The
10 technical parameters used in each step of the conventional patterning process are not
11 repeated herein. The fabrication process is simple, easy to implement, and easy for
12 industrial production.

13 **[0081]** Step S700 includes performing a conducting treatment to the semiconductor
14 layer 399 that is not covered by the gate insulating layer 500 to obtain an active layer
15 400 and a conducting layer 410, as shown in FIG. 11g.

16 **[0082]** In one embodiment, a process of performing a conducting treatment to the
17 semiconductor layer 399 that is not covered by the gate insulating layer 500 may be
18 plasma doping or the like. The plasma may be H₂ plasma, He plasma, CF₄ plasma, O₂
19 plasma, etc. The specific steps, process conditions, and parameters for plasma doping,
20 etc. are all conventional plasma doping steps, process conditions, and parameters, and
21 they are not repeated herein. The process used to achieve the active layer 400 and the
22 conducting layer 410 is simple, easy to implement, and easy for industrial production.

23 **[0083]** Step S800 includes forming an interlayer insulating layer 700, a source 800,
24 and a drain 900, as shown in FIG. 11h.

25 **[0084]** In one embodiment, the process conditions, parameters, etc. in the steps of
26 S400, S500, and S600 all are the same or similar to the previous description, and they
27 are not repeated herein.

28 **[0085]** In one embodiment, with reference to FIG. 12 and FIGS. 13a to 13b, before
29 forming the buffer layer 300 on the surface of the substrate 100, the method further
30 includes:

1 **[0086]** Step S50 includes forming a light shielding layer 200 on the substrate 100
2 with reference to FIG. 13a.

3 **[0087]** In one embodiment, an orthographic projection of the light shielding layer 200
4 on the substrate 100 covers an orthographic projection of the active layer 400 on the
5 substrate 100, and the area of the orthographic projection of the light shielding layer
6 200 on the substrate is less than the area of the orthographic projection of the gate 600
7 on the substrate 100.

8 **[0088]** In one embodiment, the process of forming the light shielding layer 200 on the
9 surface of the substrate 100 may employ vacuum evaporation, chemical vapor
10 deposition, spin coating, and inkjet printing. The conventional process parameters
11 used in these techniques are not repeated herein.

12 **[0089]** In the step S10, after the light shielding layer 200 is formed on the substrate
13 100 (S50), the buffer layer 300 is formed on the substrate 100, covering the light
14 shielding layer 200 with reference to FIG. 13b. Other steps, conditions, parameters,
15 etc. are the same or similar as those described above, and they are not repeated herein.

16 **[0090]** Another embodiment of the present disclosure provides a display substrate. In
17 one embodiment, the display substrate includes the thin film transistor described
18 above. The display substrate can achieve better performance because the thin film
19 transistor can significantly increase the on-state current.

20 **[0091]** In one embodiment, the shape, configuration, fabrication process, and the like
21 of the display substrate may be the shape, configuration, and fabrication process of
22 the conventional display substrate. Furthermore, those skilled in the art may
23 understand that, in addition to the thin film transistor described above, the display
24 substrate further includes structures and components of the conventional display
25 substrate, and the connection relationship among the structures and the components is
26 also the connection relationship among the structures and components in the
27 conventional display substrate, and details thereof are not repeated herein.

28 **[0092]** Another embodiment of the present disclosure provides a display apparatus. In
29 one embodiment, the display apparatus includes the display substrate described above.
30 Since the performance of the display substrate is better, the display apparatus can
31 achieve better performance and display effect.

1 [0093] In one embodiment, the shape, configuration, preparation process, and the like
2 of the display apparatus may be the shape, configuration, and fabrication process of
3 the conventional display apparatus. Furthermore, those skilled in the art may
4 understand that, in addition to the display substrate described above, the display
5 apparatus also includes structures and components of the conventional display
6 apparatus, and the connection relationship among the structures and the components is
7 also the connection relationship among the structures and components in the
8 conventional display apparatus, and details thereof are not repeated herein.

9 [0094] The type of display apparatus is not particularly limited, for example, it may
10 include but not limited to mobile phones, tablets, wearable devices, game consoles,
11 etc.

12 [0095] Although the embodiments of the present disclosure have been shown and
13 described, it is understood that the above-described embodiments are illustrative and
14 are not to be construed as limiting the scope of the disclosure. The embodiments are
15 subject to variations, modifications, substitutions and variations.

16 [0096] The principles and the embodiments of the present disclosure are set forth in
17 the specification. The description of the embodiments of the present disclosure is only
18 used to help understand the apparatus and method of the present disclosure and the
19 core idea thereof. Meanwhile, for a person of ordinary skill in the art, the disclosure
20 relates to the scope of the disclosure, and the technical scheme is not limited to the
21 specific combination of the technical features, but also covers other technical schemes
22 which are formed by combining the technical features or the equivalent features of the
23 technical features without departing from the inventive concept. For example, a
24 technical scheme may be obtained by replacing the features described above as
25 disclosed in this disclosure (but not limited to) with similar features.

26

CLAIMS

What is claimed is:

1. A thin film transistor, comprising:

a substrate;

a buffer layer on a surface of the substrate;

an active layer on a surface of the buffer layer opposite from the substrate;

a gate insulating layer on a surface of the active layer opposite from the substrate, and

a gate on a surface of the gate insulating layer opposite from the substrate;

wherein a width of the active layer is smaller than a width of the gate, and an orthographic projection of the gate on the substrate covers an orthographic projection of the active layer on the substrate.

2. The thin film transistor according to claim 1, wherein a conducting layer is provided at two sides of the active layer respectively and an orthographic projection of the conducting layer on the substrate partially overlaps the orthographic projection of the gate on the substrate.

3. The thin film transistor according to claim 2, wherein the buffer layer comprises:

a first sub-buffer layer on the substrate, and a material forming the first sub-buffer layer contains carriers; and

a second sub-buffer layer on a surface of the first sub-buffer layer opposite from the substrate, the second sub-buffer layer comprising at least a thin region, wherein the orthographic projection of the conducting layer covers an orthographic projection of the thin region on the substrate, and the orthographic projection of the thin region at least has an overlapping area with the orthographic projection of the gate on the substrate.

4. The thin film transistor according to claim 3, wherein a groove is provided on a surface of the second sub-buffer layer opposite from the first sub-buffer layer, and a part of the second sub-buffer layer under a bottom of the groove

1 constitutes the thin region.

2 5. The thin film transistor according to claim 3, wherein a groove is
3 provided on a surface of the second sub-buffer layer facing the first sub-buffer layer,
4 and a part of the second sub-buffer layer on a top of the groove constitutes the thin
5 region.

6 6. The thin film transistor according to any of claims 3-5, wherein a
7 thickness of the thin region is less than or equal to about 100 nm.

8 7. The thin film transistor according to any of claims 3-6, wherein a
9 material forming the first sub-buffer layer comprises silicon nitride.

10 8. The thin film transistor according to any of claims 3-7, wherein a
11 material forming the second sub-buffer layer comprises silicon dioxide.

12 9. The thin film transistor according to claim 1, wherein a material
13 forming the active layer comprises amorphous indium gallium zinc oxide.

14 10. The thin film transistor according to claim 1, wherein a width of the
15 active layer is within a range of about 1 μm to about 3 μm .

16 11. The thin film transistor according to claim 1, further comprising:
17 a light shielding layer between the substrate and the buffer layer,
18 wherein an orthographic projection of the light shielding layer on the substrate
19 covers the orthographic projection of the active layer on the substrate, and an area of
20 the orthographic projection of the light shielding layer on the substrate is smaller than
21 an area of the orthographic projection of the gate on the substrate.

22 12. A method of fabricating a thin film transistor, comprising:
23 providing a substrate;
24 forming a buffer layer on a surface of the substrate;
25 forming an active layer on a surface of the buffer layer opposite from the
26 substrate; and
27 forming a gate insulating layer and a gate sequentially on a surface of the
28 active layer opposite from the substrate,

1 wherein a width of the active layer is smaller than a width of the gate, and an
2 orthographic projection of the gate on the substrate covers an orthographic of the
3 active layer on the substrate.

4 13. The method according to claim 12, wherein forming the buffer layer on
5 the surface of the substrate comprises:

6 forming a first sub-buffer layer on the surface of the substrate, wherein a
7 material forming the first sub-buffer layer contains carriers; and

8 forming a second sub-buffer layer having at least a thin region on a surface of
9 the first sub-buffer opposite from the substrate.

10 14. The method according to claim 13, wherein forming the active layer
11 on the surface of the buffer layer opposite from substrate and forming the gate
12 insulating layer and the gate comprise:

13 forming a semiconductor layer on a surface of the second sub-buffer layer
14 opposite from the substrate;

15 annealing the semiconductor layer to enable the carriers in the first sub-buffer
16 layer to enter the semiconductor layer through the thin region of the second sub-buffer
17 layer;

18 forming an insulating layer and a metal layer on surfaces of the second sub-
19 buffer layer and the semiconductor layer opposite from the substrate;

20 patterning the metal layer and the insulating layer by one-time patterning
21 process to form the gate and the gate insulating layer respectively; and

22 performing a conducting treatment to a part of the semiconductor layer that is
23 not covered by the gate insulating layer and the gate, thereby obtaining the active
24 layer and the conducting layer.

25 15. The method according to claim 13, wherein forming the second sub-
26 buffer layer having at least a thin region comprises:

27 forming the second sub-buffer layer on a surface of the first sub-buffer
28 opposite from the substrate; and

1 forming a groove on a surface of the second sub-buffer layer opposite from the
2 substrate, wherein a part of the second sub-buffer layer under a bottom of the groove
3 constitutes the thin region.

4 16. The method according to claim 13, wherein forming the second sub-
5 buffer layer having the thin region comprises:

6 forming the second sub-buffer layer on a surface of the first sub-buffer
7 opposite from the substrate; and

8 forming a groove on a surface of the second sub-buffer layer facing the
9 substrate, wherein a part of the second sub-buffer layer on a top of the groove
10 constitutes the thin region.

11 17. The method according to any one of claims 12 to 16, before forming
12 the buffer layer on the surface of the substrate, further comprising:

13 forming a light shielding layer on the surface of the substrate,

14 wherein an orthographic projection of the light shielding layer on the substrate
15 covers an orthographic projection of the active layer on the substrate, and an area of
16 the orthographic projection of the light shielding layer on the substrate is less than an
17 area of the orthographic projection of the gate on the substrate.

18 18. A display substrate, comprising the thin film transistor according to
19 any one of claims 1 to 11.

20 19. A display apparatus, comprising the display substrate according to
21 claim 18.

Related Art

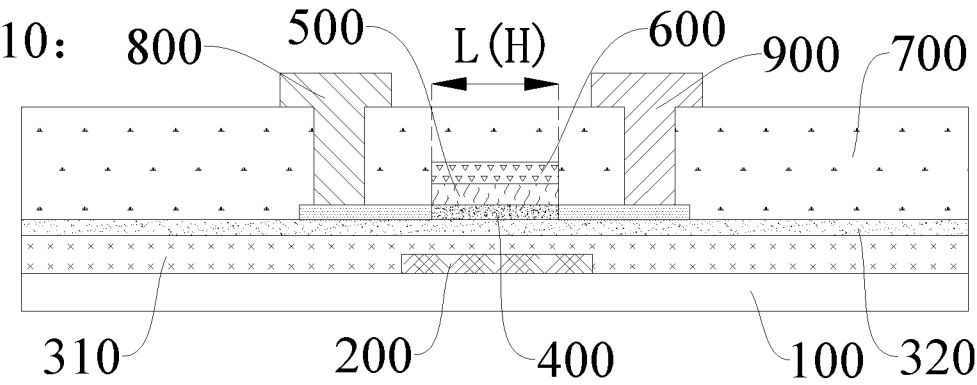


FIG.1

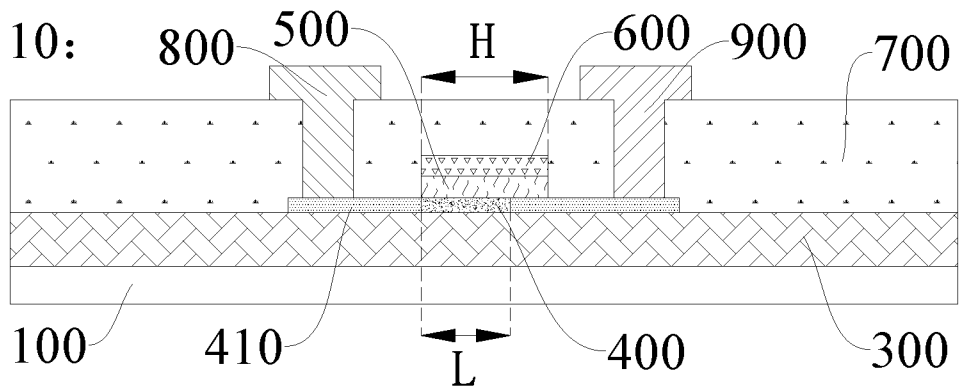


FIG. 2

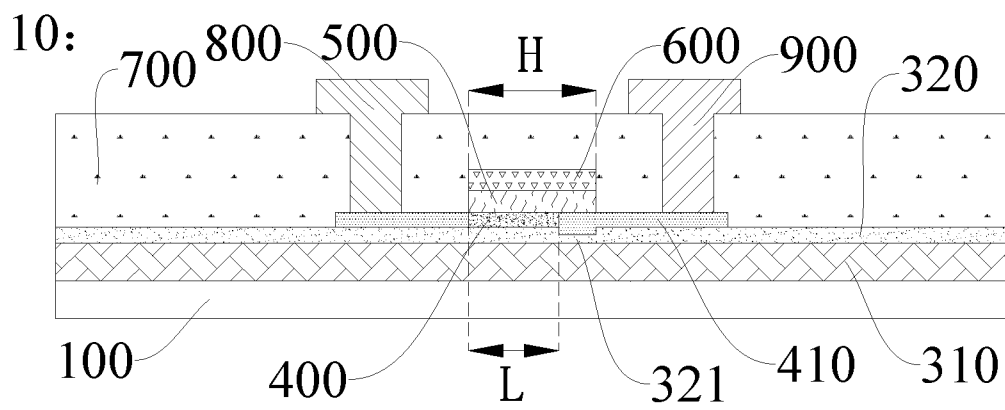


FIG. 3

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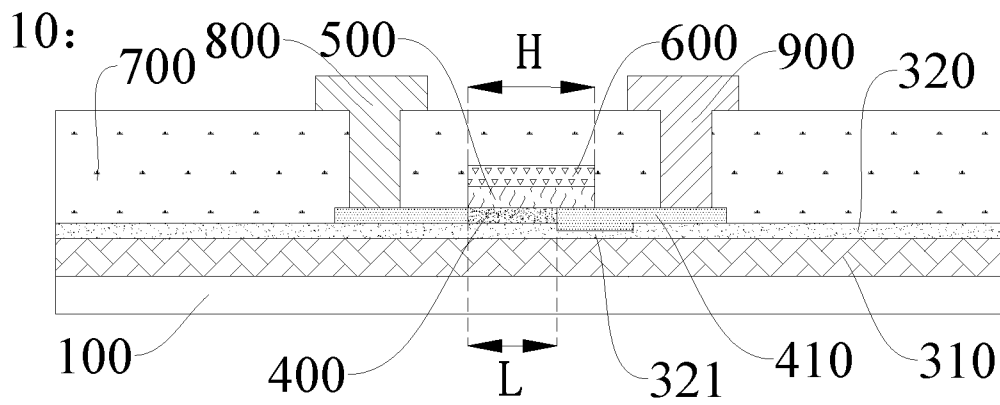


FIG. 4

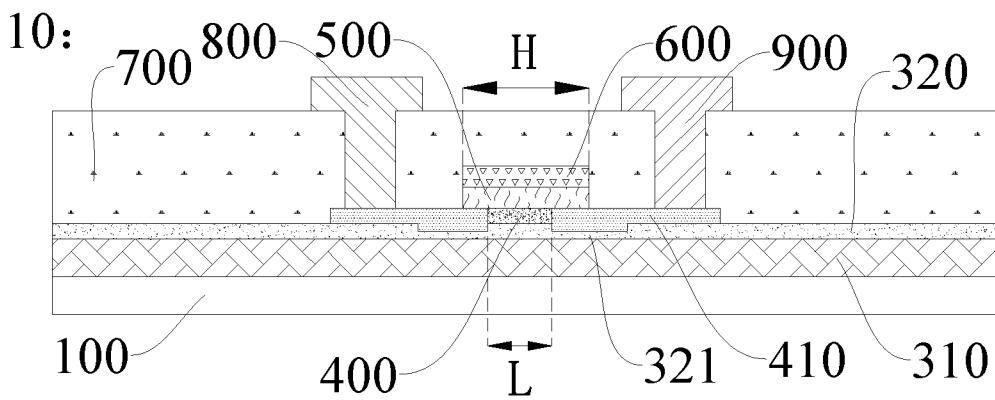


FIG. 5

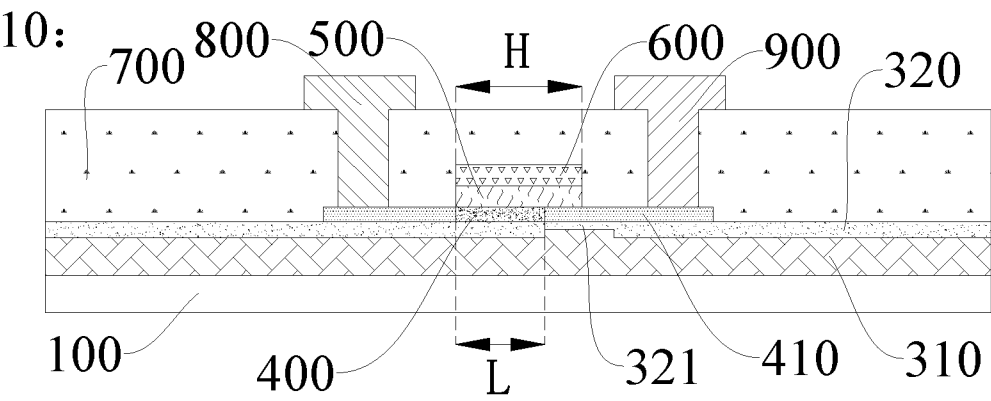


FIG.6

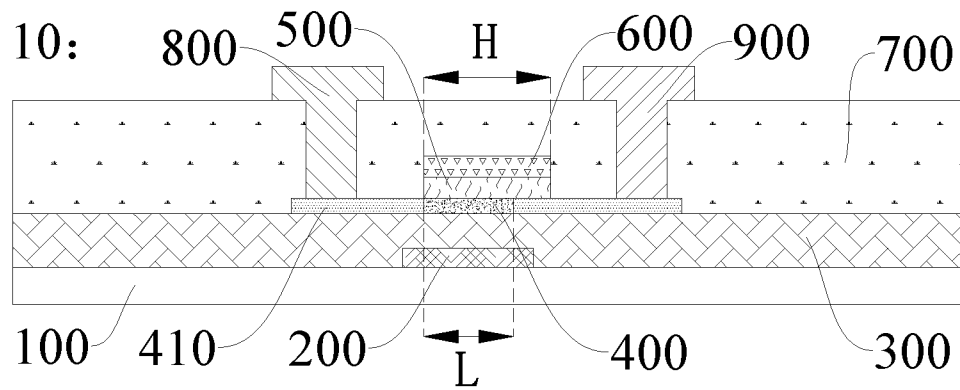


FIG.7

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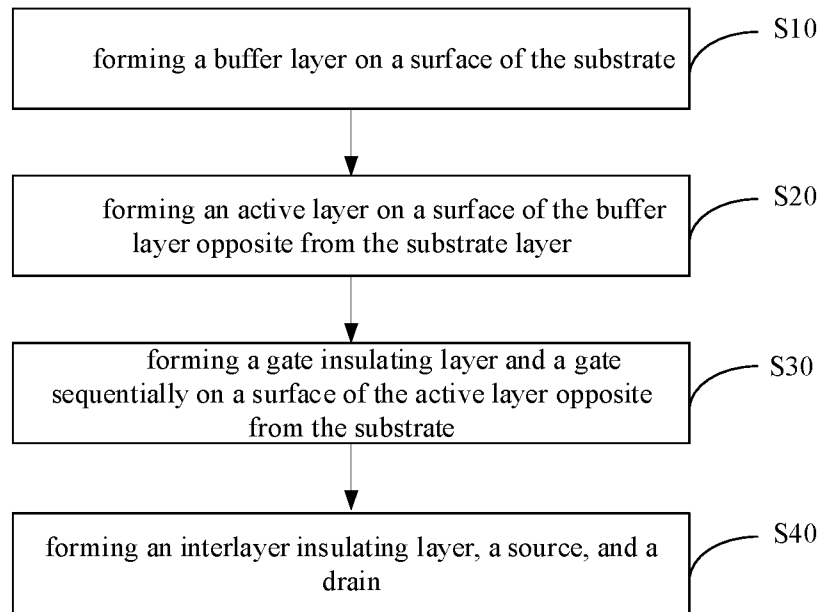


FIG.8

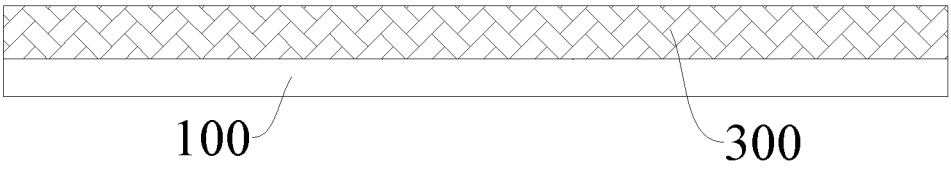


FIG.9a

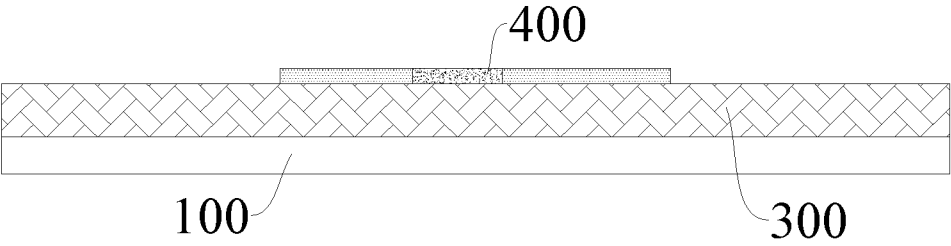


FIG.9b

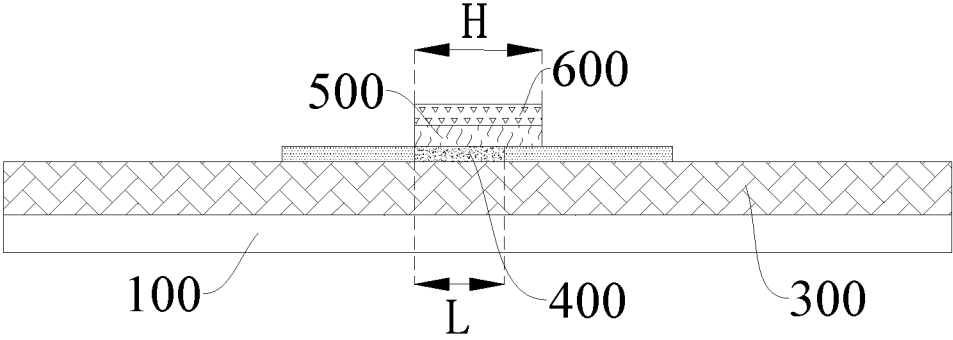


FIG. 9c

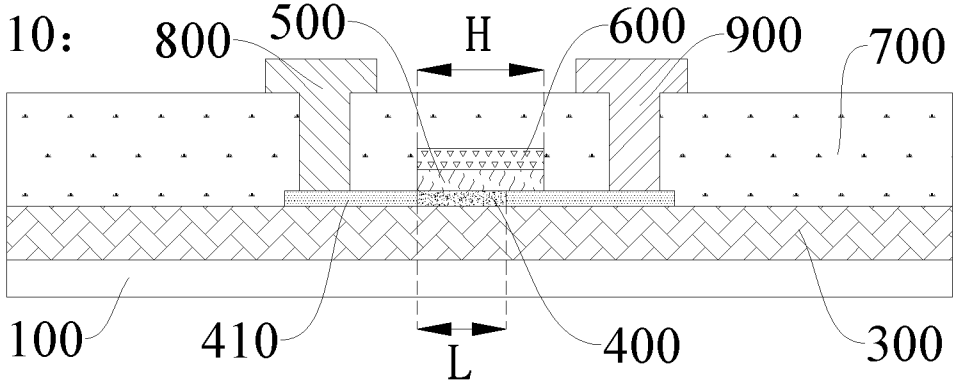


FIG. 9d

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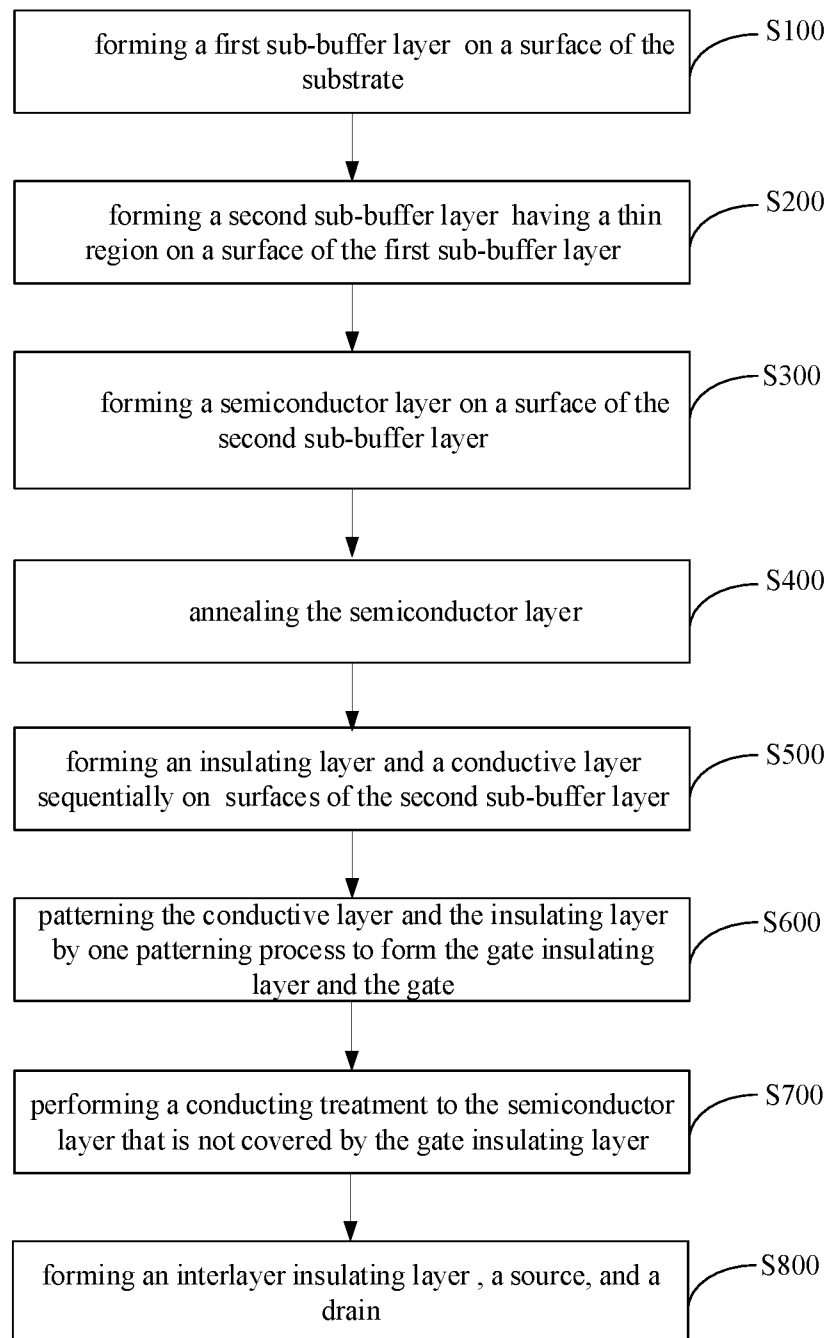


FIG.10

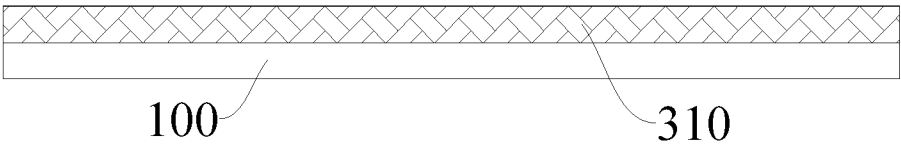


FIG.11a

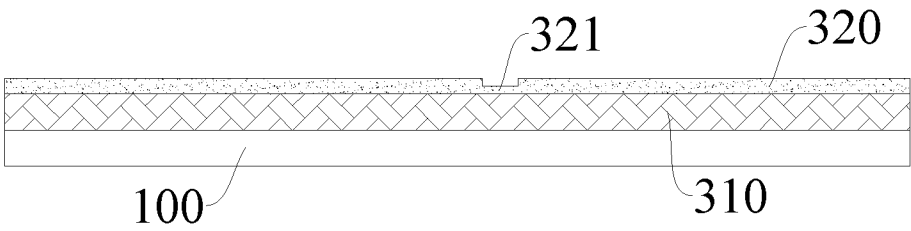


FIG.11b

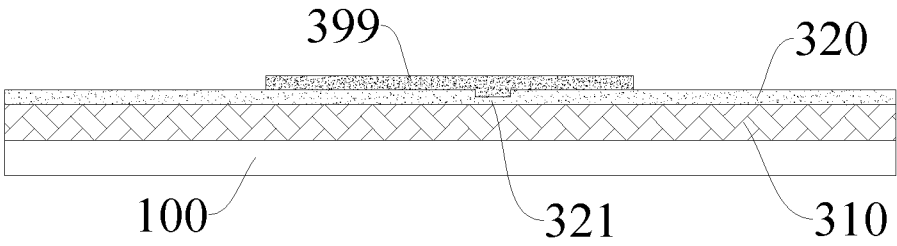


FIG.11c

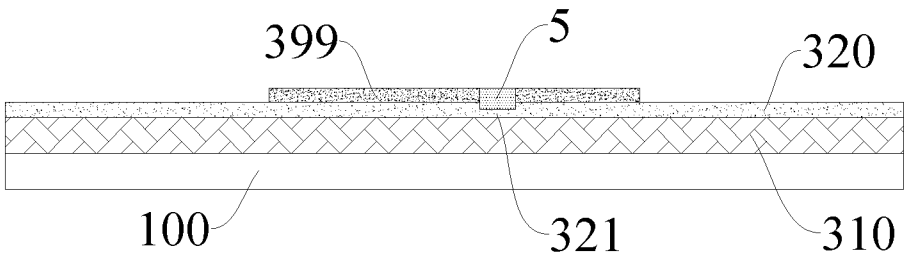


FIG.11d

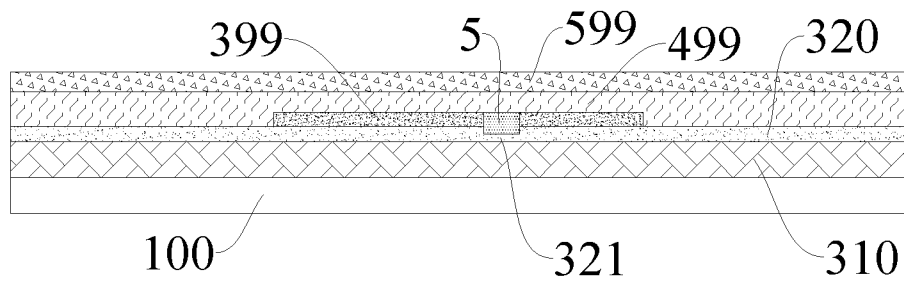


FIG.11e

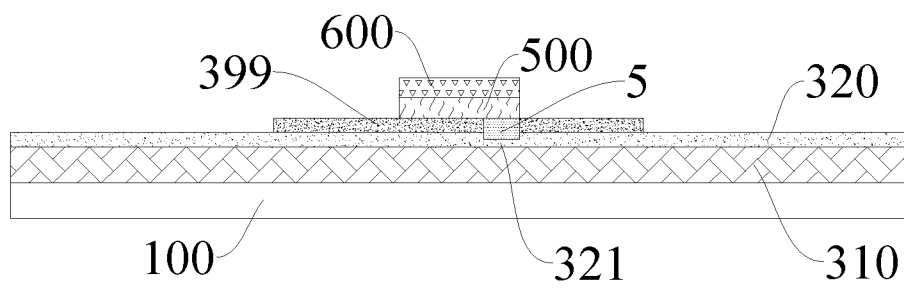


FIG.11f

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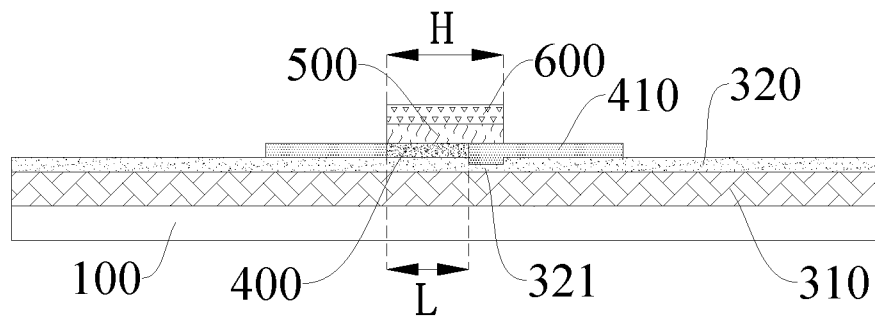


FIG. 11g

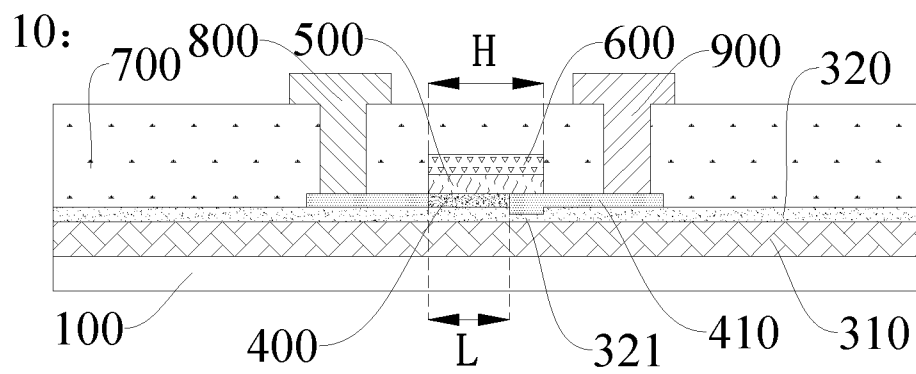


FIG. 11h

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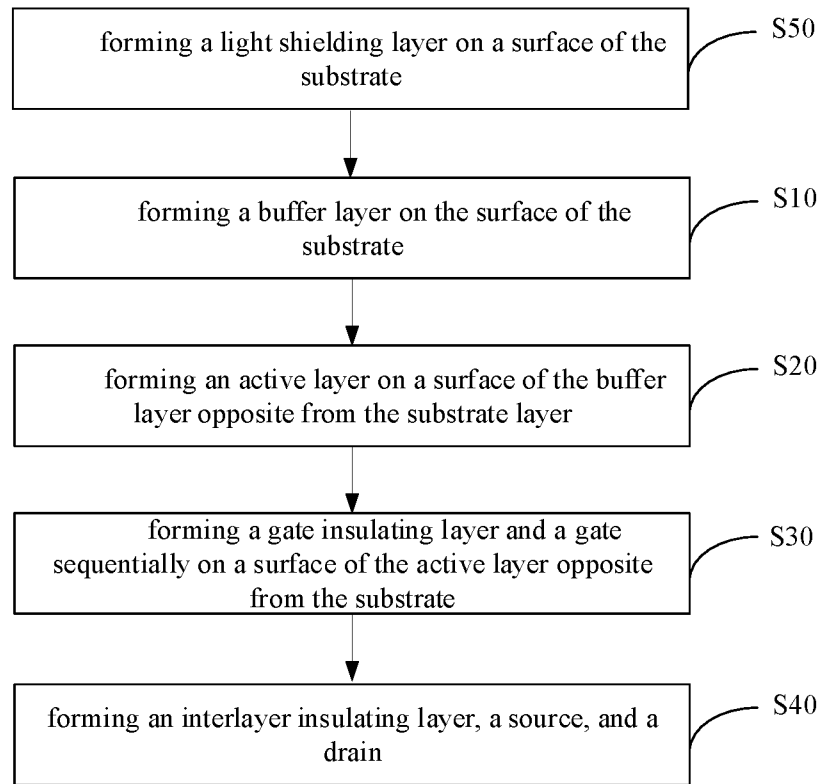


FIG. 12

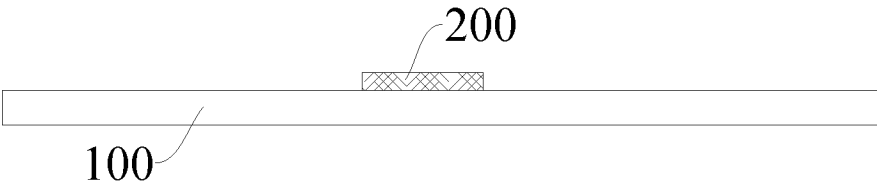


FIG.13a

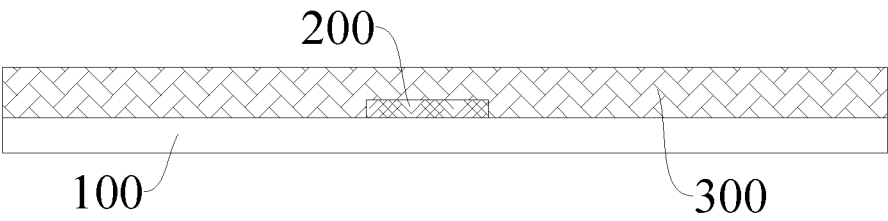


FIG. 13b

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/116180

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/786(2006.01)i; H01L 21/34(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI, IEEE: transistor, tft, gate, active, width, switch, conducting, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 109860305 A (HEFEI XINSHENG OPTOELECTRONIC TECHNOLOGY CO., LTD. et al.) 07 June 2019 (2019-06-07) description, paragraphs [0033]-[0086], and figures 1-8	1-19
X	CN 107331619 A (BOE TECHNOLOGY GROUP CO., LTD. et al.) 07 November 2017 (2017-11-07) description, paragraphs [0017]-[0102], and figures 1-2	1-19
A	CN 105097948 A (BOE TECHNOLOGY GROUP CO., LTD.) 25 November 2015 (2015-11-25) the whole document	1-19
A	CN 104681627 A (BOE TECHNOLOGY GROUP CO., LTD.) 03 June 2015 (2015-06-03) the whole document	1-19
A	US 2009230397 A1 (HITACHI DISPLAYS. LTD.) 17 September 2009 (2009-09-17) the whole document	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

15 January 2020

Date of mailing of the international search report

11 February 2020

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961454

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/116180

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	109860305	A	07 June 2019	None			
CN	107331619	A	07 November 2017	US	2019006490	A1	03 January 2019
CN	105097948	A	25 November 2015	CN	105097948	B	21 December 2018
CN	104681627	A	03 June 2015	CN	104681627	B	06 September 2019
				JP	2015112918	A	22 June 2015
				DE	102014018313	A1	11 June 2015
				JP	6238127	B2	29 November 2017
US	2009230397	A1	17 September 2009	US	8421940	B2	16 April 2013
				CN	101540332	A	23 September 2009
				JP	2009224589	A	01 October 2009
				CN	101540332	B	30 May 2012
				JP	5485517	B2	07 May 2014