United States Patent [19]
Schmersal

[11] **3,803,449**
[45] **Apr. 9, 1974**

[54] **METHOD AND APPARATUS FOR MANIPULATING DISCRETE DISCHARGE IN A MULTIPLE DISCHARGE GASEOUS DISCHARGE PANEL**

[75] Inventor: **Larry J. Schmersal,** Toledo, Ohio

[73] Assignee: **Owens-Illinois, Inc.,** Toledo, Ohio

[22] Filed: **May 3, 1971**

[21] Appl. No.: **139,533**

[52] **U.S. Cl.** .... **315/169 TV,** 315/169 R
[51] **Int. Cl.** **H05b 37/00**
[58] **Field of Search** .... 315/169, 169 TV

[56] **References Cited**

UNITED STATES PATENTS

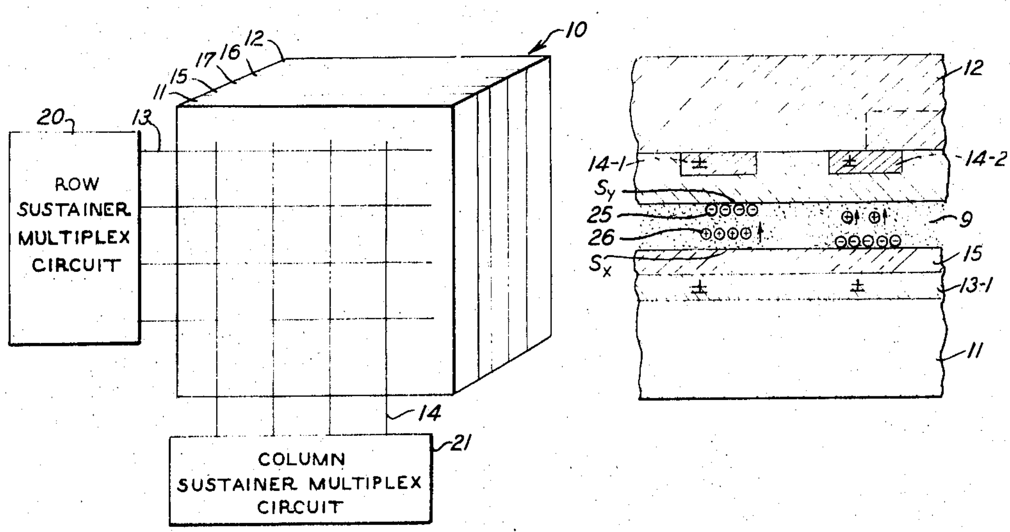
3,499,167	3/1970	Baker et al.	315/169 TV
3,513,327	5/1970	Johnson	315/169 TV X
3,526,711	9/1970	DeBoer	315/169 R X
3,588,597	6/1971	Murley, Jr.	315/169 R
3,614,739	10/1971	Johnson	315/169 TV X

Primary Examiner—Herman Karl Saalbach
Assistant Examiner—Lawrence J. Dahl
Attorney, Agent, or Firm—Jim Zegeer; Donald Keith Wedding

[57] **ABSTRACT**

There is disclosed unique methods and apparatus for manipulating the discharge condition of selected discharge sites of a multiple discharge gas discharge panel having transversely oriented, insulated, row-column conductor arrays. Periodically applied alternating pulses, particularly width modulated square pulses are used to sustain as well as manipulate the discharge condition of selected discharge sites in the panel.

28 Claims, 13 Drawing Figures



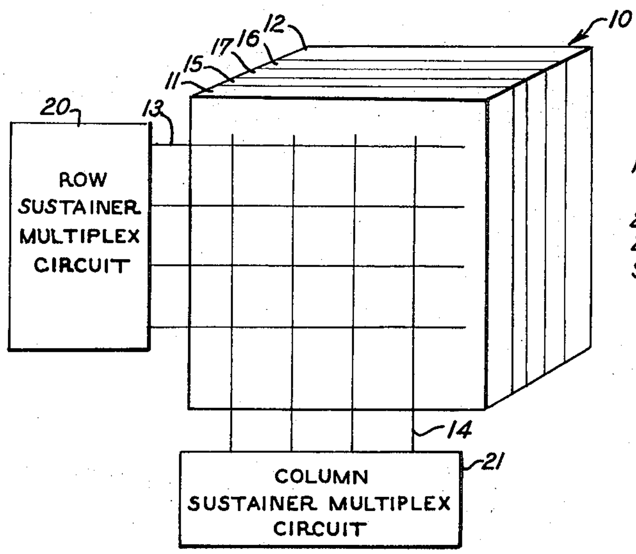


FIG. 1

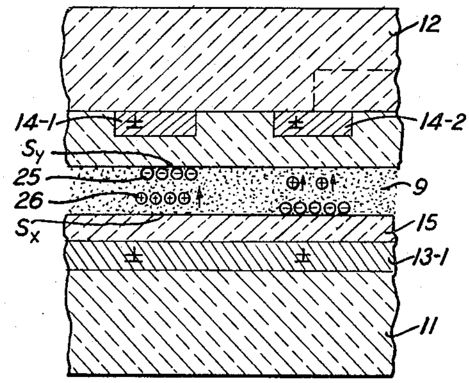


FIG. 2

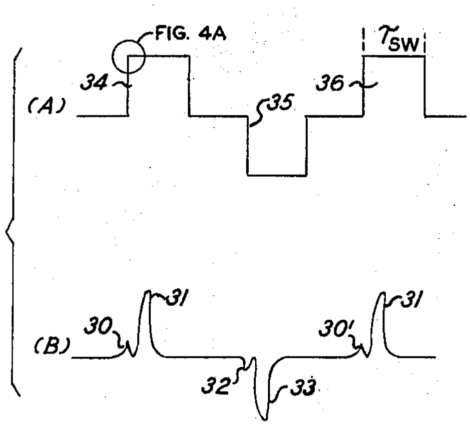


FIG. 3

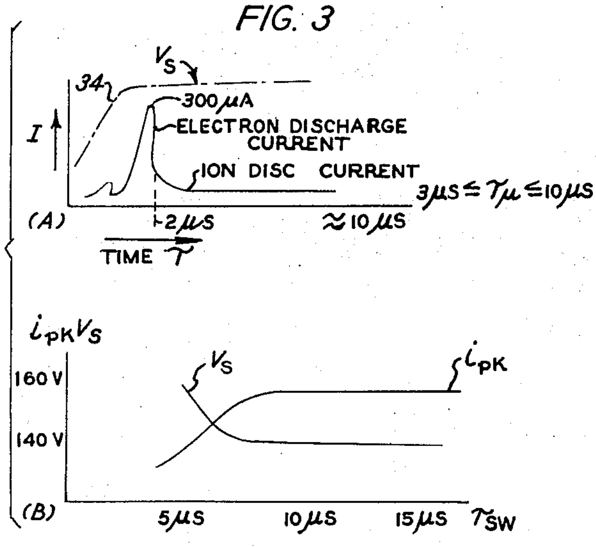


FIG. 4

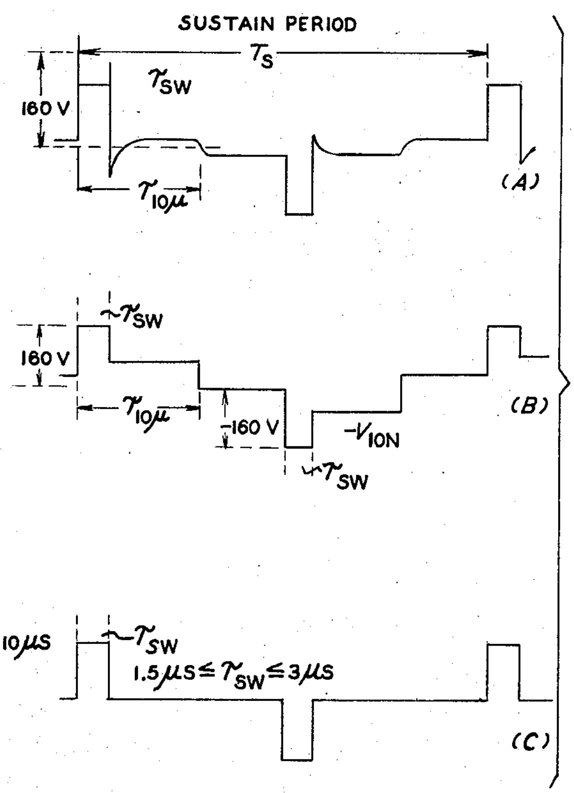


FIG. 5

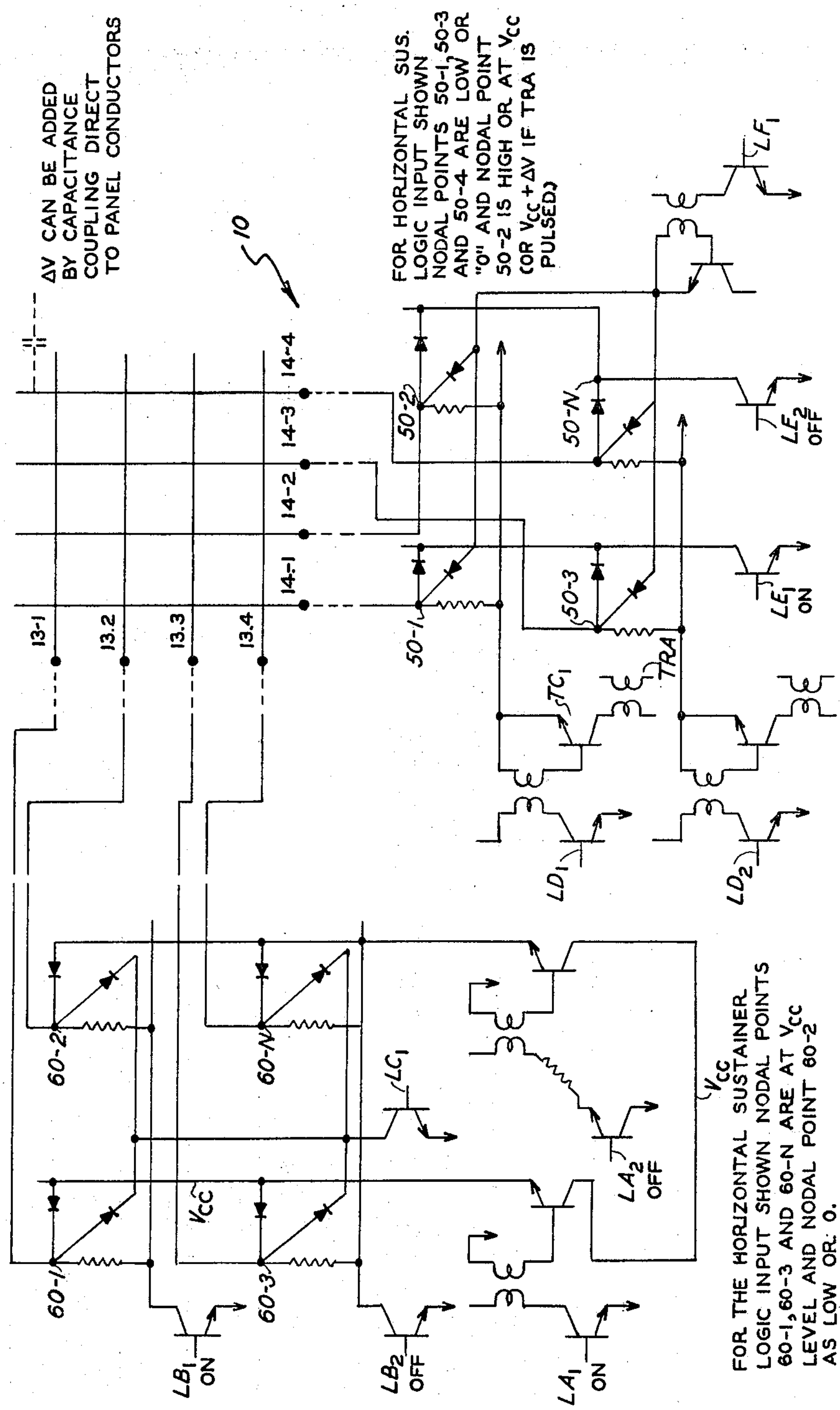
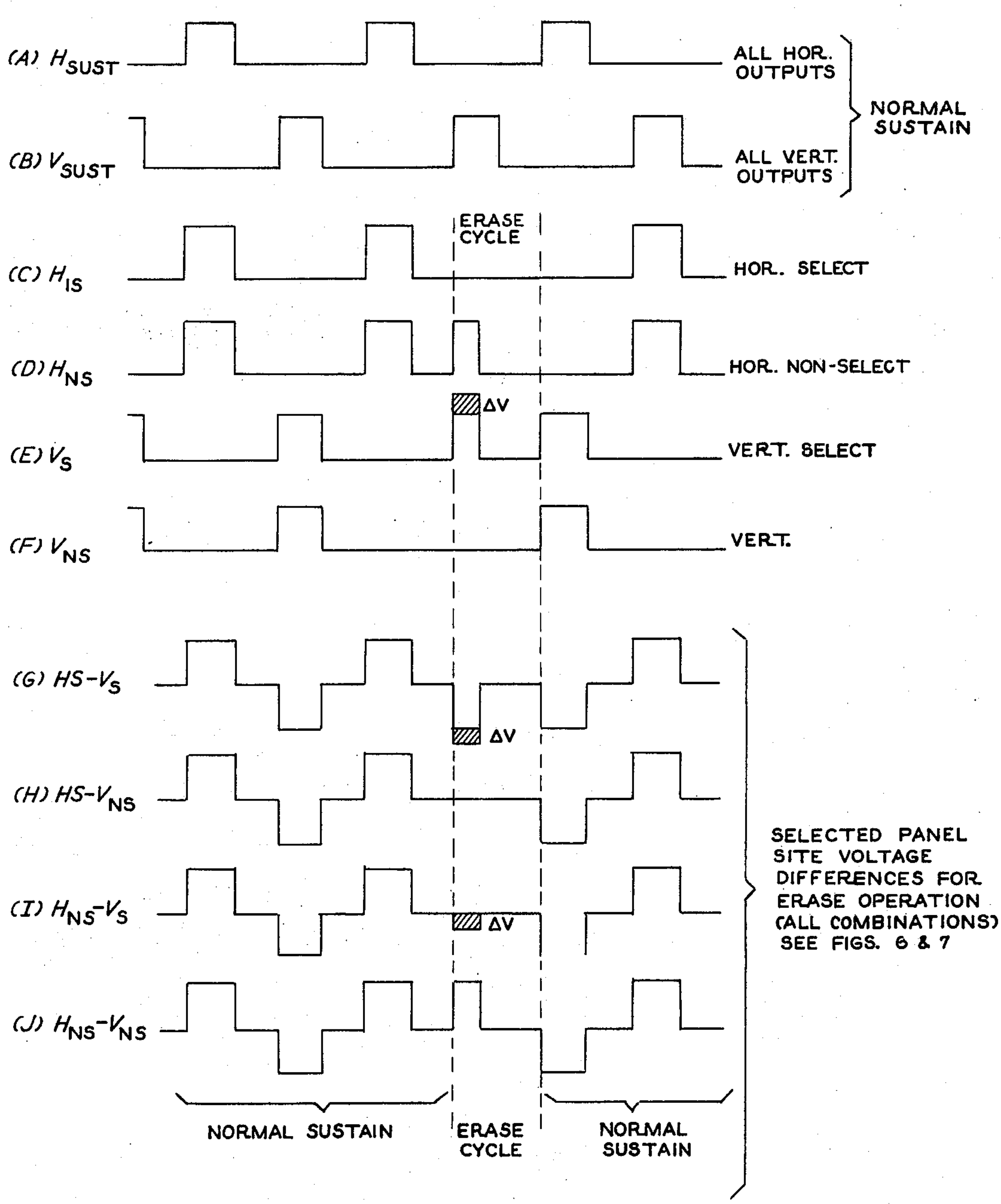

ΔV CAN BE ADDED BY CAPACITANCE COUPLING DIRECT TO PANEL CONDUCTORS
10
FOR HORIZONTAL SUS. LOGIC INPUT SHOWN NODAL POINTS 50-1, 50-3 AND 50-4 ARE LOW OR "0" AND NODAL POINT 50-2 IS HIGH OR AT VCC (OR VCC+ΔV IF TRA IS PULSED)
14-4
14-3
14-2
14-1
13-1
13.2
13.3
13.4
50-2
50-N
50-1
50-3
LF1
LE2 OFF
LE1 ON
TC1
TRA
LD1
LD2
60-2
60-N
60-1
60-3
VCC
LC1
LA2 OFF
LB1 ON
LB2 OFF
LA1 ON
FOR THE HORIZONTAL SUSTAINER LOGIC INPUT SHOWN NODAL POINTS 60-1, 60-3 AND 60-N ARE AT VCC LEVEL AND NODAL POINT 60-2 AS LOW OR 0.

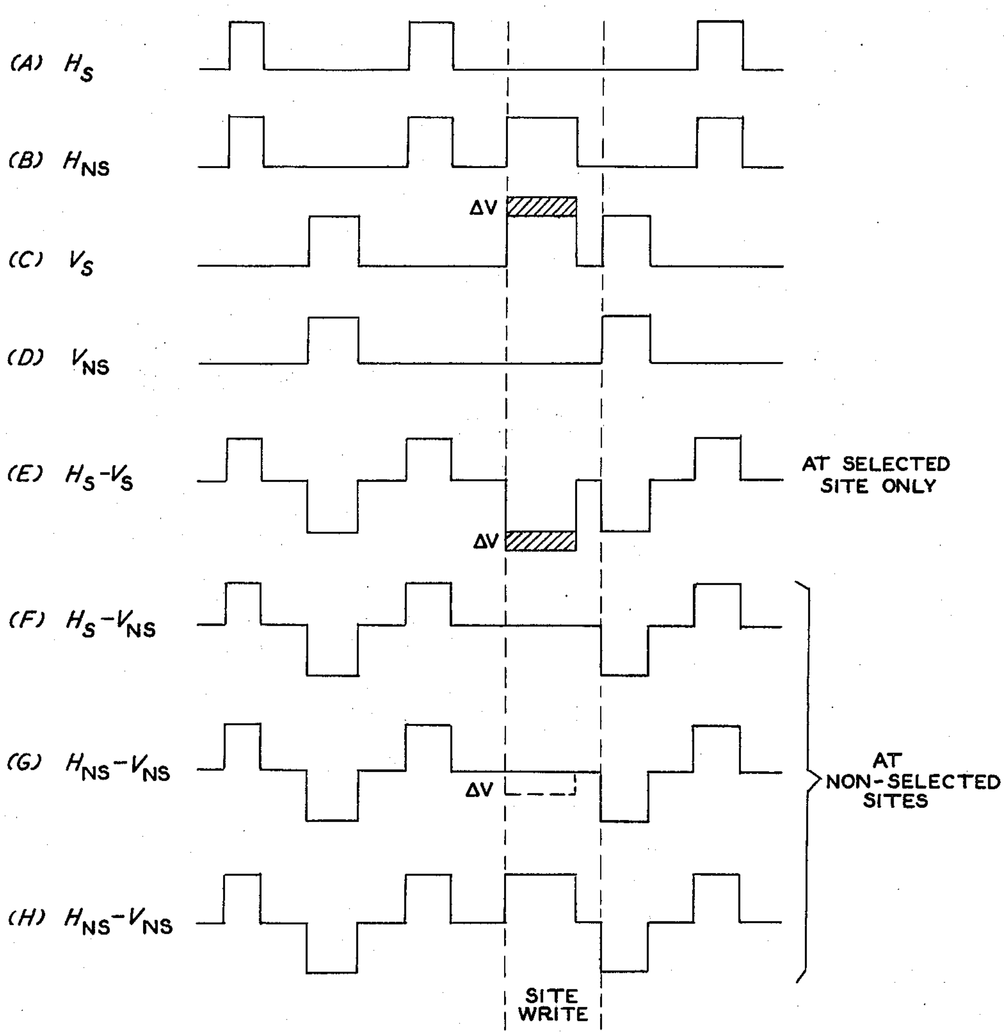
FIG. 6

FIG. 7



SITE ERASE OPERATION

FIG. 8



SINGLE SELECTED SITE WRITE OPERATION

FIG. 9

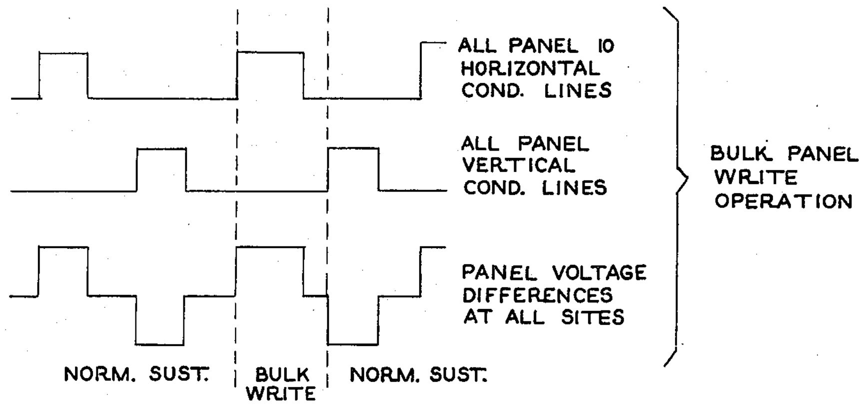


FIG. 10A

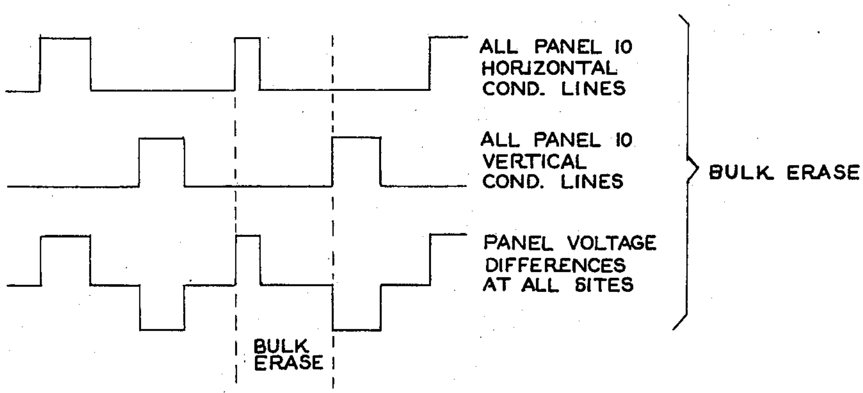


FIG. 10B

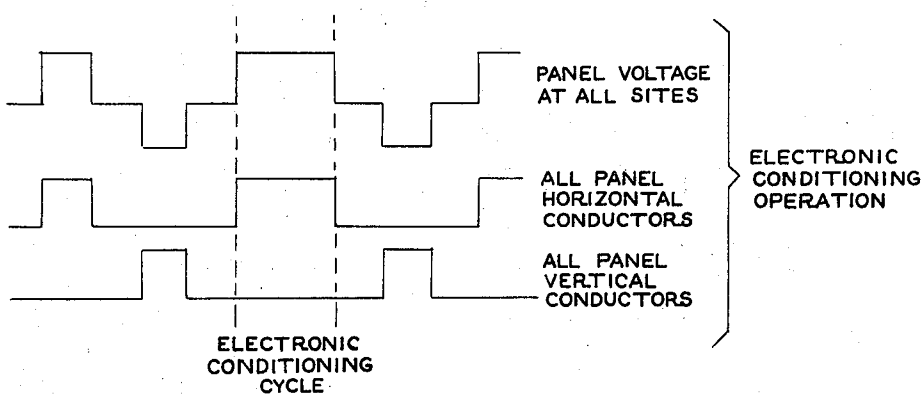


FIG. 10C

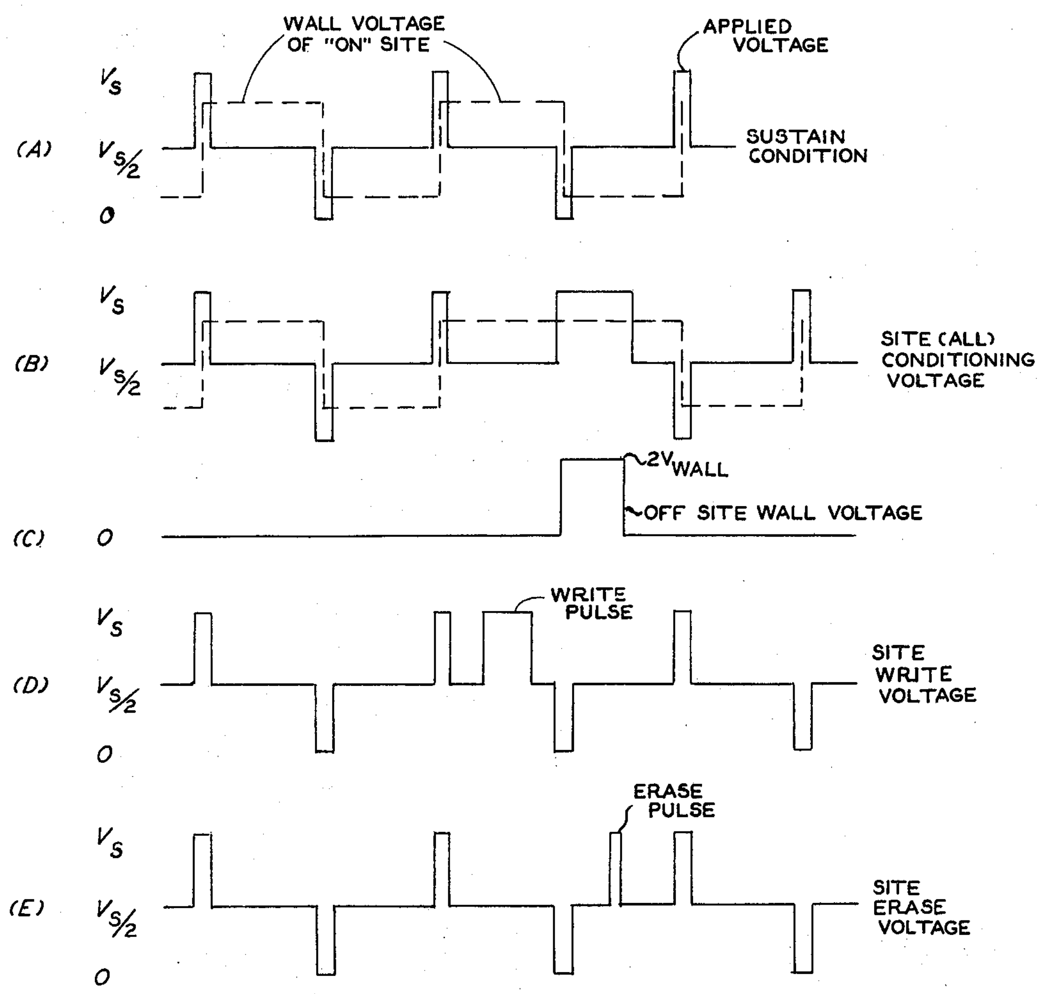

WALL VOLTAGE
OF "ON" SITE
APPLIED
VOLTAGE
V_S
(A)
$V_{S/2}$
0
SUSTAIN
CONDITION
V_S
(B)
$V_{S/2}$
SITE (ALL)
CONDITIONING
VOLTAGE
2V WALL
OFF SITE WALL VOLTAGE
(C)
0
WRITE
PULSE
V_S
(D)
$V_{S/2}$
0
SITE
WRITE
VOLTAGE
ERASE
PULSE
V_S
(E)
$V_{S/2}$
0
SITE
ERASE
VOLTAGE

FIG. 11

METHOD AND APPARATUS FOR MANIPULATING DISCRETE DISCHARGE IN A MULTIPLE DISCHARGE GASEOUS DISCHARGE PANEL

The present invention is directed to providing a new method and apparatus for sustaining, writing and erasing information on a gaseous discharge panel of the non-cellulated type disclosed in Baker et al. U.S. Pat. No. 3,499,167 and type disclosed in Bitzer et al. U.S. Pat. No. 3,559,199. In the Baker et al. patent there is disclosed a gas discharge display/memory device in which a pair of glass plate members are joined in spaced apart relation, the glass plate members carrying dielectrically coated multiple conductor arrays, the row and column conductor arrays in the active panel area being comprised of conductors extending parallel to the long direction of the plates, respectively. The plates are joined by a spacer sealant with their long axes transverse to each other with the cross points of the conductor arrays defining a matrix or array of discrete discharge sites each of which is discretely manipulatable by control of the potentials applied to the conductors.

Typically, the maintaining potentials for the discharge in such panels and the discrete sites is constituted by a periodically applied voltage, normally designated as the sustainer voltage. In the past, such voltage could be a sine wave, square wave as well as a number of other waveforms. In some cases, "gaps" were provided in the sustainer voltage so as to permit addressing of discrete sites in the panel as is disclosed in the aforementioned Bitzer patent (as also disclosed in Mayer et al. U.S. Pat. No. 3,573,542). Moreover, the discharge condition manipulating voltages may be bipolar pulse potentials which are algebraically combined in various ways and at various times with the sustainer potential to manipulate the discharge condition, particularly in rapidly turning off a selected discrete discharge site which has previously been turned on.

In accordance with the present invention, the operation of sustaining, writing and erasing information e.g. discrete discharges and selected discharge sites in a discharge panel of the general type disclosed in the aforementioned Baker et al. patent, may be accomplished by a constant amplitude pulse square wave sustainer with no additional circuitry required. Address operations, as well as sustain operations are accomplished entirely by means of modulation of the square wave pulses so as to control the strength of the discharge. In addition, it is possible to accomplish panel conditioning operations by means of a further extension of this concept. Moreover, by utilizing a sustaining waveform of the character disclosed herein, the aging is reduced; that is, the change in electrical characteristics of the panel, as a function of time for which they are burned or turned on, is improved. In addition, this type of sustainer and control can yield more light output and be more efficient than previous sustainer systems.

With regard to circuit requirements, one primary advantage over previous write/erase/sustain electronic systems for manipulating the discharge condition of selected discharge sites of a gaseous discharge panel, is that this invention permits elimination of roughly half of the circuits required in previous address system. Previous address systems, as indicated above, separated the functions of the sustain operation circuitry from the write/erase circuitry. The present invention accomplishes this operation within the framework of the sustainer and control circuits therefore. This invention may require more sustainers than in previous systems, however, as will appear further hereinafter, the multiplexing approach to such sustainers provides a degree of flexibility not heretofore available.

The invention also permits writing or erasing on either the positive or negative cycles of the sustainer at no additional cost since this means that the sustainer must produce a write or an erase pulse of an opposite polarity which the sustainers are easily capable of providing. Moreover, only one power supply will be required for writing and erasing and sustaining as well as even conditioning the panel. With respect to the panel itself, there are a number of notable advantages resulting from this invention. In previous sustainer voltage designs, there were a number of difficulties. When the sustainer voltage was at a sine waveform, the discharges were not intense enough and did not produce enough light. However, in square waves, even though enough light was produced, the high current tended to limit panel life. All waveforms, obviously, cause some modification of single individual discharge site characteristics as a function of time. It is believed that a significant contributor to this alteration in discharge site characteristic is the discharge current, and, more specifically, the ion current as opposed to the electron current in the discharge. The present invention produces more light with increased efficiency and at the same time reduces panel aging by limiting ion impaction processes.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent from the following specification and drawings wherein:

FIG. 1 is a simplified diagram of a gaseous discharge panel device and electrical diagram incorporating the invention,

FIG. 2 is an explanatory partial cross-sectional view, enlarged, but not to proportional scale,

FIGS. 3A, 3B are simplified waveform diagrams illustrating one basic feature of the invention,

FIG. 4A is a diagram showing the relation of electron and ion currents in a discharge at one selection site as plotted against time, and FIG. 4B shows the site characteristics as a function of sustained pulse width for constant wall charging as well as the peak current and change in wall voltage as a function of the difference between firing voltage and applied sustain voltage,

FIGS. 5A, 5B and 5C illustrate three sustain waveforms which may be used in the practice of the invention,

FIG. 6 shows the vertical or column sustain multiplexing circuit, incorporating the invention,

FIG. 7 shows the horizontal or row sustain multiplexing circuit incorporating the invention,

FIGS. 8A–8J shows the sustain and erase waveforms,

FIG. 9 shows the sustain waveforms for single discharge site operation,

FIGS. 10A are waveforms for illustrating the bulk panel write operation, FIG. 10B are wave forms for illustrating the bulk panel erase operation, and FIG. 10C are waveforms for illustrating the electronic "conditioning" operation panel and, FIGS. 11A–11E are another set of waveforms for illustrating other aspects of the voltage conditions for the write and erase operations.

The discharge current of a selected discharge site in a gaseous discharge display panel of the type referenced in the above mentioned Baker et al. and Bitzer et al. patent consists essentially of an electron and an ion current. The electrons are attracted to and collect upon one boundary wall of the site (the one which is instantaneously positive) and the ions to the opposite or opposing wall or boundary for the discharge site, such boundaries being defined by a dielectric or insulating coating on a crossed conductor pair locating the site. The light output resulting from the discharge is due almost solely to those electrons which are energized or excited sufficiently to emit light as a spindown from a higher energy state. The ion current contributes little or nothing to the light output but does contribute to the wall charging (see FIG. 4A). It is believed that one of the primary causes of panel degredation due to light is the bombardment of ions against the wall of a discharge site. This causes cratering and other chemical and electrical changes in the surface (FIG. 2 Sx and Sy) at each discharge site. The ions having heavier mass, travel at a lower velocity. However, their impact is $1/2MV^2$. It has been found that the current discharge resulting from both the ion and electron do not change to any great extent if the sustainer width is in excess of 10 microseconds. This suggests that the collection time required for roughly 90 percent of the ions as well as 100 percent of the electrons is in that range. The electron and collection time is around 500 nanoseconds. If the sustainer pulse width is made to be considerably below 10 microseconds the result would be that fewer ions will be collected at the wall. This results in reduced wall voltage but, at the same time aging is reduced. While it is possible, and within the contemplation of this invention, to terminate the sustainer pulse voltage immediately after collection of all the electrons, to thereby minimize the number of ions which will impact the wall of the discharge unit, this may require that the sustainer voltage be increased in amplitude. A basic aspect of this invention is that it makes use of the fact that the amount of wall charge transfered per each discharge is a function of the applied voltage and the duration for which that voltage is applied.

In FIG. 1, a gaseous discharge display panel **10**, constructed generally in the manner disclosed in Baker et al. U.S. Pat. No. 3,499,167 is constituted by a pair of support plates **11** and **12** on which are placed row (x) conductors **13** and column (y) conductors **14**, the conductor arrays having dielectric or insulative coatings **15** and **15**, respectively, applied thereto. The respective plates are joined in spaced apart relation by spacer sealant means **17** to form a thin gaseous discharge chamber in which may be placed a neon-argon gaseous mixture as is disclosed in Nolan application Ser. No. 764,577 filed August 1968. Other gaseous discharge mediums may likewise be incorporated in the panel but the improvement achieved by the use of the gas mixture recited above permits the panels to be operated without thermal shock and at the same time with good and efficient light output and memory margins. The individual conductors **13–1, 13–2 . . . 13**–N in row conductor array **13** are driven by a row conductor sustainer multiplexing circuitry **20** and the column conductors are driven by column conductor sustainer multiplexing matrix **21.** The selection matrices **20** and **21** receive input signals from a signal source, not shown, but which may be a computer, keyset, tape, card reader or other data source.

Referring now to FIG. **2,** a section of the panel **10** is shown in greatly enlarged cross-section to facilitate explanation of a basic aspect of the present invention and, is to be considered in relation to the waveforms illustrated in FIGS. **3**A, **3**B and relationships shown in FIGS. **4**A and **4**B. As noted above, the conductor arrays **13** and **14** are dielectrically or insulatively isolated from the gaseous discharge medium **9** by thin dielectric coatings on the conductor array which form charge storage surfaces Sx and Sy for charges **25** and **26** produced on discharge. Basically, two forms of charges are produced namely, ions **25** and electrons **26.** The time frame for the sweeping of charge particles from the gas volumn between the surfaces Sx and Sy is dependent upon the applied potential, spacing between the gap surfaces, gas pressure, composition etc., has been set forth above. It will be noted in this connection, and with reference to FIG. **3,** the waveform shown is the waveform of the sustainer voltage as applied across to gas from conductor arrays **13** and **14.** In FIG. **3**A, it is shown as a rectangular or square waveform and in FIG. **3**B the current flow to the panel corresponding to the discharges occurring during the applied sustainer voltage are shown. The steep rise of the sustainer voltage there is a capacitive charging current which is indicated by the numeral **30** in waveform **3**B. This capacitive charging current charges the panel capacitance. Immediately following the charging of the panel capacitance, there is a surge of current constituted by ionization of the gas. This surge current or discharge current **31** is the condition illustrated in FIG. **2** between conductor **31–1** and conductor **14–1.** In this case, the collection of electrons **25** opposite conductor **14–1** after a period of time constitutes an internal bias voltage and is sufficient to oppose the applied potential and hence terminate the discharge. This termination of the discharge is indicated by a termination or cessation of the flow of discharge current in FIG. **3**B.

On alternation of the sustainer potential, as indicated at **35** (and the ± signs) there is a small panel charging current **32** in the opposite direction. And, assuming that the sustainer voltage is maintained for a given period of time, at least the 10 microsecond interval mentioned above, there will be a subsequent discharge **33** whereby the electrons **25** will be collected upon the dielectric surfaces opposite conductor **13–1** and at the crossing point thereof with conductor **14–1** to reverse the charge conditions shown in FIG. **2.** This is illustrated in FIG. **2** between conductor **14–2** and conductor **13–1,** wherein ions **26** are tending to move towards the conductor **14–3** and the electrons **25** as collected upon the surface of dielectric storage member **15.** When the sustainer potential reverses again on the next period or interval, as is illustrated at **341** there will again be a small current **30**′ to charge capacitance of the panel and following that, and again assuming that the sustainer waveform exists or is present at the level illustrated for the time interval mentioned above, there will be another discharge current surge as indicated at **31**′ and the cycle repeats itself.

Referring now to FIG. **4,** an enlarged drawing of the applied sustainer voltage Vs as it appears across the gas is illustrated wherein the rise time or "front porch" is shown as dotted portions of the waveform; the current pulses **30, 32** to charge the capacitance of the panel has not been shown. The main current surge is labeled as the "electron discharge current" and the second time interval is labeled as ion discharge current. As indicated, the collection time required for roughly 90 percent of the ions **26** as well as 100 percent of the electrons **25** can be easily within a 10 microsecond interval so that if the sustainer voltage pulse width is controlled, the ion collection time may be controlled. In the following table there is compared the sustainer pulse width of 2 microseconds and 9 microseconds. The panel had 128 row conductors and 128 column conductors, the conductors being spaced at 33 ⅓ lines per inch with a discharge gap of about 4 mils and a dielectric coating between 1 to 2 mils thick with a pulsed square wave having a tsr of about 100 nanoseconds rise time and a τsp of about 27.5 microseconds. The number of discharge sites were on a 64 × 64 matrix or 4,096.

	τ sw=2μs			Sustain pulse width, light output, ft. 1	τ sw=9μs			Sustain width, light putput, ft. 1
	Vs.	Ipk., amps	Ip., ns		Vs.	Ipk., amps	Tpc., ns	
Last off	139				114			
1st off	148	0.30	360	5.5	121	0.55	600	3.4
1st on	164	0.78	270	10.8	144	1.4	350	8.6
Last on	171				147			

From the foregoing table It will be noted that the voltages of the panel for two different conditions goes up by roughly 20 volts and the current drops in half with a light output increase by approximately 50 percent as one goes from 9 microseconds to a 2 microsecond sustaining pulse width.

In FIG. **5**, a number of different types of sustainer voltage waveform which can be used in accordance with the invention are illustrated. In all cases, the write and erase functions as well as the collection of ions is controlled by controlling the widths of the sustaining voltage wave form. The preferred waveform or the most efficient one, is shown in FIG. 5A. In this waveform, a negative voltage swing is used to deaccelerate the ions and permit them to impact the wall at reduced velocity. However, it will be appreciated that this negative voltage swing is not necessary in order to achieve the improved results set forth hereinabove.

FIGS. **6** and **7** illustrate typical circuits which may be used in practicing the invention. Although only a four line system is shown in each case, it is obvious that it may be expanded to any size, binary or decimal on either axis (*x* or *y*) with sector at a time address capability or with random access capability.

The invention requires *x* and *y* sustainer generator sources which may be similar to those shown in Wojcik application Ser. No. 135,022 filed Apr. 19, 1971, now U.S. Pat. No. 3,742,294 issued June 26, 1973, but this invention is not limited to this type. The outputs of such sustainer sources should be matched in terms of logically controlled output pulse width uniformity. Control and modulation of pulse width can be accomplished in accordance with the circuits shown in FIGS. **6** and **7**.

Referring to FIGS. **6** and **7**, a portion of the vertical or columns sustain address circuitry (FIG. **6**) and the horizontal or row sustain address circuitry (FIG. **7**) are illustrated, respectively. It will be appreciated that various other arrangements can be used for supplying width modulated, square wave sustainer pulses to the individual row and column conductors. However, the embodiments illustrated in FIGS. **6** and **7** are preferred because this permits multiplexing of the sustainer generators. The diode selection matrix circuitry per se is disclosed in detail in Johnson application Ser. No. 60,402 filed Aug. 3, 1970 and entitled "Selection and Addressing Circuitry for Matrix Type Gas Display Panel". However, an important difference is incorporated in the present invention in that the sustainer voltage per se is used to sustain, erase and write as well as perform other operations with regard to manipulating the discharge sites of the panel. Specifically, in FIG. **6**, the numerals **50–1, 50–2, 50–3 . . . 50**–N indicate the connection points of this matrix to individual column conductors or panel lines. Thus, **50–1** would be connected to vertical or column conductor **14–1 . . .** etc. to supply pulse width modulated potentials to the column conductors and with respect to FIG. **7**, the horizontal or row conductors **13–1, 13–2** on the panel are served or supplied with pulse width modulated potential from the point in the matrix designated **60–1, 60–2 . . . 60**–N, respectively. Moreover, each such point **50** and **60** is, in effect, the nodal point of a matrix selection element, each nodal point including diodes **D1** and **D2** and a resistor the anode of diode **D1** and the cathode of diode **D2** are connected to the nodal point for pulsing in one polarity direction whereas, the opposite situation prevails in connection with the horizontal address circuitry shown in FIG. **7** namely, the diodes **D3** and **D4**, respectively, which occupy the same electrical position in the circuitry as do diodes **D1** and **D2** in the circuit of FIG. **6**, have their cathode and anode, respectively, connected to the nodal point serving the conductor line on the panel. It will be appreciated that this arrangement may be reversed and the polarity circuitry shown to supply the row conductors may be used to supply the column conductors and vice versa.

As shown, all of the resistors **R1, R2 . . .** in a row of the vertical or column sustain matrices, respectively, are connected through a switching transistors **TC1** to a source of supply potential VCC. This voltage VCC may be used with a small control voltage (ΔV) to increase the select write voltage margin, if necessary. The purpose of this added voltage is that in the event that a half-select write operation range is not sufficient for a good reliable panel electronic performance, the half-select margin may be increased by this modification. There are other methods by which the select voltage may be increased by the voltage ΔV. It should be noted that in all cases this need not actually be a DC voltage but may be a pulse voltage occurring only during the portion of the write cycle or any other portion of the cycle as may be required. Thus, this pulse voltage could be added into the system at the VCC source by means of either a transformer in series (at point TRA, for example) with the power supply line so as to induce a pulse at the proper time. By properly choosing the winding of the transformer the sustain power supply voltage could be utilized. As an alternate technique, one could use a floating power supply with associated transistor switching circuitry to provide either VCC or VCC modified as the output going to the point designated in FIG. **6**. As an alternative, capacitances can be made an integral part of the panel **10**, using the coatings **15** and **16** as dielectric for coupling such voltages to the conductor arrays.

In FIG. **6**, the multiplexing operates as follows: when LF1 is on then all of the outputs (**50–1, 50**–N) are then driven to the VCC voltage.

If transistor LE1 is on, then all the outputs associated with that vertical line are driven low (**50–1** and **50–3**) so that LE1 or LE2 cannot be on when LF1 is on. If LD1 and LD2 with LE1 and LE2 can be used to select one output to the VCC + ΔV level, and the rest low, which is a situation illustrated in FIG. **6** wherein LV1 is on, LB2 is off, LE1 is on, and LE2 is off, this causes V2 to go high with all other low. LF1 is not used in addressing but only in sustaining.

Referring now to FIG. **7** showing the row sustain address multiplex circuitry **20**, the multiplexing operation is as follows: when LC1 is on then all of the outputs (**60–1, 60–2 . . . 60**–N) are driven low or to ground potential. When LA1 or **2** is on then all of the outputs associated with the vertical line driven thereby are high (at the voltage VCC); that is, the lines **60–1** and **60–3** are on. LA1 and LA **2** cannot be on when LC1 is on. Moreover, lines LA1 and LA2 with LB1 and LB2 may be used to select one output to ground with all other outputs at the high voltage level of VCC. As shown in FIG. **7**, LB1 is on, LB2 is off, LA1 is on and LA2 is off so that this causes line **60–2** to be at ground potential with all other lines **60–1, 60–3,** and **60**–N to be at the high VCC voltage level. Moreover, LC1 and LA1 and LA2 may be used to sustain the panel in this configuration.

In order to more fully explain and illustrate various aspects of the invention, particularly regarding the erase operations, there is shown in FIG. **8** voltage waveforms for illustrating a single discharge site erase operation. In this illustration, the horizontal and vertical sustainer waveforms are illustrated in FIG. **8**A and **8**B respectively. The application of the horizontal select and horizontal non select voltage pulses are shown in lines **8**C and **8**D respectively and the vertical select and vertical non select voltage wave forms are shown in lines **8**E and **8**F respectively. Waveform **8**G shows the sustain voltage as seen by a single site. It will be noted that the normal sustain voltage preceding the erase operation or erase cycle occurs within the interval indicated and modifies only the pulse width of the sustainer voltage at the selected site. In the case illustrated, the normal sustainer pulse width is narrowed so that while there may be a small charging current to charge a panel capacitance, the sustainer voltage is removed, effectively, prior to the initiation of the discharge so that there is no discharge during the half cycle of sustainer. This removal of the sustainer thereby permits, during that time interval participation of some of the stored charge so that on the next half cycle, which is still in the same direction as the previous half cycle having had a normal discharge, there is still not another discharge because the charges are still bucking in effect the applied potential thereby providing additional time for dissipation of the stored charge. Hence, when the next pulse voltage appears, even though it will be the noraml sustaining voltage and of normal width, due to the dissipation of the stored charge as described, there will be subsequent discharge at that sight.

FIG. **9** illustrates a single write operation and waveforms. The method for providing 1) bulk write, 2) bulk erase and 3) electronic conditioning (as described in the aforementioned Baker et al. and Bitzer et al. patents) using the same constant voltage sustainer signal is shown in FIG. **10.** Notice that the erase pulse is slightly narrower than the normal sustain pulse width and that the write pulse width is wider than the normal sustain pulse width. The electronic conditioning pulse width is even wider than the normal write pulse width but less than 15 ms. Note also the required sequence with respect to conditioning, writing and erasing as to permissible places where it might occur with respect to the phase of the sustain waveform. It is not illustrated, but it is obvious that the inverted signals could just as easily be generated since there is control over the pulse duration for either the zero condition or the Vs sustainer amplitude level. The anticipated range of sustained pulse width which may be utilized in this technique is between 0.8 microseconds to 5 microseconds in duration.

From the foregoing it is apparent that by means of the present invention:

1. write/erase operations for the panel are accomplished by means of controlling the sustainer pulse width alone;

2. there is elimination of cost with respect to write/erase circuitry and the elimination of power supplies associated with same;

3. the number of lines going to the panel to be used to control the panel are significantly reduced and is in direction proportion to the number of sustainers for each plane, *x* or *y* (assuming that conductor selection matrice diodes and resistor are on the panel as in my patent application Ser. No. 62,015 filed Aug. 7, 1970);

4. the manner in which the actual address function may be manufactured into the panel by leaving holes in the dielectric in combining selected lines for proper connection to the various sustainers;

5. this write/erase technique uses a method of increasing panel life through circuits;

6. electronic "conditioning" may well be also incorporated into the same technique;

7. bulk erase operation; and

8. bulk write operation;

9. the particular waveforms contemplated herein applies narrow square pulses which cause a discharge to occur and after the electrons have flowed across the gap and established the wall charge, this potential is removed so that the ions which are slower moving particles due to their mass, do not have an electric field to impact them into the dielectric or wall surfaces S*x* and S*y*, respectively. As a result, the extent to which ions are driven into the glass wall at S*x* and S*y* sites which is considerably reduced by this waveform. This method is specially advantageous to square wave drive since the discharge current is approximately 10 times that of sine wave discharge.

The invention is not to be limited to the exact forms shown and described herein for many changes and modifications may be made, some of which are suggested herein, within the scope of the following claims.

What is claimed is:

1. A method of manipulating the discharge condition of a gas discharge information storage panel device having transversely oriented dielectrically insulated conductors on opposite sides of a thin gaseous discharge medium, which comprises applying a periodically alternating pulse potential across said gas by applying, in selectively timed relation, a first sequence of electrical pulses to the conductors oriented in a first direction and a second sequence of electrical pulses to conductors oriented in a second direction transverse relative to the direction of said conductors oriented in said first direction whereby the gaseous medium between said conductors has said periodically alternating pulse potential applied thereto, and constitutes a sustaining potential for discharges at any site in said panel device and modulating at least one electrical parameter of at least one pulse of a sequence as applied to the conductors oriented in one of said directions.

2. The invention defined in claim **1** wherein the electrical parameter that is modulated is the time duration width of said electrical pulse.

3. The invention defined in claim **2** wherein a second of the electrical parameters that is modulated is the amplitude of said electrical pulses.

4. The invention defined in claim **2** wherein the time duration of any of said electrical pulses is no greater than the time required for substantially all electrons produced on a discharge to collect on a surface of a dielectrically insulated conductor and an insignificant number of ions produced during said discharge are collected on an opposing surface of a dielectrically coated conductor.

5. The invention defined in claim **2** wherein the pulse width is widened so as to store information at a selected discharge site, said selected site being located at the cross over point of a selected pair of transverse conductors.

6. The invention defined in claim **2** wherein the pulse width is narrowed so as to remove stored information at a selected discharge site, said selected site being located at the cross over point of a selected pair of transverse conductors.

7. The invention defined in claim **1** wherein said pulse is deleted on at least a plurality of conductors of one array so as to bulk erase information stored on said panel.

8. The invention defined in claim **2** wherein said pulse width is narrowed on at least a plurality of conductors of one array so as to bulk erase information stored in said panel.

9. The invention defined in claim **2** wherein said pulse width is widened for a selected time interval on at least a plurality of conductors of one array so as to bulk write information on said panel.

10. A method of lengthening the life of a gas discharge storage device having insulated conductors supplying gas discharge condition initiating pulse potentials to the gas medium for effecting one or more discharges therein, comprising

terminating said pulse potentials prior to impaction of significant number of ions on the insulation on said conductors.

11. The method of claim **10** including the step of applying an ion repulsing potential to said conductors following termination of said discharge initiating pulse potentials to said conductors.

12. The method of conditioning for reliable discharge manipulation all discharge sites of a multiple discharge site gas discharge panel wherein the sites are defined and located by transverse row-column conductor arrays, said conductor arrays being isolated from the gas by a charge storage layer of non conductive material, and a synchronized sequence of rectangular shaped pulses are applied to said row and said column conductors in the arrays, respectively, which comprises periodically lengthening the time interval of one of the pulses applied to all conductors in at least one of said arrays.

13. The invention defined in claim **12** wherein information is entered and removed on said panel by modulating the time interval of said rectangularly shaped pulses and wherein in said step of periodically lengthening the time interval is for a longer time interval than the time interval of said pulses for entering and removing information.

14. The invention defined in claim **2** wherein the pulse width is under about 10 microsecond time duration.

15. The invention defined in claim **14** wherein the pulse width is between about 0.8 microseconds and about 5 microseconds in time duration.

16. The invention defined in claim **10** wherein said pulse width is between about 0.8 microsecond and about 5 microsecond time duration.

17. The invention defined in claim **12** wherein said pulse width is between about 0.8 microseconds and about 15 microsecond time duration.

18. In a system for manipulating and sustaining discrete discharge sites of a gas discharge display panel wherein periodically alternating pulses are continually applied to all conductors in row-column conductor arrays of said panel, said conductors being insulated from the gas, improvement in the means for manipulating the discharge condition of discharge sites located by selected ones of said row and column conductors, respectively, comprising means for modulating the time duration of at least one of said periodically alternating pulses to thereby alter the charge stored at said selected site.

19. The invention defined in claim **18** wherein said pulse time duration is initially selected to be such that during a discharge interval, the electrons produced on discharge are stored and the pulse terminated prior to any significant storage of ion charges occur.

20. The invention defined in claim **18** wherein said means for modulating includes at least one conductor multiplex selection circuit for selecting individual ones of said conductors respectively and modulating the time duration of pulse voltages applied thereto.

21. The invention defined in claim **20** wherein said multiplex selection circuit includes means for adding a voltage increase to the pulse whose time duration is modulated.

22. The invention defined in claim **20** wherein there is at least one multiplex selection circuit for the row conductors and at least one for the column conductors.

23. The invention defined in claim **22** wherein each selection circuit includes means for adding a voltage increase to the pulse whose time duration is modulated to aid in writing on said panel.

24. The invention defined in claim **19** wherein said time duration is less than 10 microseconds.

25. The invention defined in claim **24** wherein said time duration is between about 0.8 microseconds and about 8 microseconds.

26. The invention defined in claim **18** wherein said means for modulating the time duration includes circuit means for periodically simultaneously lengthening the time duration of a pulse applied to all conductors of an array beyond that necessary to initiate or terminate discharges, to thereby condition sites located thereby for uniform operation.

27. The invention defined in claim **18** including means for simultaneously shortening the time duration of pulses applied to all conductors of an array below the time duration necessary to effect a discharge at any site.

28. The invention defined in claim **18** including means for simultaneously lengthening the time duration of pulses applied to all conductors of an array to at least the time duration necessary to effect discharges at all sites located by said all conductors.

* * * * *