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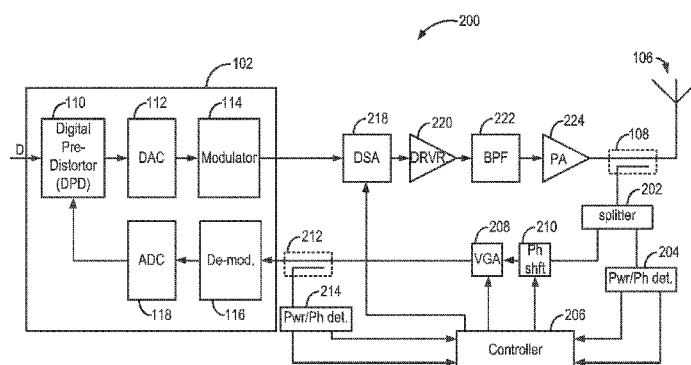


Figure 2

(57) Abstract: This disclosure provides systems, methods, and apparatus for a radio frequency transceiver. The transceiver includes a modulator for modulating a data signal onto one or more carrier signals to generate a modulated signal and a power amplifier for amplifying the modulated signal. The transceiver also includes a data pre-distorter (DPD) for pre-distorting the data signal using a look-up table that represents a non-linear transfer function that is an inverse of the non-linear transfer function of the power amplifier. The DPD selects one or more look-up tables based on a feedback signal corresponding to a power level and/or a phase of the output of the power amplifier. The transceiver also includes a controller for comparing the output of the power amplifier to a desired output level and upon sensing changes, altering the amplitude and phase of the feedback signal to substantially constant values.

DIGITAL PRE-DISTORTION LINEARIZATION FOR MOBILE COMMUNICATION

RELATED APPLICATIONS

[0001] This application claims priority to U.S. Patent Application No. 14/993,382, titled “DIGITAL PRE-DISTORTION LINEARIZATION FOR MOBILE COMMUNICATION,” and filed January 12, 2016, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] This disclosure relates to the field of wireless communication, and in particular to radio frequency (RF) transmitters.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] RF transmission systems typically include a data modulator to modulate data onto one or more carrier signals to generate a modulated signal. The RF transmission systems also can include one or more power amplifiers that amplify the modulated signal for transmission over a transmission medium. In some implementations, the power amplifiers can exhibit non-linear characteristics that can distort the amplitude and phase of the modulated signals.

SUMMARY

[0004] According to one aspect, the subject matter described in this disclosure relates to a transmitter including a modulator, a power amplifier, a digital pre-distorter (DPD) and a controller. The modulator includes at least one input to receive a data signal and an output, the modulator configured to modulate one or more carrier signals with the data signal to generate a modulated signal at its output. The power amplifier is coupled to the output of the modulator, and is configured to amplifying the modulated signal to generate a power amplifier output signal. The DPD is coupled to the at least one input of the modulator, and is configured to pre-distort the data signal prior to inputting the data signal to the modulator, the pre-distortion based in part on a feedback signal representing an amplitude and a phase of the power amplifier output signal. The controller coupled to the power amplifier and is configured to sense changes in a power level or phase of the power amplifier output signal, and alter the feedback signal such that an amplitude and a phase of the feedback signal are maintained at substantially constant values.

[0005] According to another aspect, the subject matter described in this disclosure relates to a method including modulating a data signal over one or more carrier signals using a modulator to generate a modulated signal. The method further includes amplifying the modulated signal using a power amplifier to generate a power amplifier output signal. The method also includes pre-distorting the data signal prior to modulating, the pre-distorting based in part on a feedback signal representing an amplitude and phase of the power amplifier output signal. The method further includes sensing changes in a power level or a phase of the power amplifier output signal. The method additionally includes altering, in response to sensing changes, the feedback signal such that an amplitude and a phase of the feedback signal are maintained at substantially constant values.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 shows an example wireless transmission system.

[0007] Figure 2 shows another example wireless transmission system.

[0008] Figure 3 shows an example flow diagram of a process.

[0009] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0010] The various concepts introduced above and discussed in greater detail below may be implemented in any of numerous ways, as the described concepts are not limited to any particular manner of implementation. Examples of specific implementations and applications are provided primarily for illustrative purposes.

[0011] Figure 1 shows an example wireless transmission system 100. The transmission system 100 includes a transceiver 102 coupled to a power amplifier 104, the output of which is coupled to an antenna 106. A coupler 108 is coupled to the output of the power amplifier 104 for sensing the output of the power amplifier and feeding the sensed signal back to the transceiver 102. In some implementations, for example, directional couplers or resistive couplers can be used to implement the coupler 108. The transceiver 102 includes a digital pre-distortion (DPD) module 110, a digital-to-analog converter (DAC) 112, a modulator 114, a demodulator 116, and an analog-to-digital converter (ADC) 118. The DPD module 110 can receive digital data, which is pre-distorted to compensate for the non-linearity of the power amplifier 104. The pre-distorted data is converted into an analog data signal by the DAC 112. The modulator 114 modulates a carrier signal (not shown) with the analog signal and

outputs the modulated signal to the input of the power amplifier 104. The demodulator 116 can demodulate the feedback signal from the output of the power amplifier 104 to generate a demodulated feedback signal. The ADC 118 digitizes the demodulated feedback signal and provides the digital feedback signal to the DPD module 110. The digital feedback signal can represent the power level of the output of the power amplifier 104, in two components of amplitude and phase.

[0012] In some implementations, the modulator 114 can include an amplitude modulator, a phase modulator, or a frequency modulator. In some implementations, the modulator 114 can include a quadrature modulator that modulates two separate data signals onto two separate quadrature carrier signals and combines the modulated carrier signals to generate the modulated signal. For example, in some implementations, quadrature-amplitude-modulators (QAM) such as 16-QAM, 64-QAM, 128-QAM, 256-QAM, or other higher-order QAM can be utilized to implement the modulator 114. In some such implementations, the input data received at the input of the DPD module 110 can include two separate streams of digital data, including I (in phase) and Q (quadrature phase), each of which can be pre-distorted prior to being converted into separate analog signals by the DAC 112 and provided to the modulator 114.

[0013] The power amplifier 104 can provide amplification to the modulated signal output by the modulator 114. The modulated signal output by the modulator 114 could be low or high power RF signal,. The power amplifier 104 amplifies the modulated signal to the desired power level for driving the antenna 106. In some implementations, power transistors such BJTs, MOSFETs, heterojunction-bipolar-transistors (HBT), etc., fabricated in silicon, germanium, gallium Nitride, indium-gallium-arsenide, indium-gallium-phosphide, or gallium-arsenide, technologies can be utilized to implement the power amplifier 104. In some implementations, the power amplifier 104 can be implemented using multi-stage amplifiers, where each stage can provide a portion of the overall gain of the power amplifier. In some implementations, the power amplifier 104 can provide high gain in the range of about 20 dB to about 55 dB. In some implementations, the power amplifier 104 can provide high gain over a frequency range of +/-10-20% of the desired frequency.

[0014] In some implementations, the power amplifier 104 may exhibit non-linear characteristics. For example, the power amplifier 104 may have a non-linear amplitude and/or phase transfer function. These non-linear characteristics of the power amplifier 104 may cause the amplitude and/or the phase of the output of the power amplifier 104 to be a non-linear function of the amplitude and/or phase of the input signal of the power amplifier

104. The non-linear relationship between the input and the output amplitude and/or phase in a power amplifier can generate amplitude distortion and phase distortion in the modulated signals amplified by the power amplifier. In some implementations, the amplitude and/or phase distortions may cause in-band data errors or inter-band interference. In some implementations, the amplitude and/or phase distortions also can result in high adjacent channel leakage ratio (ACLR) and higher orders of harmonics.

[0015] One approach to mitigate the effects of power amplifier non-linearity on the amplitude and phase of the modulated signals is to pre-distort the digital input signals using a non-linear transfer function that is an inverse of the non-linear characteristics of the power amplifier 104. For example, the DPD module 110 can pre-distort the digital data D prior to the data being converted to an analog signal by the DAC 112 by using a non-linear transfer function that is an inverse of the non-linear transfer function of the power amplifier 104. As a result, when the pre-distorted modulated signal is amplified by the power amplifier 104, the distortion imparted by the power amplifier 104 cancels out the pre-distortion imparted by the DPD module 110, resulting in a linearly amplified modulated signal at the output of the power amplifier 104.

[0016] In some implementations, the DPD module 110 can perform the pre-distortion using a look-up table, which includes pre-distortion values corresponding to actual values of the digital data signal D. The pre-distortion values in the look-up table can be calculated based on the inverse of the non-linear function of the power amplifier 104. In some other implementations, the DPD module 110 can implement a transformation function that represents the inverse non-linear function of the power amplifier, and can determine the pre-distortion values by transforming the received values of the digital data D using the transformation function. In some other implementations, the DPD module 110 can employ a combination of look-up tables and transformation functions to determine the pre-distorted values of the digital data signal. The look-up tables and the transformation function can be stored in memory (not shown) at the transceiver 102.

[0017] In some implementations, the DPD module 110 can adaptively determine the pre-distorted values of the digital data signal D based on the magnitude and/or phase of the output of the power amplifier 104. In some implementations, the non-linear characteristics of the power amplifier 104 can be a function of the output power of the power amplifier 104. That is, the non-linear transfer function representing the power amplifier 104 at one output power level or phase can be different from the non-linear transfer function representing the power amplifier 104 at a different output power level or phase. The output power level or phase of

the power amplifier 104, while ideally constant, can change in practice due changes in factors such as the gain of one of more transistors, temperature, or transistor parameters over time.

In adaptive implementations of the DPD module 110, the DPD module 110 can sense the output power amplitude and phase of the amplifier, and select the inverse non-linear transfer function or look-up table corresponding to the sensed output power amplitude and phase value to pre-distort the digital data signal. In some implementations, the number of look-up tables needed to implement an adaptive DPD module 110 can be quite large due to the large number of possible combinations of measured values of the power level and phase. In some such implementations, the large number of look-up tables not only occupy a large amount of memory, but also require large amounts of processing, thereby putting additional burden on the memory and processor of the transceiver 102. The following discussion in relation to Figures 2 and 3 relates to a transmission system that mitigates the need for a large number of look up tables, while still providing an effective adaptive DPD module 110.

[0018] Figure 2 shows another example wireless transmission system 200. The wireless transmission system 200 is similar to the transmission system 100 shown in Figure 1 in that, like the transmission system 100, shown in Figure 1, the transmission system 200 in Figure 2 also includes a transceiver 102, and a coupler 108. However unlike the transmission system 100 shown in Figure 1, where the output of the coupler was directly fed back to the demodulator 116, the transmission system 200 shown in Figure 2 includes additional processing modules that process the feedback signal prior to it being received by the demodulator 116. In particular, the transmission system 200 includes a splitter 202, a first power/phase detector 204, a controller 206, a voltage gain amplifier (VGA) 208, a phase shifter 210, a second coupler 212, and a second power/phase detector 214. The transmission system 200 also can include, a digital step attenuator (DSA) 218, a driver 220, and a band-pass filter 222 for processing the modulated signal output by the modulator 114 prior to it being fed to a power amplifier 224. The power amplifier 224 can be a multi-stage amplifier, where each stage can provide a portion of the overall gain of the power amplifier. In some other implementations, the power amplifier 224 can be one stage of an multi-stage power amplifier, where a preceding amplifier, such as the driver 220, can provide a portion of the overall gain. In some implementations, where higher output power, for example, above 30 dBm (1W), is needed, the power amplifier 224 may not be able to provide the gain required to output the desired output power. In some such implementations, the driver 220 can provide a portion of the required gain. The driver 220 also provides the portion of the gain linearly, and outputs sufficient current to drive the power amplifier 224. For example, the

driver 220 can provide 25 to 35 dB of gain for a power output of about 30 dBm (1 W). The band-pass filter 222 can be utilized for suppressing any out of band spurious frequency components or harmonics, and can have a very low insertion loss. [0019] As mentioned above in relation to Figure 1, the coupler 108 senses the output signal at the output of the power amplifier 104. The sensed output signal is split into two identical signals by the splitter 202. In some implementations, resistors, transformers, or a combination thereof can be used to implement the splitter 202. In some implementations, a Wilkinson divider, or directional coupler also can be utilized for implementing the splitter 202. The first of the two identical sensed signals is fed to a first power/phase detector 204 while the second of the two identical sensed signals is fed to the phase shifter 210 and the VGA 208. The first power/phase detector 204 measures the root-mean-square (RMS) power and the phase of the sensed signal. In some implementations, the power detector portion of the first power/phase detector 204 can be implemented using a full-wave rectifier, followed by a log-antilog circuit and an integrator circuit. In some implementations, a ring mixer can be utilized for implementing the phase detector portion of the first power/phase detector 204. The first power/phase detector 204 can output two analog measurement signals, one representing the measured RMS power and the other representing the measured phase of the output of the power amplifier 104.

[0020] The controller 206 can receive the two analog measurement signals output by the first power/phase detector 204. In some implementations, the controller 206 can be implemented using a microcontroller, a microprocessor, a field-programmable-gate logic (FPGA), or digital signal processor (DSP). In some implementations, the controller can include ADCs for converting analog signals to digital signals, while in some other implementations, the ADCs can be outside of the controller 206. In some implementations, the controller 206 also can include a memory for storing output power values, and programs for execution by the execution logic of the controller 206. The RMS and phase measurement signals from the first power/phase detector 204 can be converted to digital signals by the ADCs. Based on the received phase measurement values from the first power/phase detector 204 and the stored values for the desired output power level and phase of the power amplifier, the controller 206 can perform at least two functions. First, the controller 206 can adjust the attenuation provided by DSA 218 so that the output of the power amplifier 224 is substantially equal to the desired power level. Second, the controller 206 can adjust the VGA 208 and the phase shifter 210 such that the amplitude and phase of the feedback signal sent to the DPD module 110 is substantially constant.

[0021] By maintaining the feedback signal, which includes the sensed values of the power level and the phase of the output of the power amplifier 224, at substantially constant amplitude and phase, the DPD module 110 needs to store look-up tables for a relatively smaller number of combinations of power level and phase for pre-distorting the digital data signal. In some implementations, the DPD module 110 may require only one look-up table corresponding to the substantially constant values of sensed power level and phase of the output of the power amplifier 104. This reduction in the number of look-up tables needed to pre-distort the digital data signal D also reduces the memory and processing power requirements for the transceiver 102.

[0022] The controller 206 also adjusts the attenuation level or gain of the DSA 218 such that the output power level of the power amplifier is substantially equal to the desired output level. For a given desired output power level, the controller 206 can compare the instantaneous RMS power level values and phase values provided by the first power/phase detector 204 with the stored power level and phase values. If there is a difference between the desired and the instantaneous values, the controller 206 can adjust the attenuation level of the DSA such that the output power level returns to the desired output power level. For example, if the power level at the output of the power amplifier 224 decreases, the controller 206 can reduce the attenuation provided by the DSA 218. As a result, the amplitude of the modulated signal at the input of the power amplifier would increase, thereby increasing the output power level of the power amplifier 224. Similarly, if the power level of the output of the power amplifier 104 increases beyond the desired output power level, the controller 206 can increase the attenuation level of the DSA 218, thereby reducing the amplitude of the modulated signal at the input of the power amplifier 224. As a result, the power level of the output of the power amplifier 224 is reduced so that it is substantially equal to the desired power level. In some implementations, the power amplifier 224 can have adjustable gain. In some such implementations, the controller 206 can control the gain of the power amplifier 224 instead of, or in addition to, adjusting the attenuation level of the DSA 218.

[0023] In some implementations, it is desirable to operate the power amplifier at high power added efficiency (PAE). PAE is defined as the percentage of power added to a signal received at an input of the power amplifier relative to the power delivered to the power amplifier via the power supply. In some implementations, a high PAE is achieved when the power amplifier is operated at peak power output. In some implementations, the value of the output power level stored in the memory can correspond to the output of the power amplifier 224 at peak power output, so that the power amplifier 224 can operate at the highest PAE.

[0024] As mentioned above, the controller 206 can adjust the VGA 208 and the phase shifter 210 such that the amplitude and phase of the feedback signal sent to the DPD module 110 is substantially constant. In some implementations, the transmission system 200 can include additional circuitry to monitor and adjust the feedback signal. For example, the communication system can utilize the second coupler 212 to sense the feedback signal. The second coupler 212 can be similar to the coupler 108 discussed above. The output of the second coupler 212 is provided to the second power/phase detector 214, which detects the power amplitude and phase of the feedback signal. The detected power amplitude and phase of the feedback signal are provided to the controller 206, which can compare the detected amplitude and phase with the stored desired amplitude and phase of the feedback signal. If the detected values are different from the desired values, the controller can further adjust the VGA 208 and the phase shifter 210 such that the amplitude and phase of the feedback signal is substantially constant.

[0025] Figure 3 shows an example flow diagram of a process 300. In particular, the process 300 can be executed by the controller 206 shown in Figure 2. The process 300 includes sensing the power level and phase at the output of a power amplifier of a transmitter (stage 302). The process 300 further includes comparing the sensed power level and phase with stored values of power level and phase (stage 304). The process 300 also includes maintaining substantially constant the values of the sensed power level and phase fed back to a digital pre-distortion module (stage 306). The process 300 further includes adjusting the gain of an intermediate amplifier coupled to the input of the power amplifier such that the output power level of the power amplifier is substantially equal to the stored value of power level (stage 308).

[0026] The process 300 includes sensing the power level and phase at the output of a power amplifier of a transmitter (stage 302). As discussed above in relation to Figure 2, the first power/phase detector 204 can measure the RMS power level and the phase of the output of the power amplifier 104. The first power/phase detector outputs the measured RMS power level and the phase are provided to the controller 206. The process 300 further includes comparing the sensed power level and phase with stored values of power level and phase (stage 304). As discussed above, the controller 206 can access desired values of power level and phase stored in memory and compare the desired values of the power level and phase to the measured values of the power level and phase. In some implementations, the controller 206 can include ADCs to convert the analog values of the power level and phase output by

the first power/phase detector 204 into digital values before comparing with the stored values in memory.

[0027] The process also includes maintaining substantially constant, the values of the sensed power level and phase fed back to a digital pre-distortion module (stage 306). As discussed above, the sensed output of the power amplifier 224 shown in Figure 2 is fed back to the demodulator 116 via a VGA 208 and a phase shifter 210. The gain of the VGA 208 and the phase shift generated by the phase shifter 210 can be controlled by the controller 206. The controller 206, based on the comparison between the instantaneous power level and phase and the stored values of the power level and phase can adjust the gain of the VGA 208 and the phase shift of the phase shifter 210 such that the sensed output of the VGA 208 and the phase shifter has a substantially constant amplitude and phase corresponding to the desired power output level. By maintaining the amplitude and phase of the feedback signal to be substantially constant, the number of look-up tables needed by the DPD module 110 to pre-distort the digital data signal is reduced. As a result, the memory and processing burden on the transceiver for carrying out pre-distortion is advantageously reduced.

[0028] The process 300 further includes adjusting the gain of an intermediate amplifier coupled to the input of the power amplifier such that the output power level of the power amplifier is substantially equal to the stored value of power level (stage 308). As discussed above, if the output power level of the power amplifier 224 changes, the controller 206 can adjust the gain or attenuation of the DSA 218, which amplifies/attenuates the modulated signal received from the modulator. By adjusting the gain of the DSA 218, the amplitude of the modulated signal at the input of the power amplifier 224 changes, thereby changing the power level at the output of the power amplifier 224. As a result, the power amplifier 224 can operate at a desired power level. In some implementations, the stored value of the desired power level can correspond to the output power level of the power amplifier operating at peak power output. As a result, the controller 206 can maintain the operation of the power amplifier 224 at peak power output where it can achieve the highest PAE.

[0029] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein.

CLAIMS

What is claimed is:

1. A transmitter comprising:
 - a modulator having at least one input to receive a data signal and an output, the modulator configured to modulate one or more carrier signals with the data signal to generate a modulated signal at its output;
 - a power amplifier coupled to the output of the modulator, the power amplifier configured to amplify the modulated signal to generate a power amplifier output signal;
 - a digital pre-distorter (DPD) coupled to the at least one input of the modulator, the DPD configured to pre-distort the data signal prior to inputting the data signal to the modulator, the pre-distortion based in part on a feedback signal representing an amplitude and a phase of the power amplifier output signal; and
 - a controller coupled to the power amplifier configured to sense changes in a power level or phase of the power amplifier output signal, and alter the feedback signal such that an amplitude and a phase of the feedback signal are maintained at substantially constant values.
2. The transmitter of claim 1, further comprising:
 - a first variable gain amplifier positioned between the modulator and the power amplifier, the first variable gain amplifier configured to alter an amplitude of the modulated signal prior to feeding the modulated signal to the input of the power amplifier based on a control signal from the controller;
 - wherein the controller is configured to control a gain of the first variable gain amplifier such that a power level of the power amplifier output signal is substantially equal to a power level value stored in memory.
3. The transmitter of claim 2, wherein the power level value stored in memory corresponds to a peak power level of the power amplifier.

4. The transmitter of claim 2, wherein the first variable gain amplifier is a digital step attenuator, where the gain of the digital step attenuator is controlled step wise based on a digital control signal received from the controller.
5. The transmitter of claim 1, further comprising:
 - a second variable gain amplifier configured to change a power level of the feedback signal based on a first control signal received from the controller;
 - and
 - a phase shifter configured to shift the phase of the feedback signal based on a second control signal received from the controller.
6. The transmitter of claim 1, further comprising:
 - a power detector configured to measure a power level of the modulated signal output by the modulator and provide the measured power level to the controller; and
 - a first variable gain amplifier positioned between the modulator and the power amplifier and configured to alter, based on a control signal from the controller, an amplitude of the modulated signal prior to feeding the modulated signal to the input of the power amplifier,wherein the controller is further configured to control the first variable gain amplifier based on a comparison between a gain value stored in memory and a ratio of the measured power level of the modulated signal and the power level of the power amplifier output signal such that a combined gain of the first variable gain amplifier and the power amplifier is substantially equal to the gain value stored in memory.
7. The transmitter of claim 6, wherein the gain value stored in memory is a predetermined gain value.
8. The transmitter of claim 1, wherein the DPD is configured to pre-distort the data signal prior to inputting the data signal to the modulator based in part on an inverse of a non-linear transfer function of the power amplifier.

9. A method comprising:

modulating a data signal over one or more carrier signals using a modulator to generate a modulated signal;
amplifying the modulated signal using a power amplifier to generate a power amplifier output signal;
pre-distorting the data signal prior to modulating, the pre-distorting based in part on a feedback signal representing an amplitude and a phase of the power amplifier output signal;
sensing changes in a power level or a phase of the power amplifier output signal;
and
altering, in response to sensing changes, the feedback signal such that an amplitude and a phase of the feedback signal are maintained at substantially constant values.

10. The method of claim 9, further comprising:

comparing, in response to sensing changes, the power level of the power amplifier output signal with a desired power level stored in memory; and
altering, in response to the comparing, a gain of a first variable power amplifier positioned between the modulator and the power amplifier such that the sensed power level of the power amplifier output signal is substantially equal to the desired power level.

11. The method of claim 9, further comprising:

measuring a power level of the modulated signal at the output of the modulator;
determining a ratio of the measured power level of the modulated signal and the power level of the power amplifier output signal;
comparing the ratio to a gain value stored in memory; and
altering, in response to the comparing, a gain of a first variable power amplifier positioned between the modulator and the power amplifier such that a combined gain of the first variable gain amplifier and the power amplifier is substantially equal to the gain value stored in memory.

12. The method of claim 11, wherein the gain value stored in memory is a predetermined gain value.
13. The method of claim 9, wherein pre-distorting the data signal includes pre-distorting based additionally on an inverse of a non-linear transfer function of the power amplifier.

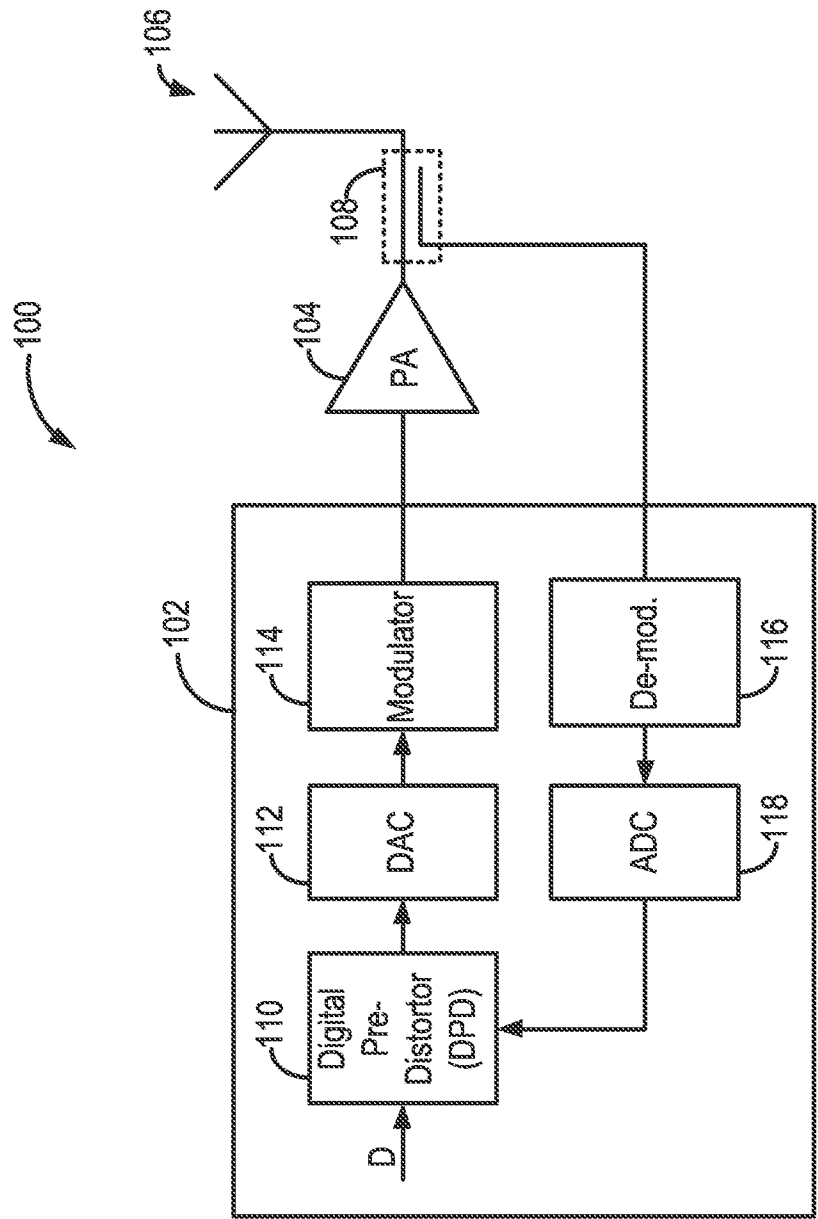


Figure 1

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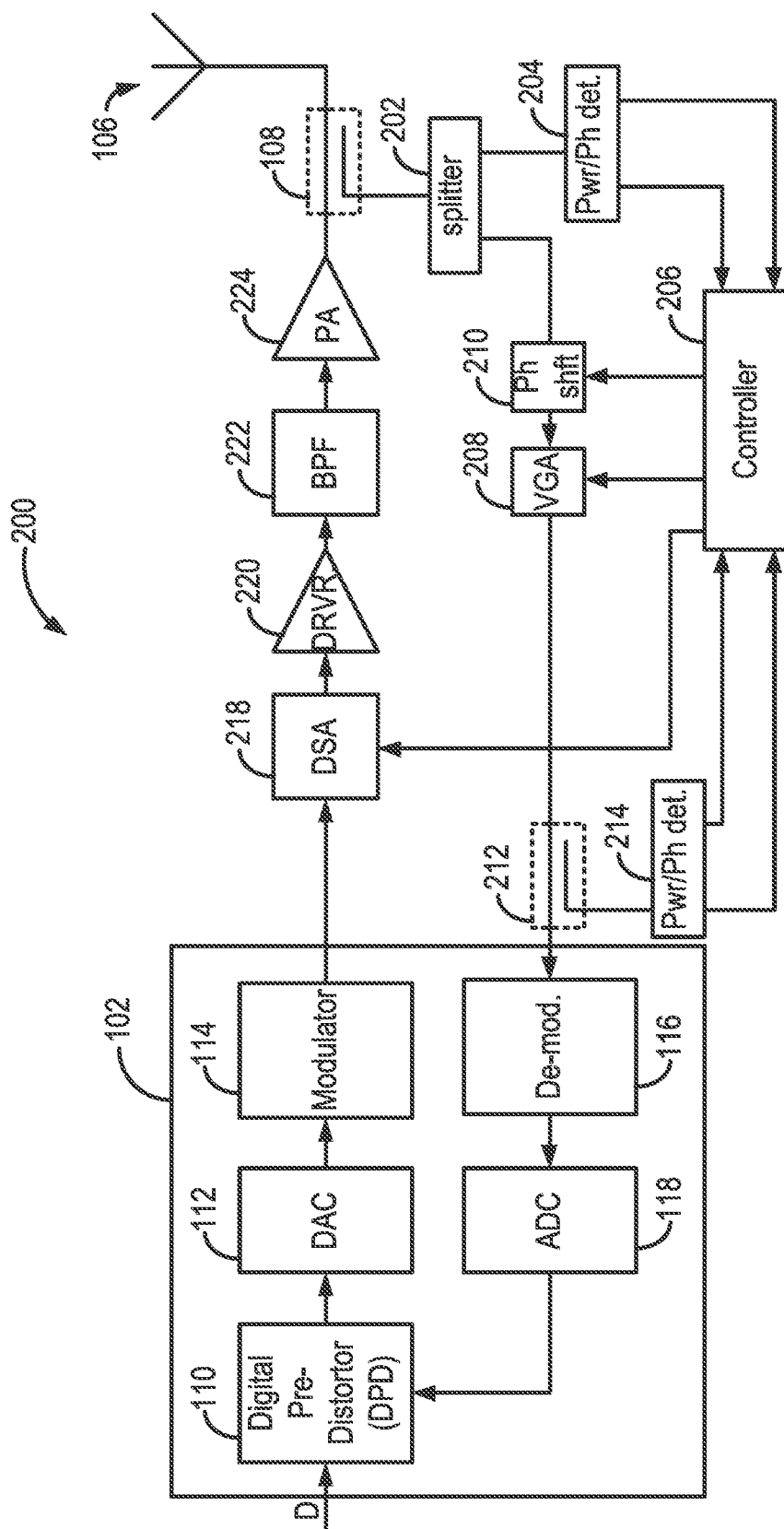


Figure 2

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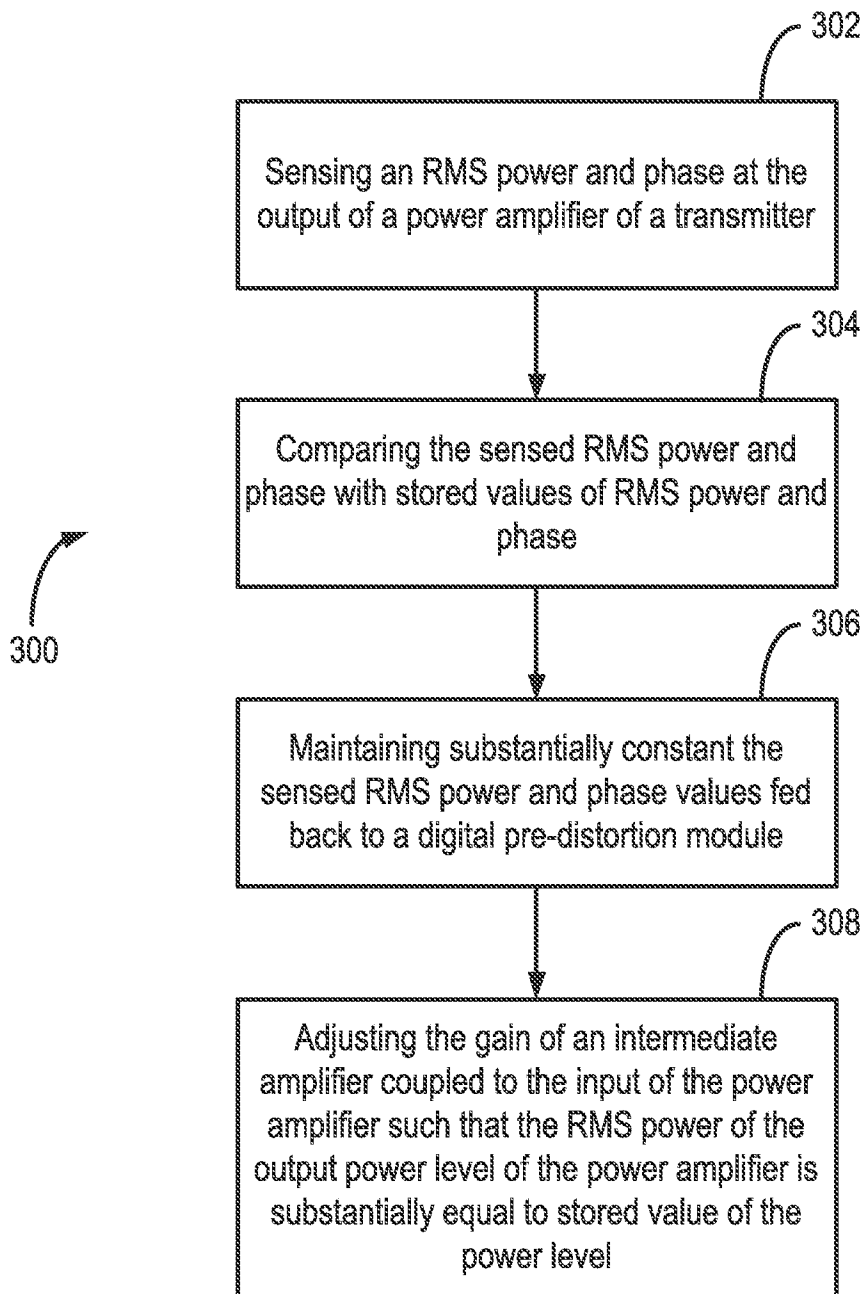


Figure 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/068007

A. CLASSIFICATION OF SUBJECT MATTER INV. H03F1/32 H03F3/19 H03F3/24 H03F1/30 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H03F		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/148874 A1 (THURINGER DANIEL JOSEPH [US] ET AL) 17 June 2010 (2010-06-17) paragraphs [0002], [0006], [0011], [0024], [0072] - [0077]; figure 4 -----	1-13
X	US 2015/207476 A1 (KOHAMA TATSUO [JP] ET AL) 23 July 2015 (2015-07-23) paragraphs [0012], [0014], [0020] - [0108]; figure 1 -----	1-13
A	US 2005/001675 A1 (SAED ARYAN [CA]) 6 January 2005 (2005-01-06) paragraphs [0167] - [0172]; figure 8 -----	1-13
<input style="width: 20px; height: 20px; margin-right: 5px;" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" style="width: 20px; height: 20px; margin-right: 5px;" type="checkbox"/> See patent family annex.		
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