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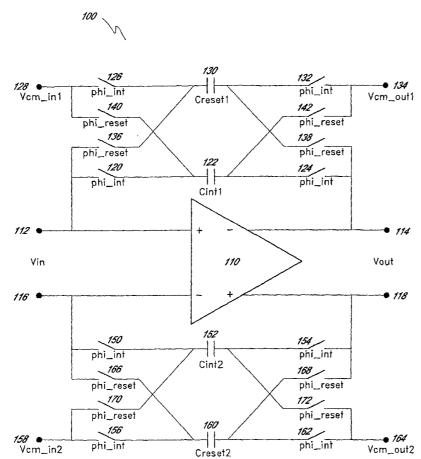
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(54) Title: INTEGRATOR RESET MECHANISM



An integrator with (57) Abstract: a reset mechanism comprises an integration capacitor and a replacement integration capacitor, wherein the integration capacitor is replaced with the replacement integration capacitor during a reset operation. A method of resetting an integrator comprises temporarily removing an integration capacitor and replacing the integration capacitor with a reset capacitor during a reset operation of the integrator. The method may further comprise temporarily removing the integration capacitor and replacing it with a reset capacitor multiple times during a single reset operation of the integrator.

WO 2005/011122 A3



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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols) IPC $7 \quad H03M$

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, COMPENDEX

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Χ	US 6 570 519 B1 (YANG YU QING) 27 May 2003 (2003-05-27)	2,4,6-9, 12
Υ	figures 2,4A	1,11,13
Υ	US 6 169 427 B1 (BRANDT BRIAN PAUL) 2 January 2001 (2001-01-02) figure 4	1,7-9
Υ	US 6 037 836 A (YOSHIZAWA ET AL) 14 March 2000 (2000-03-14) figures 1,3	7–9
Υ	US 6 194 946 B1 (FOWERS PAUL) 27 February 2001 (2001-02-27) figure 1	1,7-9

Y Further documents are listed in the continuation of box C.	Patent family members are listed in annex.
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Date of the actual completion of the international search 11 February 2005	Date of mailing of the international search report 22/02/2005
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Authorized officer Müller, U

Internal Application No PCT/US2004/021524

ation) DOCUMENTS CONSIDERED TO BE RELEVANT	
	Relevant to claim No.
US 6 061 009 A (KRONE ET AL) 9 May 2000 (2000-05-09) figure 5	7
SCHREIER R ET AL: "Multibit bandpass delta-sigma modulators using N-path structures" PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. SAN DIEGO, MAY 10 - 13, 1992, PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCAS), NEW YORK, IEEE, US, vol. Vol. 4 CONF. 25, 3 May 1992 (1992-05-03), pages 593-596, XP010061266 ISBN: 0-7803-0593-0 figure 3	1-13
US 5 796 848 A (MARTIN ET AL) 18 August 1998 (1998-08-18) figures 2,3	11,13
US 6 285 769 B1 (EDELSON JONATHAN SIDNEY ET AL) 4 September 2001 (2001-09-04) figure 2	10-13
US 5 973 536 A (MAEJIMA ET AL) 26 October 1999 (1999-10-26) figure 4	3,5
CHAO K C-H ET AL: "A HIGHER ORDER TOPOLOGY FOR INTERPOLATIVE MODULATORS FOR OVERSAMPLING A/D CONVERTERS" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE INC. NEW YORK, US, vol. 37, no. 3, 1 March 1990 (1990-03-01), pages 309-318, XP000128630 figure 1	1-13
US 6 249 237 B1 (PRATER JAMES S) 19 June 2001 (2001-06-19) figure 2	10-13
LI YU ET AL: "Mismatch cancellation for double-sampling sigma-delta modulators" CIRCUITS AND SYSTEMS, 1998. ISCAS '98. PROCEEDINGS OF THE 1998 IEEE INTERNATIONAL SYMPOSIUM ON MONTEREY, CA, USA 31 MAY-3 JUNE 1998, NEW YORK, NY, USA, IEEE, US, vol. 1, 31 May 1998 (1998-05-31), pages 356-359, XP010289627 ISBN: 0-7803-4455-3 figure 1	1–13
	US 6 061 009 A (KRONE ET AL) 9 May 2000 (2000-05-09) figure 5 SCHREIER R ET AL: "Multibit bandpass delta-sigma modulators using N-path structures" PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. SAN DIEGO, MAY 10 - 13, 1992, PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCAS), NEW YORK, IEEE, US, vol. VOL. 4 CONF. 25, 3 May 1992 (1992-05-03), pages 593-596, XP010061266 ISBN: 0-7803-0593-0 figure 3 US 5 796 848 A (MARTIN ET AL) 18 August 1998 (1998-08-18) figures 2,3 US 6 285 769 B1 (EDELSON JONATHAN SIDNEY ET AL) 4 September 2001 (2001-09-04) figure 2 US 5 973 536 A (MAEJIMA ET AL) 26 October 1999 (1999-10-26) figure 4 CHAO K C-H ET AL: "A HIGHER ORDER TOPOLOGY FOR INTERPOLATIVE MODULATORS FOR OVERSAMPLING A/D CONVERTERS" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE INC. NEW YORK, US, vol. 37, no. 3, 1 March 1990 (1990-03-01), pages 309-318, XP000128630 figure 1 US 6 249 237 B1 (PRATER JAMES S) 19 June 2001 (2001-06-19) figure 2 LI YU ET AL: "Mismatch cancellation for double-sampling sigma-delta modulators" CIRCUITS AND SYSTEMS, 1998. ISCAS '98. PROCEEDINGS OF THE 1998 IEEE INTERNATIONAL SYMPOSIUM ON MONTEREY, CA, USA 31 MAY-3 JUNE 1998, NEW YORK, NY, USA, IEEE, US, vol. 1, 31 May 1998 (1998-05-31), pages 356-359, XP010289627 ISBN: 0-7803-4455-3 figure 1

Internal Application No
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	ation) DOCUMENTS CONSIDERED TO BE RELEVANT	Delevent to claim No.	
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	
Y	BERG S K ET AL: "AN 80-MSAMPLE/S VIDEO SWITCHED-CAPACITOR FILTER USING A PARALLEL BIQUADRATIC STRUCTURE" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 30, no. 8, 1 August 1995 (1995-08-01), pages 898-905, XP000524388 ISSN: 0018-9200 figure 9	1-13	

rmation on patent family members

Inte Conal Application No PCI/US2004/021524

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 6570519	B1	27-05-2003	NONE		
US 6169427	B1	02-01-2001	NONE		<u> </u>
US 6037836	Α	14-03-2000	JP JP TW	3079368 B2 11127047 A 402837 B	21-08-2000 11-05-1999 21-08-2000
US 6194946	B1	27-02-2001	EP JP JP WO	1076874 A1 3564066 B2 2002514019 T 9957671 A1	21-02-2001 08-09-2004 14-05-2002 11-11-1999
US 6061009	A	09-05-2000	NONE		
US 5796848	Α	18-08-1998	DE CH DE DK	19545760 C1 689343 A5 29521956 U1 139196 A	20-02-1997 26-02-1999 05-11-1998 08-06-1997
US 6285769	B1	04-09-2001	NONE		
US 5973536	Α	26-10-1999	JP JP	3216490 B2 9083301 A	09-10-2001 28-03-1997
US 6249237	B1	19-06-2 0 01	NONE		