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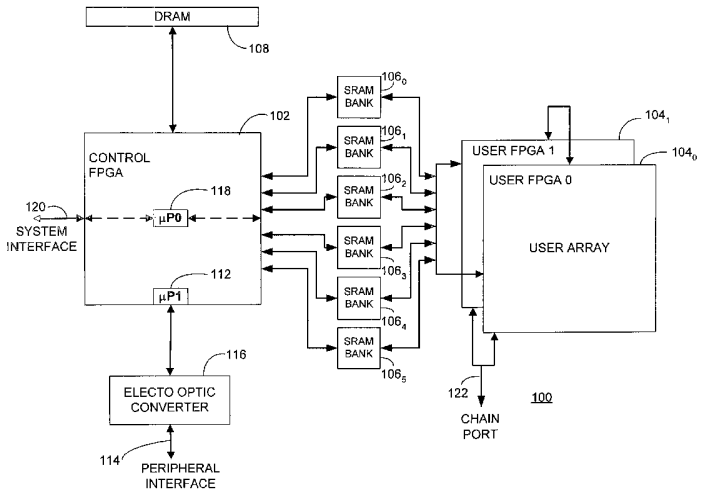
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(54) Title: ADAPTIVE PROCESSOR ARCHITECTURE INCORPORATING A FIELD PROGRAMMABLE GATE ARRAY CONTROL ELEMENT HAVING AT LEAST ONE EMBEDDED MICROPROCESSOR CORE



(57) Abstract: A multi-adaptive processor element (100) architecture incorporating a field programmable gate array ("FPGA") control element (102) having at least one embedded processor core and a pair of user FPGAs (104) forming a user array is disclosed in conjunction with high volume dynamic random access memory ("DRAM") (108) and dual-ported static random access memory ("SRAM") banks (106). In operation, the DRAM (108) is "read" using its fast sequential burst modes and the lower capacity SRAM banks (106) are then randomly loaded allowing the user FPGAs (104) to experience very high random access data rates from what appears to be a very large virtual SRAM. The reverse also happens when the user FPGAs are "writing" data to the SRAM banks. These overall control functions may be managed by an on-chip DMA engine that is implemented in the control FPGA.

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ADAPTIVE PROCESSOR ARCHITECTURE INCORPORATING A FIELD PROGRAMMABLE GATE ARRAY CONTROL ELEMENT HAVING AT LEAST ONE EMBEDDED MICROPROCESSOR CORE

BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of adaptive or reconfigurable processors. More particularly, the present invention relates to a multi-adaptive processor ("MAP™", a trademark of SRC Computers, Inc., assignee of the present invention) element architecture incorporating a field programmable gate array ("FPGA") control element having at least one embedded processor core.

Adaptive processors, sometimes referred to as reconfigurable processors, are processor elements that have the ability to alter their hardware functionality based on the program they are running. When compared to a standard microprocessor that can only sequentially execute pre-implemented logic, the adaptive processor has the ability to perform thousands of times more efficiently on a given program. When the next program is run, the logic is reconfigured via software, to again perform very efficiently. The integrated circuits used in these adaptive processors have historically fallen into two categories, namely the custom coprocessor application specific integrated circuits ("ASICs"), and the FPGAs.

Many architectures have been proposed for custom integrated circuit chips containing both microprocessor features and programmable logic portions. These chips however, represent a poor implementation for high performance general purpose adaptive computing since they still have the very high non-recurring costs associated with a high performance custom ASIC, which in turn requires very large markets to make them economically viable. In addition, since both the normal microprocessor and the programmable logic are formed on the same die, the amount of reconfigurable logic will necessarily be much less than if they were each in provided as a discrete part. Since the performance of an adaptive processor is directly proportional to the number of gates it can utilize, this solution is severely limited and is best suited for specialized, limited use, adaptive processors.

An alternative to this approach is to use FPGAs to accomplish the adaptive computing function. However, these chips have historically been relatively small in terms of gate count. In addition, some portion of the gates of the FPGA also had to be used for control functions needed to communicate with the rest of the system. This led to their use primarily in board level products that were designed to target specific families of applications with limited input/output ("I/O") functionality. However, with recent advances in FPGA geometry, features and packaging, it has now become possible to implement new board level architectures that can be used to accomplish large scale high performance general purpose adaptive computing. One such computer is based on the unique SRC Computers, Inc. MAP™ multi-adaptive processor element architecture disclosed herein.

SUMMARY OF THE INVENTION

Disclosed herein is a multi-adaptive processor element architecture incorporating an FPGA control element which may have at least one embedded processor core. The overall architecture has as its primary components three FPGAs, DRAM and dual-ported SRAM banks, with the heart of the design being the user FPGAs which are loaded with the logic required to perform the desired processing. Discrete FPGAs are used to allow the maximum amount of reconfigurable circuitry and, in a particular embodiment disclosed herein, the performance of the multi-adaptive processor element may be further enhanced by preferably using two such FPGAs to form a user array.

By using two chips, they can be advantageously placed on opposite sides of the printed circuit board opposing each other with the contacts of their ball grid array ("BGA") packages sharing a common via through the board. Since the I/O pins of these devices are programmable, the two user FPGAs of the user array can be set up as mirror-image functional pin configurations. This eliminates most of the chip-to-chip routing that would otherwise be required for their interconnection to the degree necessary to allow them to function as effectively one larger device. Further, in this manner the circuit board layer count and cost is also minimized.

This mounting technique also permits the effective use of the largest pin count packages available which will maximize the I/O capability of the user array. Interconnecting the user FPGAs in this fashion makes the electrical loading of these two chips appear as a single electrical termination on the transmission lines that are formed by the traces that connect to the chips. At high data rates, such as that required by a high performance processor, this greatly simplifies termination of these lines leading to improved signal quality and maximum data rates. In current technology, as many as 1500 pins per package can be used and this mounting technique permits the simultaneous implementation of high bandwidth chip-to-chip connectivity, high bandwidth connectivity from one user array directly into a second user array on a different multi-adaptive processor element and high bandwidth connections to multiple banks of discrete dual-ported SRAM.

The dual-ported SRAM banks are used to provide very fast bulk memory to support the user array. To maximize its volume, discrete SRAM chips may be arranged in multiple, independently connected banks. This provides much more capacity than could be achieved if the SRAM were only integrated directly into the FPGAs. Again, the high input/output ("I/O") counts achieved by the particular packaging employed and disclosed herein currently allows commodity FPGAs to be interconnected to six, 64 bit wide SRAM banks achieving a total memory bandwidth of 4.8 Gbytes/sec with currently available devices and technology.

In operation, the high volume DRAM is "read" using its fast sequential burst modes and the lower capacity SRAM banks are then randomly loaded allowing the user FPGAs to experience very high random access data rates from what appears to be a very large virtual SRAM. The reverse also happens when the user FPGAs are "writing" data to the SRAM banks. These overall control functions may be managed by an on-chip DMA engine that is implemented in the control FPGA.

Specifically disclosed herein is an adaptive processor element for a computer system comprising a first control FPGA; a system interface bus coupled to the control FPGA for coupling the processor element to the

computer system; dynamic random access memory (DRAM) coupled to the control FPGA; dual-ported static random access memory (SRAM) having a first port thereof coupled to the control FPGA; and a user array comprising at least one second user FPGA coupled to a second port of the dual-ported SRAM. Various computer system implementations of the adaptive processor element of the present invention disclosed herein are also provided. In each of the possible system level implementations, it should be noted that, while a microprocessor may be used in conjunction with the adaptive processor element(s), it is also possible to construct computing systems using only adaptive processor elements and no separate microprocessors.

Further disclosed herein is an adaptive processor using a discrete control FPGA having embedded processors, a system interface, a peripheral interface, a connection to discrete DRAM and a connection to one port of discrete dual ported SRAM, as well as discrete FPGAs forming a user array, with connections between the FPGAs forming the user array and to a second port of the dual ported discrete SRAM as well as chain port connections to other adaptive processors. The adaptive processor may comprise multiple discrete FPGAs coaxially located on opposite sides of a circuit board to provide the largest possible user array and highest bandwidth, while minimizing chip to chip interconnect complexity and board layer count. Dual-ported SRAM may be used and connected to the control chip and user array in conjunction with DRAM connected to the control chip, to form high speed circular transfer buffers.

An adaptive processor as previously described may further comprise an embedded processor in the control FPGA to create a high speed serial I/O channel to allow the adaptive processor to directly connect to peripheral devices such as disk drives for the purpose of reducing the bandwidth needed on the system interface. It may further comprise logic implemented in the control FPGA to create a high speed serial I/O channel to allow the adaptive processor to directly connect to peripheral devices such as disk drives for the purpose of reducing the bandwidth needed on the system interface. A system interface allows interconnection of multiple adaptive processors

without the need for a host microprocessor for each adaptive processor and an embedded microprocessor in the control chip can be used to decode commands arriving via the system interface.

Further, an adaptive processor as previously described comprises SRAM used as common memory and shared by all FPGAs in the user array and can use separate peripheral I/O and system interconnect ports for the purpose of improving system scalability and I/O bandwidth. DRAM may further be used to provide for large on board storage that is also accessible by all other processors in the system.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

Fig. 1A is a functional block diagram of a particular, representative embodiment of a multi-adaptive processor element incorporating a field programmable gate array ("FPGAs") control element having embedded processor cores in conjunction with a pair of user FPGAs and six banks of dual-ported static random access memory ("SRAM");

Fig. 1B is a simplified flowchart illustrative of the general sequence of "read" and "write" operations as between the dynamic random access memory ("DRAM") and SRAM portions of the representative embodiment of the preceding figure;

Fig. 2 is a system level block diagram of an exemplary implementation of a computer system utilizing one or more of the multi-adaptive processor elements of Fig. 1A in conjunction with one or more microprocessors and memory subsystem banks as functionally coupled by means of a memory interconnect fabric;

Fig. 3 is a further system level block diagram of another exemplary implementation of a computer system utilizing one or more of the multi-

adaptive processor elements of Fig. 1A in conjunction with one or more microprocessors functionally coupled to a shared memory resource by means of a switch network;

Fig. 4 is an additional system level block diagram of yet another exemplary implementation of a computer system utilizing one or more of the multi-adaptive processor elements of Fig. 1A in conjunction with one or more microprocessors and having shared peripheral storage though a storage area network ("SAN"); and

Fig. 5 is a partial cross-sectional view of a particular printed circuit board implementation of a technique for the mounting and interconnection of a pair of user FPGAs of possible use in the representative multi-adaptive processor element of Fig. 1A.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

With reference now to Fig. 1A, a functional block diagram of a particular, representative embodiment of a multi-adaptive processor element 100 is shown. The multi-adaptive processor element 100 comprises, in pertinent part, a discrete control FPGA 102 operating in conjunction with a pair of separate user FPGAs 104_0 and 104_1. The control FPGA 102 and user FPGAs 104_0 and 104_1 are coupled through a number of SRAM banks 106, here illustrated in this particular implementation, as dual-ported SRAM banks 106_0 through 106_5. An additional memory block comprising DRAM 108 is also associated with the control FPGA 102.

The control FPGA 102 includes a number of embedded microprocessor cores including µP1 112 which is coupled to a peripheral interface bus 114 by means of an electro optic converter 116 to provide the capability for additional physical length for the bus 114 to drive any connected peripheral devices (not shown). A second microprocessor core µP0 118 is utilized to manage the multi-adaptive processor element 100 system interface bus 120, which although illustrated for sake of simplicity as a single bi-directional bus, may actually comprise a pair of parallel unidirectional busses. As illustrated, a chain port 122 may also be provided to enable additional

multi-adaptive processor elements 100 to communicate directly with the multi-adaptive processor element 100 shown.

The overall multi-adaptive processor element 100 architecture, as shown and previously described, has as its primary components three FPGAs 102 and 104_0, 104_1, the DRAM 108 and dual-ported SRAM banks 106. The heart of the design is the user FPGAs 104_0, 104_1 which are loaded with the logic required to perform the desired processing. Discrete FPGAs 104_0, 104_1 are used to allow the maximum amount of reconfigurable circuitry. The performance of this multi-adaptive processor element 100 may be further enhanced by using a maximum of two such FPGAs 104 to form a user array. By using two chips, they can be placed on opposite sides of the circuit board from each other as will be more fully described hereinafter.

The dual-ported SRAM banks 106 are used to provide very fast bulk memory to support the user array 104. To maximize its volume, discrete SRAM chips may be arranged in multiple, independently connected banks 106_0 through 106_5 as shown. This provides much more capacity than could be achieved if the SRAM were only integrated directly into the FPGAs 102 and/or 104. Again, the high input/output ("I/O") counts achieved by the particular packaging employed and disclosed herein currently allows commodity FPGAs to be interconnected to six, 64 bit wide SRAM banks 106_0 through 106_5 achieving a total memory bandwidth of 4.8 Gbytes/sec.

Typically the cost of high speed SRAM devices is relatively high and their density is relatively low. In order to compensate for this fact, dual-ported SRAM may be used with each SRAM chip having two separate ports for address and data. One port from each chip is connected to the two user array FPGAs 104_0 and 104_1 while the other is connected to a third FPGA that functions as a control FPGA 102. This control FPGA 102 also connects to a much larger high speed DRAM 108 memory dual in-line memory module ("DIMM"). This DRAM 108 DIMM can easily have 100 times the density of the SRAM banks 106 with similar bandwidth when used in certain burst modes. This allows the multi-adaptive processor element 100 to use the SRAM 106

as a circular buffer that is fed by the control FPGA 102 with data from the DRAM 108 as will be more fully described hereinafter.

The control FPGA 102 also performs several other functions. In a preferred embodiment, control FPGA 102 may be selected from the Virtex Pro family available from Xilinx, Inc. San Jose, CA, which have embedded Power PC microprocessor cores. One of these cores (µP0 118) is used to decode control commands that are received via the system interface bus 120. This interface is a multi-gigabyte per second interface that allows multiple multi-adaptive processor elements 100 to be interconnected together. It also allows for standard microprocessor boards to be interconnected to multi-adaptive processor elements 100 via the use of SRC SNAP™ cards. ("SNAP" is a trademark of SRC Computers, Inc., assignee of the present invention; a representative implementation of such SNAP cards is disclosed in United States Patent Application Serial No. 09/932,330 filed August 17, 2001 for: "Switch/Network Adapter Port for Clustered Computers Employing a Chain of Multi-Adaptive Processors in a Dual In-Line Memory Module Format" assigned to SRC Computers, Inc., the disclosure of which is herein specifically incorporated in its entirety by this reference.) Packets received over this interface perform a variety of functions including local and peripheral direct memory access ("DMA") commands and user array 104 configuration instructions. These commands may be processed by one of the embedded microprocessor cores within the control FPGA 102 and/or by logic otherwise implemented in the FPGA 102.

To increase the effective bandwidth of the system interface bus 120, several high speed serial peripheral I/O ports may also be implemented. Each of these can be controlled by either another microprocessor core (e.g. µP1 112) or by discrete logic implemented in the control FPGA 102. These will allow the multi-adaptive processor element 100 to connect directly to hard disks, a storage area network of disks or other computer mass storage peripherals. In this fashion, only a small amount of the system interface bus 120 bandwidth is used to move data resulting in a very efficient system interconnect that will support scaling to high numbers of multi-adaptive

processor elements 100. The DRAM 108 on board any multi-adaptive processor element 100 can also be accessed by another multi-adaptive processor element 100 via the system interface bus 120 to allow for sharing of data such as in a database search that is partitioned across several multi-adaptive processor elements 100.

With reference additionally now to Fig. 1B, a simplified flowchart is shown illustrative of the general sequence of "read" and "write" operations as between the DRAM 108 and SRAM bank 106 portions of the representative embodiment of the preceding figure. At step 150, reads are performed by the DMA logic in the control FPGA 102 using sequential addresses to achieve the highest bandwidth possible from the DRAM 108. At step 152 the DMA logic then performs "writes" to random address locations in any number of the SRAM banks 106.

Thereafter, at step 154, the use of dual-ported SRAM allows the control FPGA 102 to continuously "write" into the SRAM banks 106 while the user FPGAs 104 continuously "reads" from them as well. At step 156, the logic in the user FPGAs 104 simultaneously performs high speed "reads" from the random addresses in the multiple SRAM banks 106. As indicated by step 158, the previously described process is reversed during "writes" from the user FPGAs 104 comprising the user array.

Briefly, the high volume DRAM 108 is "read" using its fast sequential burst modes and the lower capacity SRAM banks 106 are then randomly loaded allowing the user FPGAs 104 to experience very high random access data rates from what appears to be a very large virtual SRAM. The reverse also happens when the user FPGAs are "writing" data to the SRAM banks 106. These overall control functions may be managed by an on-chip DMA engine that is implemented in the control FPGA 102.

With reference additionally now to Fig. 2, a system level block diagram of an exemplary implementation of a computer system 200 is shown. This particular embodiment of a computer system 200 may utilize one or more of the multi-adaptive processor elements 100_0 through 100_N of Fig. 1A in

conjunction with one or more microprocessors 202_0 through 202_M and memory subsystem banks 206_0 through 206_M as functionally coupled by means of a memory interconnect fabric 204.

With reference additionally now to Fig. 3, a further system level block diagram of another exemplary implementation of a computer system 300 is shown. This particular embodiment of a computer system 300 may also utilize one or more of the multi-adaptive processor elements 100_0 through 100_N of Fig. 1A in conjunction with one or more microprocessors 302_0 through 302_M functionally coupled to a switch network 304 by means of a system interface bus 320 and, in turn, to a shared memory resource 306. Through the provision of individual peripheral interface busses 314, each of the multi-adaptive processor elements 100_0 through 100_N may directly access attached storage resources 308 as may one or more of the microprocessors 302_0 through 302_M through a peripheral bus 312. A number of chain ports 322 may provide direct coupling between individual multi-adaptive processor elements 100_0 through 100_N.

With reference additionally now to Fig. 4, an additional system level block diagram of yet another exemplary implementation of a computer system 400 is shown. This particular implementation of a computer system 400 may additionally utilize one or more of the multi-adaptive processor elements 100_0 through 100_N of Fig. 1A in conjunction with one or more microprocessors 402_0 through 402_M coupled to the multi-adaptive processing elements 100 through respective system interface buses 420 and SNAP cards 416 as previously described. The multi-adaptive processor elements 100_0 through 100_N may be directly coupled to each other by means of chain ports 422 as shown.

In this implementation, the microprocessors 402_0 through 402_M are coupled by means of a network 404 and the multi-adaptive processor elements 100_0 through 100_N and microprocessors 402_0 through 402_M may each have a directly coupled storage element 408 coupled to a peripheral interface 414 or 412 respectively. Alternatively, the multi-adaptive processor elements 100_0 through 100_N and microprocessors 402_0 through 402_M may each be coupled to a storage area network ("SAN") to access shared storage 410.

With reference additionally now to Fig. 5, a partial cross-sectional view of a particular printed circuit board 500 is shown. In accordance with the mounting configuration shown, the two user FPGAs 104_0 and 104_1 (Fig. 1A) may be mounted and interconnected as shown, particularly when furnished in a ball grid array ("BGA") configuration. The contacts of the user FPGAs 104_0 and 104_1 are soldered to opposing sides of a multi-layer printed circuit board 502 which includes a number of through board vias 504 with associated, offset contact pads 506. A number of electrical interconnects 508 provide electrical connections to the vias 504 and contact pads 506 and, in turn, to both of the user FPGAs 104_0 and 104_1.

Discrete FPGAs 104 are used for the user array to allow the maximum amount of reconfigurable circuitry. The performance of this multi-adaptive element 100 (Fig. 1A) is further enhanced by using a preferred two of such FPGAs 104 to form the user array. By using two chips, they can be placed on opposite sides of the printed circuit board 502 opposing each other with the contacts of their BGA packages sharing a common via 504 through the board. Since the I/O pins of these devices are programmable, the two user FPGAs 104_0 and 104_1 can be set up as mirror-image functional pin configurations. This eliminates most of the chip-to-chip routing that would otherwise be required for their interconnection to the degree necessary to allow them to function as effectively one larger device. Further, in this manner circuit board 502 layer count and cost is also minimized. This mounting technique also permits the effective use of the largest pin count packages available which will maximize the I/O capability of the user array. Interconnecting the user FPGAs 104 of the user array in this fashion makes the electrical loading of these two chips appear as a single electrical termination on the transmission lines that are formed by the traces that connect to the chips. At high data rates, such as that required by a high performance processor, this greatly simplifies termination of these lines leading to improved signal quality and maximum data rates. In current technology, as many as 1500 pins per package can be used and this mounting technique permits the simultaneous implementation of high bandwidth chip-to-chip connectivity, high bandwidth

connectivity from one user array directly into a second user array on a different multi-adaptive processor element 100 and high bandwidth connections to multiple banks of discrete dual-ported SRAM 106.

With respect to the exemplary implementations of the computer systems 200 (Fig. 2), 300 (Fig. 3) and 400 (Fig. 4), it should be noted that, while the microprocessors 202, 302 and 402 respectively may be furnished as commercially available integrated circuit microprocessors, other implementations for such a processor or processing element may also be used, for example, the multi-adaptive processor element 100 disclosed herein.

While there have been described above the principles of the present invention in conjunction with specific computer system architectures and multi-adaptive processor element configurations, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is:

CLAIMS

WE CLAIM:

1. An adaptive processor element for a computer system comprising:

a first control FPGA;

a system interface bus coupled to said control FPGA for coupling said processor element to said computer system;

dynamic random access memory (DRAM) coupled to said control FPGA;

dual-ported static random access memory (SRAM) having a first port thereof coupled to said control FPGA; and

a user array comprising at least one second user FPGA coupled to a second port of said dual-ported SRAM.

2. The processor element of claim 1 wherein said first control FPGA comprises at least one embedded microprocessor core.

3. The processor element of claim 2 wherein said at least one embedded microprocessor core is coupled to said system interface bus.

4. The processor element of claim 2 wherein said at least one embedded microprocessor core is coupled to a peripheral interface bus.

5. The processor element of claim 4 further comprising:

at least one storage element coupled to said peripheral interface bus.

6. The processor element of claim 4 further comprising:

a storage area network coupled to said peripheral interface bus.

7. The processor element of claim 1 wherein said system interface bus is coupled to said computer system by means of a switch network.

8. The processor element of claim 7 further comprising:

at least one processor coupled to said switch network.

9. The processor element of claim 7 further comprising:

a shared memory resource coupled to said switch network.

10. The processor element of claim 1 wherein said system interface bus is coupled to a processor by means of a switch network adapter port.

11. The processor element of claim 10 wherein said processor is coupled to another processor by means of a switch network.

12. The processor element of claim 1 wherein said dual-ported SRAM comprises a plurality of dual-ported SRAM devices.

13. The processor element of claim 12 wherein said dual-ported SRAM comprises six dual-ported SRAM devices.

14. The processor element of claim 1 wherein said user array comprises second and third user FPGAs.

15. The processor element of claim 14 wherein said second and third user FPGAs are mounted on opposite sides of a circuit board having a plurality of interconnecting vias therethrough.

16. The processor element of claim 1 further comprising:

a chain port coupled to said user array for providing direct access to at least one other processor element of said computer system.

17. A computer system comprising:

a switch network;

at least one adaptive processor element comprising a first control FPGA, a system interface bus coupled to said control FPGA for coupling said processor element to said switch network, dynamic random access memory (DRAM) coupled to said control FPGA, dual-ported static random access memory (SRAM) having a first port thereof coupled to said control FPGA and a user array comprising at least one second user FPGA coupled to a second port of said dual-ported SRAM;

at least one processor coupled to said switch network; and

a shared memory resource coupled to said switch network.

18. The computer system of claim 17 wherein said first control FPGA comprises at least one embedded microprocessor core.

19. The computer system of claim 18 wherein said at least one embedded microprocessor core is coupled to said system interface bus.

20. The computer system of claim 18 wherein said at least one embedded microprocessor core is coupled to a peripheral interface bus.

21. The computer system of claim 20 further comprising:
at least one storage element coupled to said peripheral interface bus.

22. The computer system of claim 20 further comprising:
a storage area network coupled to said peripheral interface bus.

23. The computer system of claim 17 wherein said at least one processor comprises another adaptive processor element.

24. The computer system of claim 17 wherein said at least one processor comprises a plurality of processors.

25. The computer system of claim 24 wherein said at least one processor is coupled to another one of said plurality of processors by means of said switch network.

26. The computer system of claim 17 wherein said dual-ported SRAM comprises a plurality of dual-ported SRAM devices.

27. The computer system of claim 26 wherein said dual-ported SRAM comprises six dual-ported SRAM devices.

28. The computer system of claim 17 wherein said user array comprises second and third user FPGAs.

29. The computer system of claim 28 wherein said second and third user FPGAs are mounted on opposite sides of a circuit board having a plurality of interconnecting vias therethrough.

30. The computer system of claim 17 further comprising:

a chain port coupled to said user array for providing direct access to at least one other processor element of said computer system.

31. A computer system comprising:

a network;

at least one processor coupled to said network;

a switch network adapter port in operative association with said at least one processor;

at least one adaptive processor element comprising a first control FPGA, a system interface bus coupled to said control FPGA for coupling said processor element to said switch network adapter port, a peripheral interface bus coupled to said control FPGA, dynamic random access memory (DRAM) coupled to said control FPGA, dual-ported static random access memory (SRAM) having a first port thereof coupled to said control FPGA and a user array comprising at least one second user FPGA coupled to a second port of said dual-ported SRAM; and

at least one storage element coupled to said peripheral interface bus.

32. The computer system of claim 31 wherein said first control FPGA comprises at least one embedded microprocessor core.

33. The computer system of claim 32 wherein said at least one embedded microprocessor core is coupled to said system interface bus.

34. The computer system of claim 32 wherein said at least one embedded microprocessor core is coupled to said peripheral interface bus.

35. The computer system of claim 31 wherein said at least one storage element comprises:

a storage area network coupled to said peripheral interface bus.

36. The computer system of claim 35 wherein said at least one processor is also coupled to said storage area network.

37. The computer system of claim 31 wherein said at least one processor comprises another adaptive processor element.

38. The computer system of claim 31 wherein said at least one processor comprises a plurality of processors and a switch network adapter port in operative association with each of said plurality of processors.

39. The computer system of claim 38 wherein each of said plurality of processors is coupled to another one of said plurality of processors by means of said network.

40. The computer system of claim 31 wherein said dual-ported SRAM comprises a plurality of dual-ported SRAM devices.

41. The computer system of claim 40 wherein said dual-ported SRAM comprises six dual-ported SRAM devices.

42. The computer system of claim 31 wherein said user array comprises second and third user FPGAs.

43. The computer system of claim 42 wherein said second and third user FPGAs are mounted on opposite sides of a circuit board having a plurality of interconnecting vias therethrough.

44. The computer system of claim 31 further comprising:

a chain port coupled to said user array for providing direct access to at least one other processor element of said computer system.

45. A circuit board having opposite first and second sides thereof, said circuit board comprising:

first and second pluralities of bonding pads affixed in a generally mirror image relationship to one another on said opposite first and second sides of said circuit board respectively;

first and second integrated circuit devices having programmable input/output pins bonded to a subset of said first and second pluralities of bonding pads respectively; and

a plurality of vias formed intermediate said opposite first and second sides of said circuit board for electrically interconnecting opposing ones of said subset of said first and second pluralities of bonding pads.

46. The circuit board of claim 45 wherein said first and second integrated circuit devices comprise a user array for an adaptive processor element.

47. The circuit board of claim 45 wherein said first and second integrated circuit devices comprise first and second FPGAs.

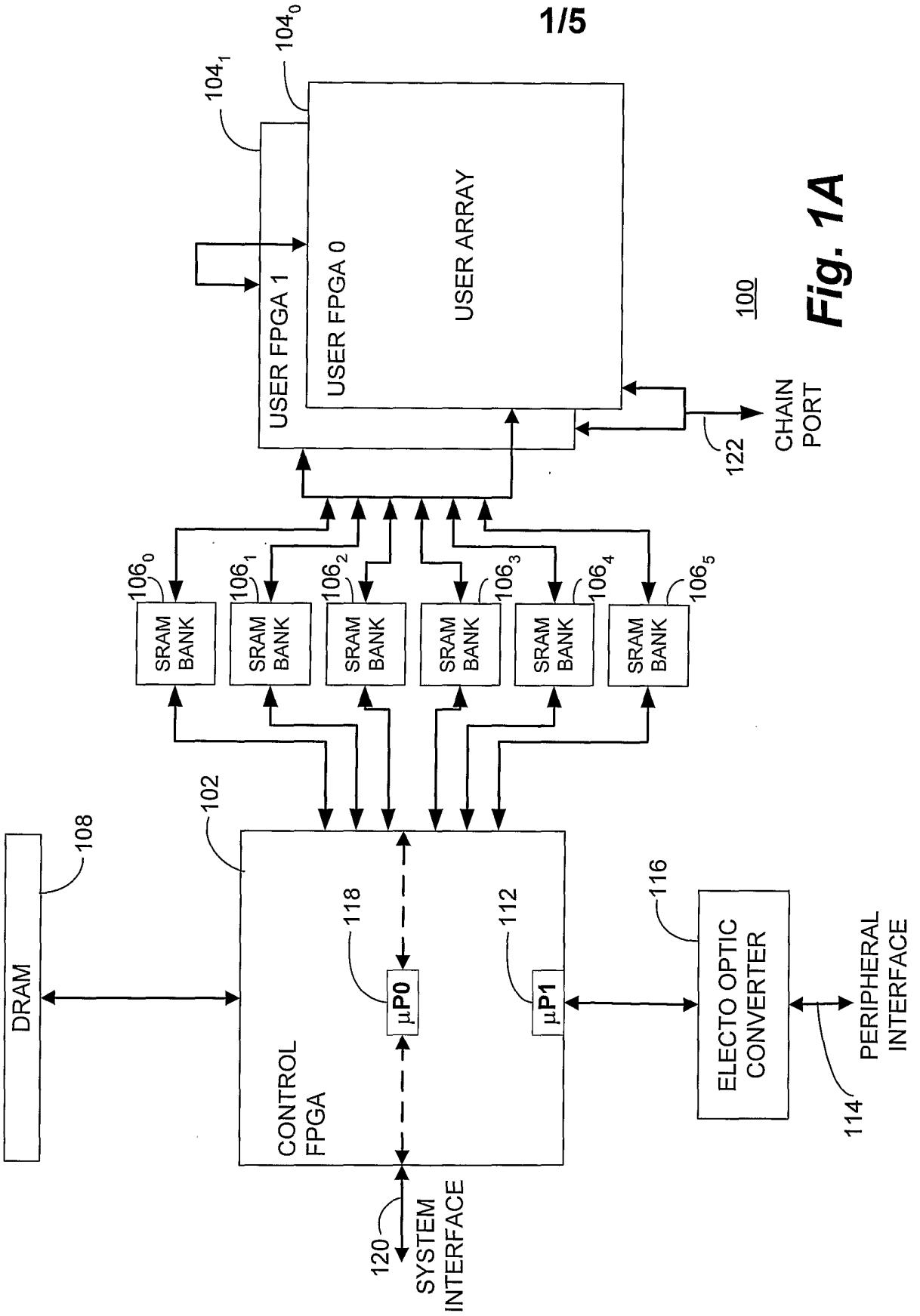

104_0
104_1
USER FPGA 1
USER FPGA 0
USER ARRAY
100
CHAIN PORT
122
106_0
106_1
106_2
106_3
106_4
106_5
SRAM BANK
102
108
DRAM
CONTROL FPGA
118
µP0
112
µP1
116
ELECTO OPTIC CONVERTER
PERIPHERAL INTERFACE
114
120
SYSTEM INTERFACE

Fig. 1A

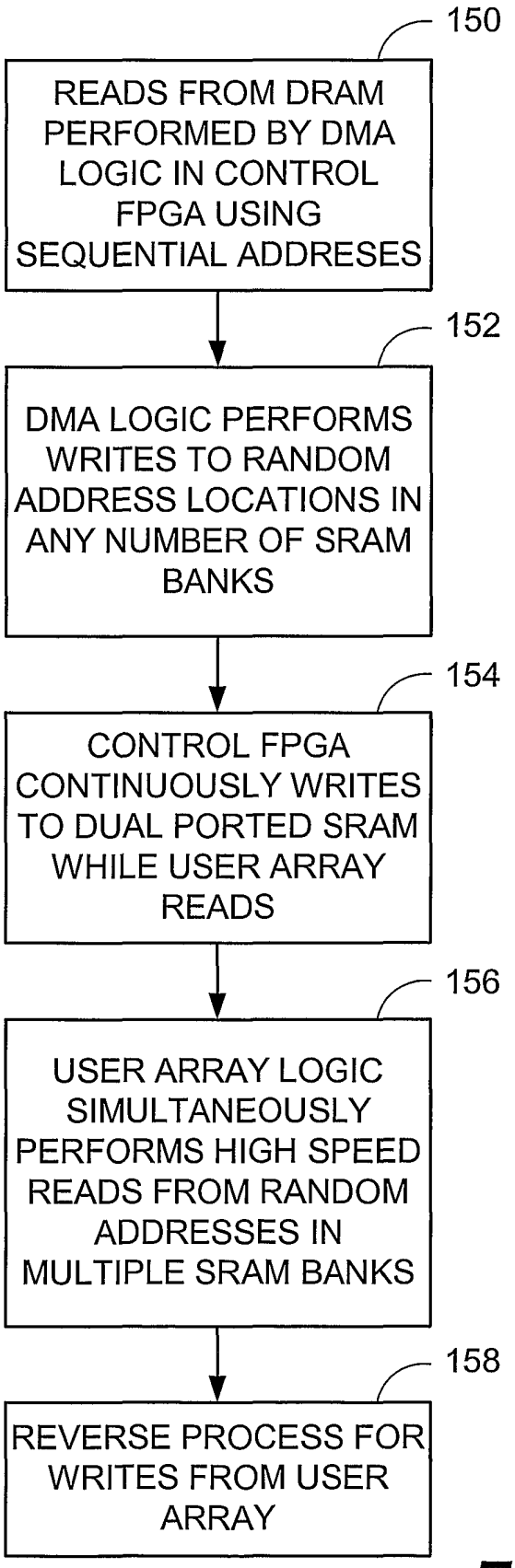
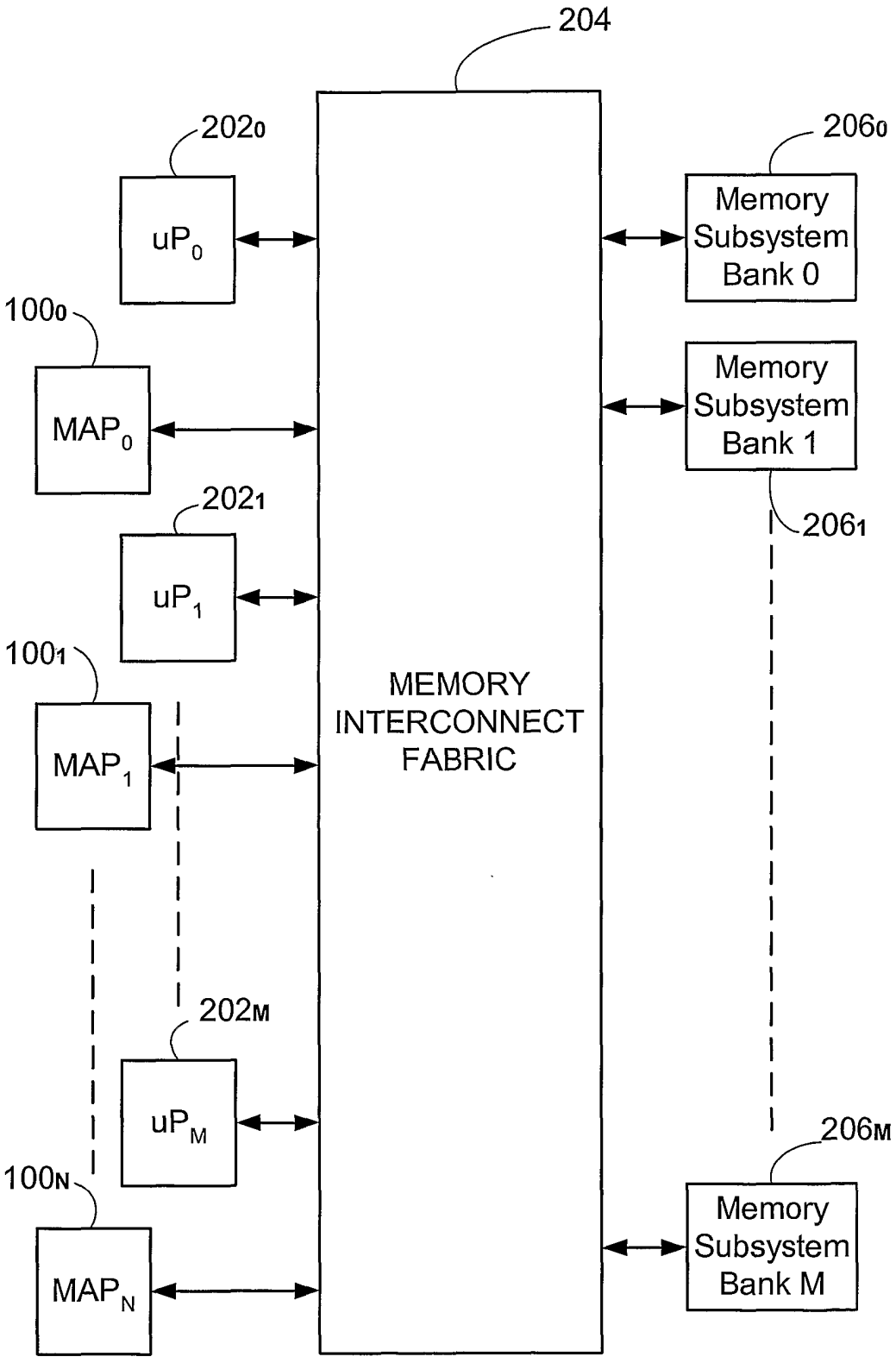

150
READS FROM DRAM PERFORMED BY DMA LOGIC IN CONTROL FPGA USING SEQUENTIAL ADDRESES
152
DMA LOGIC PERFORMS WRITES TO RANDOM ADDRESS LOCATIONS IN ANY NUMBER OF SRAM BANKS
154
CONTROL FPGA CONTINUOUSLY WRITES TO DUAL PORTED SRAM WHILE USER ARRAY READS
156
USER ARRAY LOGIC SIMULTANEOUSLY PERFORMS HIGH SPEED READS FROM RANDOM ADDRESSES IN MULTIPLE SRAM BANKS
158
REVERSE PROCESS FOR WRITES FROM USER ARRAY

Fig. 1B


204
202₀
uP₀
206₀
Memory Subsystem Bank 0
100₀
MAP₀
Memory Subsystem Bank 1
202₁
uP₁
206₁
100₁
MAP₁
MEMORY INTERCONNECT FABRIC
202M
uPM
206M
100N
MAPN
Memory Subsystem Bank M

200

Fig. 2

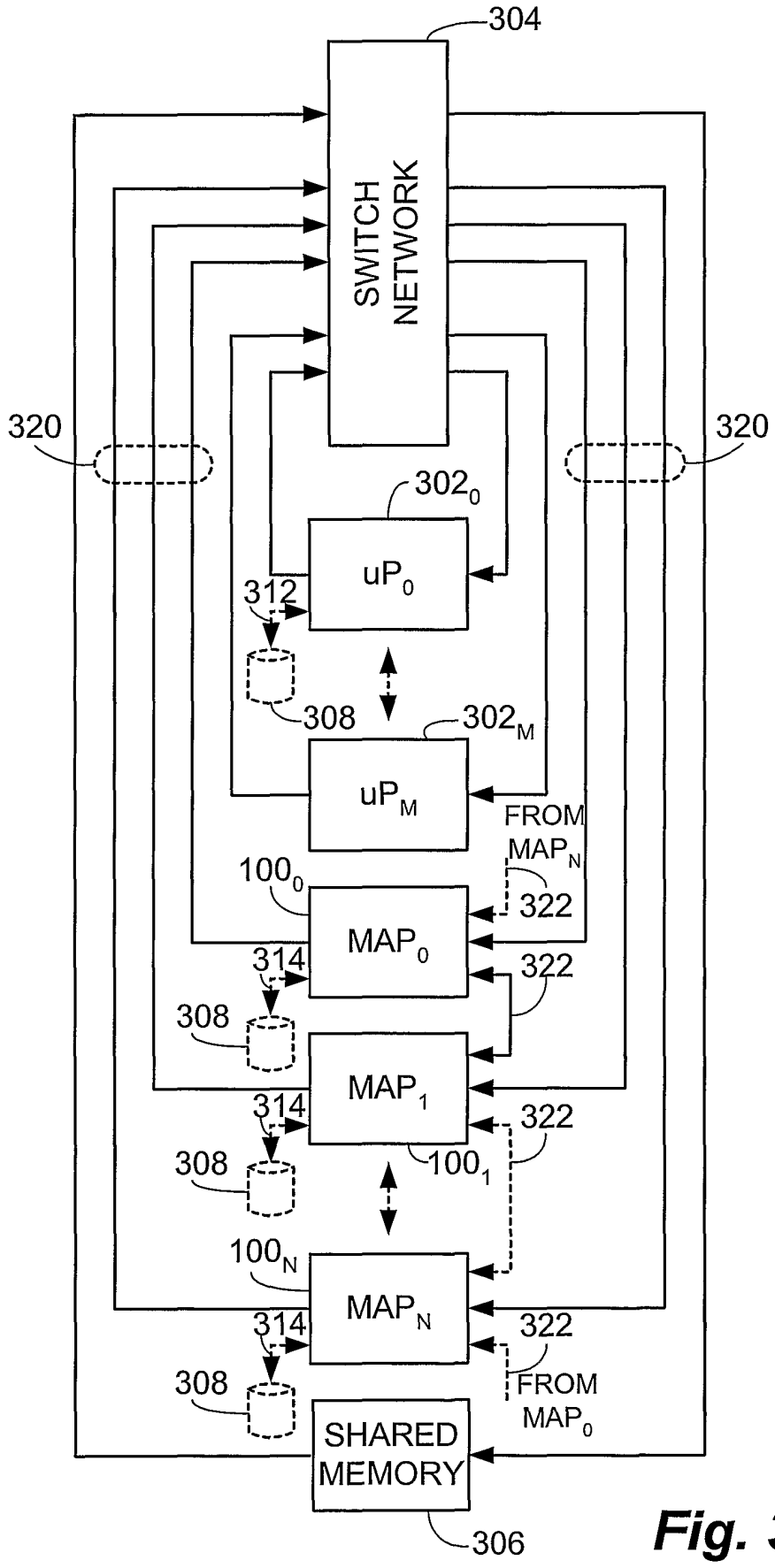

304
SWITCH NETWORK
320
320
302$_0$
uP$_0$
312
308
302$_M$
uP$_M$
FROM MAP$_N$
100$_0$
322
MAP$_0$
314
322
308
MAP$_1$
314
322
308
100$_1$
100$_N$
MAP$_N$
314
322
308
FROM MAP$_0$
SHARED MEMORY
306
300

Fig. 3

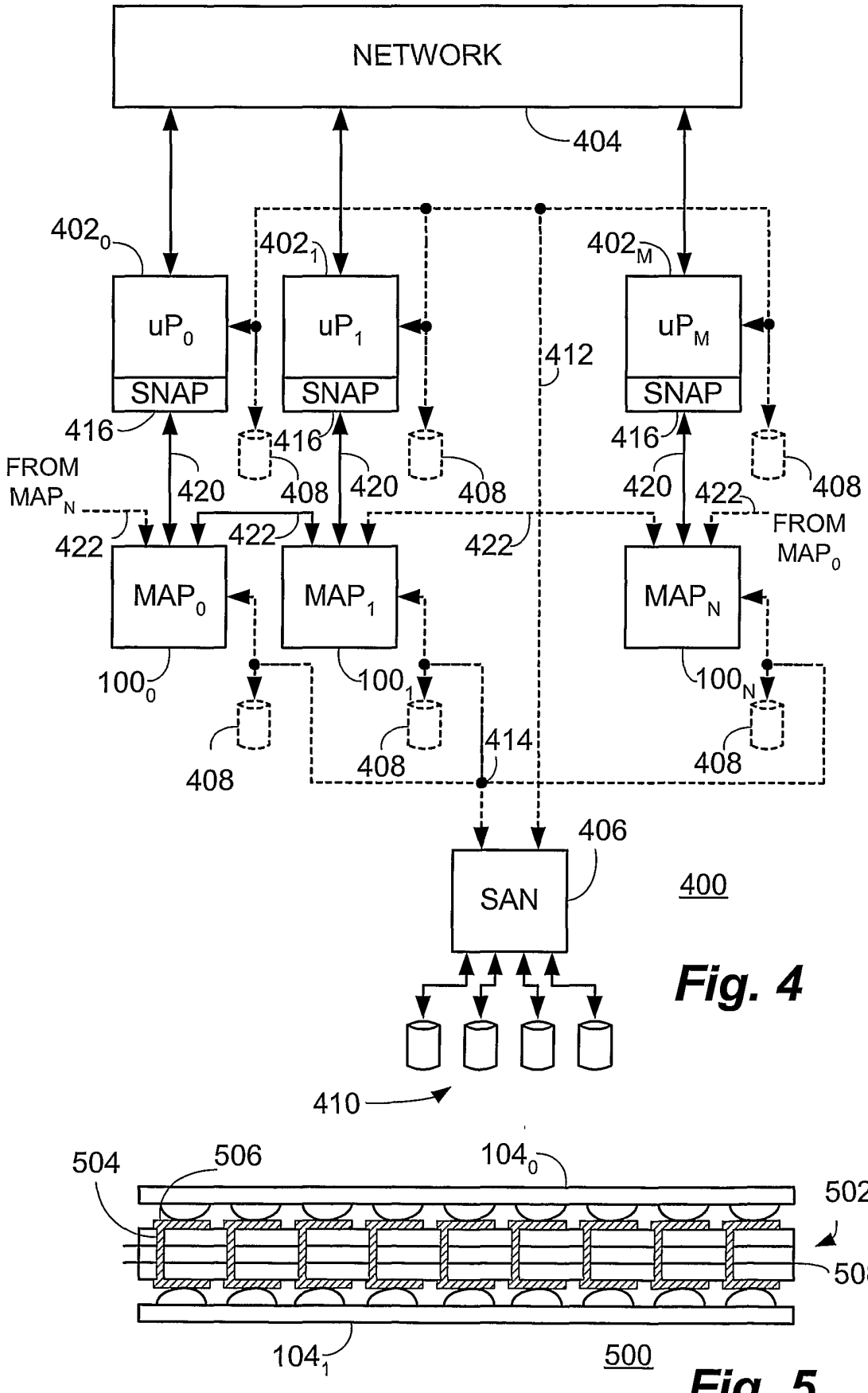

NETWORK
404
402$_0$
402$_1$
402$_M$
uP$_0$
uP$_1$
uP$_M$
SNAP
SNAP
SNAP
412
416
416
416
FROM MAP$_N$
420
408
420
408
420
422
408
422
422
422
FROM MAP$_0$
MAP$_0$
MAP$_1$
MAP$_N$
100$_0$
100$_1$
100$_N$
408
408
408
414
406
SAN
400
410

Fig. 4

504
506
104$_0$
502
508
104$_1$
500

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/38844

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G06F 12/00, 13/00; H01L 27/10, 29/73
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 709/221; 710/8-14; 711/2, 104, 105; 713/1, 100; 716/16; 257/202-203, 209; 326/38-41, 47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,892,962 A (CLOUTIER) 6 April 1999, col. 2, lines 10-60	1-44, 46-47
Y	US 6,356,109 B1 (FURUTA et al) 12 March 2002	7-11, 17-44, 46-47
A, E	US 6,496,971 B1 (LESEA et al) 17 December 2002, col. 4, lines 1-37	1, 17, 31
Y, P	US 6,414,391 B1 (CORISIS et al) 2 July 2002, col. 1, lines 22-30	45
A, P	US 6,441,483 B1 (AKRAM) 27 August 2002, col. 1, lines 40-45, col. 8, lines 7-55	45

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 13 FEBRUARY 2003	Date of mailing of the international search report 03 MAR 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer for PIERRE VITAL Telephone No. (703) 306-5839

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/38844

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/38844

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

709/221; 710/8-14; 711/2, 104, 105; 713/1, 100; 716/16; 257/202-203, 209; 326/38-41, 47

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-44, drawn to an adaptive processor element comprising control and user FPGAs.
Group II, claim(s) 45-47, drawn to a circuit board having opposite first and second sides comprising a plurality of bonding pads affixed in a image relationship to one another and interconnected by a plurality of vias.
The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: In invention II, the plurality of bonding pads affixed in a image relationship to one another and interconnected by a plurality of vias is not a requirement of Invention I.