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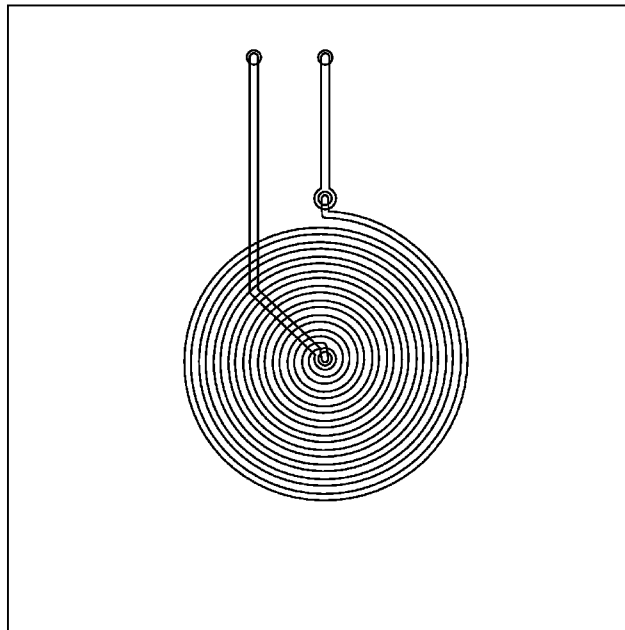


FIG. 20

(57) Abstract: A circuit assembly may include a first layer arranged as a substrate, a second layer having a spiral pattern attached to the substrate, wherein the spiral pattern contains a deformable conductor. A circuit assembly may include a first portion of a deformable inductor fabricated on a first layer of the circuit assembly; and a second portion of the deformable inductor fabricated on a second layer of the circuit assembly and electrically connected to the first portion of the deformable inductor. A method may include sensing an interaction with a deformable inductor, wherein the deformable inductor may include an inductive pattern of deformable conductor, and a deformable substrate arranged to support the inductive pattern of deformable conductor. An article of manufacture may include an inductive pattern of deformable conductor, and a deformable substrate arranged to support the inductive pattern of deformable conductor.



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DEFORMABLE INDUCTORS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from U.S. Provisional Patent Application Ser. No. 62/985,116 filed March 4, 2020 which is incorporated by reference.

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BACKGROUND

[0003] The inventive principles of this patent disclosure relate generally to deformable conductive materials, and more specifically to structures having electrical connections and/or layers with deformable conductive materials, and methods of forming such structures.

SUMMARY

[0004] A circuit assembly may include a first layer arranged as a substrate, a second layer having a spiral pattern attached to the substrate, wherein the spiral pattern contains a deformable conductor. The circuit assembly may further include a third layer attached to the second layer to encapsulate the deformable conductor in the second layer. The third layer may include one or more vias containing a deformable conductor. The circuit assembly may further include a fourth layer attached to the third layer to encapsulate the deformable conductor in the third layer. The fourth layer may include one or more passages arranged as traces and containing a deformable conductor. The circuit assembly may further include a fifth layer attached to the fourth layer to encapsulate the deformable conductor in the fourth layer. The fifth layer may include one or more vias containing a deformable conductor.

[0005] A circuit assembly may include a first portion of a deformable inductor fabricated on a first layer of the circuit assembly; and a second portion of the deformable inductor fabricated on a second layer of the circuit assembly and electrically connected to the first portion of the deformable inductor. The second portion of the deformable inductor may be formed as a

pattern including at least a partial turn. The pattern may include a substantially complete turn. The circuit assembly may further include a deformable substrate disposed between the first layer and the second layer. The first portion of the deformable inductor may be electrically connected to the second portion of the deformable inductor through a via in the deformable substrate.

[0006] A method may include sensing an interaction with a deformable inductor, wherein the deformable inductor may include an inductive pattern of deformable conductor, and a deformable substrate arranged to support the inductive pattern of deformable conductor. Sensing the interaction may include sensing a self-inductance of the deformable inductor. Sensing the interaction may include sensing a mutual-inductance of the deformable inductor. The mutual-inductance may include a mutual inductance with a structure.

[0007] An article of manufacture may include an inductive pattern of deformable conductor, and a deformable substrate arranged to support the inductive pattern of deformable conductor. The article may include an article of clothing. The article of clothing may include a glove. The inductive pattern of deformable conductor may be located at a fingertip of the glove.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Fig. 1 is an exploded view illustrating an embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0009] Fig. 2 is a partially exploded perspective view of an example embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0010] Figs. 3A through 3E are cross-sectional views taken through line A-A in Fig. 2 showing some possible example implementation details and alternative embodiments according to some inventive principles of this patent disclosure.

[0011] Fig. 4 is a partially exploded perspective view of another example embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0012] Figs. 5A-5C are cross-sectional views taken through line A-A in Fig. 4 showing some possible example implementation details and alternative embodiments according to some inventive principles of this patent disclosure.

[0013] Fig. 6 is a partially exploded perspective view of another example embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0014] Figs 7A and 7B through 15A and 15B illustrate embodiments of circuit assemblies and embodiments of methods for fabricating the circuit assemblies according to some inventive principles of this patent disclosure.

[0015] Fig. 16 is a cross-sectional view illustrating another embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0016] Fig. 17 is a cross-sectional view illustrating another embodiment of a circuit assembly according to some inventive principles of this patent disclosure.

[0017] Figs. 18 and 19 are a plan view and a cross-sectional view, respectively, of a via structure according to some inventive principles of this patent disclosure.

[0018] Fig. 20 is a compositive view showing the relative alignment of components of an inductor assembly according to the principles of this disclosure.

[0019] Figs. 21-25 illustrate first through fifth layers, respectively, of an inductor assembly according to the principles of this disclosure.

[0020] Fig. 26 is a top plan view showing how the layers of Figs. 21-25 may appear when fully assembled according to the principles of this disclosure.

DETAILED DESCRIPTION

[0021] The embodiments and example implementation details described below are for purposes of illustration. The drawings are not necessarily shown to scale. The inventive principles are not limited to these embodiments and details.

[0022] Some of the inventive principles of this patent disclosure relate to electrical connections between components and deformable conductive materials in circuit assemblies.

[0023] Fig. 1 is an exploded view illustrating an embodiment of a circuit assembly according to some inventive principles of this patent disclosure. The embodiment of Fig. 1 includes a substrate 100 having a pattern of contact points 102 formed from deformable conductive material and supported by the substrate. An electric component 104 is also supported by the substrate 100 and has one or more terminals 106 arranged in a pattern corresponding to the pattern of contacts points 102. The terminals 106 are shown with dashed lines (phantom view) as they are located on the bottom of the electric component 104. One or more of the terminals 106 of the electric component 104 may contact one or more of the corresponding contact points 102 to form one or more electrical connections between the electric component and the contact points. The one or more terminals 106 may contact one or more of contact points 102,

for example, as the electric component 104 is attached to, brought closer to, or otherwise supported by, the substrate 100 as shown by arrow 108. Some of the inventive principles may thus enable the creation of electrical connections without soldering or any other conventional process for creating electrical connections.

[0024] The contact points 102 may be supported by the substrate 100, for example, by being formed directly on the surface of the substrate, by being recessed into the substrate, by being formed on another layer of material above the substrate, or in other ways. The electric component 104 may be supported by the substrate 100, for example, by being attached directly to the surface of the substrate, by being attached to another component that is supported by the substrate, by being supported by the pattern of contact points 102, or in other ways.

[0025] The assembly of Fig. 1 may further include a pattern of conductive traces formed from deformable conductive material and supported by the substrate. The pattern of conductive traces may be interconnected with the pattern of contact points.

[0026] The embodiment of Fig. 1 may be implemented with a wide variety of materials and components. For example, the substrate may be fabricated from natural or synthetic rubber or plastic materials including any silicone based materials such as polydimethylsiloxane (PDMS), thermoplastic polyurethane (TPU), ethylene propylene diene terpolymer (EPDM), neoprene, polyethylene terephthalate (PET) as well as epoxies and epoxy based materials, fabrics, wood, leather, paper, fiberglass and other composite materials, and other insulating materials and/or combinations thereof.

[0027] The deformable conductive materials may be provided in any form including liquid, paste, gel, powder, or other form having a soft, flexible, stretchable, bendable, elastic, flowable viscoelastic, or otherwise deformable characteristic including Newtonian and non-Newtonian characteristics. The deformable conductive materials may be realized with any electroactive materials including, but not limited to, deformable conductors including conductive gels such as gallium indium alloys (also referred to by the trademark "Metal Gel"), some examples of which are disclosed in U.S. Patent Application Publication No. 2018/0247727 published on August 30, 2018 which is incorporated by reference and International Patent Application PCT/US2017/019762 filed February 27, 2017 which is incorporated by reference and was published on September 8, 2017 as International Publication No. WO 2017/151523 A1 which is also incorporated by reference. Other suitable electroactive materials may include any conductive

metals including gold, nickel, silver, platinum, copper, etc.; semiconductors based on silicon, gallium, germanium, antimony, arsenic, boron, carbon, selenium, sulfur, tellurium, etc., semiconducting compounds including gallium arsenide, indium antimonide, and oxides of many metals; organic semiconductors; and conductive nonmetallic substances such as graphite. Other examples of conductive gels include gels based on graphite or other allotropes of carbon, ionic compounds or other gels.

[0028] U.S. Patent Application Publication No. 2020/0066628 published on February 27, 2020 is incorporated by reference. US Patent Application Publication No. 2019/0056277 which was published February 21, 2019 is incorporated by reference. US Patent Application Publication No. 2020/0381349 which was published December 3, 2020 is incorporated by reference. US Patent Application Publication No. 2020/0386630 which was published December 10, 2020 is incorporated by reference.

[0029] The electric component may be any electrical, electronic, electromechanical, or other electric devices including but not limited to integrated circuits, transistors, diodes, LEDs, capacitors, resistors, inductors, switches, terminals, connectors, displays, sensors, printed circuit boards, or other devices. The electric components may be in the form of bare components, or they may be partially or fully enclosed in various types of packages. In the case of integrated circuits and other semiconductors, a wide range of package types may be used as described in more detail below. Integrated circuits in the form of bare dies or dies mounted on substrates but not fully enclosed in a package such as chip-scale device may also be used.

[0030] The pattern of contact points may include any number and arrangement of contact points, including a single contact point, depending on number and arrangement of terminals on the electric component or components and the number and arrangement of electrical connections.

[0031] Fig. 2 is a partially exploded perspective view of an example embodiment of a circuit assembly according to some inventive principles of this patent disclosure. The embodiment of Fig. 2 includes an integrated circuit (IC) 116 in a surface mount package having terminals in the form of leads 118A-118F. A substrate 110 has a pattern of contact points 112A-112F (also referred to collectively as 112) made from deformable conductive material and arranged to match the footprint of the leads 118A-118F (also referred to collectively as 118) on integrated circuit 116. In this example, the contact points are formed in the shape of solder pads which

would conventionally be used to make electrical connections between the IC and a printed circuit board. Conductive traces 114A-114F (also referred to collectively as 114) , which may also be made from deformable conductive material, are connected to the contact points 112A-112F and end at the edges of the substrate 110 in this cutaway view. The traces 114A-114F may be used, for example, to connect the integrated circuit 116 to other components, circuitry, terminals, etc. The leads 118A-118F contact the corresponding contact points 112A-112F when the integrated circuit 116 is placed onto the substrate as shown by arrow 120.

[0032] In the embodiment of Fig. 2, the contact points 112 and traces 114 are formed on the top surface of, and protrude above, the substrate 110 by, for example, flexographic printing, block printing, jet printing, 3-D printing, stenciling, masked spraying, extruding, rolling, or brushing, screen printing, pattern deposition, or any other suitable technique.

[0033] Figs. 3A-3E are cross-sectional views taken through line A-A in Fig. 2 showing some possible example implementation details and alternative embodiments.

[0034] In Fig. 3A, the IC 116 is shown prior to placement on the substrate 110.

[0035] Fig. 3B shows the IC 116 placed on the substrate 110 and forming ohmic contacts between the leads 118 and contact points 112. The IC 116 is secured to the substrate 110 by a layer of adhesive 122. In this example, the leads 118 have displaced some of the deformable conductive material of the contact points 112 which may conform to the shape of the leads 118 and may provide additional surface area and improved electrical connections.

[0036] Fig. 3C illustrates an embodiment similar to that of Fig. 3B but with an encapsulant 124 covering the integrated circuit 116, leads 118, contact points 112 and traces 114. The encapsulant 124 may also fill the space between the integrated circuit 116, leads 118 and substrate 110. Examples of materials suitable for encapsulant 124 include silicone based materials such as PDMS, urethanes, epoxies, polyesters, polyamides, varnishes, and any other material that may provide a protective coating and/or help hold the assembly together.

[0037] Fig. 3D illustrates an embodiment in which the integrated circuit 116 directly contacts the substrate 110 which may be used, for example, with a substrate 110 made from an inherently adhesive or sticky material, or when an encapsulant will provide adequate strength for holding the integrated circuit 116 to the substrate 110. In this embodiment, the leads 118 may press further into the contact points 112.

[0038] Fig. 3E illustrates an embodiment in which an additional layer of material 126 is attached to the upper surface of the substrate 110 and located under the pattern of contact points 112. The layer 126 may perform various functions. For example, in an implementation in which the substrate is fabricated from a flexible or stretchable material, layer 126 may be made from a more rigid or less stretchable material to prevent flexing or stretching of the region of the substrate directly under the integrated circuit or other electric component which may possibly cause failure of the connections between terminals 118 of the integrated circuit 116 and the contact points 112. As another example, the layer 126 may perform a heat sinking or heat dissipating function for the integrated circuit 116 or other electric component. The additional layer 126 may alternatively be located under the substrate 110, within the substrate, or in any other suitable location. The layer 126 may be formed as a continuous sheet of material, or it may be patterned, for example, with openings for any or all of the contact points 112, traces 114, integrated circuit 116, or other components. Examples of materials that may be used for the layer 126 include some forms of TPU, fiberglass, PET, and other relatively rigid or non-stretchable materials.

[0039] Fig. 4 is a partially exploded perspective view of another example embodiment of a circuit assembly according to some inventive principles of this patent disclosure. The embodiment of Fig. 4 is similar to that of Fig. 2, but the contact points 126A-F are formed by recesses in the substrate 128 that are partially or fully filled with deformable conductive material. The embodiment of Fig. 4 also includes traces 130 that are recessed in the substrate.

[0040] The recesses in the substrate may be formed by removing portions of a sheet of material by drilling, routing, etching, cutting or any other method of removing material with mechanical optical (e.g. laser), chemical, electrical, ultrasound or other apparatus or combination thereof. Alternatively, the substrate may be formed with recesses in it by molding, casting, 3-D printing, or other formation process. The deformable conductive material may be deposited in the recesses through any of the processes mentioned above including printing, stenciling, spraying, rolling, brushing, and any other technique for depositing material in the recesses. Additionally, the recesses may be overfilled with deformable conductive material and then any suitable technique including scraping, rolling, brushing, etc. may be used to remove excess material so that it is flush with, or slightly above or below the surrounding surface of the substrate as described in more detail below.

[0041] Figs. 5A-5C are cross-sectional views taken through line A-A in Fig. 4 showing some possible example implementation details and alternative embodiments.

[0042] In Fig. 5A, the IC 132 is shown prior to placement on the substrate 128.

[0043] Fig. 5B shows the IC 132 placed on the substrate 128 and forming ohmic contacts between the leads 134 and contact points 126. In this example the IC 132 is mounted directly to the substrate 110 which may, for example, have a self-adhesive surface. Alternatively, the IC 132 may be attached to the substrate using adhesives or any other suitable technique. In this example, the leads 134 protrude downward into the contact points 126 and displace some of the deformable conductive material which may conform to the shape of the leads 134 and may provide additional surface area and improved electrical connections.

[0044] The integrated circuits shown in Figs. 2, 3A-3E, 4, and 5A-5B are packaged in surface mount package such as the SOT23-6 (small outline transistor, six lead) package, but any other types of IC packages and electronic components may be used in accordance with the inventive principles of this patent disclosure. For example, lead-less chip carriers may have terminals with flat lead surfaces that provide a good interface to any of the disclosed contact points without disrupting the patterns of deformable conductive material. Some other types of packages that may work well include packages with protruding solder structures such as ball grid arrays (BGAs) and wafer-level chip-scale packaging (WL-CSP), and packages with slightly protruding leads such as leaded chip carriers, since the solder structures or leads may sink slightly into the contact points to create reliable ohmic connections without displacing so much of the deformable conductive material that it disrupts the patterns.

[0045] Fig. 5C illustrates an embodiment in which a chip-scale package 136 with solder bumps 138 is adhered to the substrate 128.

[0046] Fig. 6 illustrates an embodiment in which an additional layer of material 142 is attached to the surface of the substrate 140 after formation of the pattern of contact points 144 and traces 146, but before attachment of the integrated circuit 148. The layer 142 may be similar, for example, to the layer 126 in the embodiment of Fig. 3E. In this embodiment, the layer 142 includes openings for the contact points 144.

[0047] In addition to packaged integrated circuits and other devices, bare integrated circuit dies and other components may be used in accordance with the inventive principles of this patent disclosure. For example, an IC die having bonding or contact pads may be attached to a

substrate having a flush or protruding pattern of contact points that corresponds to the pattern of bonding or contact pads on the die. This may typically require that the die may be mounted upside down (that is, with the bonding or contact pads facing the top surface of the substrate) such that the contact points with deformable conductive material form ohmic connections with the bonding or contact pads.

[0048] Although the deformable conductive material is generally shown as being flush with surface of the substrate in the embodiments of Figs. 4, 5A-5C and 6, the deformable conductive material may alternatively be formed shy of (i.e., recessed below) or proud of (i.e., protruding above) the surface of the substrate. Material may be formed shy of the surface, for example, by only partially filling some or all of the recesses with material, or by removing some material by scraping, brushing, gouging, etching, evaporating, etc. Material may be formed proud of the surface by pattern depositing, stenciling, various forms of printing, etc. In some embodiments, material may be formed proud of the surface by using a release layer with a pattern that matches the pattern of the recesses. The release layer may be positioned over the substrate and the pattern of recesses may be over-filled and then scraped flush with the top surface of the release layer. The release layer may then be removed to leave protruding material in a manner similar to the embodiments described below.

[0049] The contact points and traces are generally shown on the surface of, or extending part way into, the substrate in the embodiments of Figs. 2, 3A-3E, 4, 5A-5C, and 6. In other embodiments, some or all of the contact points and/or traces may extend through the entire thickness of substrate. For example, contact points may be implemented as vias through the substrate, which, in turn, may serve as a layer in one of the embodiments described below.

[0050] Some additional inventive principles of this patent disclosure relate to circuit assemblies having layers with passageways containing deformable conductive materials. The inventive principles relating to electrical connections and the inventive principles relating layers with passageways are independent principles having independent utility. However, some additional inventive principles of his patent disclosure may combine some of these separate principles resulting in more inventive principles in ways that may provide synergistic results.

[0051] Figs 7A and 7B through 15A and 15B illustrate embodiments of circuit assemblies and embodiments of a methods for fabricating the circuit assemblies according to some inventive principles of this patent disclosure. Figs. 7B, 8B, 9B, 10B, 11B, 12B, 13B, 14B and 15B are cross-

sectional views taken through line A-A in the perspective views of Figs. 7A, 8A, 9A, 10A, 11A, 12A, 13A, 14A and 15A, respectively.

[0052] Fig. 7A is a perspective view of a substrate 150, a first layer 152 of insulating material, and a release layer 154. Fig. 7B is a cross-sectional view taken through line A-A of Fig. 7A. The substrate 150 and first layer 152, as well as any of the insulating layers shown in Figs. 8A and 8B through 15A and 15B, may be fabricated from any of the insulating materials discussed above with respect to the embodiment of Fig. 1. For example, the substrate 150 and first layer 152 may be fabricated from a stretchable TPU or epoxy-based material. The substrate 150 may generally be an uninterrupted sheet of material, whereas the first layer 152 of insulating material and the release layer 154 have a pattern of passages 156 and 158, in this example channels, cut through their entire thicknesses to create a mask or stencil. The release layer 154, which may be thinner than the first layer, is stacked on the first layer 152, and may be fabricated from any of the insulating materials discussed above with respect to the embodiment of Fig. 1. For example, the release layer 154 may be fabricated from a thin layer of PET. In embodiments in which the release layer 154 is eventually removed, it may also be fabricated from conductive materials including alloys or pure forms of metals, as well as metalized plastics or other conductive materials.

[0053] The passages 156 and 158 may be formed in the first layer 152 of insulating material and the release layer 154 using any suitable subtractive technique such as laser cutting, drilling, routing, die cutting, water-jet cutting, etc. In other embodiments, the first layer 152 and/or the release layer may be formed by an additive manufacturing technique such as 3-D printing, pattern deposition, etc.

[0054] Fig. 8A is a perspective view of the substrate 150 and first layer 152 of insulating material after the first layer has been stacked on the substrate. Fig. 8B is a cross-sectional view taken through line A-A of Fig. 8A. The substrate 150 and first layer 152 of insulating material may be bonded, fused or cured together, or otherwise attached to each other with any suitable processes and/or materials. For example, if the substrate 150 and first layer 152 are fabricated from TPU or other thermoplastic, they may be bonded together with heat and pressure. As another example, if the substrate 150 and first layer 152 are fabricated from an inherently adhesive material such as some epoxy-based materials, they may be bonded together by pressing the layers together. In yet another example, the substrate 150 and first layer 152 may be fabricated from a UV-curable and exposed to a UV light source after stacking. The stacking

and bonding of the two layers may close off the bottoms of the channels 156 and 158 so there is little or no leakage when they are filled with material.

[0055] Fig. 9A is a perspective view of the substrate 150, first layer 152 of insulating material, and release layer 154 after the channels 156 and 158 have been over-filled with deformable conductive material 160.

[0056] Referring to Figs. 9A and 9B, the channels 156 and 158 have been over-filled with deformable conductive material 160, which may be implemented with any of the deformable conductive material discussed above with respect to the embodiment of Fig. 1. For example, a conductive gel may be used as the deformable conductive material. The material may be over-filled using any suitable technique such as extruding, rolling, swabbing, spraying, printing, brushing, deposition, etc. In one example embodiment, the material may be over-filled using a cotton swab to work the deformable conductive material completely into the channels 156 and 158.

[0057] Referring to Figs. 10A and 10B, excess deformable conductive material 160 may be removed from the surface of the release layer 154 by scraping with a tool 162 as shown by arrow 164. This may cause excess material to form a mound 166 in front of the tool 162 which may help fill any under-filled areas of the channels 156 and 158. Excess material may be discarded or recycled for use with other assemblies. Examples of items that may be used for the tool 162 include a straight-edge ruler, squeegee, spatula, scraper blade, etc. In other embodiments, alternative techniques may be used to remove excess deformable material such as rolling, brushing, etching, etc. In one example embodiment, a roller that is preloaded with deformable conductive material may be used to both apply the material and remove excess material by squeezing it out from under the roller in a single step.

[0058] Referring to Figs. 11A and 11B, the deformable conductive material is shown generally flush with the top surface 167 of the release layer 154 with all or most excess material removed. Depending on the technique used to remove excess material, there may still be thin patches of deformable conductive material remaining on the top surface of the release layer 154. Thus, the release layer may be removed by, for example, peeling it off to leave a clean top surface 168 on the first layer 152 of insulating material as shown in Figs. 12A and 12B.

[0059] The deformable conductive material 160 in channels 156 and 158 is shown generally flush with the top surface 168 of the first layer 152 of insulating material in Figs. 12A and 12B.

This may be accomplished by using a release layer that is thin enough (e.g., a few microns or tens of microns, or a few thousandths of an inch thick) that the remaining deformable conductive material is effectively flush. (In some embodiments, the thickness of the release layer 154 may be exaggerated in the views of Figs. 7A and 7B through 11A and 11B.) In some embodiments, if even a small amount of protrusion needs to be avoided, a small amount of the deformable conductive material 160 may be removed from the channels 156 and 158 by scraping, brushing, etc. prior to removal of the release layer 154, thereby leaving the deformable conductive material 160 flush with the top surface 168 of the first layer 152 of insulating material.

[0060] In some embodiments, it may be beneficial to have the deformable conductive material 160 slightly proud of the surface. In some embodiments, the thickness of the release layer 154 may purposely be set to a value that may cause the deformable conductive material 160 to protrude above the top surface 168 of the first layer 152 of insulating material by a predetermined amount.

[0061] The structure illustrated in Figs 12A and 12B has utility as fabricated, or as a base for additional layers. For example, as fabricated, it may be used as a pattern of contact pads to engage the terminals of an electric device that may be mounted on, or supported by, the first layer 152 as described above with respect to Figs. 1 through 6. In such an application, it may be beneficial for the deformable conductive material 160 to protrude above the top surface 168 of the first layer 152 of insulating material, for example to better engage the terminals of the electric device. The pattern of conductive channels 156 and 158 may be modified to include different numbers, sizes, shapes, etc. of conductive passageways to function as contact points and/or traces.

[0062] As fabricated, the embodiment illustrated in Figs. 12A and 12B, or with a modified pattern of passageways, may also be used as a circuit element itself. For example, the channels 156 and 158 filled with deformable conductive material 160 may function as a transmission line such as a strip line or in circuit capacitor. In such an implementation, a layer of encapsulant may be formed over the top of the layer 152 to enclose and protect the deformable conductive material 160.

[0063] As mentioned above, the structure as illustrated in Figs 12A and 12B, or with a modified pattern of passageways, may also be used as a base for additional layers. For example,

referring to Figs. 13A and 13B, a second layer 170 of insulating material may be stacked on top of the first layer 152. The second layer 170 may have a pattern of passages, at least one of which communicates with one or more of the passages in the first layer 152. In the example of Figs. 13A and 13B, the pattern includes through vias 172 and 174 that align with the traces formed by channels 156 and 158, respectively, in the first layer 152. Other parts of the second layer 170 may serve to enclose the deformable conductive material within portions of the channels 156 and 158 in the first layer 152. The second layer 170 and vias 172 and 174 may be formed and attached using any of the materials and techniques disclosed for the first layer 152, including the user of a release layer. For brevity, the intermediate steps in which the second layer 170 is formed and attached are not illustrated, and the second layer is shown in its final form in Figs. 13A and 13B.

[0064] As is visible in Fig. 13B, the via 172 in the second layer 170 aligns and communicates with a portion of channel 156 in the first layer 152. Thus, when the via 172 is filled with deformable conductive material, it forms a continuous conductive structure with the channel 156.

[0065] The vias 172 and 174 in the second layer 170 may serve numerous functions. For example, they may function as contact points for one or more electric devices, they may function as circuit elements themselves, for example as a transmission line or sensor, they may electrically connect the traces formed by channels 156 and 158 in the first layer 152 with traces in another layer above the second layer, etc. The pattern of vias 172 and 174 shown in Figs. 13A and 13B is merely one example, and the pattern may be modified to include any number, shape, arrangement, etc., of conductive passageways.

[0066] Referring to Figs. 14A and 14B, a third layer 176 of insulating material may be stacked on the second layer 170 of insulating material. The third layer 176 may have a pattern of passages, at least one of which communicates with one or more of the passages in the second layer 170. In the example of Figs. 14A and 14B, the pattern includes channels 178 and 180 that align with the vias 172, and 174, respectively, in the second layer 170. The third layer 176 and channels 178 and 180 may be formed and attached using any of the materials and techniques disclosed for the first and second layers 152 and 170, including the user of a release layer. For brevity, the intermediate steps in which the third layer 176 is formed and attached are not illustrated, and the third layer is shown in its final form in Figs. 14A and 14B.

[0067] As with the patterns of passages in the first and second layers 152 and 170, the pattern of channels 178 and 180 in the third layer 176 may serve numerous functions. For example, they may function as contact points for one or more electric devices, they may function as circuit elements themselves, for example as a transmission line or sensor, they may function as traces that are electrically connected to the vias 172 and 174 in the second layer 170, etc. The pattern of channels 178 and 180 shown in Figs. 14A and 14B is merely one example, and the pattern may be modified to include any number, shape, arrangement, etc., of conductive passageways.

[0068] Referring to Figs. 15A and 15B, a fourth layer 182 of insulating material may be stacked on the third layer 176 of insulating material. The fourth layer 182 may have a pattern of passages, at least one of which communicates with one or more of the passages in the third layer 176. In the example of Figs. 15A and 15B, the pattern includes pads 184 and 186 that align with the channels 178 and 180, respectively, in the third layer 176. Other parts of the fourth layer 182 may serve to enclose the deformable conductive material within portions of the channels 178 and 180 in the third layer 176. The fourth layer 182 and pads 184 and 186 may be formed and attached using any of the materials and techniques disclosed for the first, second, and third layers 152, 170 and 176, including the user of a release layer. For brevity, the intermediate steps in which the fourth layer 182 is formed and attached are not illustrated, and the fourth layer is shown in its final form in Figs. 15A and 15B.

[0069] As with the patterns of passages in the other layers, the pattern of pads 184 and 186 in the fourth layer 182 may serve numerous functions. For example, they may function as contact points for one or more electric devices, they may function as circuit elements themselves, for example as a transmission line or sensor, they may function as vias that electrically connect the channels 178 and 180 in the third layer 176, to passages in additional layers above the fourth layer 182, they may function as contact points for making "hard-to-soft" connections between hard external terminals and the deformable conductive material, etc. The pattern of pads 184 and 186 shown in Figs. 15A and 15B is merely one example, and the pattern may be modified to include any number, shape, arrangement, etc., of conductive passageways.

[0070] As is visible in Fig. 15B, there is one continuous conductive path through the channel 156 in the first layer 152, the via 172 in the second layer 152, the channel 178 in the third layer 176 and the pad 184 in the fourth layer 182. The layers and passages in the embodiments shown in Figs. 7A and 7B through 15A and 15B are for purposes of illustration only and may be modified to create any type of circuit arrangement. For example, the order of the layers of vias

and pads and layers with traces may be changed. Some layers may include both traces and vias and pads.

[0071] In some example embodiments, one or more of the insulating layers may be formed a TPU or a stretchable epoxy-based material. Stretchable epoxy-based materials may also provide a self-adhesive surface for bonding electric components to the layer, and for bonding layers to each other. Other examples of materials with adhesive properties include some thermally activated adhesives like polyurethane (PU) adhesives, thermoset adhesives with different chemistry such as some silicones, acrylics or others, and any pressure sensitive adhesive of any chemistry, etc.

[0072] Such materials may result in embodiments of circuit assemblies that may be flexible and/or stretchable enough for use in clothing, medical electronics worn against or close to a patient's body, etc. In some embodiments, one or more release layers may be left in place on the surface of a layer of insulating material. In other embodiments, release layers may be omitted entirely. Although the passages shown in the embodiments of Figs. 7A and 7B through 15A and 15B are generally shown extending the entire way through the layers of insulating materials, in other embodiments, some or all of the passages may only extend part of the way through one or more of the layers of insulating materials.

[0073] In some embodiments, electric components may be integrated into a stack of layers, for example, between layers. For example, one or more internal layers of a stack may have a cutout section to accommodate the height of a device such as an integrated circuit package. In some other embodiments, some components such as resistors and/or capacitors, as well as smaller IC packages and bare IC dies may be small enough to place between layers, especially if the layers are relatively soft and or pliable.

[0074] Fig. 16 is a cross-sectional view illustrating another embodiment of a circuit assembly according to some inventive principles of this patent disclosure. For purposes of illustration, the embodiment of Fig. 16 is shown having layers similar to those in Fig. 15B, but the inventive principles are not limited to these details. The embodiment of Fig. 16 may include a layer, sublayer, or portion of a layer (referred to collectively as a "sublayer") 177 on or in which a pattern of conductive elements has been formed. In this example, the sublayer 177 is interposed between the second layer 170 and the third layer 176 over the right-hand portion of the stack. The third and fourth layers 176 and 182 are formed with a step to accommodate the

sublayer 177. In other embodiments, the sublayer may replace a portion of a layer, an entire layer or be added as another entire layer. The sublayer 177 may be thinner, thicker or the same thickness as any of the other layers.

[0075] Any or all of the conductive elements on layer 177 may be formed from any of the deformable conductive materials disclosed above. The pattern of conductive elements may also include a mix of deformable and non-deformable conductive elements. The sublayer 177 may be fabricated from any of the insulating materials disclosed above and attached to other layers as described above. The pattern of elements may include traces, vias, pads, circuit elements including transmission lines and sensors, etc. The pattern of elements may be formed on the sublayer 177 through any of the techniques described above. In some embodiments, it may be beneficial to form some or all of the elements through a printing process such as a reel-to-reel (R2R) process. This may enable the creation of finer conductive elements to accommodate smaller electric components or interconnects, or to accommodate components or interconnects having generally different characteristics.

[0076] In the embodiment of Fig. 16, the sublayer 177 has a pattern including two traces 188 and 190 connected to pads 192 and 194 that align with terminals 196 and 198, respectively, on an electric component 200. Vias 202 and 204 through the third layer 176 connect the pads 192 and 194 with the terminals 196 and 198, respectively. The electric component 200 in this example is shown as a bare integrated circuit die on which the terminals 196 and 198 are formed as bonding or contact pads, but any other type of electric component may be used. In this example, the IC die 200 is adhesively attached to the third layer 176, but it may be attached in any other manner.

[0077] The pattern of conductive elements formed on the sublayer 177 may be interconnected with any other traces, vias, pads, components, etc. In the example of Fig. 16, trace 190 on sublayer 177 is electrically connected to trace 178 in layer 176 through hybrid trace/via 208 formed in the step portion of layer 176 which accommodates the thickness of the sublayer 177. In other embodiments, the portion of layer 176 over the sublayer 177 may be omitted, and the fourth layer 182 may be formed on a plane formed by the remaining portion of layer 176 and the sublayer 177.

[0078] Fig. 17 is a cross-sectional view illustrating another embodiment of a circuit assembly according to some inventive principles of this patent disclosure. The embodiment of Fig. 17 is

similar to that of Fig. 16, but the entire portion of the third layer 176 under the IC die 200 is omitted, as are the vias 202 and 204. The IC die is attached to the top surface of sublayer 177 with a layer of adhesive 206, and the bonding or contact pads 196 and 198 directly contact the pads 192 and 194, respectively, which are formed from deformable conductive material.

[0079] Fig. 18 is a plan view of a via structure according to some inventive principles of this patent disclosure. Fig. 19 is a cross-sectional view taken along line A-A in Fig. 18. The embodiment of Figs. 18 and 19, which may utilize any of the materials and fabrication techniques described above, includes a substrate 210, and first and second layers 212 and 216 of insulating material stacked on the substrate 210. The first layer 212 includes a trace 214. The second layer includes a via 218 formed over, and communicating with, the trace 214. As shown in Fig. 18, the via 218 has an extended length in the X axis (as compared to the Y axis) which may be an axis along which the assembly of Fig. 18 is subjected to a strain, a shear force, and/or a stretching deformation. By extending the length of the via along the X axis, it may provide a more robust connection between the via 218 and the trace 214 which may tend to slide past each other when the assembly may be stretched along the X axis.

[0080] The technique of extending a conductive element in a direction of expected stretch is illustrated in the context of a via in Figs. 18 and 19, but it may also be applied to any other passages, interconnects or structures. In some embodiments, other aspects of the relative sizes and shapes of vias, traces, and other features may be adjusted to accommodate stretching. For example, in some embodiments, vias may have a diameter that is about half the trace width.

[0081] Figs. 20-26 illustrate an embodiment of an inductor assembly according to the principles of this disclosure. Although the embodiment illustrated in Figs. 20-26 is not limited to any particular materials and/or fabrication techniques, it may be fabricated using any of the materials and/or fabrication techniques described herein.

[0082] Figs. 21-25 illustrate first through fifth layers (or Layer 1 through Layer 5), respectively, which, for convenience, may be arbitrarily designated as top through bottom layers. Layer 5 (the bottom layer) shown in Fig. 25 may be implemented as a substrate to support Layer 4 in which a spiral passage has been formed as shown in Fig. 24. Layer 4 may be bonded to Layer 5 and the spiral passage may be filled with a deformable conductor, thereby forming a spiral inductor. Layer 4 may then be covered with Layer 3 which may have two vias formed therein as shown in

Fig. 23. Layer 3 may be bonded to Layer 4, thereby encapsulating the deformable conductor in Layer 4. The two vias in Layer 3 may then be filled with deformable conductor. Layer 3 may then be covered with Layer 2 which may have passages for traces formed therein as shown in Fig. 22. Layer 2 may be bonded to Layer 3, thereby encapsulating the deformable conductor in Layer 3. The passages in Layer 2 may then be filled with deformable conductor. The vias in Layer 3 may align with the ends of the spiral inductor and the traces in Layer 2 to form electrical connections between the spiral inductor in Layer 4 and the traces in Layer 2. Layer 2 may be covered with Layer 1 (the top layer) which may have two vias formed therein as shown in Fig. 21. Layer 1 may be bonded to Layer 2, thereby encapsulating the deformable conductor in Layer 2. The two vias in Layer 1 may then be filled with deformable conductor to form interconnects for interfacing the spiral inductor, for example, to electronic circuitry.

[0083] Fig. 20 is a compositive view showing the relative alignment of the features illustrated in Figs. 21-25 when fully assembled. Fig. 26 is a top plan view showing how the layers of Figs. 21-25 may appear when fully assembled, assuming transparency in the layers.

[0084] The embodiment illustrated in Figs. 20-26 may be employed in a wide variety of applications using myriad combinations of materials according to the principles of this disclosure. For example, an embodiment fabricated with flexible and/or stretchable layers (e.g., various thermoset films, sheets, etc., and/or thermoplastic polyurethane (TPU)) may be integrated into one or more fingertips of a glove to enable sensing of the interaction of fingertips with other objects and/or surfaces, either in direct contact or through proximity sensing. Such sensing may be accomplished, for example, by measuring changes in the self- and/or mutual-inductance of the inductor, either by itself, or through the interaction with other electro-active or magnetically active structures such as plates, sheets, coils, etc. of metals and/or other conductors, etc., as well as sources of electric, magnetic or electromagnetic power, energy, signals, fields, etc. Such sensing may also be accomplished, for example, by using the structure for capacitive sensing, either individually, or in combination with inductive sensing, electrostatic sensing, etc.

[0085] Embodiments constructed according to the inventive principles of this patent disclosure may result in highly functional circuit assemblies that may reduce the cost of the assembly since they may allow for the use of less expensive unpackaged electronic devices and also eliminate soldering steps. Embodiments constructed according to the inventive principles of this patent disclosure may also provide improved reliability because the elimination of solder

may reduce the heating associated with soldering and may also provide improved cooling by eliminating device packaging which may serve as a barrier to heat dissipation.

[0086] Some additional example embodiments are set forth in the following numbered clauses.

[0087] 1. A circuit assembly comprising:

[0088] a first layer arranged as a substrate;

[0089] a second layer having a spiral pattern attached to the substrate, wherein the spiral pattern contains a deformable conductor.

[0090] 2. The circuit assembly of clause 1 further comprising a third layer attached to the second layer to encapsulate the deformable conductor in the second layer.

[0091] 3. The circuit assembly of clause 2 wherein the third layer includes one or more vias containing a deformable conductor.

[0092] 4. The circuit assembly of clause 3 further comprising a fourth layer attached to the third layer to encapsulate the deformable conductor in the third layer.

[0093] 5. The circuit assembly of clause 4 wherein the fourth layer includes one or more passages arranged as traces and containing a deformable conductor.

[0094] 6. The circuit assembly of clause 5 further comprising a fifth layer attached to the fourth layer to encapsulate the deformable conductor in the fourth layer.

[0095] 7. The circuit assembly of clause 6 wherein the fifth layer includes one or more vias containing a deformable conductor.

[0096] 8. The circuit assembly of clause 1 wherein the first and second layers comprise one or more deformable materials.

[0097] 9. The circuit assembly of clause 1 wherein the spiral pattern containing the deformable conductor has an inductance.

[0098] 10. A circuit assembly comprising:

[0099] a first portion of a deformable inductor fabricated on a first layer of the circuit assembly; and

[0100] a second portion of the deformable inductor fabricated on a second layer of the circuit assembly and electrically connected to the first portion of the deformable inductor.

- [0101] 11. The circuit assembly of clause 10 wherein the first portion of the deformable inductor comprises a substantially straight portion.
- [0102] 12. The circuit assembly of clause 10 wherein the second portion of the deformable inductor is formed in a pattern comprising at least a partial turn.
- [0103] 13. The circuit assembly of clause 12 wherein the pattern comprises a substantially complete turn.
- [0104] 14. The circuit assembly of clause 10 further comprising a deformable substrate disposed between the first layer and the second layer.
- [0105] 15. The circuit assembly of clause 14 wherein the first portion of the deformable inductor is electrically connected to the second portion of the deformable inductor through a via in the deformable substrate.
- [0106] 16. The circuit assembly of clause 15 further comprising a third portion of deformable inductor fabricated on the first layer of the circuit assembly.
- [0107] 17. The circuit assembly of clause 16 wherein the via comprises a first via, and the third portion of the deformable inductor is electrically connected to the second portion of the deformable inductor through a second via in the deformable substrate.
- [0108] 18. The circuit assembly of clause 17 wherein the second portion of the deformable inductor is formed in a pattern comprising a substantially full turn.
- [0109] 19. The circuit assembly of clause 18 wherein the second portion of the deformable inductor comprises a spiral pattern.
- [0110] 20. A method comprising:
- [0111] sensing an interaction with a deformable inductor;
- [0112] wherein the deformable inductor comprises:
- [0113] an inductive pattern of deformable conductor; and
- [0114] a deformable substrate arranged to support the inductive pattern of deformable conductor.
- [0115] 21. The method of clause 20 wherein sensing the interaction comprises sensing a self-inductance of the deformable inductor.

- [0116]** 22. The method of clause 20 wherein sensing the interaction comprises sensing a mutual-inductance of the deformable inductor.
- [0117]** 23. The method of clause 22 wherein the mutual-inductance comprises a mutual inductance with a structure.
- [0118]** 24. The method of clause 23 wherein the structure is electro-active.
- [0119]** 25. The method of clause 23 wherein the structure is magnetic.
- [0120]** 26. The method of clause 20 wherein the interaction is with an object.
- [0121]** 27. The method of clause 20 wherein the interaction is with a surface.
- [0122]** 28. The method of clause 20 wherein the sensing comprises capacitive sensing.
- [0123]** 29. The method of clause 20 wherein the sensing comprises electrostatic sensing.
- [0124]** 30. The method of clause 20 wherein the sensing comprises contact sensing.
- [0125]** 31. The method of clause 20 wherein the sensing comprises proximity sensing.
- [0126]** 32. An article of manufacture comprising:
- [0127]** an inductive pattern of deformable conductor; and
- [0128]** a deformable substrate arranged to support the inductive pattern of deformable conductor.
- [0129]** 33. The article of manufacture of clause 32 wherein the article comprises an article of clothing.
- [0130]** 34. The article of manufacture of clause 33 wherein the article of clothing comprises a glove.
- [0131]** 35. The article of manufacture of clause 34 wherein the inductive pattern of deformable conductor is located at a fingertip of the glove.
- [0132]** Since the inventive principles of this patent disclosure can be modified in arrangement and detail without departing from the inventive concepts, such changes and modifications are considered to fall within the scope of the following claims. The use of terms such as first and second are for purposes of differentiating different components and do not necessarily imply the presence of more than one component.

CLAIMS

1. A circuit assembly comprising:
 - a first layer arranged as a substrate;
 - a second layer having a spiral pattern attached to the substrate, wherein the spiral pattern contains a deformable conductor.
2. The circuit assembly of claim 1 further comprising a third layer attached to the second layer to encapsulate the deformable conductor in the second layer.
3. The circuit assembly of claim 2 wherein the third layer includes one or more vias containing a deformable conductor.
4. The circuit assembly of claim 3 further comprising a fourth layer attached to the third layer to encapsulate the deformable conductor in the third layer.
5. The circuit assembly of claim 4 wherein the fourth layer includes one or more passages arranged as traces and containing a deformable conductor.
6. The circuit assembly of claim 5 further comprising a fifth layer attached to the fourth layer to encapsulate the deformable conductor in the fourth layer.
7. The circuit assembly of claim 6 wherein the fifth layer includes one or more vias containing a deformable conductor.
8. A circuit assembly comprising:
 - a first portion of a deformable inductor fabricated on a first layer of the circuit assembly;
 - and
 - a second portion of the deformable inductor fabricated on a second layer of the circuit assembly and electrically connected to the first portion of the deformable inductor.
9. The circuit assembly of claim 8 wherein the second portion of the deformable inductor is formed in a pattern comprising at least a partial turn.

10. The circuit assembly of claim 9 wherein the pattern comprises a substantially complete turn.
11. The circuit assembly of claim 8 further comprising a deformable substrate disposed between the first layer and the second layer.
12. The circuit assembly of claim 11 wherein the first portion of the deformable inductor is electrically connected to the second portion of the deformable inductor through a via in the deformable substrate.
13. A method comprising:
sensing an interaction with a deformable inductor;
wherein the deformable inductor comprises:
an inductive pattern of deformable conductor; and
a deformable substrate arranged to support the inductive pattern of deformable conductor.
14. The method of claim 13 wherein sensing the interaction comprises sensing a self-inductance of the deformable inductor.
15. The method of claim 13 wherein sensing the interaction comprises sensing a mutual-inductance of the deformable inductor.
16. The method of claim 15 wherein the mutual-inductance comprises a mutual inductance with a structure.
17. An article of manufacture comprising:
an inductive pattern of deformable conductor; and
a deformable substrate arranged to support the inductive pattern of deformable conductor.

18. The article of manufacture of claim 17 wherein the article comprises an article of clothing.

19. The article of manufacture of claim 18 wherein the article of clothing comprises a glove.

20. The article of manufacture of claim 19 wherein the inductive pattern of deformable conductor is located at a fingertip of the glove.

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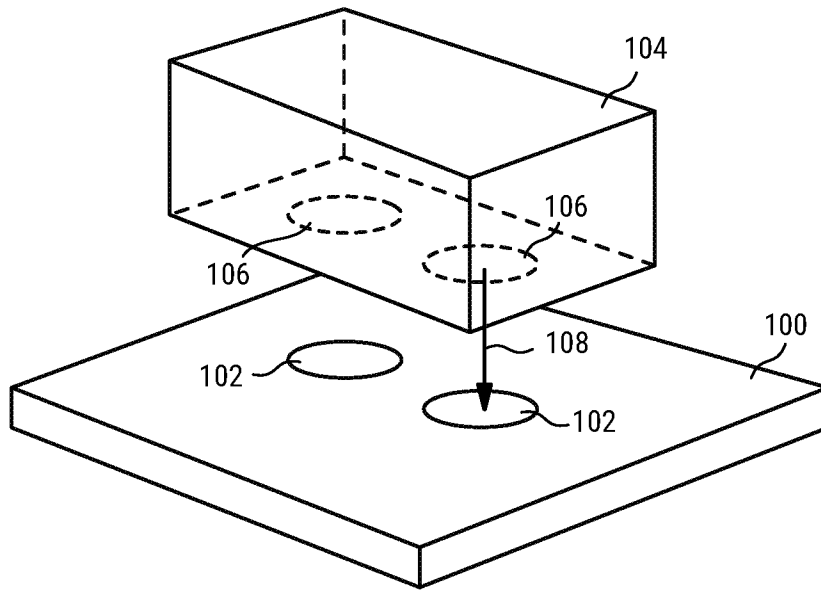


FIG. 1

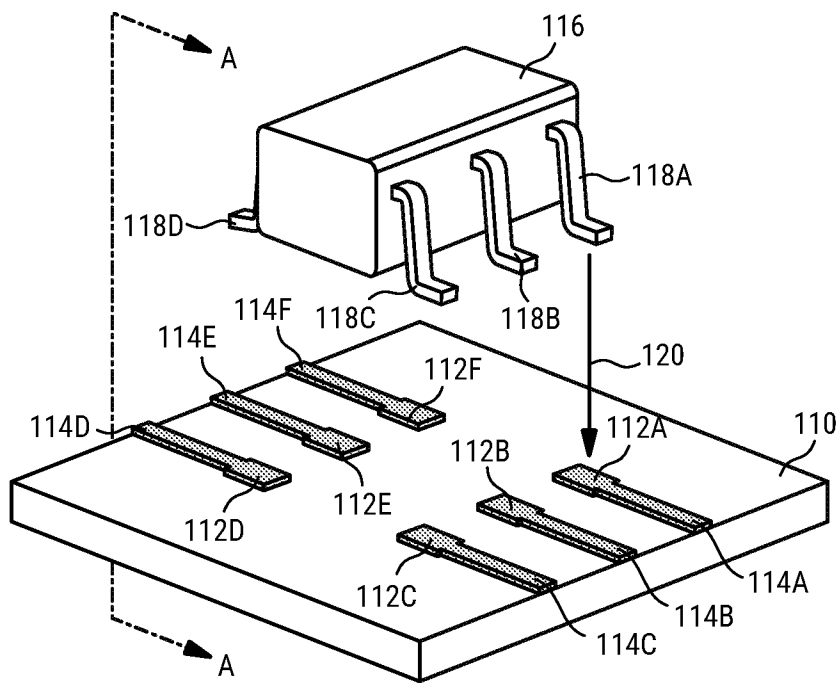


FIG. 2

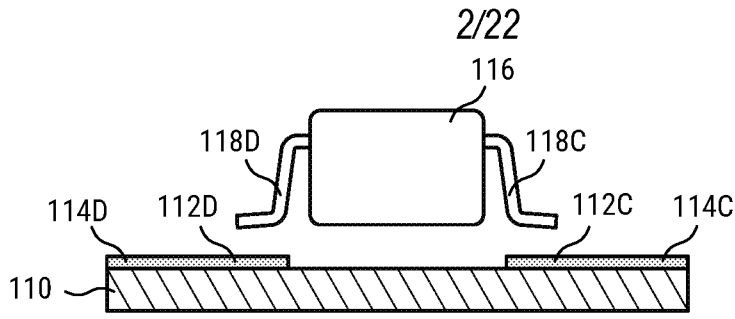


FIG. 3A

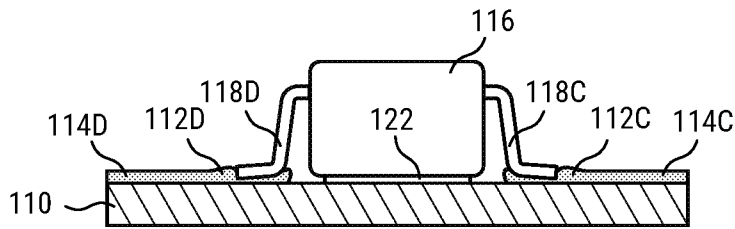


FIG. 3B

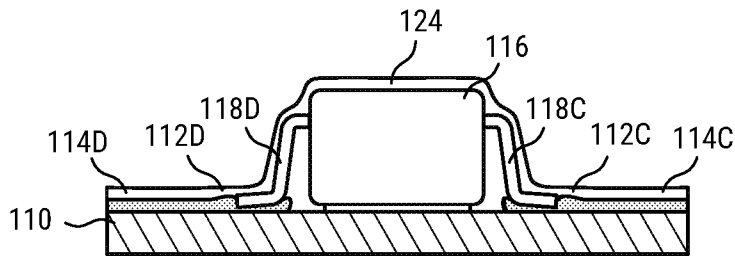


FIG. 3C

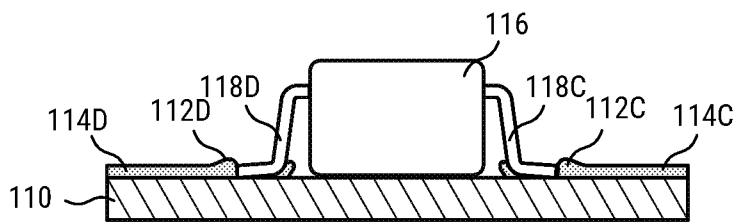


FIG. 3D

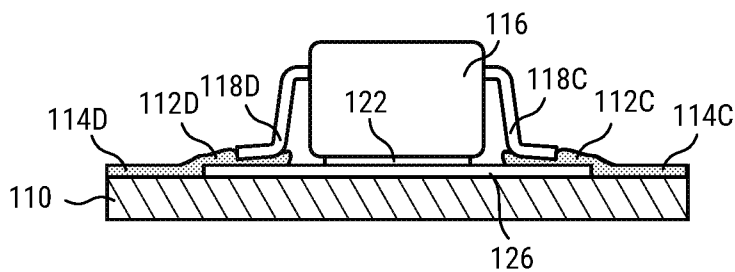


FIG. 3E

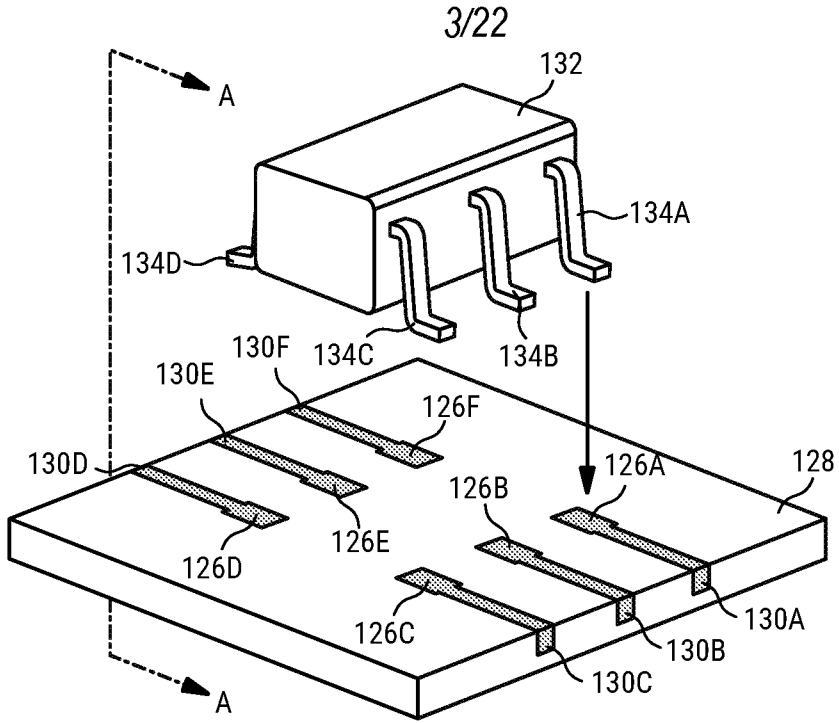


FIG. 4

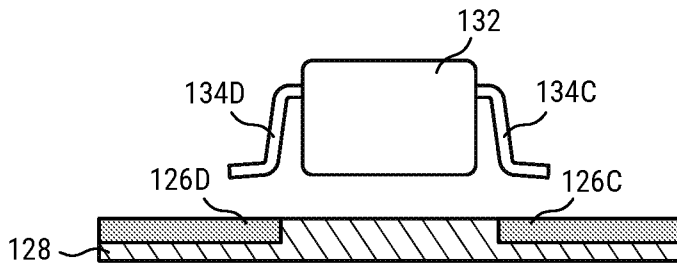


FIG. 5A

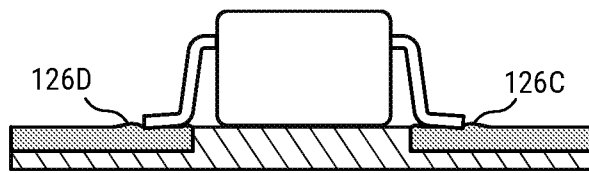


FIG. 5B

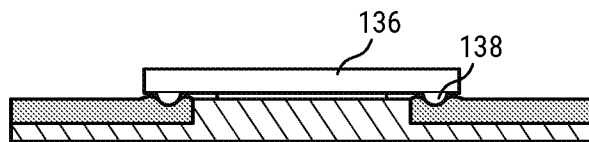


FIG. 5C

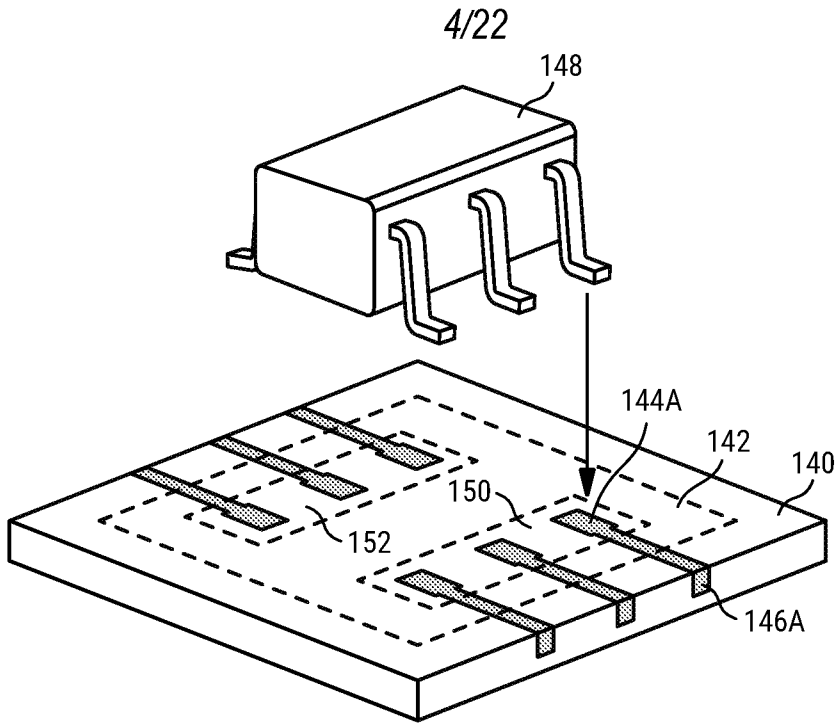


FIG. 6

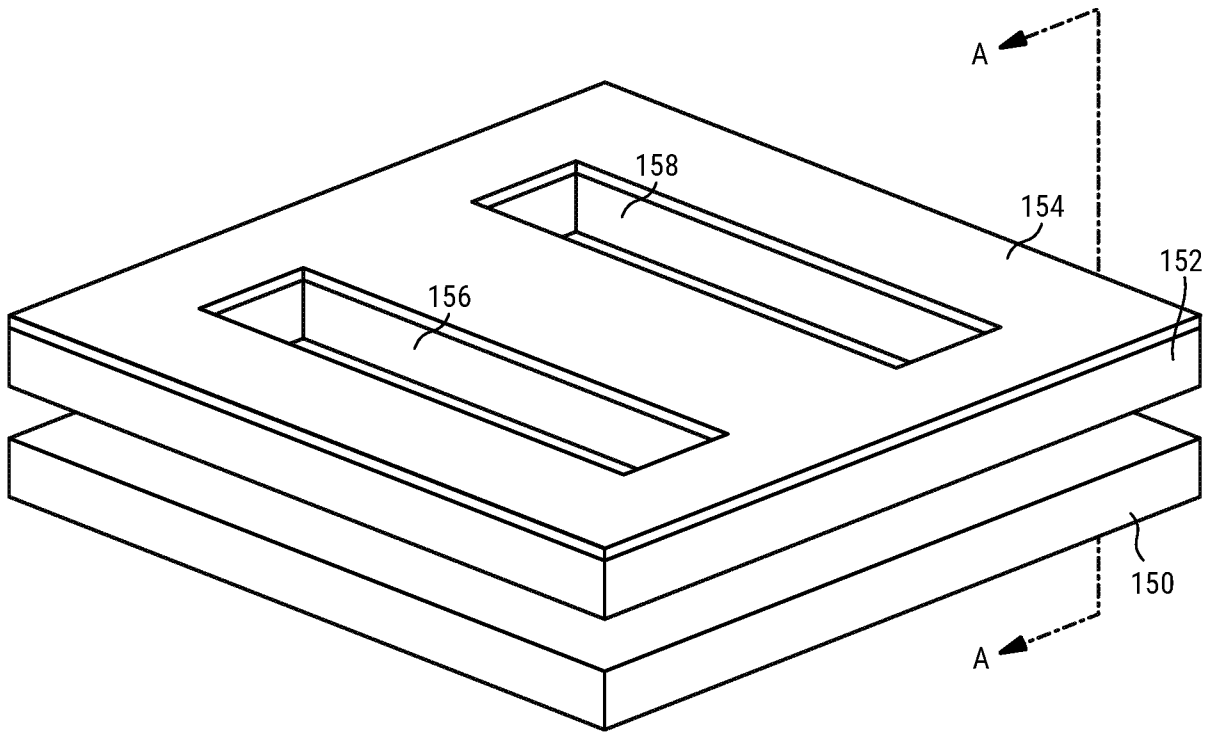


FIG. 7A

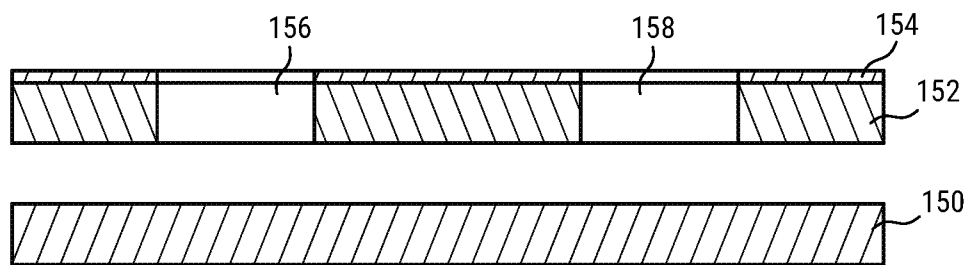


FIG. 7B

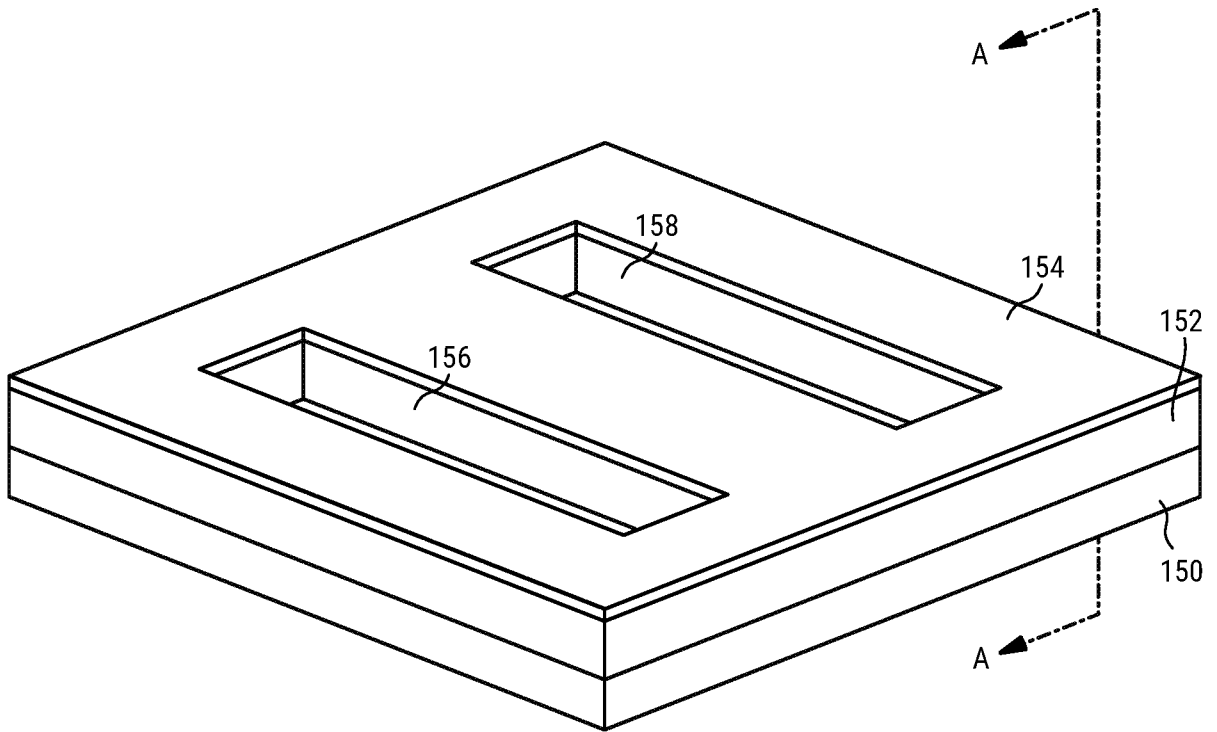


FIG. 8A

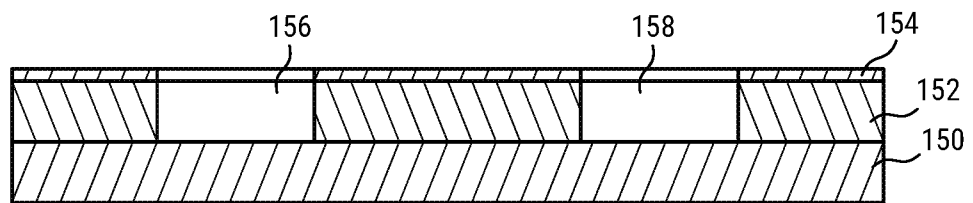


FIG. 8B

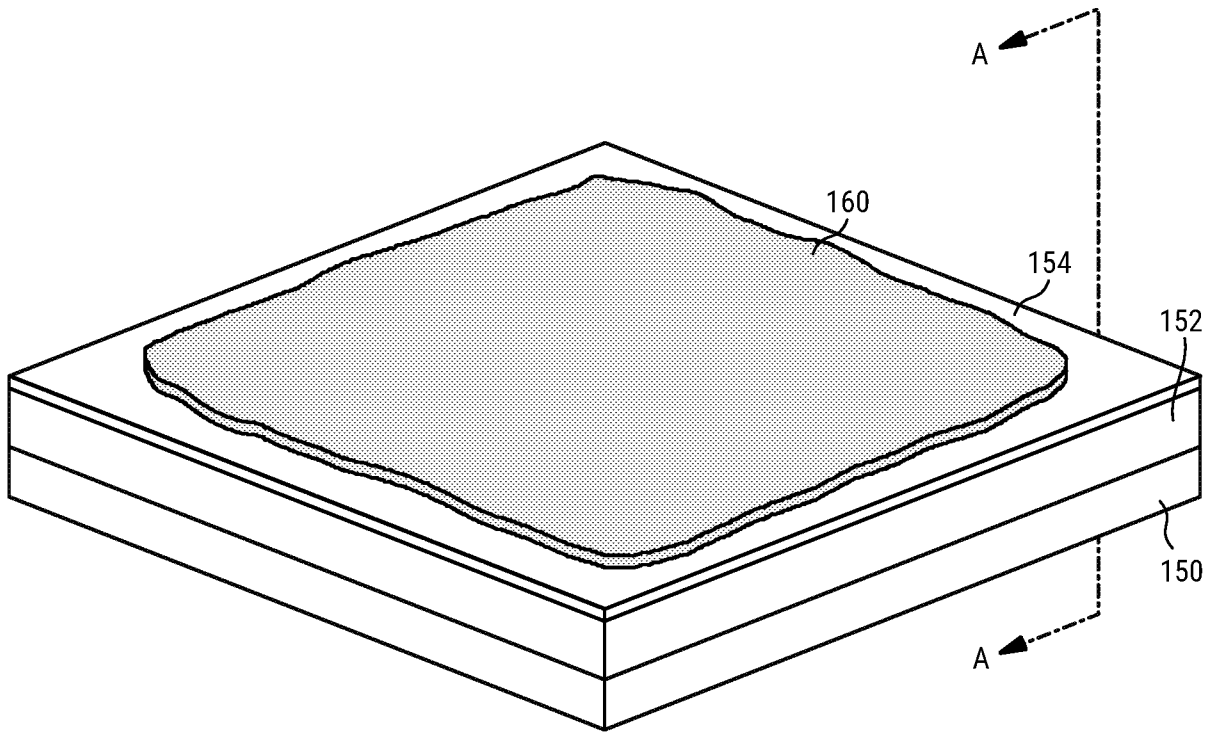


FIG. 9A

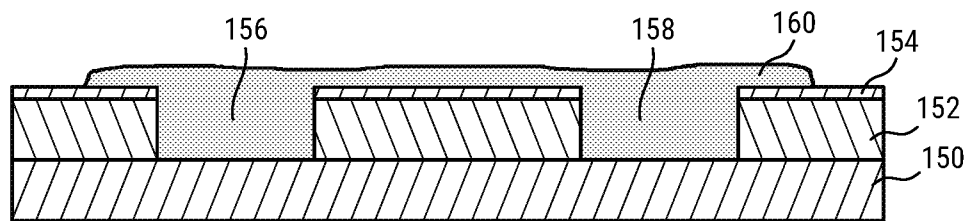


FIG. 9B

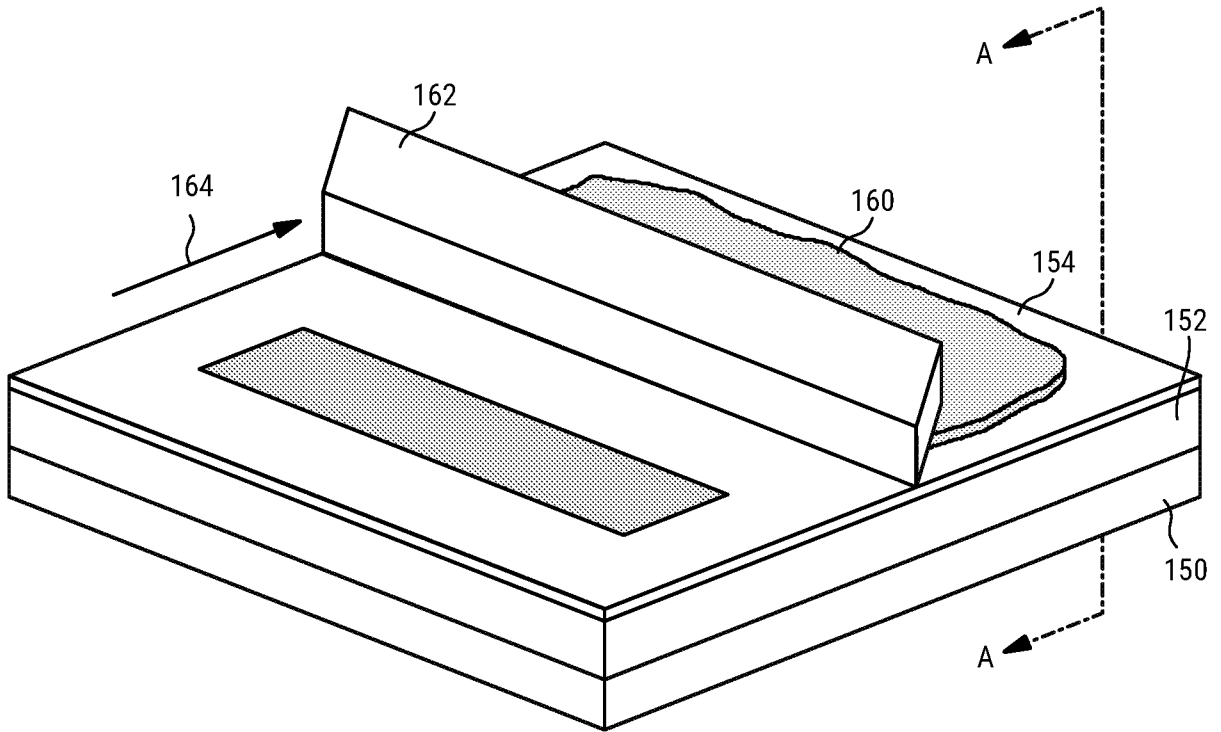


FIG. 10A

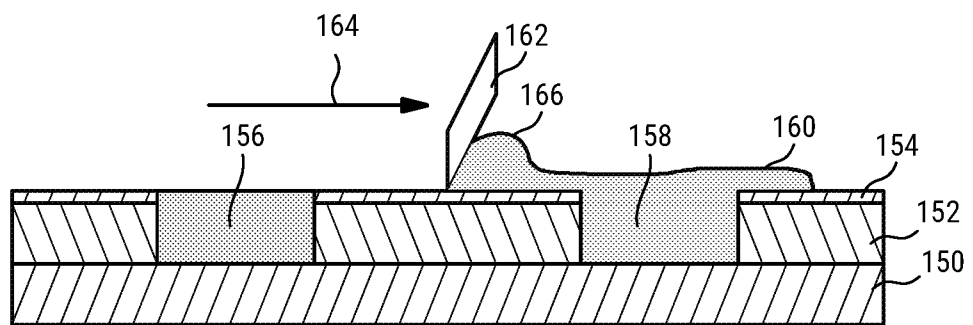


FIG. 10B

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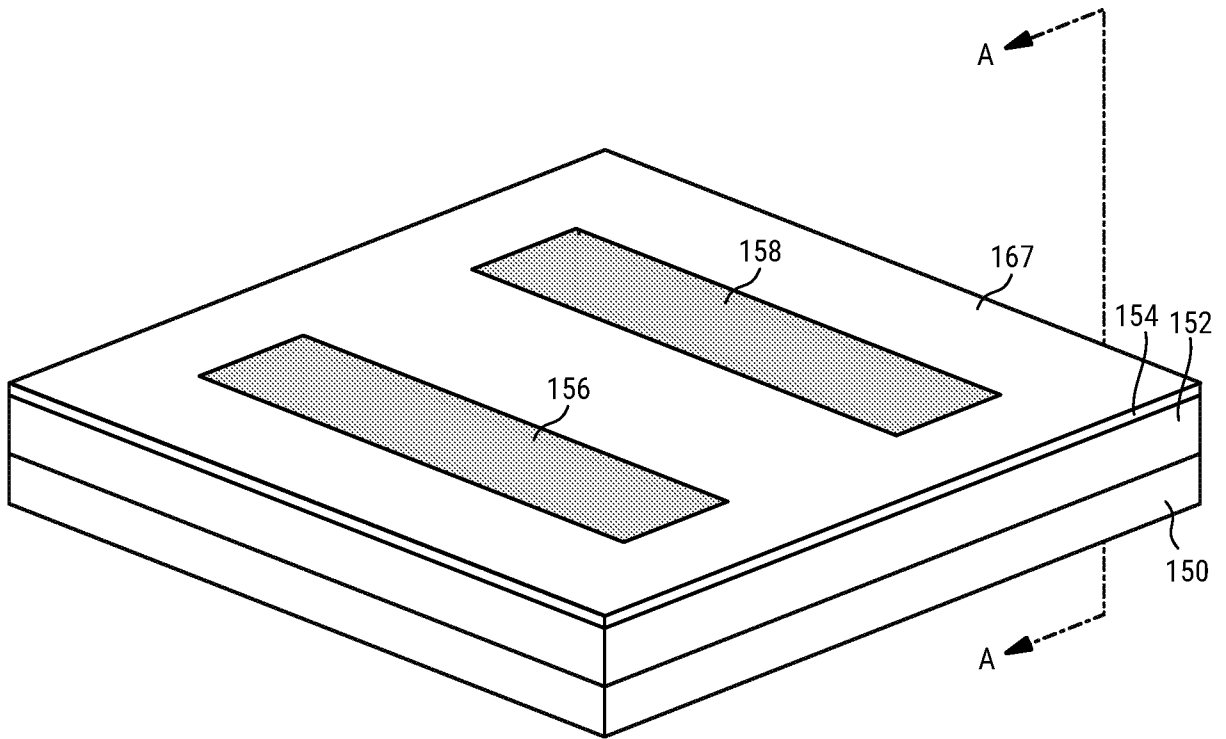


FIG. 11A

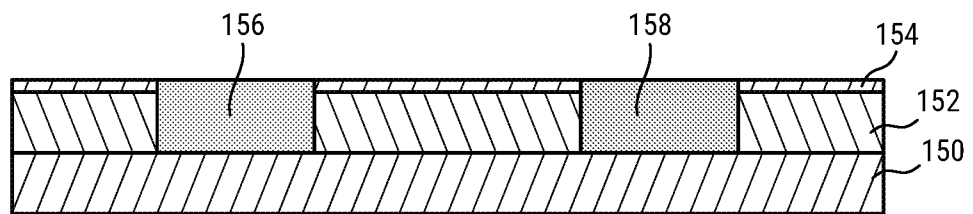


FIG. 11B

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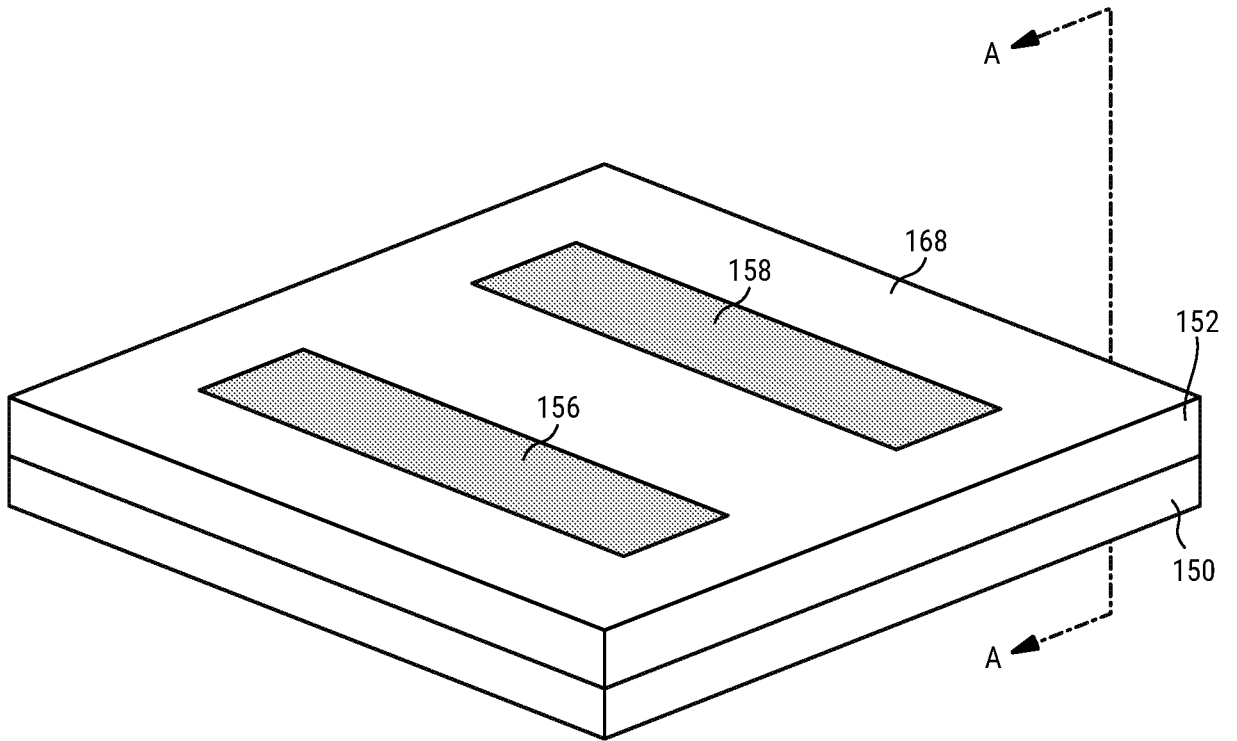


FIG. 12A

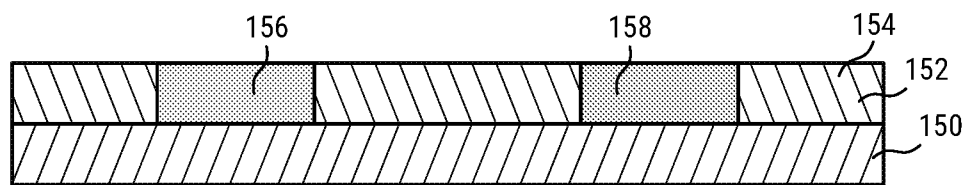


FIG. 12B

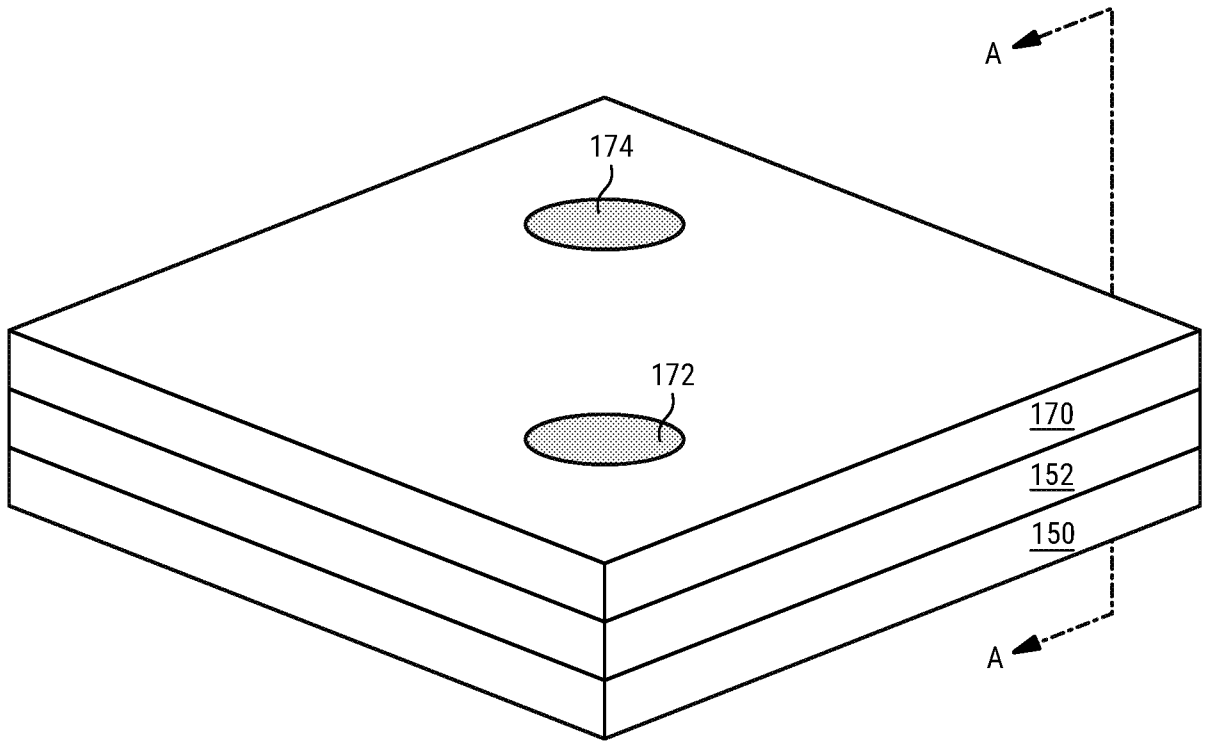


FIG. 13A

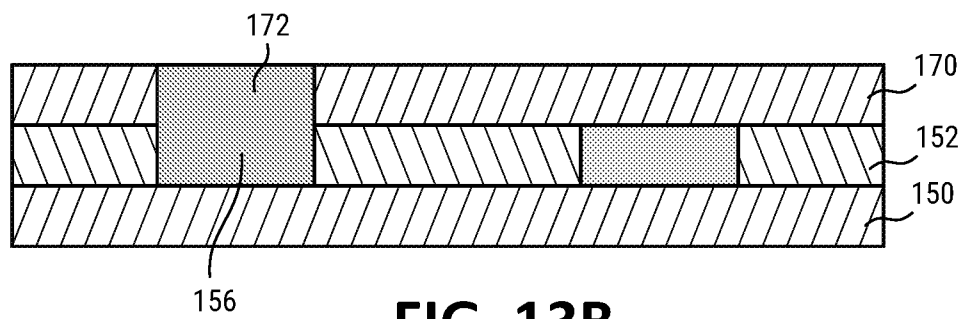


FIG. 13B

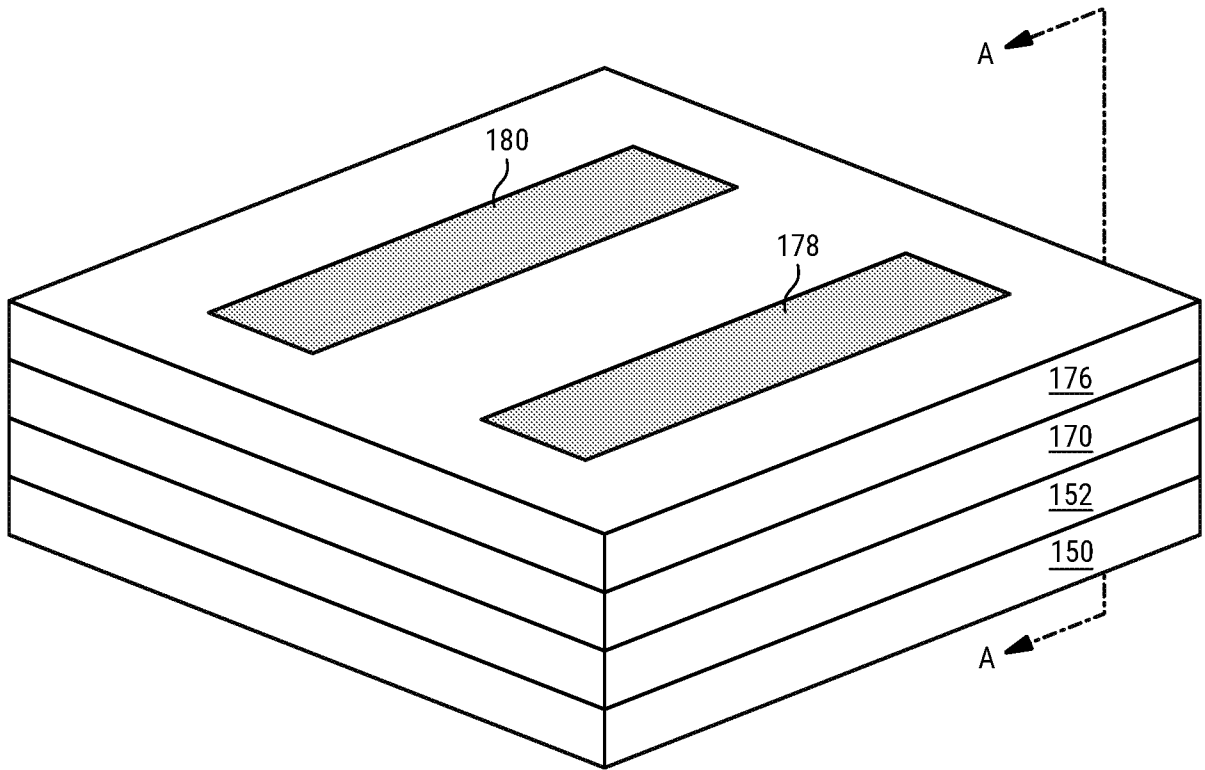


FIG. 14A

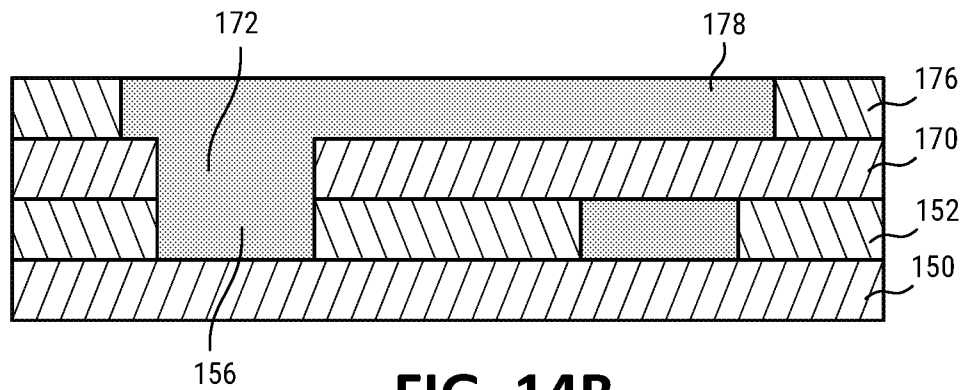


FIG. 14B

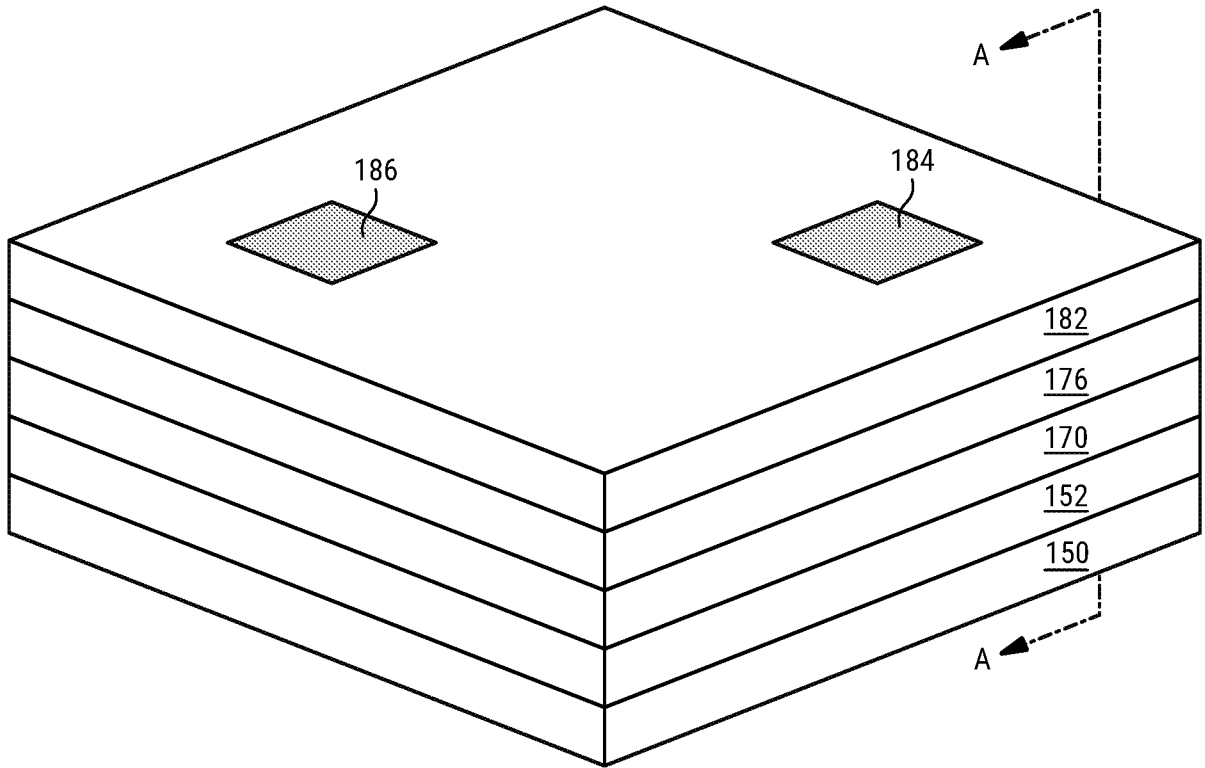


FIG. 15A

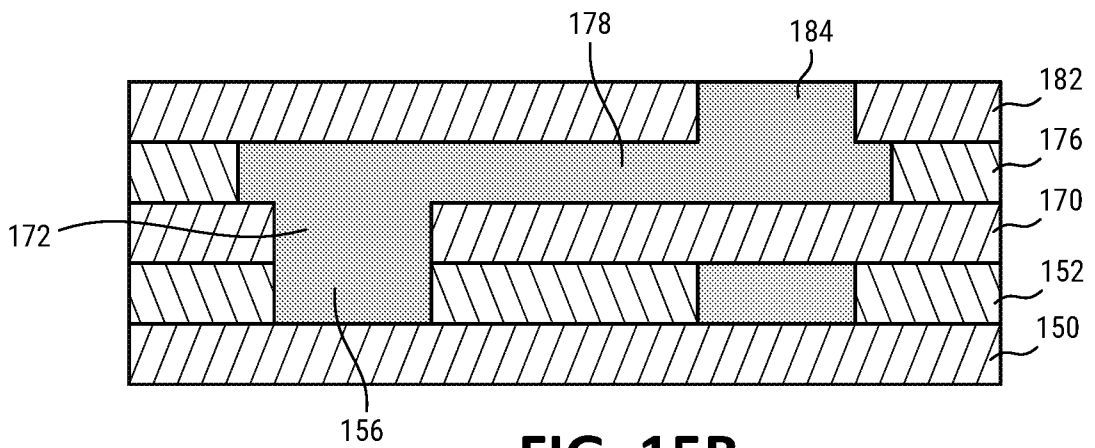


FIG. 15B

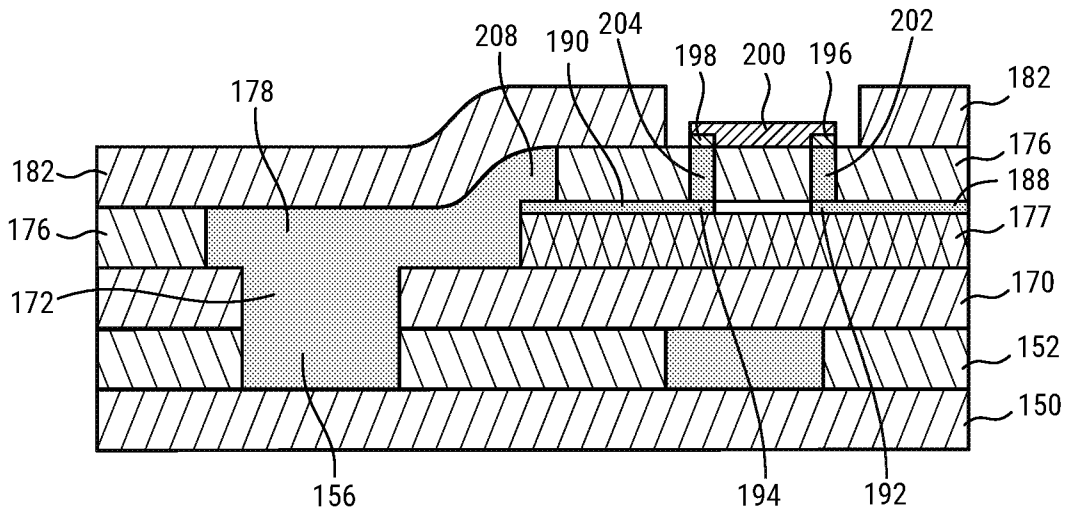


FIG. 16

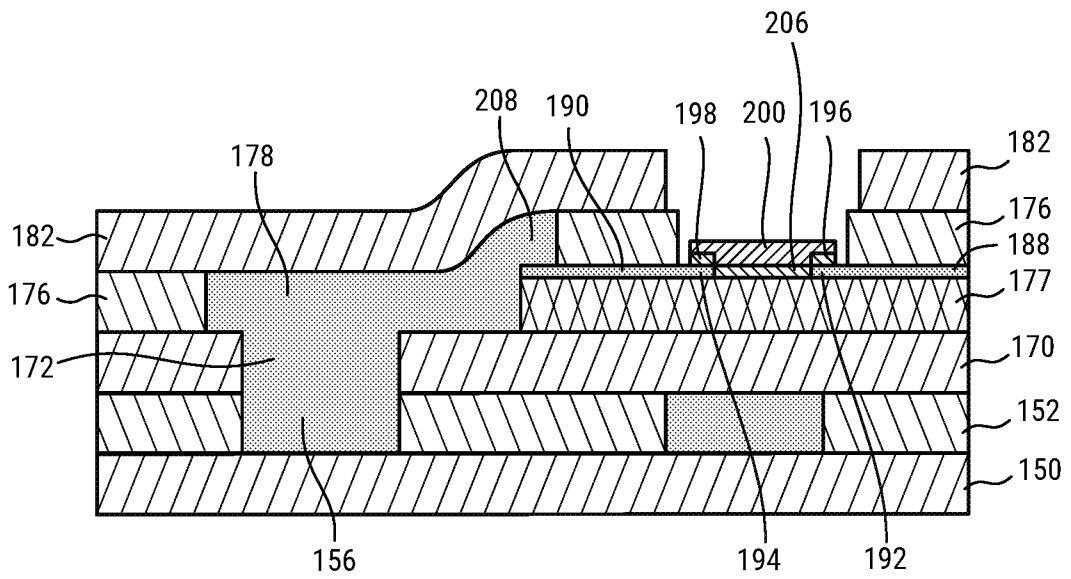


FIG. 17

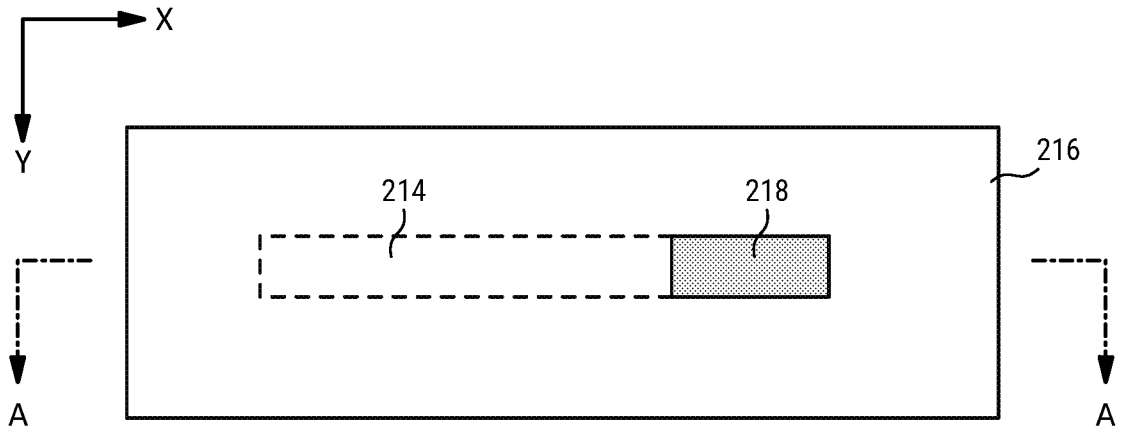


FIG. 18

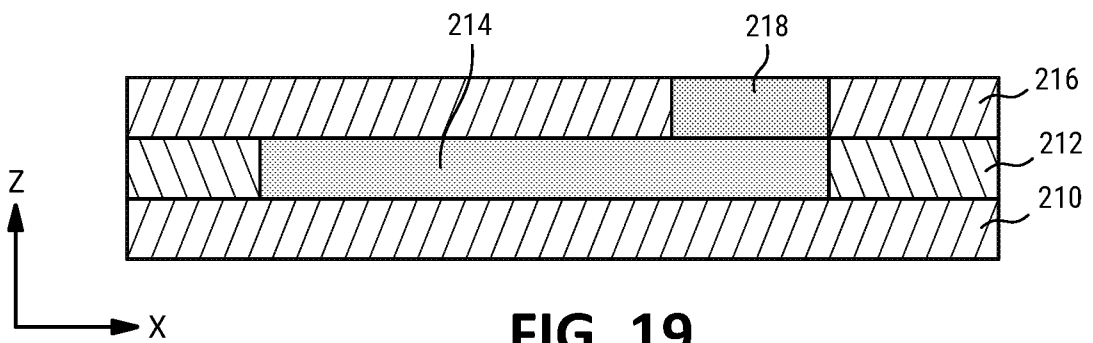


FIG. 19

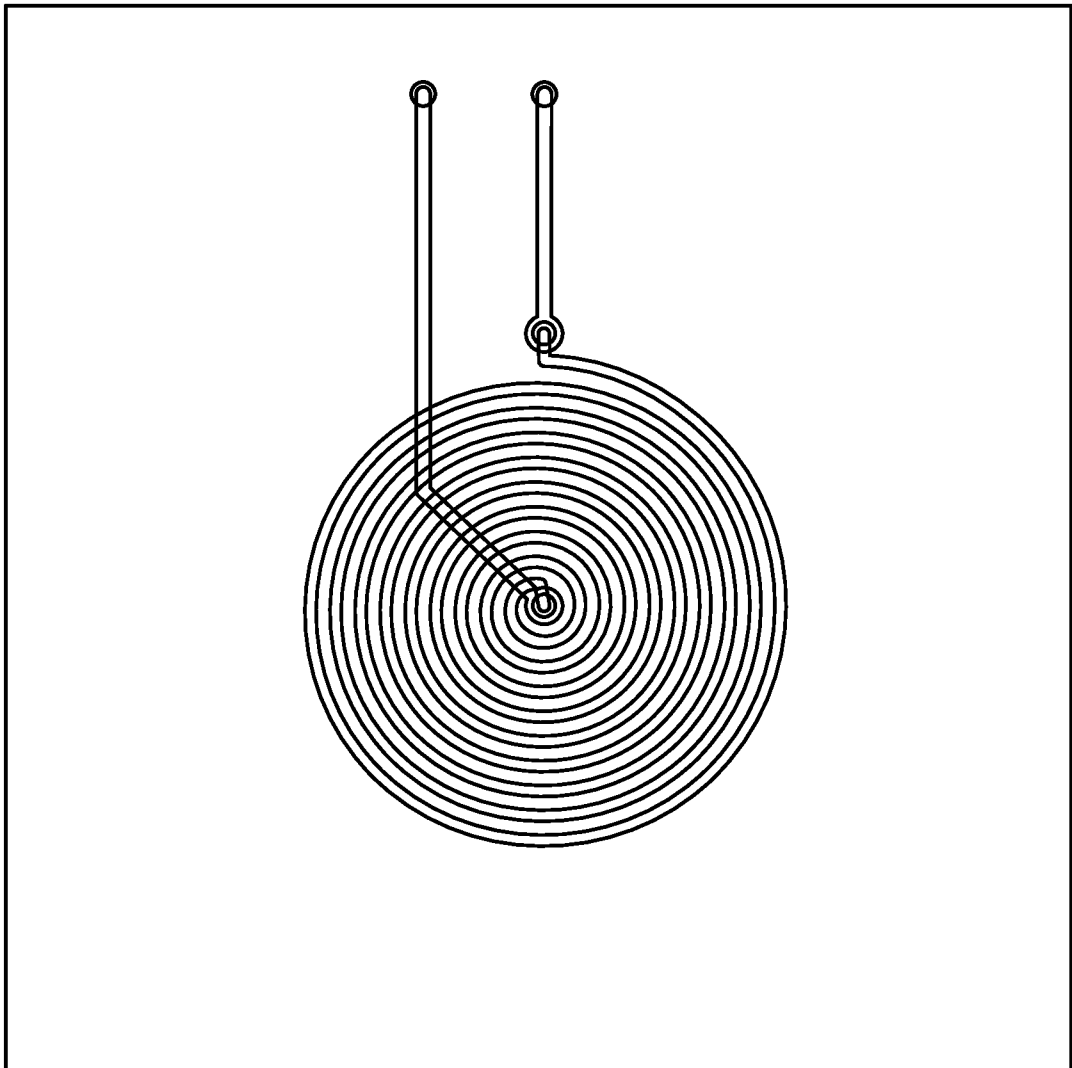


FIG. 20

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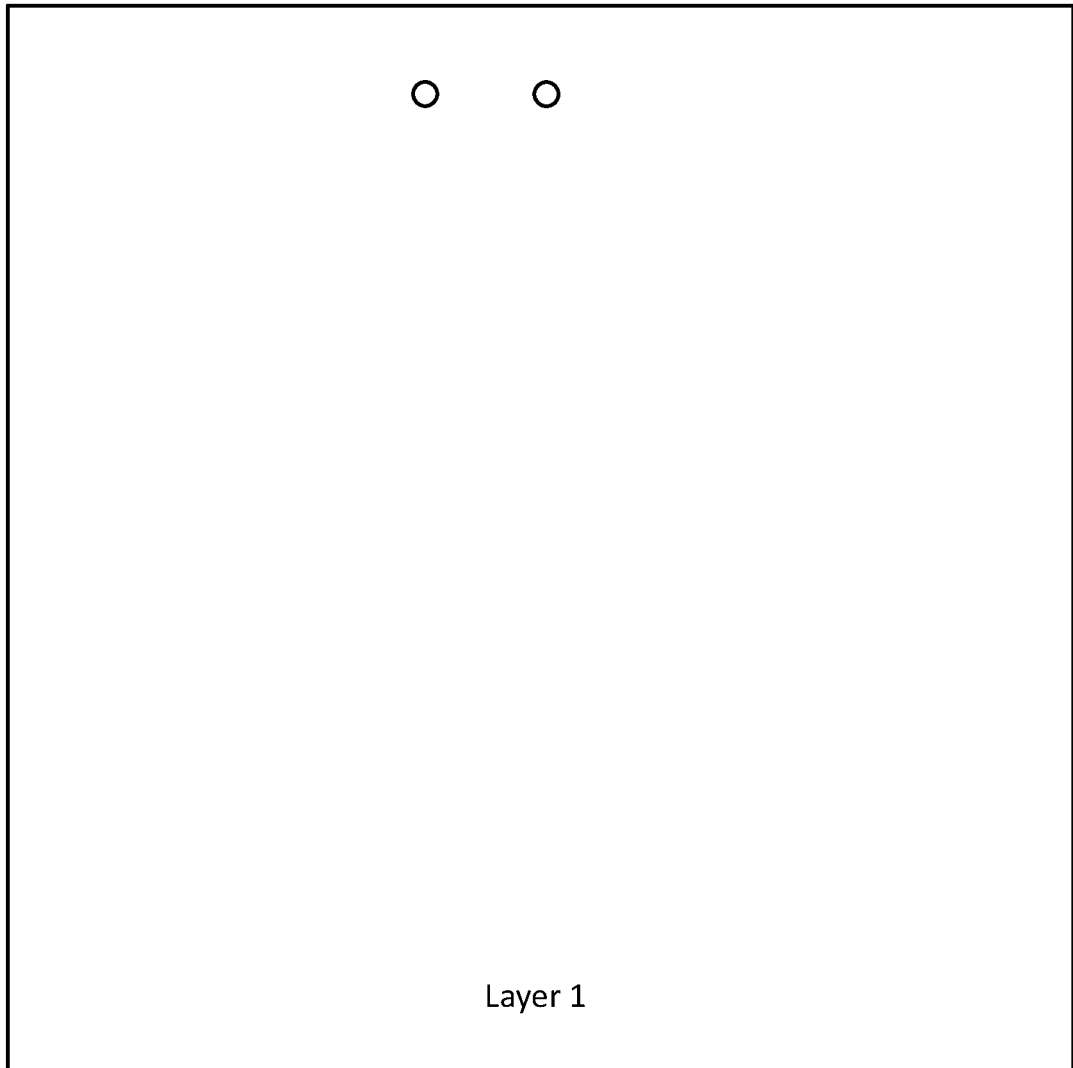


FIG. 21

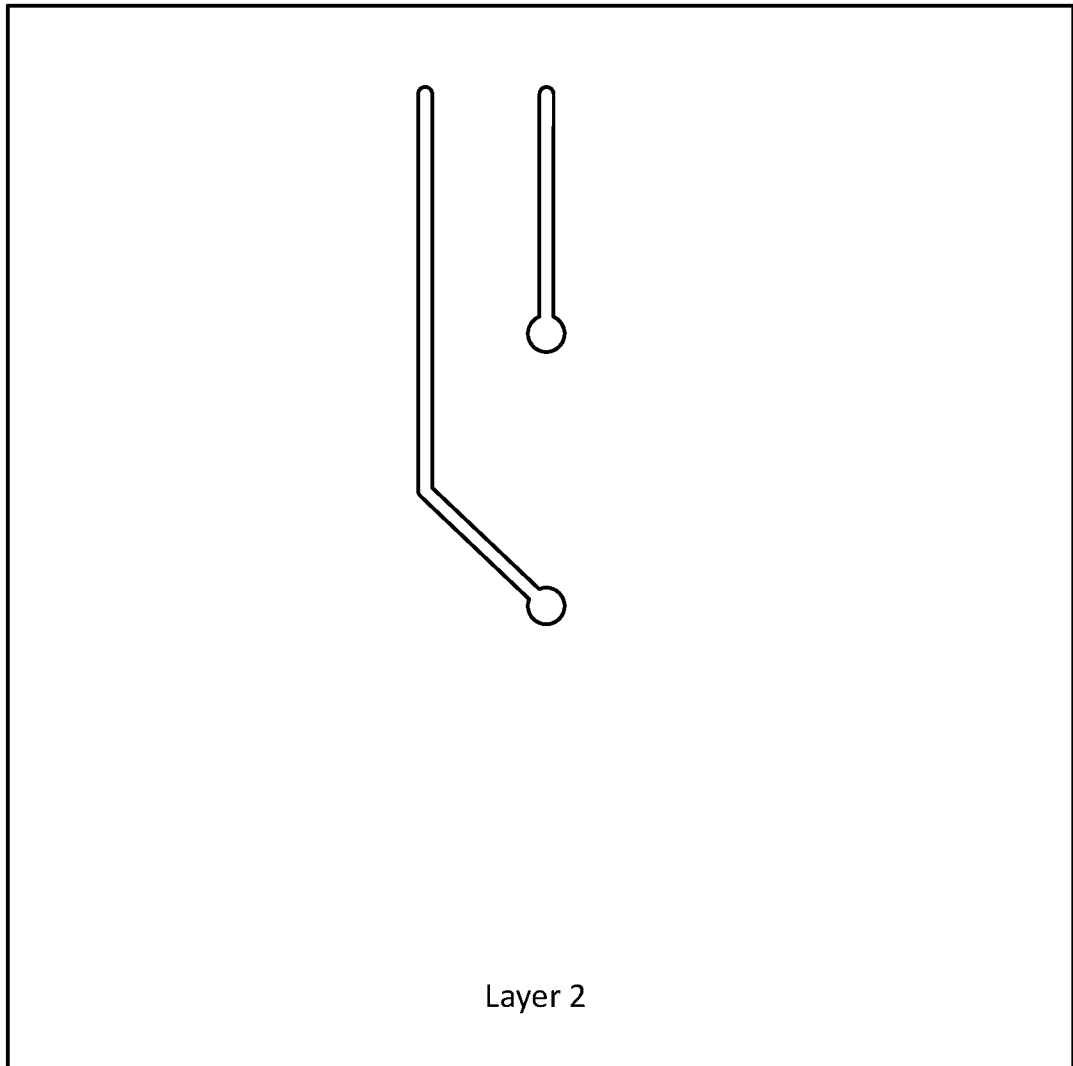


FIG. 22

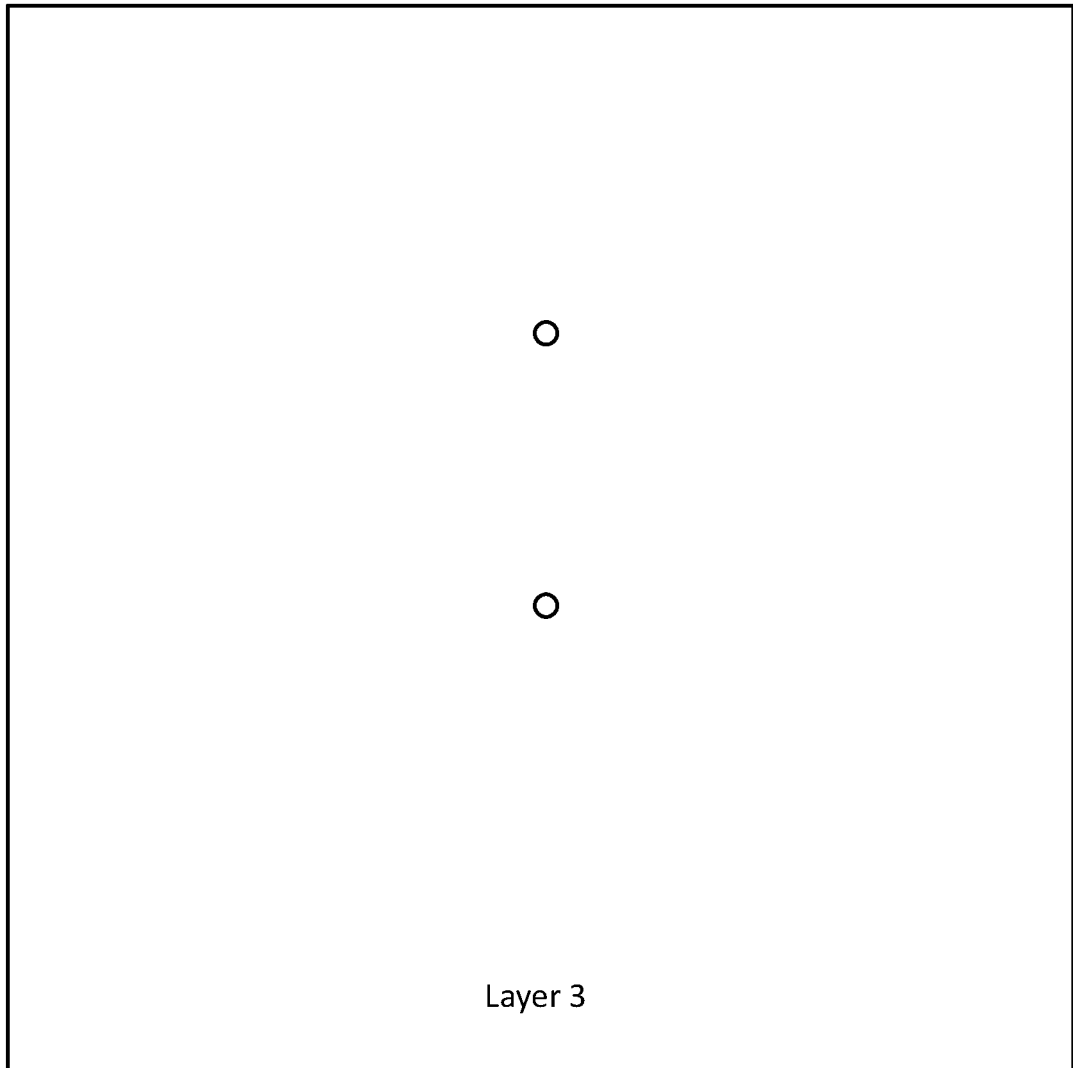


FIG. 23

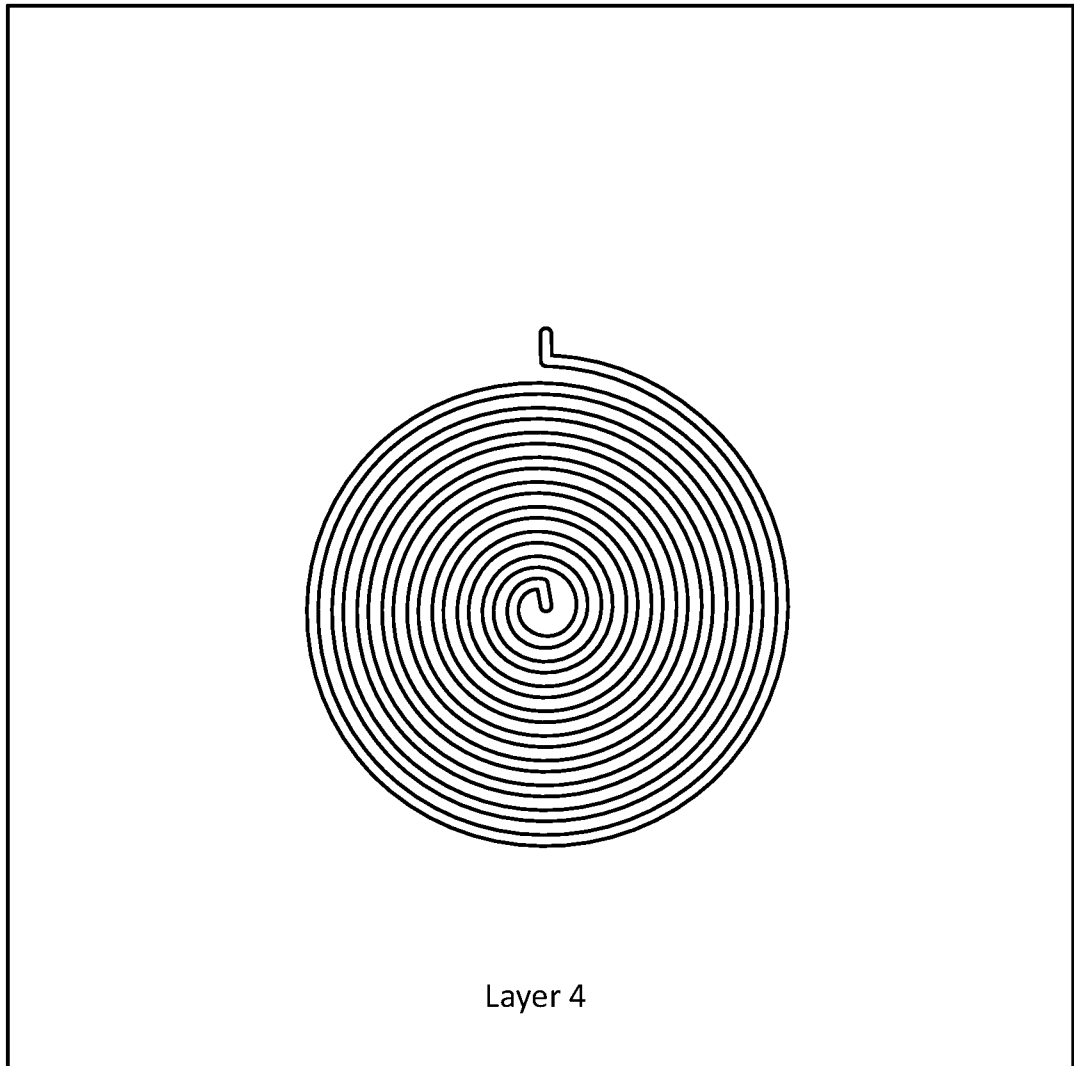


FIG. 24

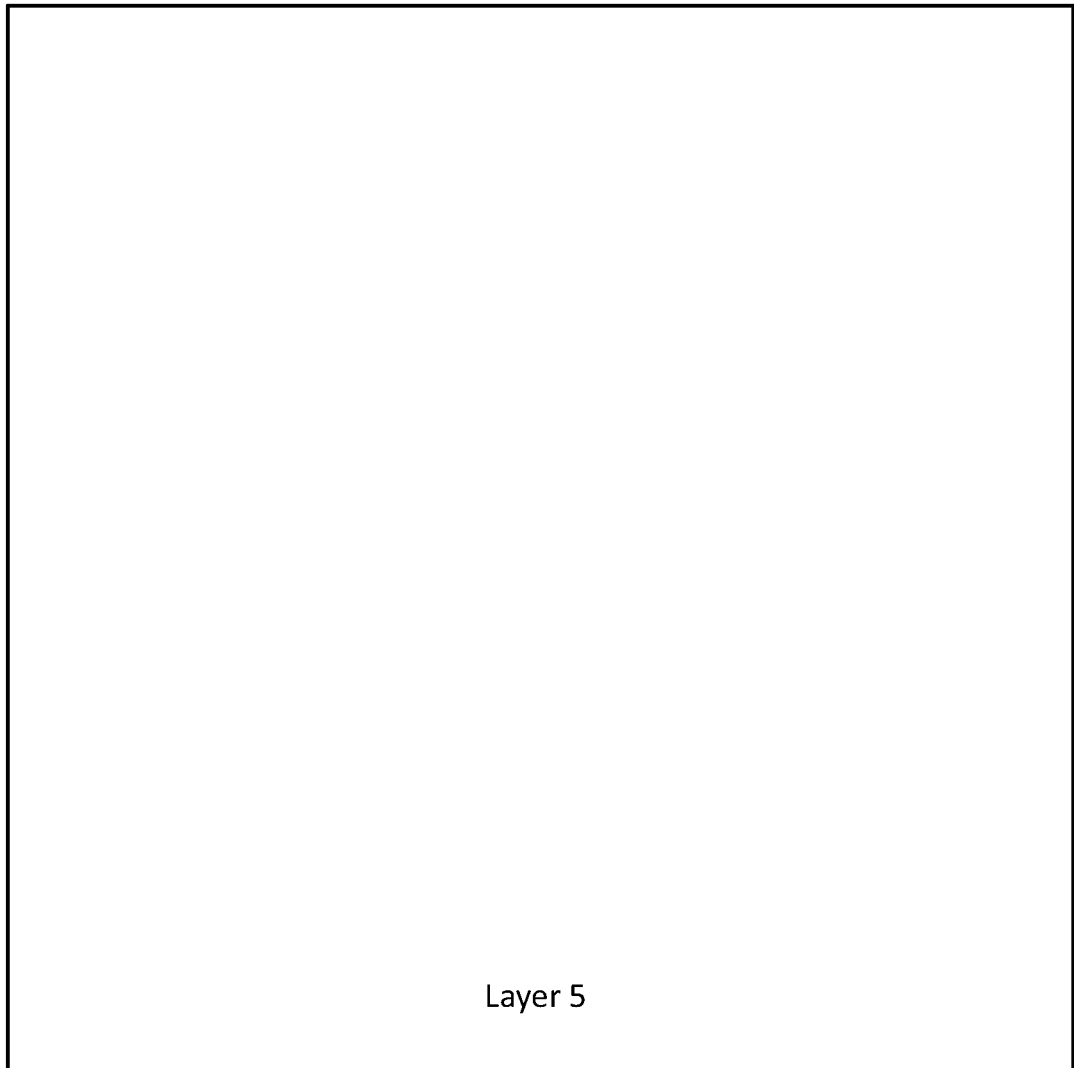


FIG. 25

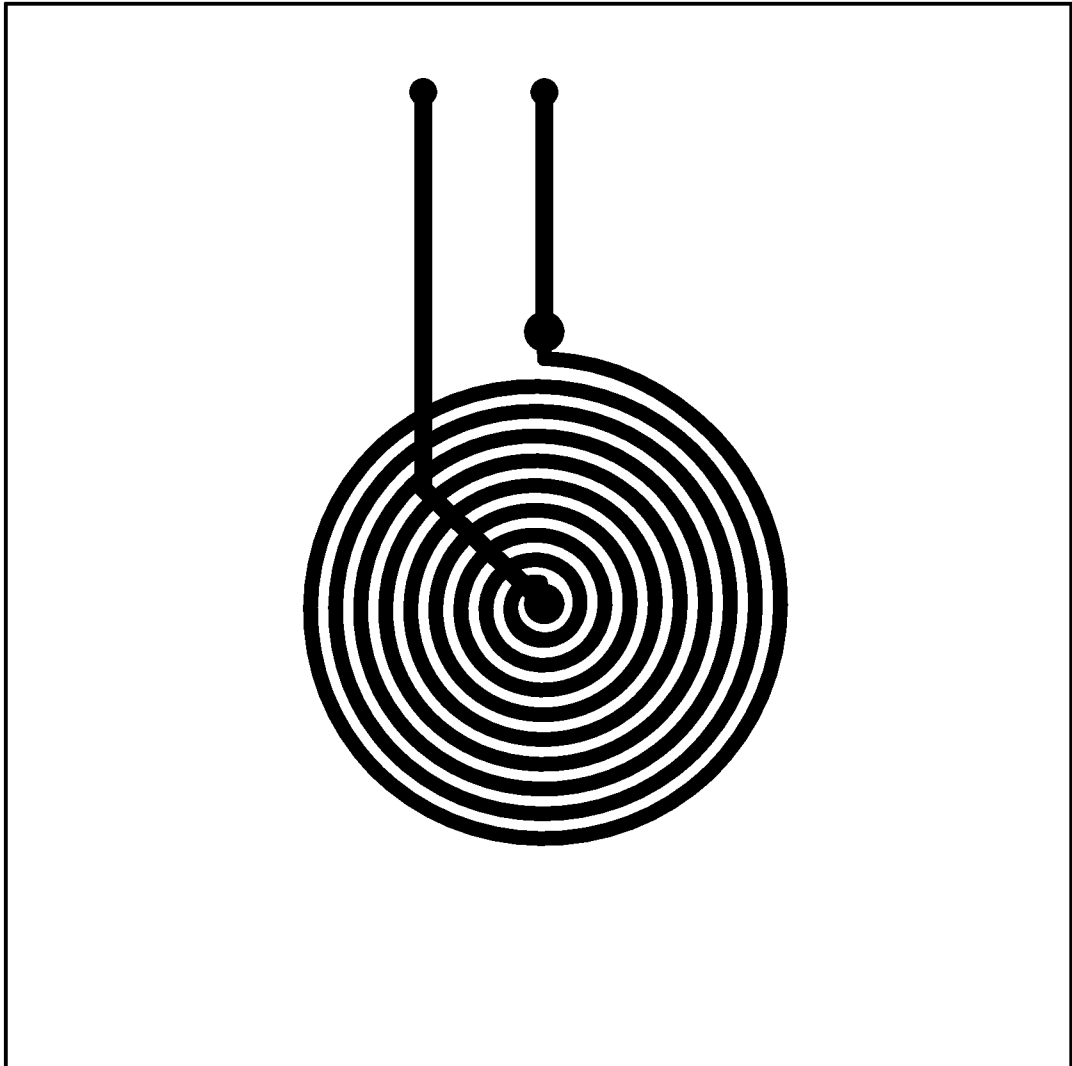


FIG. 26

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/020920

A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - G01R 27/26; G01D 5/12; G01D 5/14; G01D 5/20 (2021.01) CPC - G01R 27/26; G01D 5/12; G01D 5/14; G01D 5/20 (2021.05)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) see Search History document		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched see Search History document		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) see Search History document		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 2017/0323714 A1 (U.S. ARMY RESEARCH LABORATORY ATTN: RDRL-LOC-I) 09 November 2017 (09.11.2017) entire document	13, 14 — 1-3, 8-12, 15, 16
X — Y	US 5,913,830 A (MILES) 22 June 1999 (22.06.1999) entire document	17, 18 — 19, 20
Y	US 2005/0268699 A1 (PAPAKOSTAS et al) 08 December 2005 (08.12.2005) entire document	1-3, 8-12
Y	US 2004/0073137 A1 (LLOYD et al) 15 April 2004 (15.04.2004) entire document	15, 16
Y	US 2003/0009087 A1 (KEIRSBILCK) 09 January 2003 (09.01.2003) entire document	19, 20
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 15 May 2021		Date of mailing of the international search report JUN 02 2021
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300		Authorized officer Harry Kim Telephone No. PCT Helpdesk: 571-272-4300