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(72) Inventor BRUCE JAMES ROGERS

(19)

(54) IMPROVEMENTS IN DATA RECOVERY APPARATUS

(71) We, SPERRY RAND CORPORATION, a Corporation organised under the laws of the State of Delaware, United States of America, of 1290 Avenue of the Americas, New York, New York 10019, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to data recovery apparatus in which a phase-locked oscillator is employed to track an input signal.

The use of phase-locked oscillators in digital data processing systems is well known. In such systems the phase-locked oscillator serves to track input data pulses, supplied for example from a magnetic read head, for the purpose of recovering the recorded data. It is generally desired that the data bits be recorded as densely as possible in the interest of increasing the storage capacity of the recording medium. As a consequence of this dense storage or high packing density, the read pulses representative of the respective data bits may be shifted from their appropriate positions relative to one another. Bit shift is caused by an interaction of each read pulse with adjacent read pulses. The amount of bit shift which may occur is dependent on the packing density and the data pattern. In the case of a data pattern where the pulses are uniformly or periodically spaced from one another, the bit shift, if any, is usually inconsequential. On the other hand, where the data pattern is non-uniform or aperiodic, the individual pulses are shifted in dependence on both the nominal spacing between pulses and the difference in spacing of each pulse from the preceding and following pulses with the bit shift being greater for relatively closely spaced pulses and less for relatively widely spaced pulses having the same space differential.

In recognition of the bit shift problem, the development of the magnetic data recording and recovery art has been concerned with the generation of encoding techniques which not only reduce the bit shift but also afford self-clocking for eliminating the need for a separate clock track on the recording medium. NRZ code, for example, which is characterised by a change from one signal level to another on the occurrence of a one data bit following a zero data bit and by a change back to the original signal level when a zero follows a one, is not capable of self-clocking because of the long interval which exists between signal transitions for a succession of either ones or zeros. Phase modulation (PM) code, which is characterized by a signal transition in one direction for a one bit and a signal transition in the opposite direction for a zero bit, assures the frequency occurrence of signal transitions and therefore is capable of self-clocking. However, signal transitions are also required between ones and zeros to assure that the one and zero signal transitions are made in the proper direction. The need for these additional signal transitions intermediate the data bit transitions aggravates the bit shift problem. Frequency modulation (FM) code is characterized by advantages and limitations similar to those of PM code. Another encoding technique commonly known as modified frequency modulation (MFM) eliminates the transitions between data bits and also avoids long intervals without any transitions, thereby affording the advantages of both high packing density and self-clocking. A variation of the MFM code known as doubly modified frequency modulation (M^2FM) also affords both of these advantages and is preferred for one reason or another in some instances.

In both MFM and M^2FM encoding systems, one bits are recorded and reproduced at one time in a bit cell or interval, for instance at the centre thereof, while zero bits are recorded and reproduced in accordance with specific encoding rules so as to occur at another time in the bit cell, for instance, at the leading or trailing edge.

The specific encoding rules determine those zeros which are recorded and those which are not recorded. In other words, zeros are recorded only as necessary to achieve self-clocking. Upon read-out from the recording medium, both the ones and the recorded zeros are reproduced, so the data recovery apparatus must operate in a manner to respond to the reproduced ones and disregard the reproduced zeros.

The present invention will be described in relation to recovery of M²FM encoded data which will be explained subsequently in greater detail by reference to the drawings provided herewith for use in conjunction with the description of the preferred embodiment. In any event, from the foregoing comments concerning bit shift and a scrutiny of the accompanying drawings, it will be appreciated, as is indeed the case, that one bits of M²FM code tend to be shifted more than zero bits. This characteristic of the bit shift of M²FM encoded data can be used to advantage for enhancing the data recovery.

In a data recovery system employing a phase-locked oscillator, the oscillator functions to provide a reference signal which is fed back for phase comparison with a signal representing the input data bits to control the frequency of the oscillator such that it tracks the input signal. The oscillator thus inherently generates a data recovery gating signal. This gating signal is typically symmetrical, that is, it has a fifty percent duty cycle, so that it is at one level half the time in each cycle for gating or recovering one bits and is at another level for the remainder of each cycle during the time when zero bits may be present. By the use of appropriate logic circuits responsive to the gating signal, zero bits are blocked so that the recovered signal is representative only of the one bits present in the originally recorded data pattern. In the case of M²FM code where it is known that one bits tend to be shifted more than zero bits, it has been recognized that data recovery can be improved by allocating more than fifty percent of the data recovery gating signal cycle to recovery of one bits and proportionately less to the interval in which zero bits may be present. This is accomplished by the provision of an asymmetrical data recovery gating signal. Heretofore, systems operating in this fashion have been constructed with analogue circuits coupled in the phase-locked oscillator feedback path, with the attendant requirement for precision components to achieve desired accuracy, thereby making the systems complex and expensive to produce and maintain. The present invention provides a system comprising digital components for producing the phase comparator reference signal and asymmetrical data recovery signal, which reduces system complexity, with a concomitant reduction in manufacturing and maintenance costs.

According to the present invention a data recovery apparatus includes a counter to count output pulses from a variable-frequency oscillator, a logic circuit which supplies, in response to an output signal from the counter and a signal indicating the presence of a data pulse in an input data pulse stream, a reference signal to a comparator circuit which compares the timing of the reference signals with the timing of the data pulses thereby to drive a control signal for the variable-frequency oscillator to cause the oscillator to synchronize with a harmonic of the fundamental frequency of the input data pulse stream, and means deriving a data recovery signal from an output signal of the counter and applying it to an output gating circuit to provide a data recovery window for significant bits of the input data pulse stream.

The invention will be further described by way of example with reference to the accompanying drawings, in which

Figure 1 is a block diagram of part of a data recovery apparatus incorporating the present invention system,

Figure 2 shows the input data waveform corresponding to the illustrated data pattern,

Figure 3 shows various waveforms useful in explaining the operation of the invention,

Figure 4 shows the phase-locked oscillator of Figure 1, showing the logic block thereof in greater detail, and

Figure 5 is a table illustrating the binary count notation for the repetitive decimal count used in the preferred embodiment.

The preferred embodiment of the invention will be described with reference to recovery of an M²FM encoded signal which may be obtained, for example, by read-out from a magnetic disc and supplied as an input data pulse stream to the data recovery apparatus shown in Figure 1. An illustrative M²FM encoded input data pattern and the related input data pulse stream are shown in Figure 2, from which it will be appreciated that 1 data bits are represented by a pulse at the centre of a timing interval (bit cell) and 0 data bits are represented, in the present example, by a pulse at the start of a timing interval. Each 1 data bit is represented by a pulse but 0 data bits are represented by a pulse only when neither a 1 bit n or a pulse representing a 0 bit is present in the immediately preceding timing interval. The minimum interval between pulses is T which occurs for successive 1 bits, and the maximum interval

between pulse is 2.5 T which occurs for a 1 bit following three successive 0 bits. Intermediate pulse intervals of 1.5 T and 2 T also occur in accordance with the input data pattern.

Refer now to Figures 1 and 3 where the latter depicts waveforms occurring at various points in phase-locked oscillator 6 relative to the first four timing intervals from left to right in Figure 2, only a part of the first and fourth timing intervals being shown in Figure 3. The M^2FM encoded input data pulse stream is applied to input terminal 7 of the phase-locked oscillator. Monostable flip-flop 8 serves to stretch each input data pulse to provide positive and negative elongated pulses at the Q and $\overline{Q}$ terminals thereof respectively. These elongated pulses have a duration equal to one-half the nominal value of T. During the data recovery operation the $\overline{CLAMP}$ signal on terminal 7' is at a high level and thus inactive so the negative elongated pulses at the $\overline{Q}$ terminal of flip-flop 8 feed through a negated-input OR gate 9 to provide positive phase comparator variable input pulses as shown in Figure 3, at the VI input terminal of phase comparator and charge pump 10. Phase comparator and charge pump 10 is a Motorola (Registered Trade Mark) model MC4044 integrated circuit coupled as shown in the drawing. The positive elongated pulses provided at the Q terminal of flip-flop 8 are applied to logic circuit 11 for reasons which will be described subsequently with reference to Figure 4.

Voltage controlled oscillator 12 is controlled to run at a frequency which is a harmonic of the frequencies corresponding to the T, 1.5 T, 2 T and 2.5 T spacings of the input data pulse stream. The oscillator output pulses are applied to the input terminal of counter 13 which is a four stage binary counter wired to count repetitively from zero to nine. The counter stages provide respective output signals at terminals A, B, C and D which vary in response to the applied oscillator output pulses in conventional binary fashion as shown in Figure 5. Logic circuit 11 functions in response to the counter output signals to provide a phase comparator reference input pulse via lead 14 and negated-input OR gate 15 to input terminal RI of phase comparator and charge pump 10 for each input data pulse received at input terminal 7 of the phase-locked oscillator. The phase comparator and charge pump 10 compares the time displacement between the trailing edges of the phase comparator variable input and reference input pulses to provide at the output of the phase comparator and charge pump a phase error signal representative of such time displacement. This error signal in turn is applied through filter 16 to control the frequency of voltage controlled oscillator 12. In accordance with conventional phase-locked oscillator operation, the gain and bandwidth of filter 16 are set during the data recovery operation to respond to long term drift of the input data pulse stream occurring over several cycles thereof and so as not to respond to instantaneous jitter as caused, for instance, by bit shift which was discussed hereinbefore.

It will be noted that the signal at counter terminal C is asymmetrical and has a 40/60 duty cycle. The 40 percent and 60 percent parts of the counter terminal C signal serve as data gating signals for 0 bits and 1 bits respectively. The 60 percent part of the counter terminal C signal which corresponds to the 1 bits to be recovered for the purpose of reproducing the input data pattern is typically referred to as the recovery window. The phase locked oscillator functions in a manner to keep the recovery window centered on the 1 data bits irrespective of frequency variations of the input data pulse stream which cause either an increase or decrease of the nominal spacings between the data bits. In like manner, the 40 percent part of the counter terminal C signal is kept centered on the 0 data bits. As indicated in Figure 3, the counter terminal C signal has a period T corresponding to the fundamental period of the input data pulse stream. If the frequency of the input data pulse stream decreases causing the spacings between the data bits to increase, voltage controlled oscillator 12 is varied to run at a lower frequency so that the period of the counter terminal C signal increases to correspond to the increased spacing between the data bits; but the 40 and 60 percent parts thereof remain at such percentages for the increased period. Likewise, if the frequency of the input pulse data stream increases causing the spacings between the data bits to decrease, the voltage controlled oscillator is varied to run at a higher frequency so that the period of the counter terminal C signal decreases to correspond to the reduced spacing between the data bits with the 40 and 60 percent parts again remaining at such percentages for the decreased period.

Recovery of the original input data pattern is accomplished by feeding the input data pulse stream on lead 17 to one input terminal of AND gate 18 and by feeding the counter terminal C signal on lead 19 through inverter 20 to the other input terminal of AND gate 18. Coincidence of the inverted 60 percent recovery window with the 1 bits causes those bits to be transmitted through AND gate 18 whereas the 0 bits are blocked. Since the 60 percent

recovery window occurs in the centre of each timing interval, the absence of a 1 bit in any interval is indicative of a 0 bit for those intervals.

The manner in which the phase-locked oscillator and particularly the feedback portion thereof, comprising the counter and logic circuits, functions to slave the 60/40 recovery gating signal to the input data pulses will now be described more specifically with reference to Figures 3, 4 and 5. It will be apparent that when the phase-locked oscillator is initially switched into operation, the desired time relationship between the data bits and the respective parts of the recovery gating signal may not occur, that is, the 1 bits and 0 bits may not be coincident with the 60 and 40 percent parts respectively of the recovery gating signal. The manner in which this lock-in is accomplished will be described hereinafter. For the moment, though, to maintain continuity with the preceding discussion, it will be assumed that lock-in has been achieved so the 1 bits are in the 60 percent part and the 0 bits are in the 40 percent part of the recovery gating signal. It will be further assumed that flip-flops 23, 24 and 26 are initially set such that the signals at the $\overline{Q}$ terminals thereof are high, and that voltage controlled oscillator 12 is running at a frequency ten times the frequency corresponding to the fundamental period T of the input data pulse stream. From the ensuing description, it will be appreciated that flip-flops 23 and 24 do in fact initially settle with a high level signal at the $\overline{Q}$ terminals thereof when the voltage controlled oscillator is running and no input data pulses are applied to the phase-locked oscillator, while the signal at the $\overline{Q}$ terminal of flip-flop 26 is low at counts 1 and 6 and high for all other counts. Now consider the data recovery operation commencing with the reception of input data pulse 21a which is representative of a 1 bit occurring in the centre of the 60 percent part of the recovery gating signal. For the assumed conditions, application of the input data pulse 21a to input terminal 7 triggers monostable flip-flop 8 producing at the $\overline{Q}$ terminal thereof an elongated negative pulse which is transmitted through the negated-input OR gate 9 to produce at the output thereof a positive phase comparator variable input pulse 22a which in turn is applied to terminal VI of phase comparator and charge pump 10.

The pulse produced at the $\overline{Q}$ terminal of flip-flop 8 and the phase comparator variable input pulse 22a both have a duration equal to one-half the nominal timing interval T. Application of input data pulse 21a to flip-flop 8 also produces at the Q terminal thereof a positive elongated pulse which is applied to the clock (CK) terminal of flip-flop 23. The positive going leading edge of this pulse drives the Q terminal of flip-flop 23 to a high signal level which in turn is applied to the J terminal of flip-flop 24. As indicated in the drawings, the leading edges of the input data pulse 21a and the related phase comparator variable input pulse 22a coincide with count one of the repetitive count of counter 13. The manner in which the count of one is aligned with the input data pulse will be explained more fully in conjunction with the subsequent description of the lock-in operation.

Proceeding now with the description of the operation in the data recovery mode, at the count of four the signal at counter terminal B switches from a high (1) level to a low (0) level thereby providing a positive going signal at the output of inverter 29 which is coupled via line 33 to the clock (CK) terminal of flip-flop 24 causing the signal at the $\overline{Q}$ terminal thereof to switch to a low level. This low level signal acts by way of line 34 to reset flip-flop 23 driving the signal at flip-flop 23 terminal Q low. The low level signal at the $\overline{Q}$ terminal of flip-flop 24 is also applied through the gate 15 to present a high level phase comparator reference input pulse 37a to terminal RI of phase comparator and charge pump 10. At a count of five, the signals at counter terminals A and C are high and the signal at counter terminal B is low. The high level counter signals at terminals A and C are applied to AND gate 36 in coincidence with the high level signal provided at the output of inverter 29 to produce at the output of AND gate 36 a high level signal which is applied through OR gate 32 to the D terminal of flip-flop 26. Thus, the next oscillator pulse, corresponding to count six, clocks flip-flop 26 driving the signal at the $\overline{Q}$ terminal thereof low. This low level signal, referred to in the drawings as a reference input control pulse, resets flip-flop 24 driving the signal at its terminal $\overline{Q}$ high and thereby terminating the phase comparator reference input pulse 37a. Now in this case where the input data pulse 21a has occurred at the centre of the 60 percent recovery window, the phase comparator variable and reference input pulses terminate simultaneously so the phase comparator and charge pump 10 acts to produce a signal level at the output of filter 16 to maintain voltage controlled oscillator 12 at its nominal frequency as indicated in Figure 3. The circuit operation is the same for input data pulse 21b which produces phase comparator variable input pulse 22b and phase comparator reference input pulse 37b which also terminate simultaneously as

a consequence of input data pulse 22b being located at the centre of its recovery window. Such action occurs because at the count of six the signal at the D terminal of flip-flop 26 becomes low whereupon clocking thereof at count seven drives the signal at the $\overline{Q}$ terminal thereof back to a high level. Then at the next count of zero the signals at counter terminals A, B, C and D are all simultaneously low and thus produce at the outputs of inverters 28, 29 and 30 simultaneous high level signals which are applied through AND gate 31 and OR gate 32 to provide a high level signal at the D terminal of flip-flop 26 in readiness for clocking thereof at the count of one occurring in coincidence with the reception of input pulse 21b.

When the input pulse occurs early in the recovery window as indicated by input pulse 21b', the related phase comparator variable input pulse 22b', which is of predetermined duration as explained hereinbefore, terminates prior to the termination of the phase comparator reference input pulse 37b as a result of which the phase comparator and charge pump 10 and filter 16 tend to change the oscillator frequency until the subsequent phase comparator reference input pulses terminate once again simultaneously with the terminal of the phase comparator variable input pulses. It will be appreciated that this action causes the counter output signals to be shifted such that the centre of recovery window 38 of the counter terminal C signal moves into coincidence with the leading edge of input pulse 21b'. As previously mentioned, the time constant of filter 16 is typically selected so that shifting of the recovery window occurs only in response to a general drift in the same direction of all of the input pulses 21a, 21b etc. Similar action occurs, with the recovery window being shifted in the opposite direction, when the input pulses occur late relative to the nominal locations as indicated, for example by input pulse 21b''. In this instance the related phase comparator variable input pulse 22b'' terminates after the termination of the phase comparator reference input pulse 37b which tends to change the oscillator frequency such that the phase comparator reference input pulses terminate once again concurrently with the termination of the phase comparator variable input pulses.

In the case of a 0 bit, as represented by input pulse 21c, a phase comparator variable input pulse 22c and a phase comparator reference input pulse 37c are produced for phase comparison as explained with reference to the 1 bits except that in this instance the counts of eight and one serve respectively to generate and terminate the phase comparator reference input pulse. On a count of eight the counter terminal B signal switches from a high (1) to a low (0) level, the same as it does on a count of four, for the purpose of initiating the phase comparator reference input pulse 37c by clocking flip-flop 24. On a count of one, the phase comparator variable input pulse 37c is terminated by the clocking of flip-flop 26 and resultant resetting of flip-flop 24. Early and late occurrences of the 0 bits cause shifting of the recovery window in the same manner as explained for the 1 bits.

From the foregoing description it will be recognized that a phase comparator reference input pulse is produced for phase comparison with a phase comparator variable input pulse only when an input data pulse is present. In the absence of an input data pulse, neither a phase comparator variable input pulse nor a phase comparator reference input pulse is produced for phase comparison and control of the voltage controlled oscillator. Thus, the phase locked oscillator operates satisfactorily for both periodic and aperiodic input pulse data streams.

Lock-in operation prior to data recovery may be accomplished as follows. Initially a clock signal, derived for instance from a crystal oscillator providing precisely controlled periodic pulses at a nominal spacing T and corresponding to the clock used for recording the data on the magnetic disc is applied to input terminal 7 while the $\overline{\text{CLAMP}}$ signal is high and inactive. Phase locked oscillator 6 functions in response to the clock signal in such a way that the signal at the output of filter 16 is set to a level representative of the centre of the tolerance limits of the phase locked oscillator.

The magnetic disc on which the data is recorded typically contains a preamble consisting of a sequence of 1 bits each spaced at interval T from adjacent bits. After the phase locked oscillator has settled at a quiescent state in response to the crystal oscillator pulses, the crystal oscillator is disconnected from the phase locked oscillator input terminal and replaced by the source of the preamble pulses. At the instant of applying the first preamble pulse, the $\overline{\text{CLAMP}}$ signal is switched to a low level. This disables monostable flip-flop 8 so it does not respond to the preamble pulse, sets flip-flop 26 driving the signal at its $\overline{Q}$ terminal low and provides simultaneous positive going pulses to input terminals VI and RI of phase comparator and charge pump 10. The $\overline{\text{CLAMP}}$ signal going low also disables voltage controlled oscillator 12 and loads a count of one into counter 13. At the occurrence of the next preamble pulse as determined, for example, by the coincidence of such preamble pulse and a

delayed replica of the first preamble pulse, the $\overline{\text{CLAMP}}$ signal switches back to a high level. This removes the disable signal from flip-flop 8 but not in time for it to respond to the instant preamble pulse. Hence, the $\overline{\text{CLAMP}}$ signal going high causes the signals at terminals VI and RI of the phase comparator and charge pump simultaneously to go low whereby the filter output signal remains at its quiescent value. The $\overline{\text{CLAMP}}$ signal going high also removes the disable signal from voltage controlled oscillator 12 permitting it to start oscillating after a delay of one cycle. A Texas Instruments Model 74S124 voltage controlled oscillator functions in this manner. Thereafter, some additional preamble pulses are applied to input terminal 7 and the phase locked oscillator responds as previously explained for data recovery, with the signal at the output of filter 16 settling at a quiescent value corresponding to the interval T between preamble pulses. This interval T may be greater or less than the interval between the crystal oscillator recording pulses depending on the speed of the magnetic disc during recovery relative to its speed during recording. After a predetermined number of preamble pulses the phase locked oscillator is then ready for recovery of data pulses.

WHAT WE CLAIM IS:—

1. Data recovery apparatus including a counter to count output pulses from a variable-frequency oscillator, a logic circuit which supplies, in response to an output signal from the counter and a signal indicating the presence of a data pulse in an input data pulse stream, a reference signal to a comparator circuit which compares the timing of the reference signals with the timing of the data pulses thereby to derive a control signal for the variable-frequency oscillator to cause the oscillator to synchronize with a harmonic of the fundamental frequency of the input data pulse stream, and means deriving a data recovery signal from an output signal of the counter and applying it to an output gating circuit to provide a data recovery window for significant bits of the input data pulse stream.

2. Data recovery apparatus according to Claim 1, in which the reference signal is supplied to the comparator circuit at a selected count.

3. Data recovery apparatus according to Claim 1 or 2 in which the data recovery signal is unsymmetrical.

4. Data recovery apparatus according to Claim 3 in which the counter is a binary counter arranged in operation to count cyclically from zero up to a number which is not a power of 2, and in which the unsymmetrical data recovery signal is an output signal of the counter.

5. Data recovery apparatus according to any preceding claim in which the input data pulse stream is applied to a monostable switching circuit which switches for a time substantially half the fundamental period of the input data pulses and in which the comparator circuit operates on the trailing edges of the pulses from the monostable switching circuit and from the logic circuit.

6. Data recovery apparatus according to any preceding claim in which the control signal is applied to the variable-frequency oscillator through a low-pass filter to eliminate jitter due to bit shift in the input data pulse stream.

7. Data recovery apparatus organised and arranged to operate substantially as shown in and as herein described with reference to the accompanying drawings.

For the Applicants,
P. A. MICHAELS,
Chartered Patent Agent.

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4 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

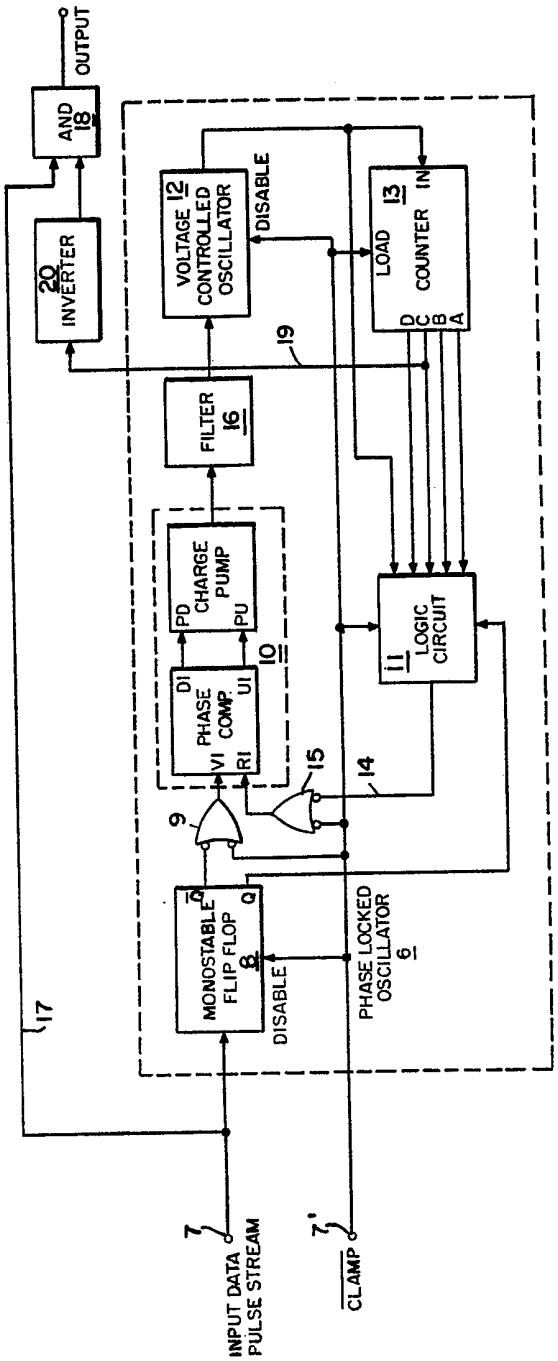


FIG. 1

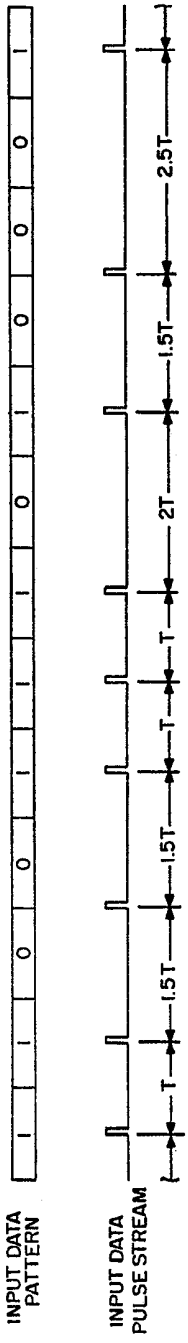
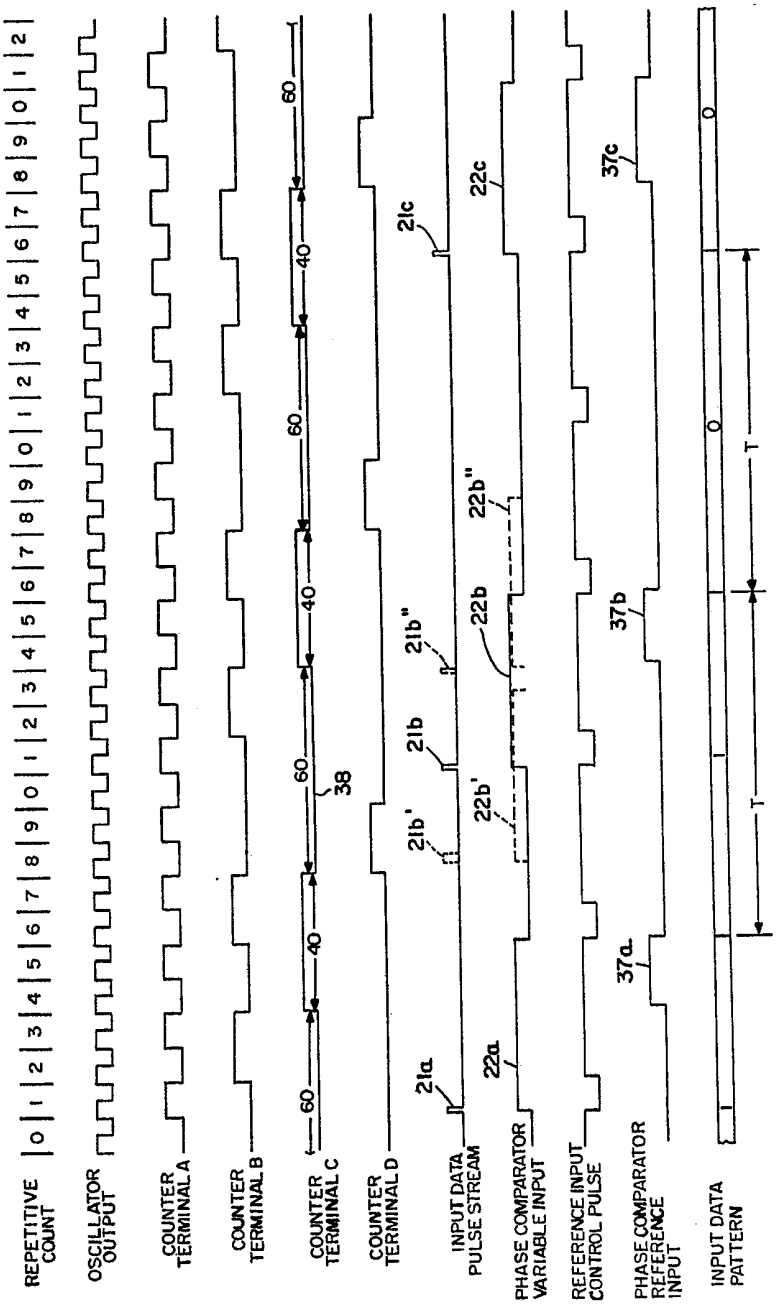


FIG. 2

REPETITIVE COUNT	BINARY COUNT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

FIG. 5

FIG. 3


REPETITIVE COUNT
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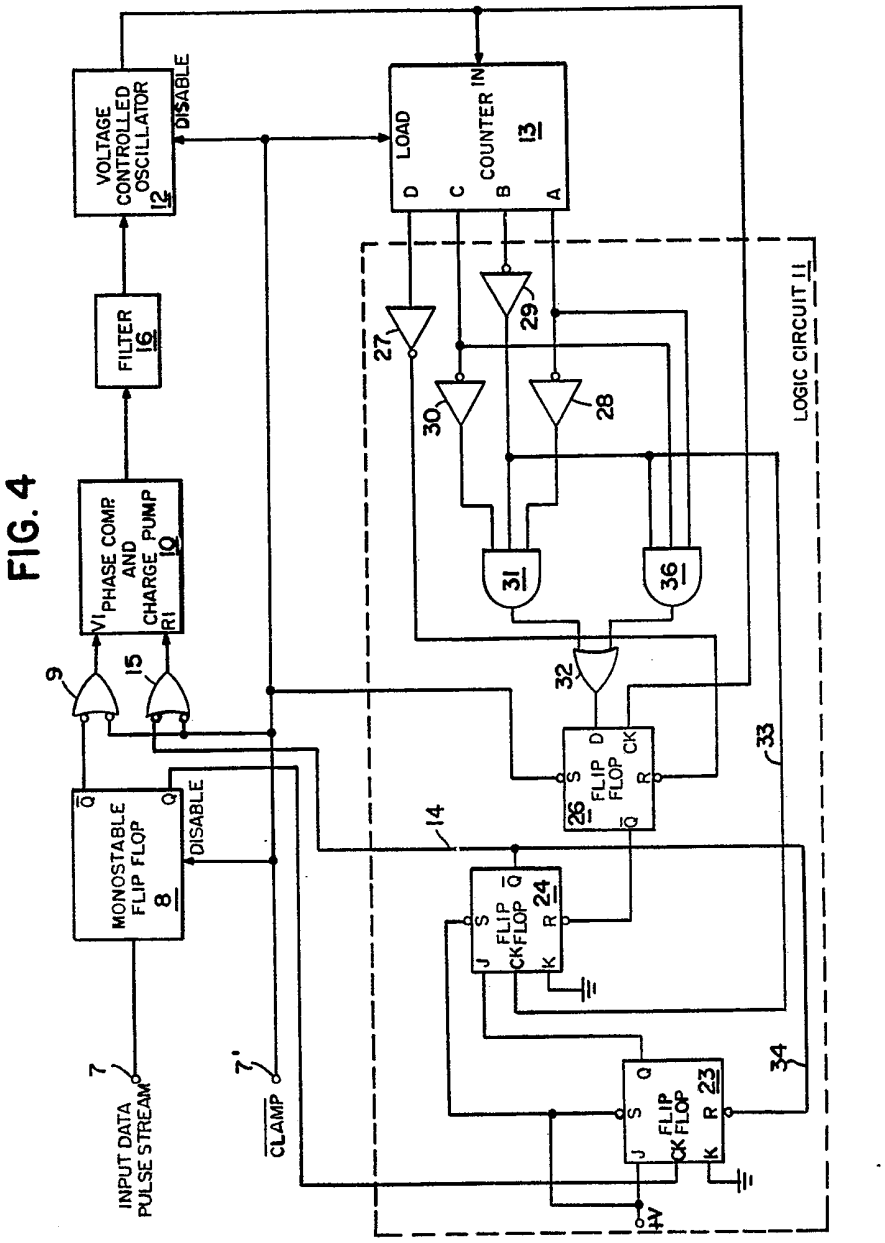
OSCILLATOR OUTPUT
COUNTER TERMINAL A
COUNTER TERMINAL B
COUNTER TERMINAL C
60
40
60
38
COUNTER TERMINAL D
INPUT DATA PULSE STREAM
21a
21b'
21b
21b"
21c
PHASE COMPARATOR VARIABLE INPUT
22a
22b'
22b
22b"
22c
REFERENCE INPUT CONTROL PULSE
PHASE COMPARATOR REFERENCE INPUT
37a
37b
37c
INPUT DATA PATTERN
0
1
0
T
T

FIG. 4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COUNTER 13
LOAD
D
C
B
A
IN
FILTER 16
PHASE COMP AND CHARGE PUMP 10
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R1
LOGIC CIRCUIT 11
27
29
30
28
31
36
32
33
9
15
FLIP FLOP 26
D
CK
S
R
Q
MONOSTABLE FLIP FLOP 8
DISABLE
14
FLIP FLOP 24
J
K
FLIP FLOP 23
34
7
INPUT DATA PULSE STREAM
7'
CLAMP
+V