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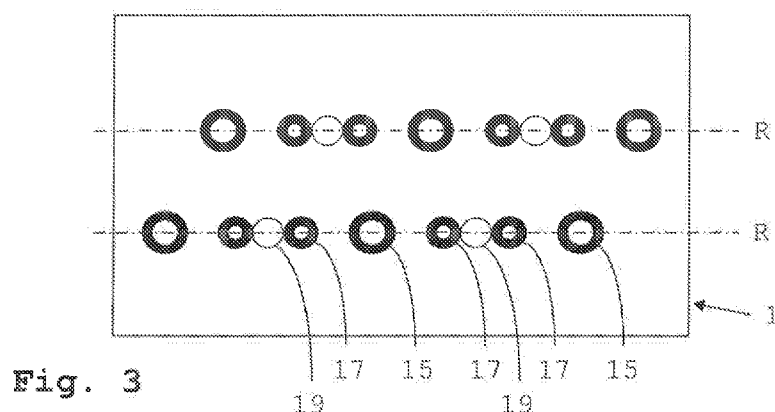
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(54) Title: STRUCTURED CIRCUIT BOARD AND METHOD



(57) Abstract: A circuit board (1) is provided comprising a plurality of insulating layers, at least one ground layer and at least one layer comprising signal traces. The circuit board comprises at least a first conductive via (17) and a second conductive via (17). The first conductive via and the second conductive via penetrate through at least a first insulating layer of the plurality of insulating layers and are connected to a signal trace. The first conductive via and the second conductive via are arranged adjacent each other. At least in the first insulating layer the first conductive via and the second conductive via are separated in a first direction of separation (R) by a first adjustment portion comprising a dielectric material property different from the first insulating layer.

STRUCTURED CIRCUIT BOARD AND METHOD

TECHNICAL FIELD

The present disclosure relates to the field of electric circuit boards, in particular to multi-layered electric circuit boards and to connectors comprising the same.

5

BACKGROUND

It is generally known that signals, in particular high frequency signals, which are transmitted through transmission lines may suffer from insertion losses. The magnitude of the insertion loss depends on the signal frequency, the transmission line geometry and the material properties. The magnitude of the insertion loss is generally indicated in units of dB loss, 0 dB meaning no loss, -6 dB meaning a loss of a factor two compared to the incident value and -20 dB indicating a loss of a factor ten. A signal transmitted through a transmission line having a first portion with one geometry bordering a second portion with another geometry may suffer significant losses at the border between the first and second portions.

It is further generally known that transmission lines arranged close to each other may exhibit signal cross talk. Also this effect is dependent on the signal frequency and on the geometries and the material properties of the transmission lines concerned .

Obviously both insertion loss and cross talk are undesirable and much research effort is spent designing transmission lines and/or interconnection devices, such as connectors, wherein these effects are reduced or prevented for one or more particular frequencies, preferably over wide frequency ranges.

The most effective methods found to date include widely separating the affected conductors and/or providing additional components for shielding and/or grounding in-between them. However, these solutions counteract the ongoing strive for
5 smaller, less costly devices which preferably also are suited for transmitting a plurality of signals at various high frequencies .

US 2002/0027020 discloses a through-hole structure for connecting a connector to a printed circuit board, the through-
10 hole structure comprising a signal through-hole having a conductive layer therein for supplying a signal to the printed circuit board, power through-holes having a conductive layer therein for supplying power to the printed circuit board, and dielectric constant adjusting portions formed among the signal
15 through-hole and the power through-holes. The through-hole structure is provided to reduce interference and noise in a connector portion of a printed circuit board connected to a high frequency connector, in which the signal through-hole is surrounded by the power through-holes.

US 2006/0255876 discloses a compact via transmission
20 line for a printed circuit board having preferred characteristic impedance and capable of miniaturizing the printed circuit board including a multilayer printed circuit board, and extending the frequency range of a via transmission line mounted on the printed circuit board, and a design method of the same. The
25 transmission line has a central conductor forming an inner conductor layer boundary make up a signal via hole, a plurality of via holes arranged around the central conductor form an outer conductor layer boundary, and a plurality of conductor plates
30 formed of a printed circuit board conductor layer, is further provided with a constitutive parameter adjustment clearance hole between the inner and outer conductor layer boundaries of the compact via transmission line, and electrically isolates to

prevent cross-talk of a signal propagating through a signal via hole with other signals in a high-frequency signal band. The disclosed via transmission lines are of the coaxial type, with each signal via hole being surrounded by a shield of ground via holes.

It is an object of the present disclosure to provide improved interconnection devices for high frequency signals, preferably at low voltages (below 5V), which are compatible with increased demands for miniaturisation, low noise levels and manufacturing cost-effectiveness.

SUMMARY

In a first aspect, a circuit board according to claim 1 is provided. The first and second conductive vias facilitate connection, e.g. of connector contacts, to the signal traces. The first adjustment portion allows adjustment of the impedance of the first and/or second conductive vias to an appropriate value by providing the adjustment portion with one or more appropriately selected dielectric material properties. In this way, signals traveling through conductive vias separated in such way exhibit less interaction than in the absence of the first adjustment portion. Further and/or alternatively, the first adjustment portion allows reducing the separation between the conductive vias, and thus an object size, while any interaction between signals transmitted through the conductive vias may be maintained below a predetermined level.

The dielectric material property affected by the adjustment portion may be at least one of the relative dielectric constant, the relative permittivity and the absorption of the material.

The first insulating layer may comprise portions with dielectric material properties at different locations. The adjustment portion is configured to provide a local variation of

the dielectric material properties compared to the insulating layer material surrounding the first and second conductive vias and/or the adjustment portion so as to adjust the interaction and/or impedance to an appropriate value. The adjustment portion
5 may comprise or form a local disruption (in the material) of the first insulating layer.

In a desirable circuit board, the first conductive via and second conductive via are configured as a differential signal pair for differential signaling. Differential signaling
10 allows transmission of signals with increased integrity and reliability at increased frequencies and with reduced power compared to single-ended transmission. Geometrical and the environment (electrical length) differences along one conductor of a differential signal pair with respect to the other
15 conductor of the pair may lead to signal skew and noise; this should be avoided. Impedance mismatch along a differential signal pair may lead to reflections and insertion losses; this should be avoided too. The circuit board according to claim 2 allows providing a desired improved impedance adaptation and -
20 matching to further portions of a differential signal pair transmission line.

The circuit board of claim 3 provides shielding of at least the first conductive via, improving signal quality. Impedance mismatch between the first (and/or second) conductive
25 via and connected circuitry due to the third conductive via may be reduced and/or prevented by the second adjustment portion.

The circuit boards of claims 4 and 5 provide an improved strip-line configuration which is beneficial for signal transmission, in particular at high signal frequencies. A strip
30 line geometry allows reducing device size and facilitates layered construction. It has surprisingly been found by the applicant that significant improvements may be achieved in different frequency ranges by providing just the first

adjustment portion or all of the first, second and third adjustment portions.

The circuit board of claim 6 provides an improved stripline geometry accommodating a plurality of signals. In particular when the first and second via and the fifth and sixth via are configured as two differential signal pairs, reduced insertion loss is achievable. In particular when adjustment portions are provided in at least the first insulating layer, significantly reduced cross talk between the pairs is achievable.

The circuit board of claim 7 is particularly suited for high frequency signals, in particular with frequencies of approximately 10 GHz and higher.

The circuit board of claim 8 provides a particular improvement since air has a minimum relative dielectric constant and relative permittivity and thus facilitates providing a large difference with the material of the insulating layer and associated improvement of the circuit board. Such circuit board also reduces manufacturing costs compared to manufacturing a circuit board with adjustment portions of different materials. Air gaps further allow reducing separation between charged conductors without risking short-circuiting. An adjustment portion may comprise a plurality of air gaps.

The circuit boards of claims 9 and/or 10 provide improvements by one or more appropriately formed adjustment portions, where applicable advantageously all adjustment portions. Larger adjustment portions generally result in further improved transmission; in particular for adjacent differential signal pairs, larger adjustment portions with lower dielectric constant, e.g. air gaps with a size of approximately a diameter of the separated conductive vias, provide improved cross talk separation. The size of the adjustment portion(s) in one or both directions specified in these claims is preferably chosen to

provide a desired impedance corresponding to an impedance of an adjoining portion of a transmission line of which the conductive vias are a portion.

5 The circuit board of claim 11 provides improved conductive vias for a plurality of signal transmission lines and in particular a plurality of differential signal pairs. Different pairs of conductive vias experience reduced interaction and cross talk and improved impedance matching.

10 Arranging the conductive vias in a row further facilitates connection to a connector. Arranging the conductive vias in a plurality of rows facilitates arranging a large plurality of conductors and thus of transmission lines with predictable interaction in a restricted volume.

15 Parallel rows may be staggered and may be mutually separated by one or more adjustment portions.

In another aspect a circuit board according to claim 12 is provided. The circuit board provides improved impedance matching to connecting circuitry of the differential signal pairs formed by the second and third conductive vias and the fifth and sixth conductive pairs, respectively. Further, cross talk and insertion losses are reduced, in particular for high signal frequencies, e.g. higher than approximately 5GHz and more so for signal frequencies higher than approximately 10 GHz.

25 In another aspect a circuit board according to claim 13 is provided. The circuit board allows close packing of plural differential signal pairs, with reduced insertion losses for and reduced cross talk between the different differential signal pairs, improving signal transmission through the pairs, in particular at high signal frequencies of approximately 5 GHz and higher .

A connector comprising a circuit board as described above facilitates interconnection to further circuitry with

reduced losses in signal quality. The circuit board itself may further comprise one or more circuits such as filters.

The invention will hereafter be more fully explained with reference to the drawings showing an embodiment of the invention by way of example.

BRIEF DESCRIPTION OF FIGURES

DETAILED DESCRIPTION OF EMBODIMENTS

It is noted that the drawings are schematic, not necessarily to scale and that details that are not required for understanding the present invention may have been omitted. The terms "upward", "downward", "below", "above", and the like relate to the embodiments as oriented in the drawings. Further, elements that are at least substantially identical or that perform an at least substantially identical function are denoted by the same numeral.

Fig. 1 shows a cross section of a portion of a prior art multi-layer circuit board 1, shown in top view in Fig. 2. Fig. 2 is a top view of the circuit board 1 of Fig. 1, with the cross section of Fig. 1 indicated. The circuit board 1 comprises a plurality of insulating layers 3 separated by a plurality of ground layers 5 and a plurality of layers comprising signal traces 7 (only one signal trace 7 shown in Fig. 1). The insulating layers may be substantially identical or may differ from each other in one or more aspects, in particular size and/or one or more dielectric material properties. The circuit board 1 further comprises a plurality of through holes 9 (only two shown in Fig. 1) which penetrate through one or more of the insulating layers 3 of the board 1. The through hole 9 comprises a conductive plating layer 11 and optionally conductive plating flanges 13, or: pads, on outer surfaces of the board 1, together forming conductive vias 15 and 17. The conductive via 15 is

connected to one or more ground layers 5 (here: all ground layers) and is termed a ground via 15. The conductive via 17 is insulated from the ground layers 5 and is connected to one or more signal traces 7 (here: one signal trace 7), the conductive via 17 is therefore also called a signal via 17. Adjacent vias 15, 17 are separated by portions of the circuit board 1 and insulated from each other by portions of the insulating layers 3.

As best visible in Fig. 2, in the circuit board 1 a plurality of conductive vias 15, 17 are arranged adjacent each other in rows R defining a direction of separation between the adjacent vias, which rows R, are optionally substantially parallel each other and which are optionally staggered with respect to each other as shown here. The conductive arrangement shown in Fig. 2 is that of a strip line geometry with conductors arranged as ground 15 - signal 17 - signal 17 - ground 15 - signal 17 - signal 17 - ground 15, which is very well suited for parallel transmission of differential signals through adjacent signal conductors (in the form of ground vias 15), shielded from each other and their environment by ground conductors (ground vias 15). However, the use may be different, i.e. not with differential signalling.

It will be apparent that in the shown circuit board 1 the ground vias 15 are somewhat larger than the signal vias 17. Further, in the direction of the row R, the mutual separation between each via 15, 17 is equal.

Alternatively, both types of vias 15, 17 may have equal sizes. Also, different sizes may exist between (groups of) ground vias 15 and/or signal vias 17. The vias may also be arranged equidistant with respect to an (imaginary) centre line, or be separated by varying distances.

Figs. 3 and 4 show different embodiments of improved circuit boards 1 of a construction generally similar to the circuit board 1 of Figs. 1 and 2.

However, different to the circuit board 1 of Figs. 1 and 2, in the circuit board of Fig. 3, adjacent signal vias 17 are separated by adjustment portions 19 comprising a dielectric material property different from the first insulating layer. In between a signal via 17 and a ground via 15, there is no such adjustment portion.

In the circuit board of Fig. 4, all vias 15, 17 adjacent each other in a row R are separated by adjustment portions 19, 21. The adjustment portions 19 separate signal vias 17, and the adjustment portions 21 separate a signal via 17 and a ground via 15.

The adjustment portions 19, 21 may be of equal size. Here, however, the adjustment portions 19 between signal vias 17 are larger (here: have a larger diameter) than the adjustment portions 21 between a signal via 17 and a ground via 15. As set out above, the adjustment portions 19, 21 may comprise or be simply holes in the material of the circuit board 1 filled with the ambient atmosphere of the circuit board, e.g. air.

In another embodiment, a circuit board 1 may comprise a row R comprising along the row a signal via 17, an adjustment portion 19, a signal via 17, an adjustment portion 21 and a ground via 15, such as a single sided strip line arrangement of signal-signal-ground with adjustment portions in between. This is shown in cross section in Fig. 5 wherein the adjustment portions 19, 21 are formed as air gaps penetrating through the circuit board 1.

Simulations have been performed of propagation of a differential signal pulse sent through a pair of signal vias 17 of the circuit boards 1 of Figs. 2-4 as well as of a similar circuit board comprising adjustment portions only between ground

vias and signal vias, but not between adjacent signal vias (thus, such circuit board may be seen as the inverse of the circuit board of Fig. 3). In the simulation, all adjustment portions 19, 21 of the boards considered have been simulated as tubular air gaps of substantially circular outer shape. The simulations are for signal traces towards the bottom side of the circuit board 1 when the signal is supplied on the top side of the respective signal via 17, i.e. the signal has had to travel almost the entire length of the signal via 17 through the circuit board 1.

Fig. 6 shows the results of a simulation of the differential insertion loss of a differential signal pulse. Here, the closer the curve is to 0 dB, the better.

Figs. 7A and 7B show the results of the simulations for differential impedance to signal traces 7 at 50 picoseconds, or: for a signal velocity of 10 GBits/second, and 25 picoseconds, or: for a signal velocity of 20 GBits/second, respectively. Here, the closer the curve is to 100 Ohm differential impedance, the better.

Fig. 8 shows the result for near end cross talk between the pair and Fig. 9 shows the result for far end cross talk between the pair. Here, the lower the curve is, the better.

In Figs. 6-9, a drawn line represents the results of Fig. 2 ("no air pockets"), dash-dotted line the results of Fig. 3 ("... Btwn sig vias only"), a dotted line the results of Fig. 4 ("Circ. air pock." = circular air gaps, between all vias), and a dashed line the results of circuit board with adjustment portions only between ground vias and signal vias, but not between adjacent signal vias ("... Btwn sig and gnd vias").

From Figs. 6-9 it will be apparent that at substantially all signal frequencies 0-20 GHz, the provision of adjustment portions has a beneficial effect on all simulated aspects. In a frequency region between approx. 8-10 GHz there is

little difference in the insertion loss between the different circuit board arrangements (Fig. 6). The effects for differential pair cross talk become increasingly noticeable at increasing frequencies, in particular at frequencies of approx. 10 GHz and higher (Figs. 8, 9).

Fig. 10 shows another embodiment of an improved circuit board 1, similar to the circuit board 1 of Fig. 4. In this circuit board 1, the adjustment portions 19 and 21 are formed as substantially rectangular slots, extending substantially perpendicular to the direction of each row R along which the vias 15, 17 are arranged.

Figs. 11-14 show the results of simulations just as for Figs. 6-9. For Figs. 11-14, in each case the adjustment portions have been taken as rectangular air gaps, instead of circular air gaps. Here, the dimensions of the adjustment portions are chosen with a width in the direction of the row R of approx one half times the separation between the vias 15, 17 and having a length perpendicular to the direction of the row R of approx. twice the diameter of the vias.

From a comparison between Figs. 6-9 and 11-14, it will be apparent that also in this case the provision of adjustment portions 19, 21 is beneficial to the behaviour of signal pulses through the circuit board 1.

In fact, in Fig. 11 it is visible that for a frequency range of approx. 6-11 GHz, insertion loss may be reduced by not having adjustment portions between all vias. For such frequencies, also the differential impedance shows less variation (Fig. 12A). However, it is again found that providing adjustment portions between all vias reduces the cross talk for all frequencies (Figs. 13 and 14). Thus, depending on the prospective use, e.g. the intended signal frequency to be transmitted through the vias and whether or not using

differential signalling, one may select to use more or less adjustment portions.

An adjustment portion in the form of an air gap may be wholly or partially plugged by insertion of a dielectric object
5 into the air gap to obtain a desired behaviour.

Fig. 15 shows, in cross section view similar to Figs. 1 and 5, a variation of a circuit board 1. The circuit board 1 has a thickness τ , and comprises a conductive signal via 17, which is connected to a signal trace 7 that is arranged relatively
10 close to the top of the circuit board 1. A portion of the plating layer 11 and the flange 13 on the bottom side of the conductive via 17 are absent, compared to the vias 15, 17 discussed before, so that a via is formed which is conductive over only a fraction of its length. The via 17 has a conductive
15 portion (here in the form of the plating 11) which extends through the circuit board 1 along a direction of extension E for a distance D which is less than the thickness T of the circuit board 1. Along the direction of extension E, or: instead of the absent portion of the via 17, an adjustment portion 23 is
20 arranged comprising one or more dielectric material properties different from those of one or more insulating layers 3. As a consequence, any antenna-effect is prevented of a portion of the via 17 extending towards the bottom side of the circuit board 1 significantly further than the position on which the conducting
25 portion 11 of the via 17 connects with a trace 7. The circuit board 1 may comprise plural partially conductive vias 15, 17, of which the lengths of the conductive portions may be equal or different depending on the level on or within the circuit board 1 that via is connected to one or more conductive traces or
30 layers. Such structure of a via of which a conducting portion extends only partly into the circuit board may also be employed for one or more ground vias 15.

In the circuit board 1 shown in Fig. 5, adjacent the signal via 17 a ground via 15 is formed just as in the embodiments shown above. Between adjacent signal vias 17 and signal and ground vias 15, 17 one or more adjustment portions 19, 21 may be provided as described before (not shown) .

Such circuit board 1 of Fig. 15 may be manufactured easily by forming a circuit board comprising a desired number of vias, arranging a plating layer 11 and flanges 13 in regular fashion in all vias. In this way, a method of manufacturing of the board as a whole need not be altered. In an optional subsequent step the plating layer 11 and the flange 13 are then removed from the circuit board 1 in the desired amount at the selected vias 15, 17. Such removal may e.g. be done by drilling a recess along the selected plated through via 15, 17 with an appropriate tool, e.g. a drill bit having a larger size (diameter) than (the plating of) the via. The recess may be left empty or be partly or wholly filled with a dielectric material to form an adjustment portion 23 with one or more desired properties .

Figs. 16-17B show the results of simulations, as before, for a circuit board 1 comprising a row R of vias 15, 17 which are mutually separated with rectangular air gaps 19, 21 as in Fig. 10, wherein the signal vias 17 are partially conductive and the ground vias 15 are fully conductive as in Fig. 15 (dotted line, "FP with air pockets") . For comparison the results of a circuit board 1 of Fig. 2 are also shown in the Figs 16-17B (drawn line, "Nominal FP") .

It will be apparent from a comparison with the other simulation results that the improved circuit board 1 provides significantly less differential insertion loss (Fig. 16) at substantially all frequencies and a significantly improved differential impedance at signal frequencies of 10 GHz (Fig. 17A) and 20 GHz (Fig. 17B) .

Fig. 18 is a top view of an alternative embodiment of a circuit board 1 showing that compound adjustment portions 19A, 21A separating vias 15, 17 may be formed from a plurality of subsidiary adjustment portions 19B, 21B arranged close together.

5 In the shown embodiment, substantially rectangular compound adjustment portions 19A, 21A are formed by series of adjacent substantially circular subsidiary adjustment portions 19B, 21B. The subsidiary adjustment portions 19B, 21B may be substantially identical or different. Other arrangements of more or less
10 subsidiary adjustment portions 19B, 21B are also conceivable.

The invention is not restricted to the above described embodiments which can be varied in a number of ways within the scope of the claims. For instance a circuit board may comprise more or less conducting vias.

15 Conducting vias and adjustment portions need not be arranged in straight rows, nor symmetrically with respect to a straight or bent row. Adjacent rows need not be parallel.

In between parallel rows R of conducting vias in Figs. 2-4 and 10 spaces are arranged, which may be used for routing
20 traces. Rows R may be separated by one or more adjustment portions .

In a circuit board, conducting vias may be separated by several adjustment portions adjacent each other in the direction of separation of the vias. Thus, a larger compound adjustment
25 portion may be formed.

Adjustment portions may be formed by drilling an array of holes or recesses into the circuit board and selectively plating the vias such that one or more adjacent conducting vias are separated by unplated vias.

30 A conducting via may be connected to plural traces on one or more layers of the circuit board. A ground layer may be conducting across large portions of its area or comprise a number of ground traces.

Elements and aspects discussed for or in relation with a particular embodiment may be suitably combined with elements and aspects of other embodiments, unless explicitly stated otherwise .

CLAIMS

1. A circuit board (1) comprising a plurality of insulating layers (3), at least one ground layer (5) and at least one layer comprising signal traces (7), the circuit board comprising at least a first conductive via (17) and a second
5 conductive via (17),

wherein the first conductive via and the second conductive via penetrate through at least a first insulating layer (3) of the plurality of insulating layers and are connected to a signal trace,

10 wherein the first conductive via and the second conductive via are arranged adjacent each other

wherein at least in the first insulating layer the first conductive via and the second conductive via are separated in a first direction of separation (R) by a first adjustment
15 portion (19, 19A) comprising a dielectric material property different from the first insulating layer.

2. The circuit board (1) of claim 1, wherein the first conductive via (17) and second conductive via (17) are
20 configured as a differential signal pair.

3. The circuit board of any preceding claim, comprising a third conductive via (15) adjacent the second conductive via (17) opposite the first conductive via (17), penetrating through
25 at least the first insulating layer (3) and connected to at least one of a ground trace and a ground layer (5),

wherein the second conductive via and the third conductive via are separated in a second direction of separation (R) by a second adjustment portion (21, 21A) comprising a
30 dielectric material property different from the first insulating layer.

4. The circuit board of claim 1 or 2, comprising a third conductive via (15) adjacent the second conductive via (17) and a fourth conductive via (15) adjacent the first conductive via (17), the third conductive via and the fourth conductive via penetrating through at least the first insulating layer (3) and being connected to at least one of a ground trace and a ground layer (5), wherein the first to fourth conductive vias are arranged mutually adjacent in a row (R) as ground - signal - signal - ground.

5. The circuit board (1) of claim 4, wherein the second conductive via (17) and the third conductive via (15) are separated in the direction of the row (R) by a second adjustment portion (21, 21A) comprising a dielectric material property different from the first insulating layer (3), and

wherein the fourth conductive via (15) and the first conductive via (17) are separated in the direction of the row (R) by a third adjustment portion (21, 21A) comprising a dielectric material property different from the first insulating layer.

6. The circuit board (1) of claim 1 or 2, comprising a third conductive via (15) arranged adjacent the second conductive via (17) opposite the first conductive via (17) and fourth, fifth, sixth and seventh conductive vias (15, 17, 17, 15) arranged adjacent the first conductive via (17) opposite the third conductive via,

wherein the first, second, fifth and sixth conductive vias (17, 17, 17, 17) penetrate through at least the first insulating layer (3) and are connected to a signal trace (7), and the third, fourth and seventh conductive vias (15, 15, 15) penetrate through at least the first insulating layer (3) and

are connected to at least one of a ground trace and a ground layer (5), such that the first to seventh conductive vias (15, 17, 17, 15, 17, 17, 15) are arranged mutually adjacent in a row (R) as ground - signal - signal - ground - signal - signal - ground,

wherein at least the fifth and sixth conductive vias penetrate through at least one of the first insulating layer and a second insulating layer (3)

wherein in at least one of the first and second insulating layers the fifth conductive via and the sixth conductive via are separated in the direction of the row (R) by a further adjustment portion (19) of insulating material comprising a dielectric material property different from at least one of the first and second insulating layers.

7. The circuit board (1) of claim 6, wherein all adjacent first to seventh conductive vias (15, 17, 17, 15, 17, 17, 15) are mutually pairwise separated in the direction of the row (R) by adjustment portions (21, 21A; 19, 19A; 21, 21A; 21, 21A; 19, 19A; 21, 21A) comprising a dielectric material property different from at least one insulating layer (3), preferably all layers, penetrated by the respective pair of mutually adjacent conductive vias.

8. The circuit board (1) of any preceding claim wherein at least a portion of at least one of the adjustment portion (s) (19, 19A, 19B, 21, 21A, 21B) is formed as an air-gap.

9. The circuit board (1) of any preceding claim, wherein two adjacent conductive vias (17, 17; 15, 17) are mutually separated by a separation distance along a respective direction of separation (R) wherein at least one of the adjustment portion (s) (19, 19A; 21, 21A) separating the two

adjacent conductive vias in the respective direction of separation is formed to extend between the two adjacent conductive vias in that respective direction of separation for a length of more than approximately one quarter, preferably more than approximately one half, most preferably for more than approximately three quarters of the separation distance between the two adjacent conductive vias.

10. The circuit board (1) of any preceding claim, wherein two adjacent conductive vias (17, 17; 15, 17) are mutually separated by a separation distance along a respective direction of separation (R) wherein at least one of the adjustment portion (s) (19, 19A; 21, 21A) separating the two adjacent conductive vias in the respective direction of separation is formed to extend between the two adjacent conductive vias in a direction substantially perpendicular to that respective direction of separation for a length of more than approximately one, preferably more than approximately one and a half, most preferably for more than approximately two times the size of at least one of the two adjacent conductive vias in a direction substantially perpendicular to that respective direction of separation.

11. The circuit board (1) of any preceding claim, comprising plural rows (R) of adjacent conductive vias (15, 17) penetrating at least the first insulating layer (3), wherein the adjacent conductive vias within each row are mutually pairwise separated in the direction of the row by adjustment portions (19, 19A, 21, 21A) comprising a dielectric material property different from at least the first insulating layer.

12. A circuit board (1) comprising a plurality of insulating layers (3), at least one ground layer (5) and at

least one layer comprising signal traces (7), the circuit board comprising at least seven conductive vias (15, 17, 17, 15, 17, 17, 15) arranged mutually adjacent in a row (R) ,

wherein the first, fourth and seventh conductive vias (15), as counted along the row, penetrate through at least the first insulating layer and are connected to at least one of a ground trace and a ground layer, and wherein the second, third, fifth and sixth conductive vias (17), as counted along the row, penetrate through at least the first insulating layer and are connected to a signal trace, such that the first to seventh conductive vias are arranged as ground - signal - signal - ground - signal - signal - ground,

and wherein the second and third conductive vias, as counted along the row, are configured as a first differential signal pair and the fifth and sixth conductive vias, as counted along the row, are configured as a second differential signal pair,

wherein the adjacent first to seventh conductive vias are mutually pairwise separated in the direction of the row by adjustment portions (21, 21A; 19, 19A; 21, 21A; 21, 21A; 19, 19A; 21, 21A) comprising air gaps so as to provide a dielectric material property different from at least the first insulating layer .

13. A circuit board (1) comprising a plurality of insulating layers (3), at least one ground layer (5) and at least one layer comprising signal traces (7),

the circuit board comprising a plurality of mutually parallel adjacent rows (R) comprising at least seven conductive vias (15, 17, 17, 15, 17, 17, 15) arranged mutually adjacent in the respective row,

wherein the first, fourth and seventh conductive vias (15) , as counted along the row, penetrate through at least the

first insulating layer and are connected to at least one of a ground trace and a ground layer, and wherein the second, third, fifth and sixth conductive vias (17), as counted along the row, penetrate through at least the first insulating layer and are
5 connected to a signal trace, such that the first to seventh conductive vias are arranged as ground - signal - signal - ground - signal - signal - ground, with the second and third conductive vias being configured as a first differential pair and the fifth and sixth conductive vias being configured as a
10 second differential signal pair,

wherein the adjacent first to seventh conductive vias within each row are mutually pairwise separated in the direction of the row by adjustment portions (21, 21A; 19, 19A; 21, 21A; 21, 21A; 19, 19A; 21, 21A) comprising air gaps so as to provide
15 a dielectric material property different from at least the first insulating layer.

14. A connector comprising the circuit board (1) of any one of the preceding claims.

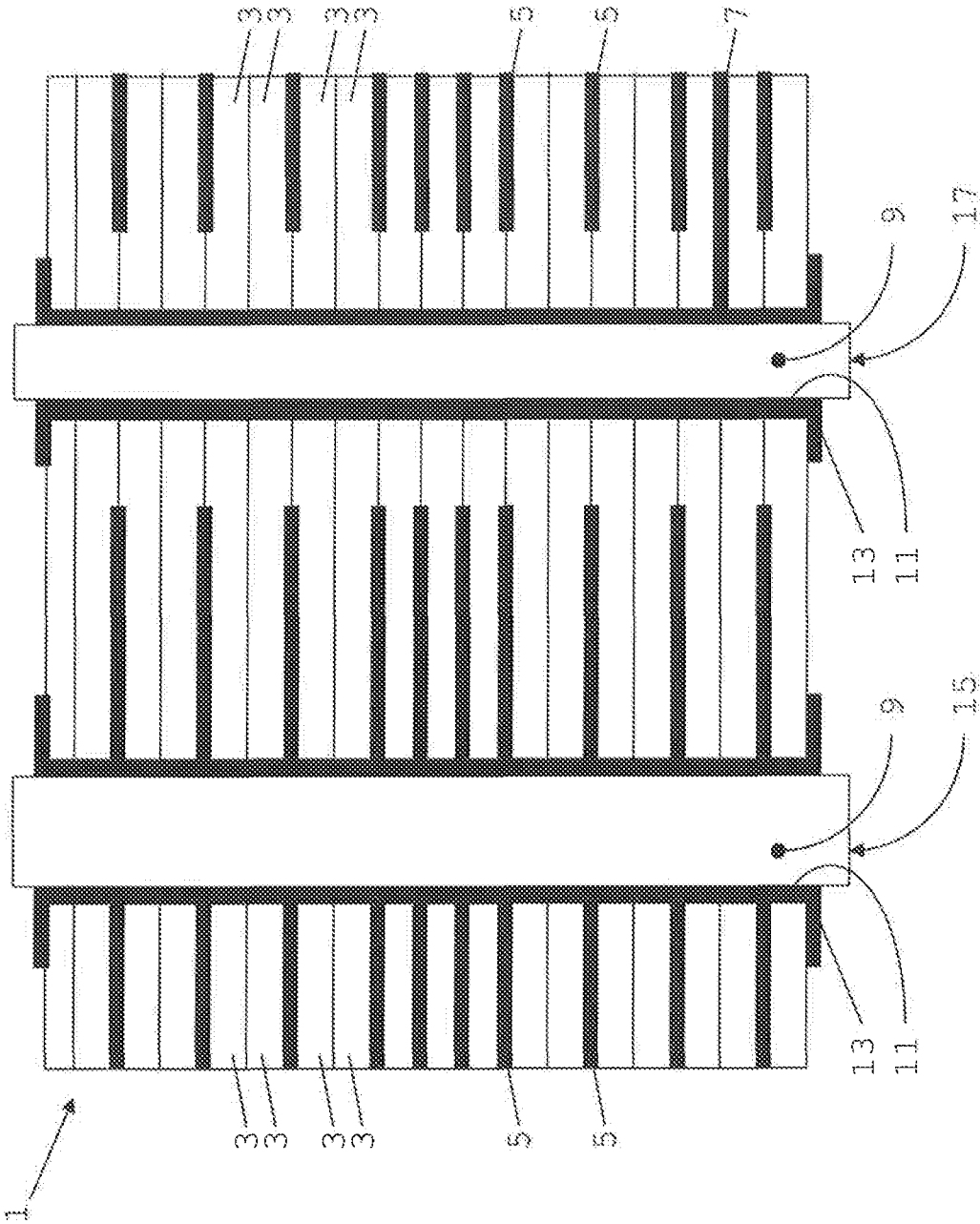


Fig. 1

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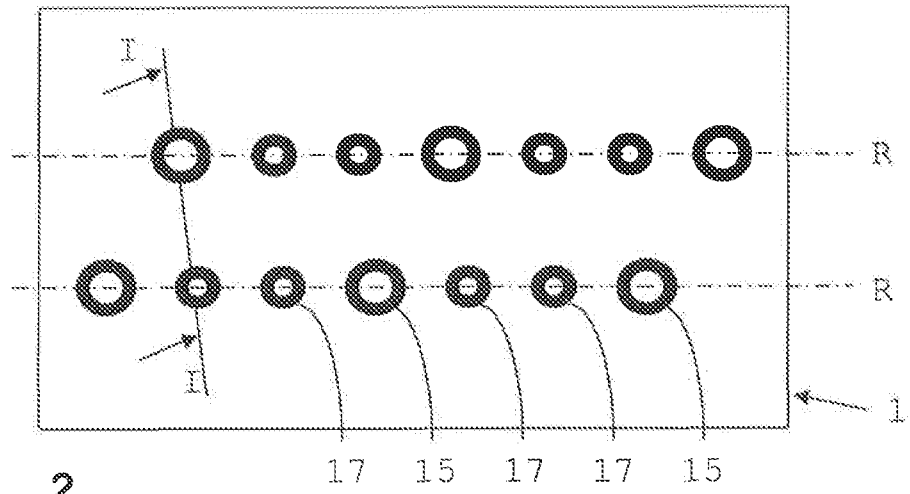


Fig. 2

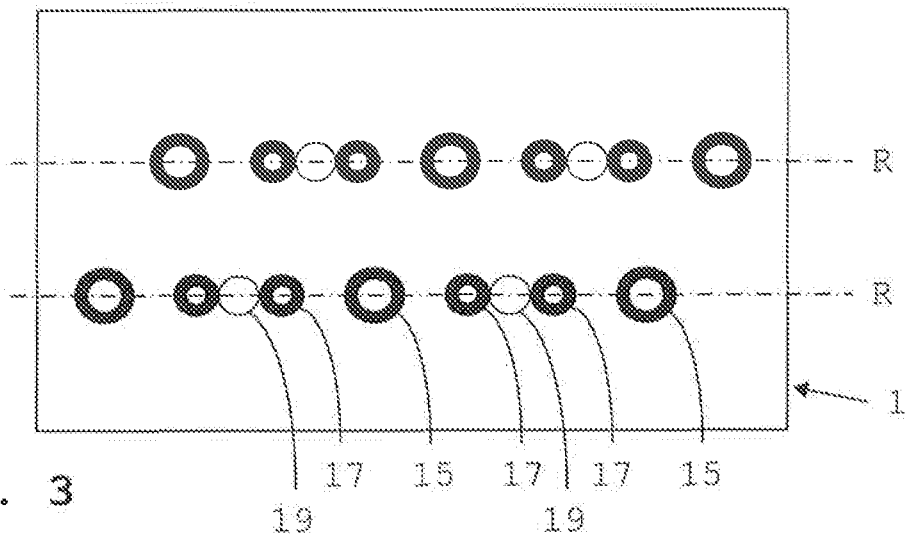


Fig. 3

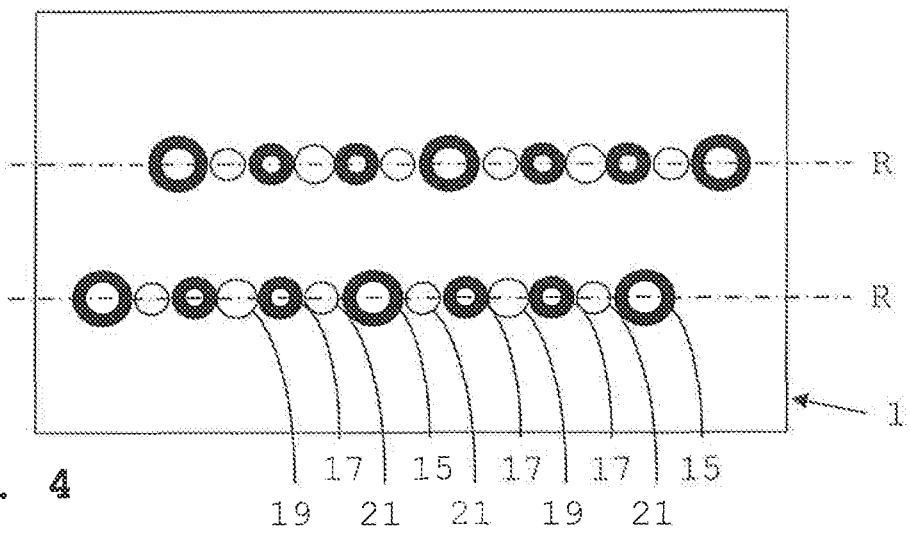
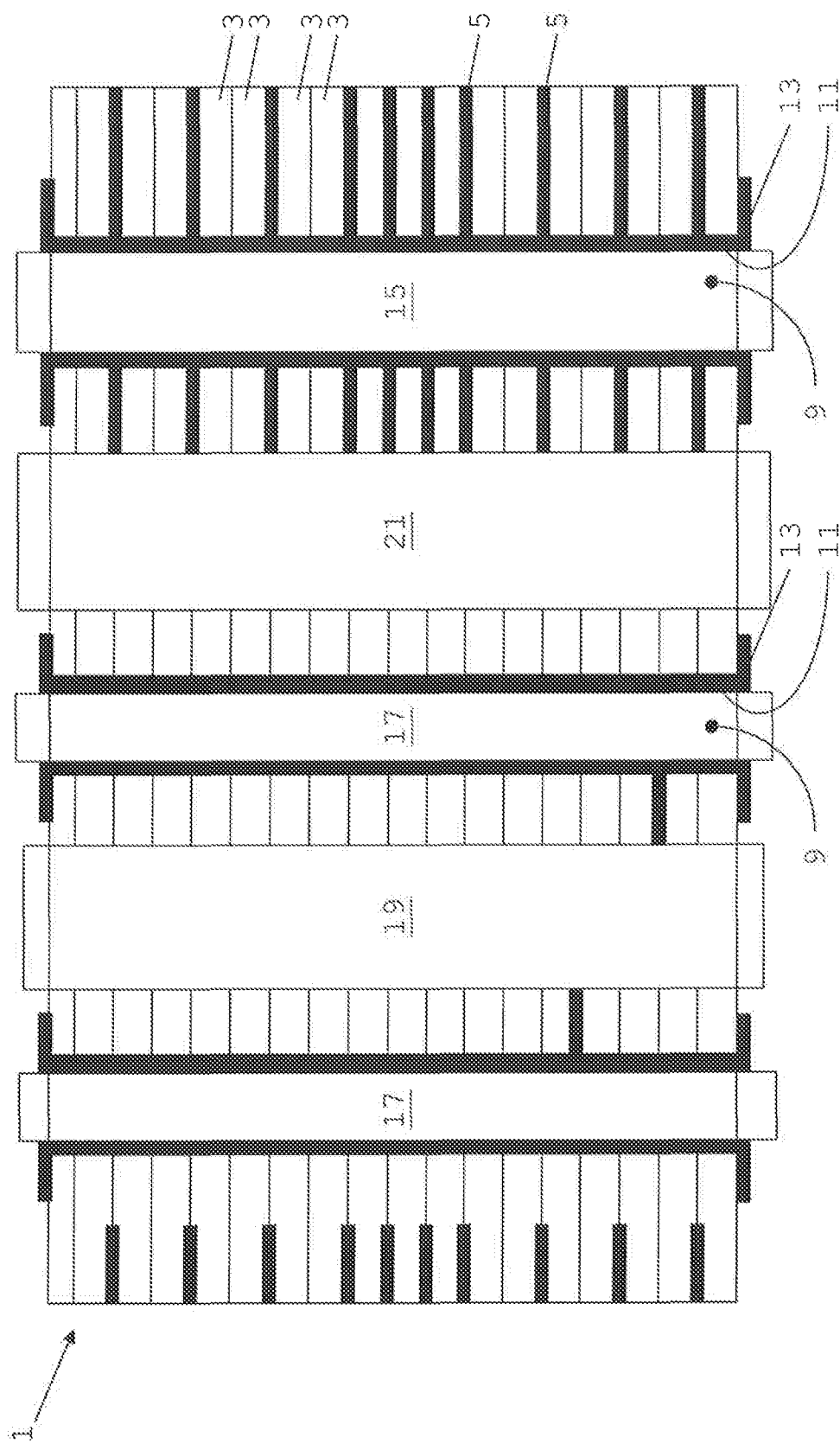


Fig. 4

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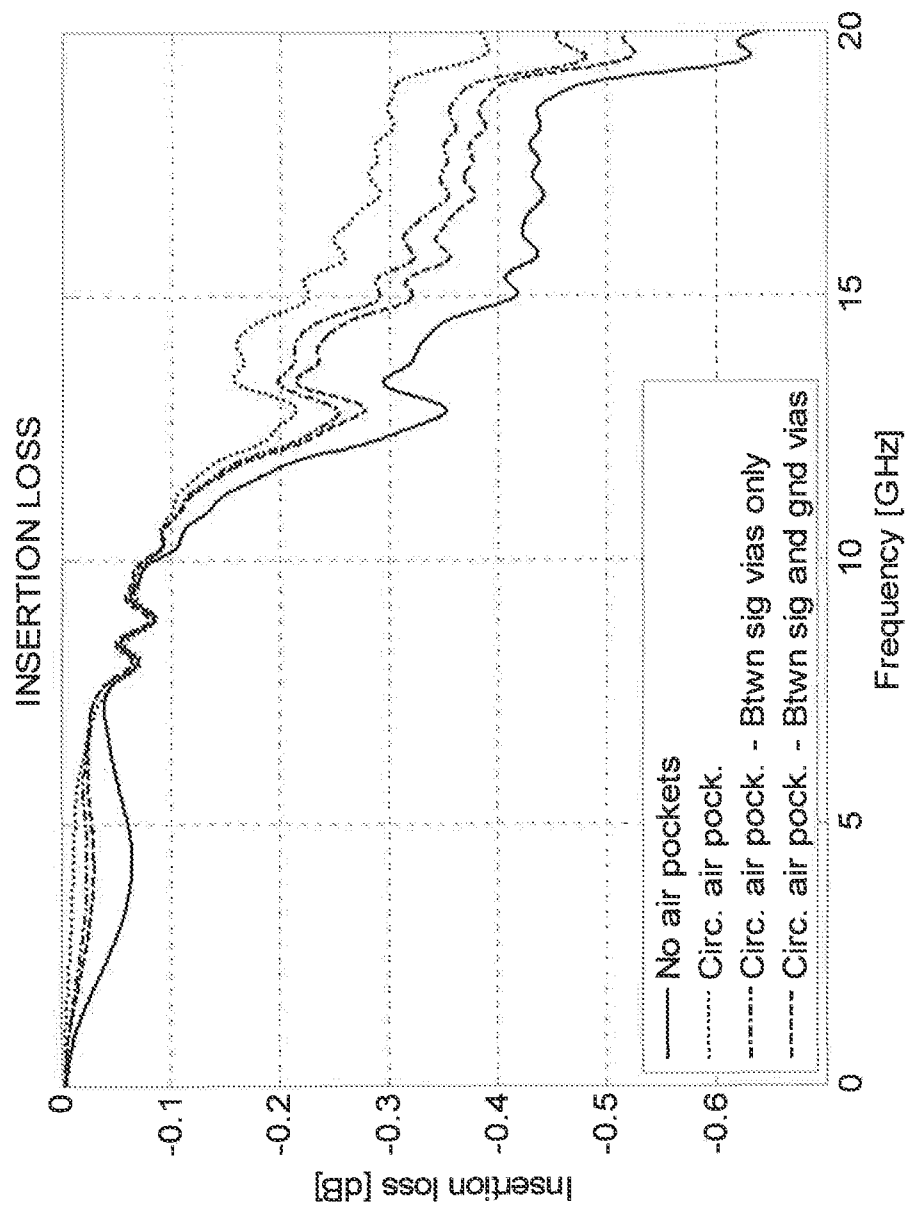


Fig. 6

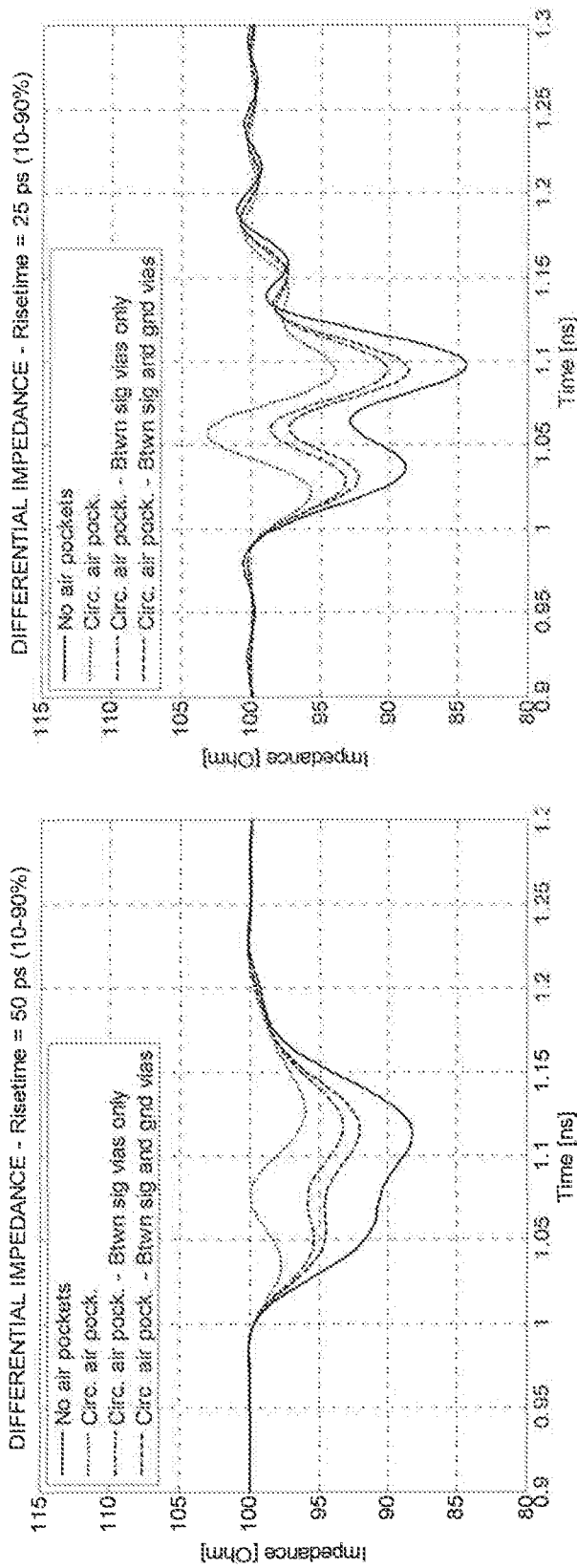


Fig. 7A

Fig. 7B

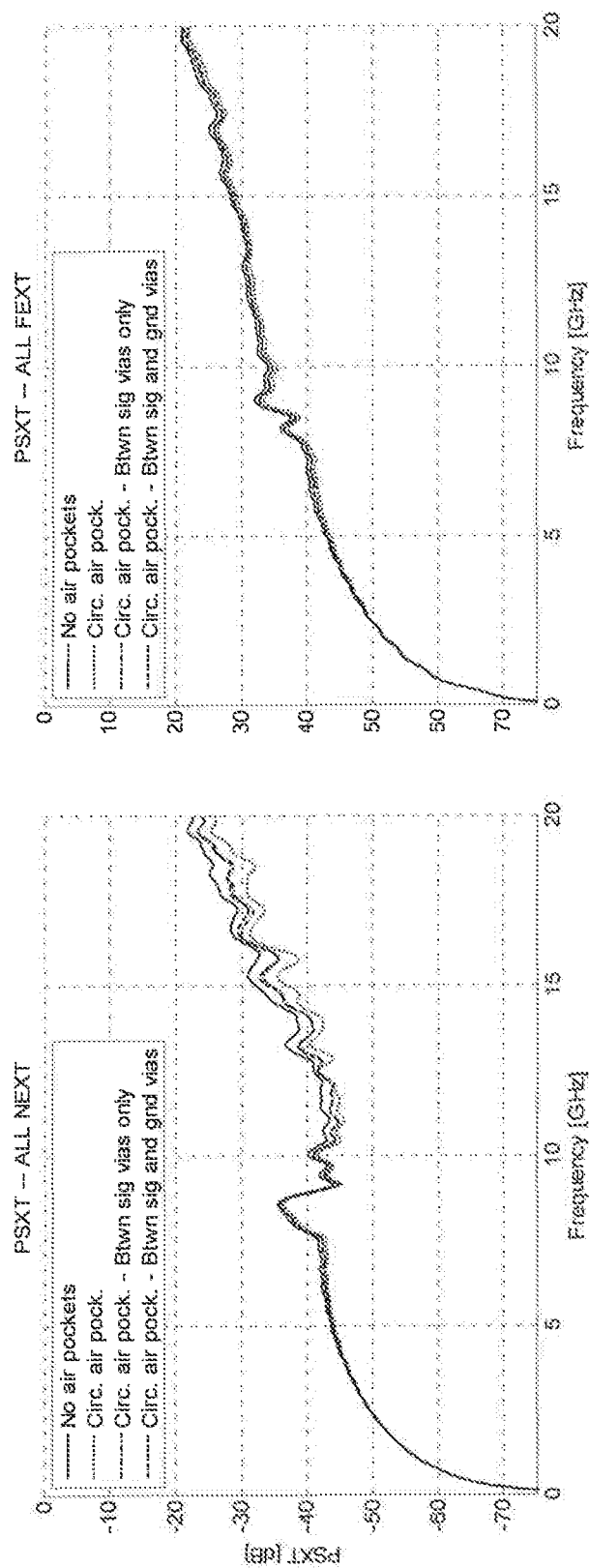
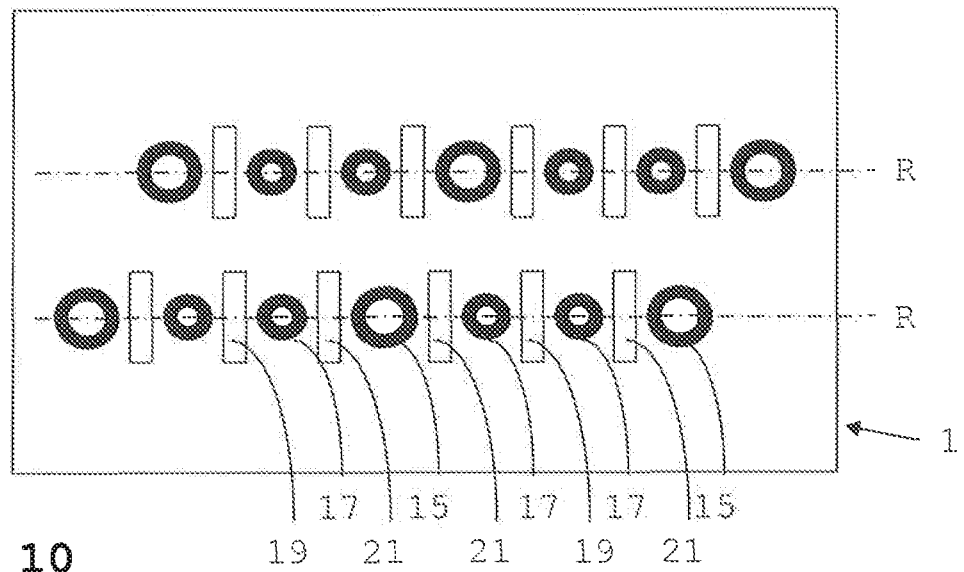
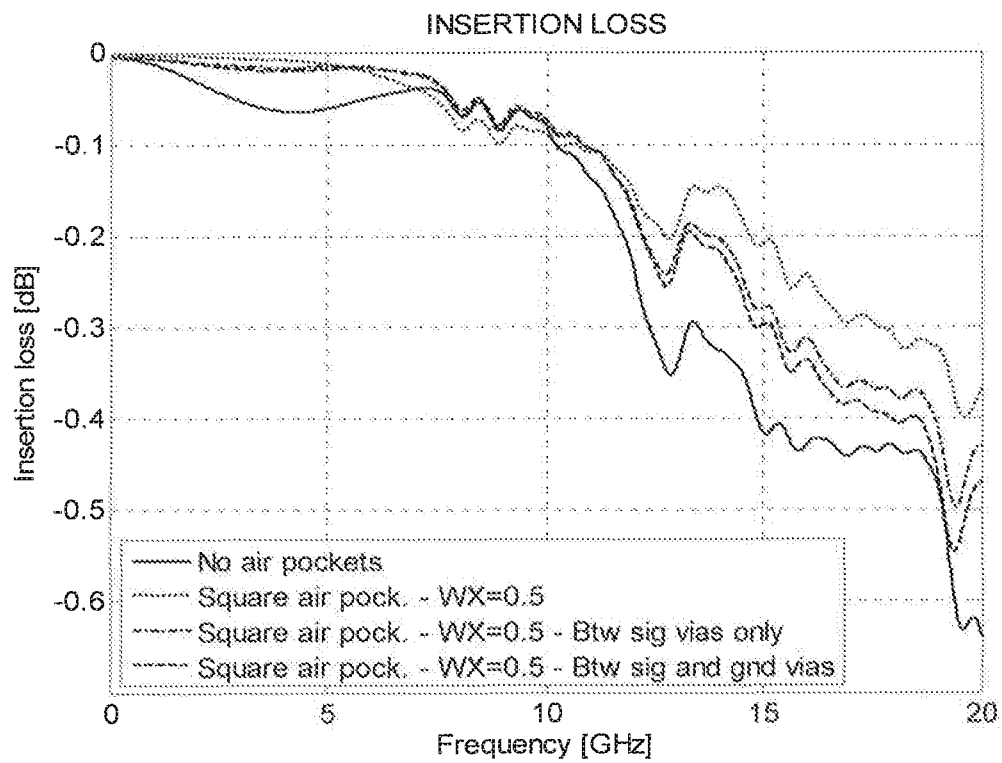


Fig. 9

Fig. 8

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**Fig. 10****Fig. 11**

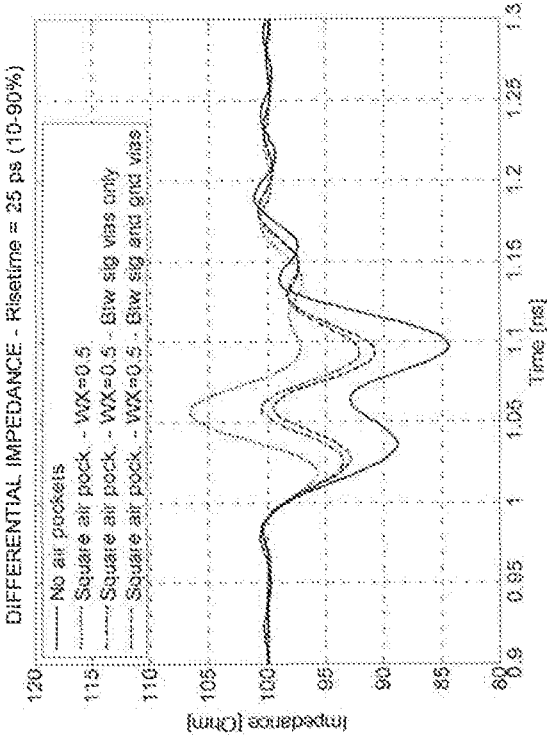


Fig. 12B

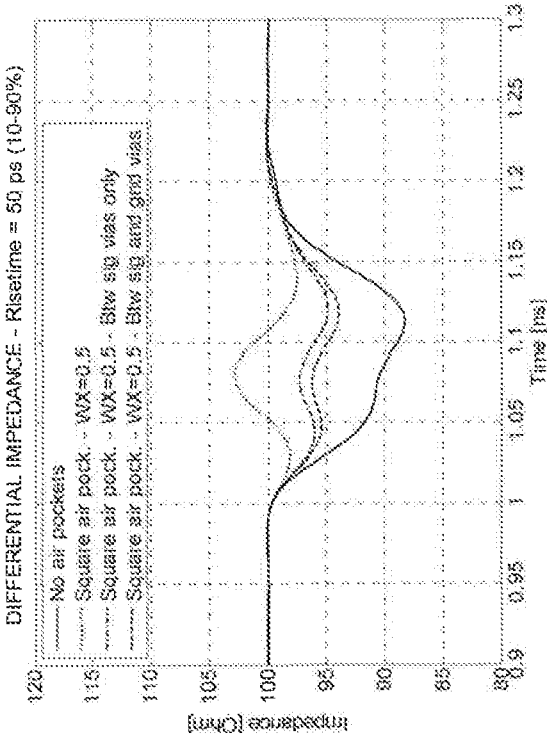


Fig. 12A

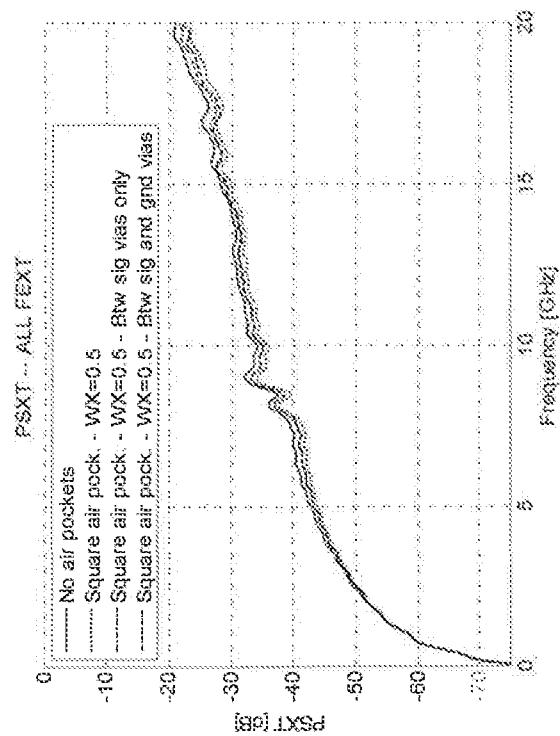


Fig. 14

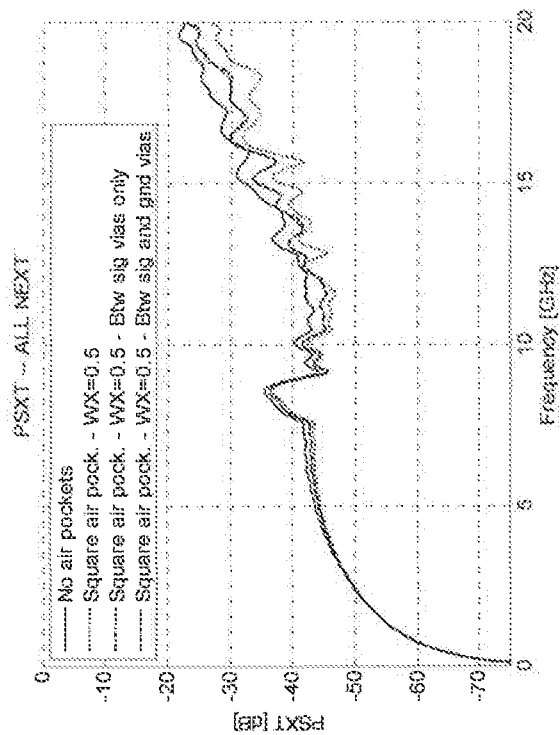


Fig. 13

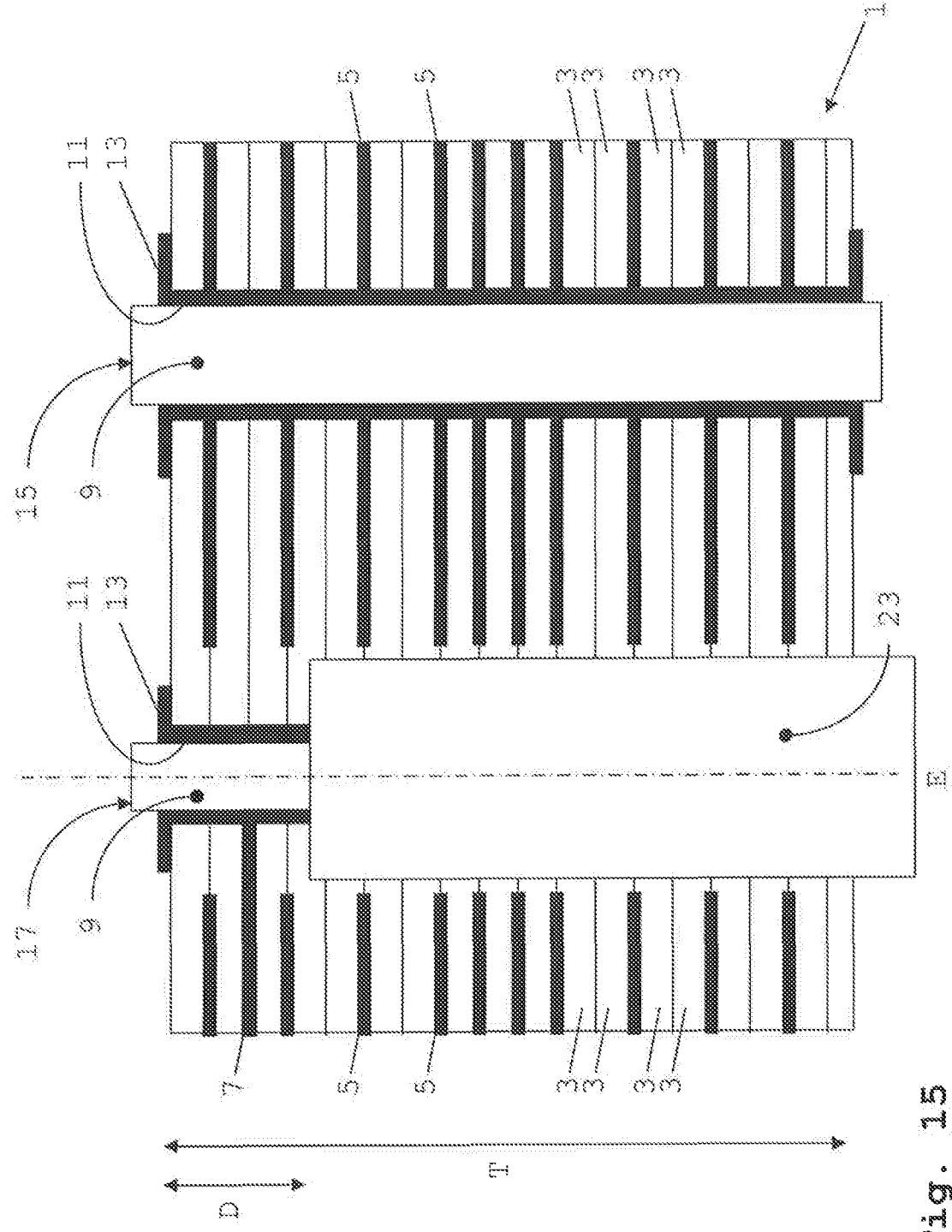


Fig. 15

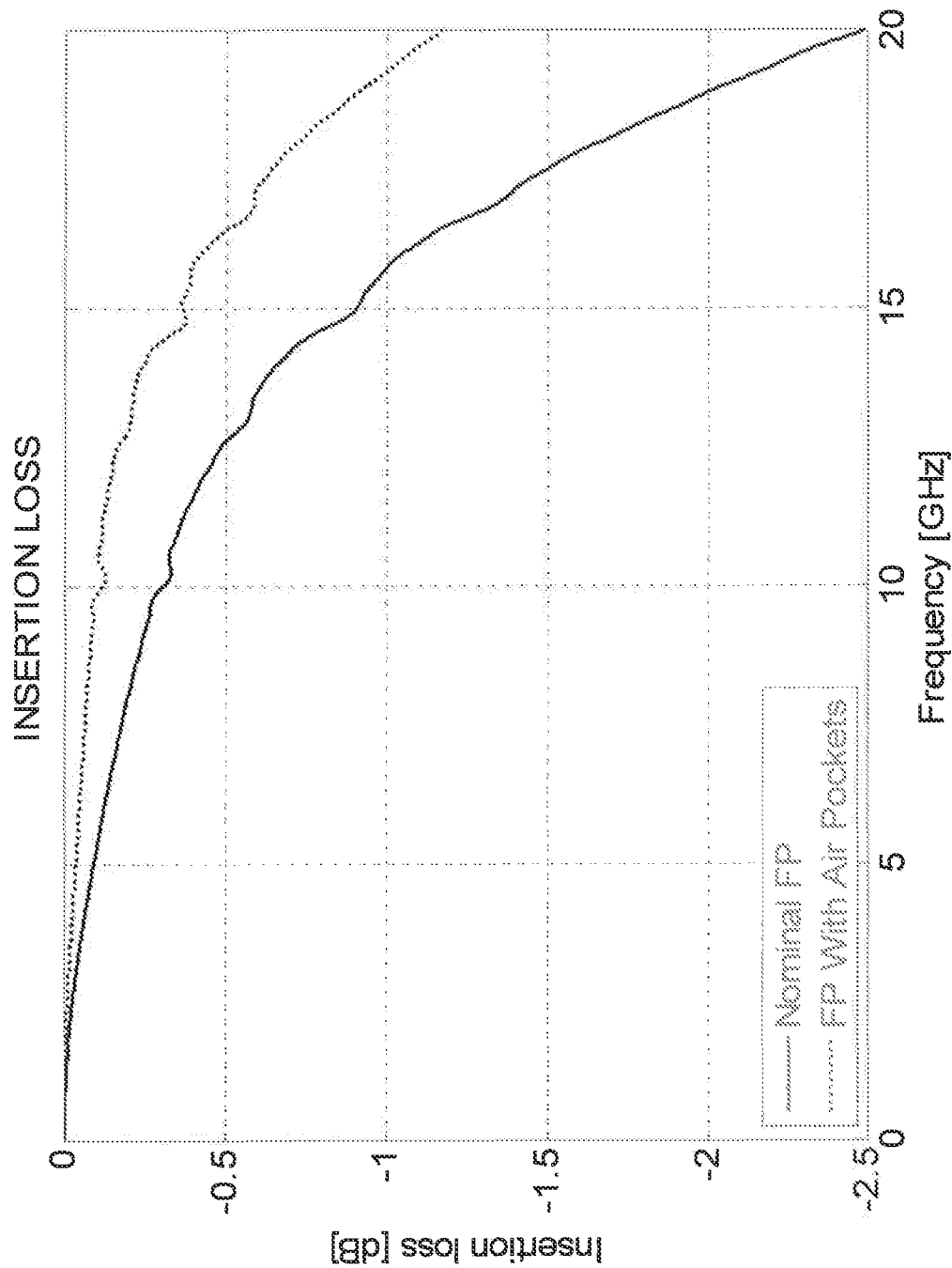


Fig. 16

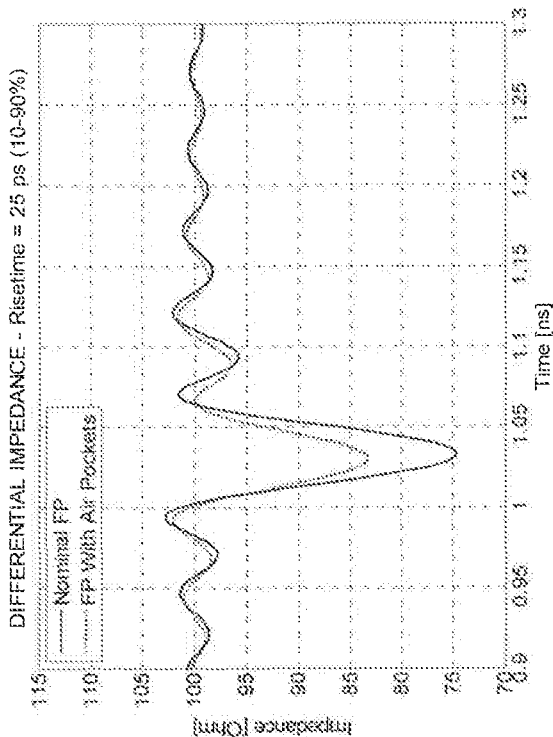


Fig. 17B

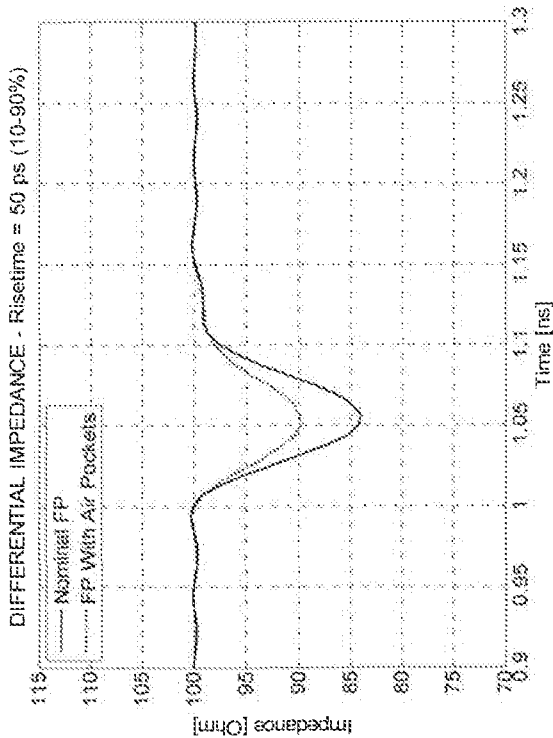


Fig. 17A

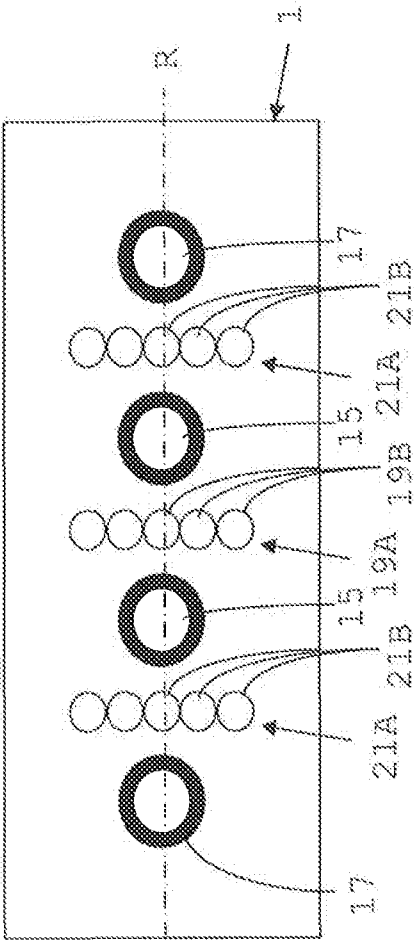


Fig. 18

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/06Q785

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05K1/Q2 H01R13/646
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05K H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/056999 A1 (KASHIWAKURA KAZUHIRO [JP]) 5 March 2009 (2009-03-05)	1-5, 8, 11, 14
Y	the whole document	6, 7, 9, 10, 12, 13
Y	----- US 2009/201658 A1 (LEMKE TIMOTHY A [US] ET AL) 13 August 2009 (2009-08-13) the whole document -----	6, 7, 9, 10, 12, 13



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search

9 September 2011

Date of mailing of the international search report

06/10/2011

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Fax: (+31-70) 340-3016

Authorized officer

Moje, Andreas

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2011/06Q785

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009056999 AI	05-03-2009	CN 101378633 A JP 2009059873 A	04-03-2009 19-03-2009
US 2009201658 AI	13-08-2009	CN 101953027 A CN 101953028 A US 2009203263 AI US 2010099306 AI W0 2009102407 AI W0 2009102408 AI	19-01-2011 19-01-2011 13-08-2009 22-04-2010 20-08-2009 20-08-2009