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(54) METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

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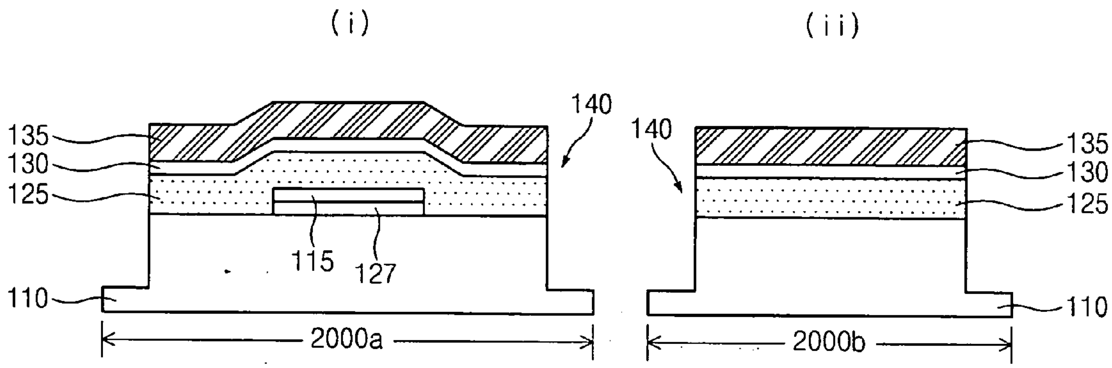
(57) **ABSTRACT**

A method for fabricating a semiconductor device is provided, the method including forming a SiGe epitaxial layer pattern and a first Si epitaxial layer pattern on a semiconductor substrate, forming a second Si epitaxial layer on the entire surface, etching the second Si epitaxial layer and a predetermined thickness of the semiconductor substrate to form a trench defining an active region, removing the SiGe epitaxial layer pattern through a sidewall of the trench to form a space under the first Si epitaxial layer, forming a gap-filling insulating film to at least fill up the space and the trench, forming a gate oxide film on the second Si epitaxial layer, and depositing and patterning a gate conductive layer and a hard mask layer on the entire surface to form a gate in the gate region.



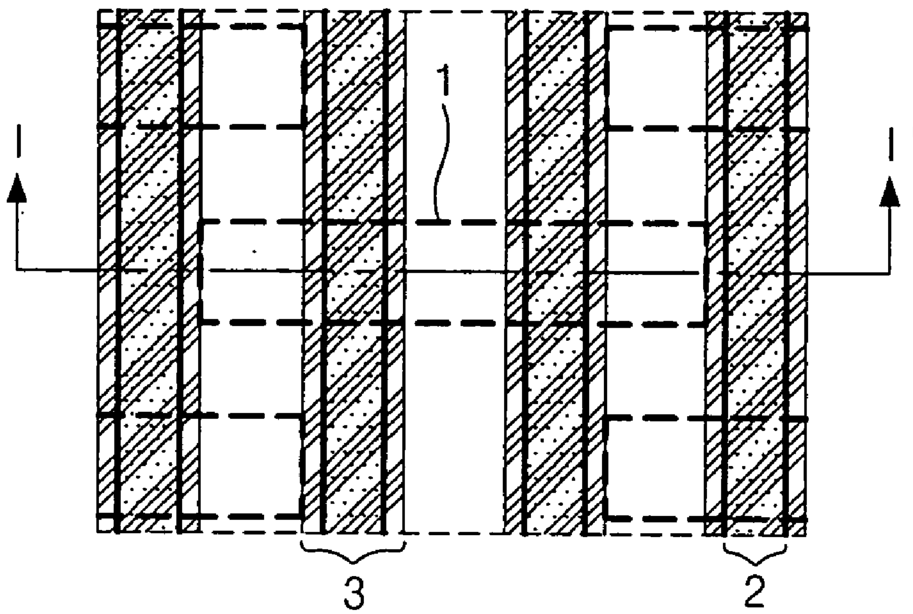


Fig.1
(Prior Art)

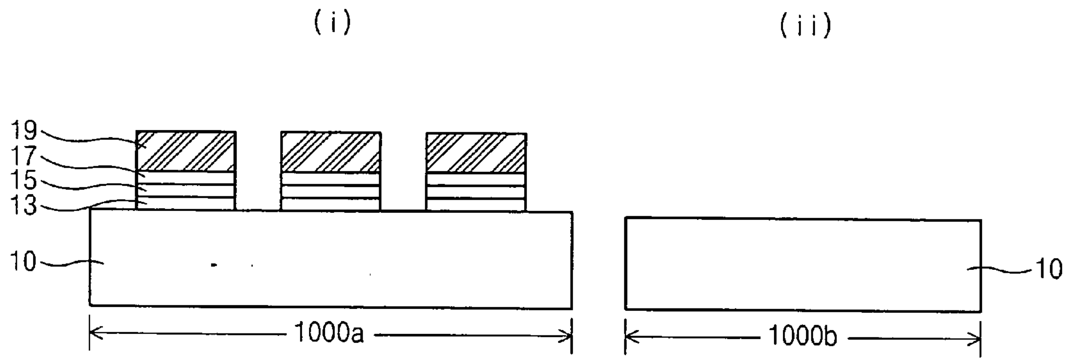


Fig.2A
(Prior Art)

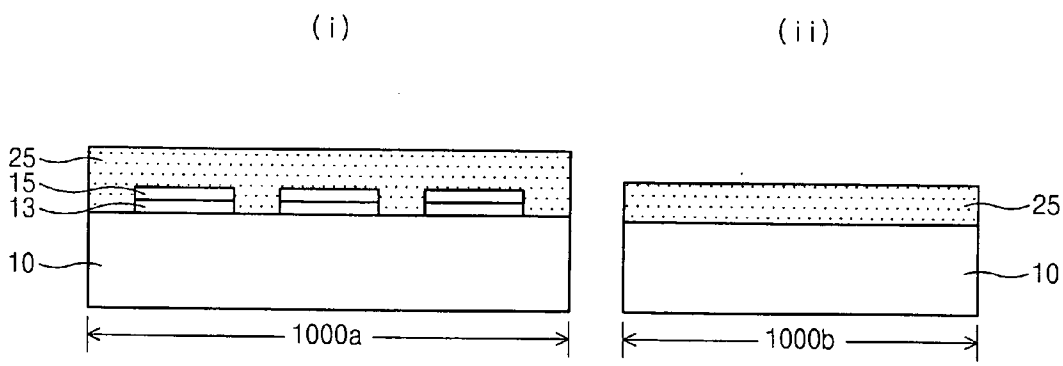


Fig.2B
(Prior Art)

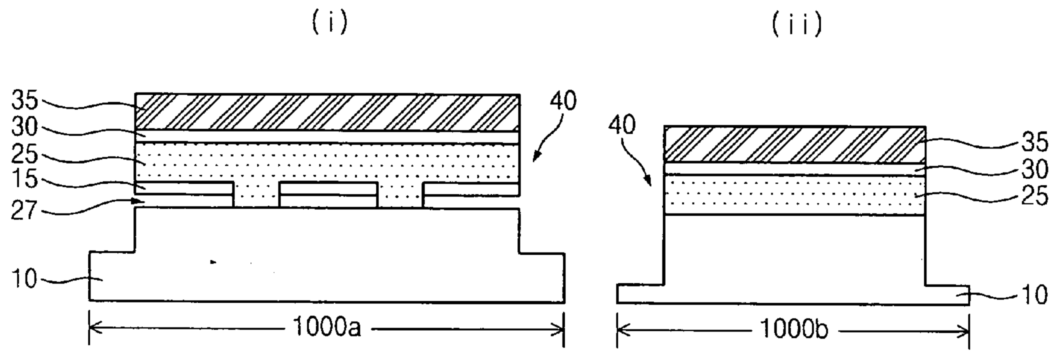


Fig.2C
(Prior Art)

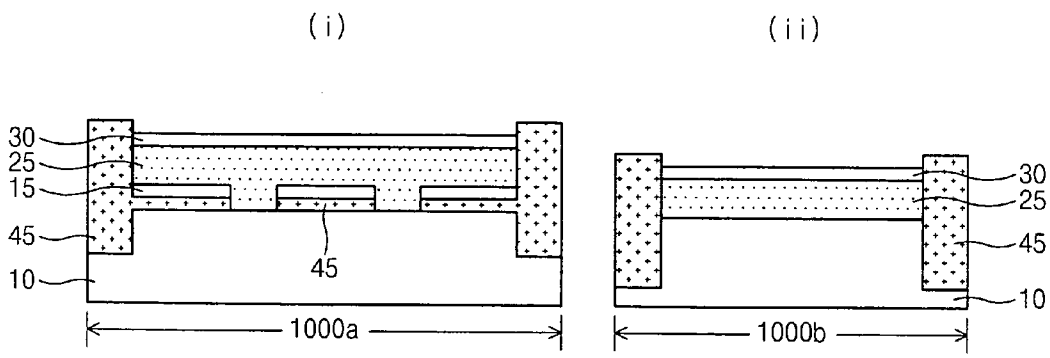


Fig.2D
(Prior Art)

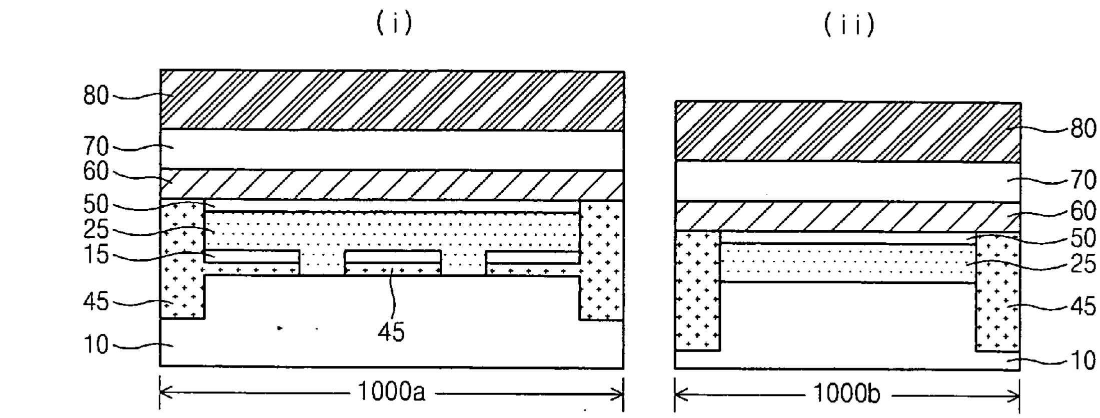


Fig.2E
(Prior Art)

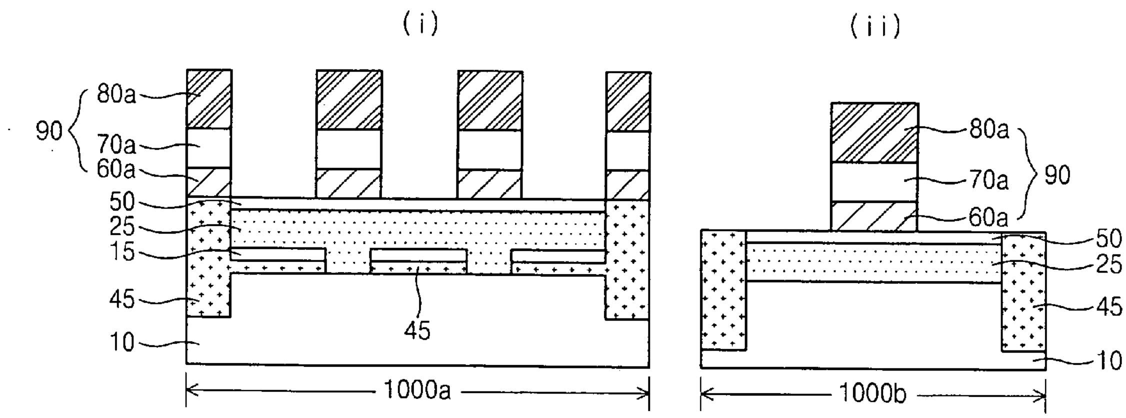


Fig.2F
(Prior Art)

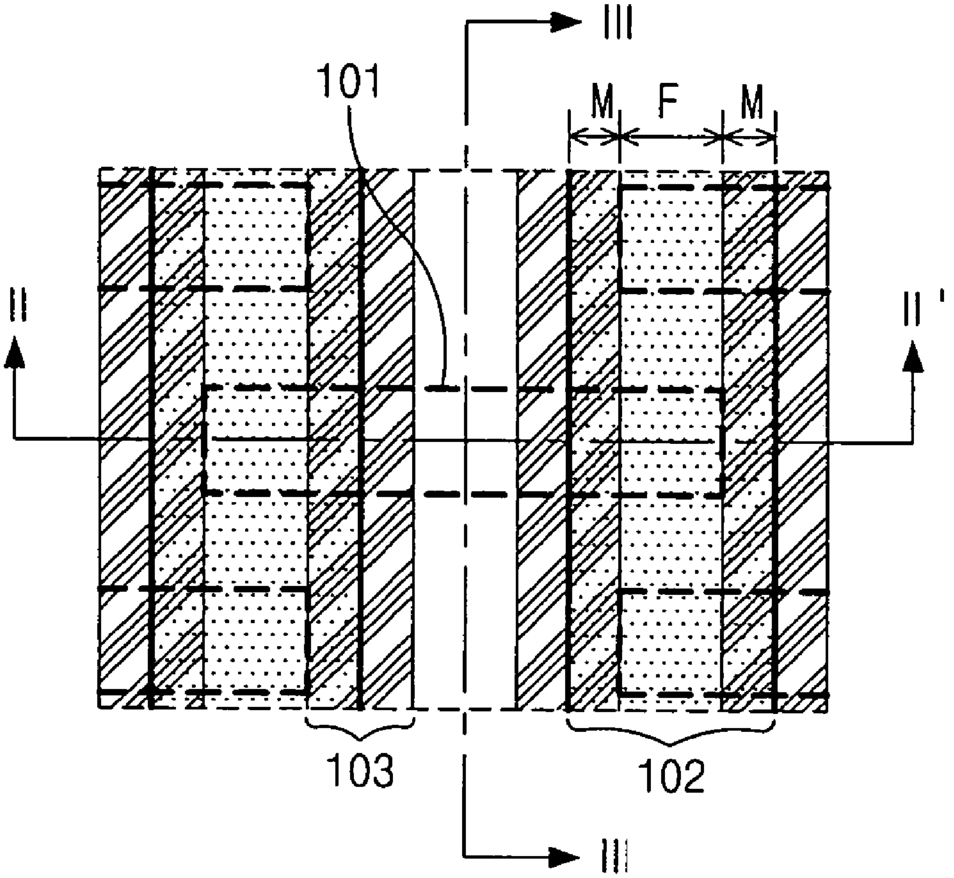


Fig.3

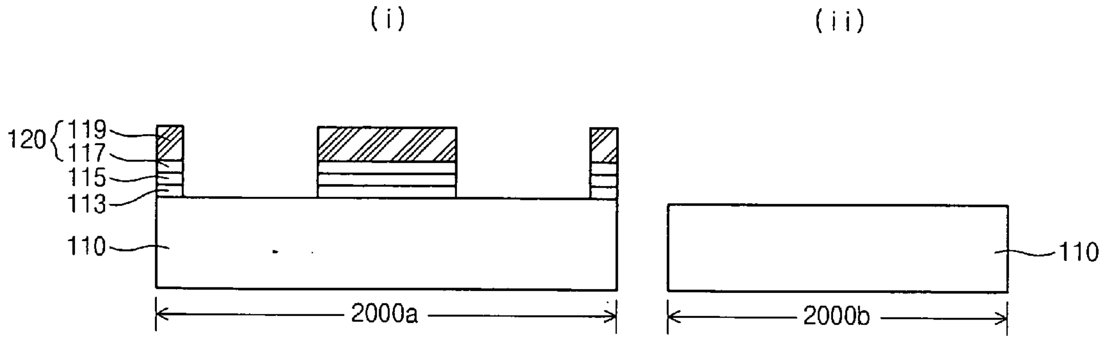

(i)
(ii)
120
119
117
115
113
110
110
2000a
2000b

Fig.4A

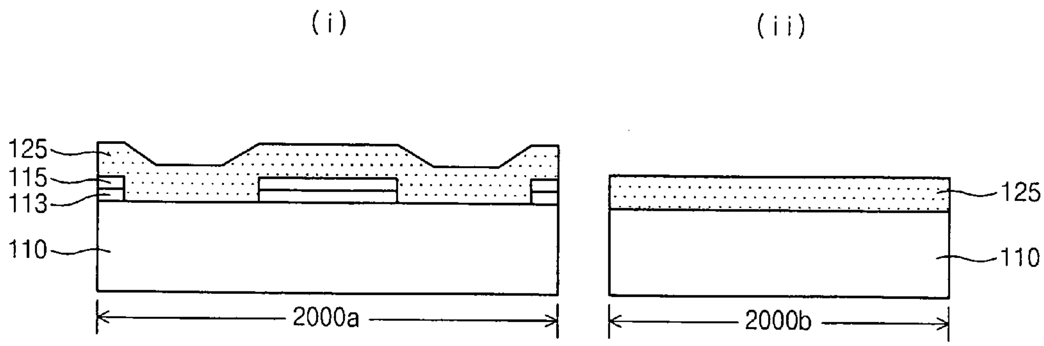

(i)
(ii)
125
115
113
110
125
110
2000a
2000b

Fig.4B

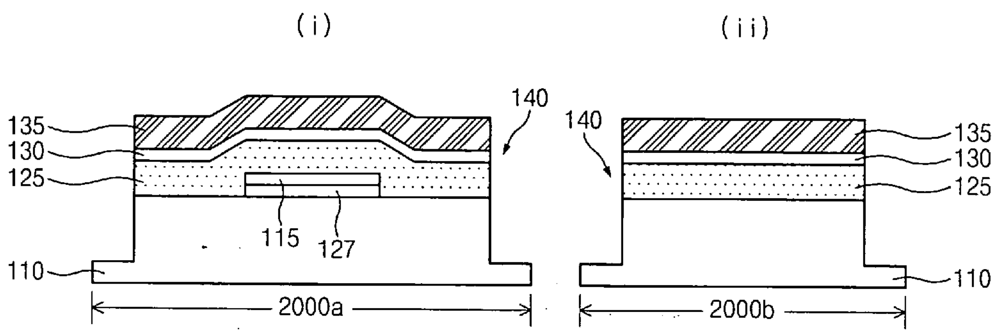

(i)
(ii)
135
130
125
140
115
127
110
2000a
140
135
130
125
110
2000b

Fig.4C

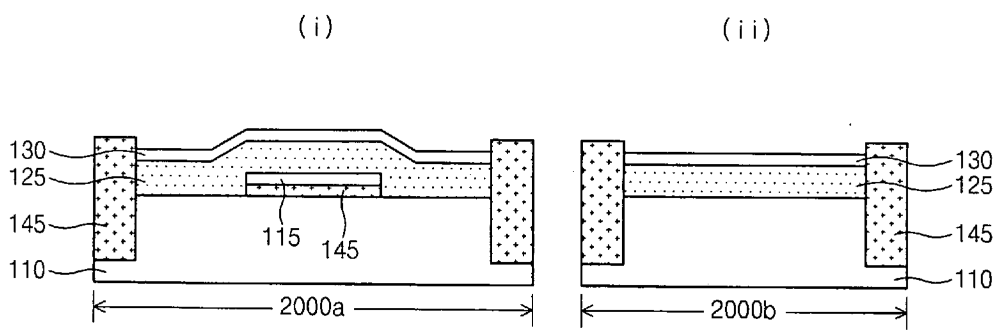

(i)
(ii)
130
125
145
110
115
145
2000a
130
125
145
110
2000b

Fig.4D

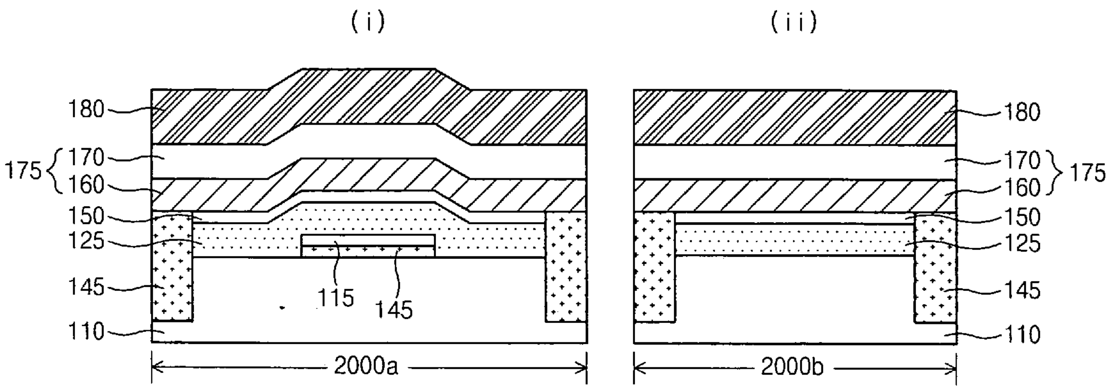

(i)
(ii)
180
175
170
160
150
125
145
115
145
110
2000a
2000b

Fig.4E

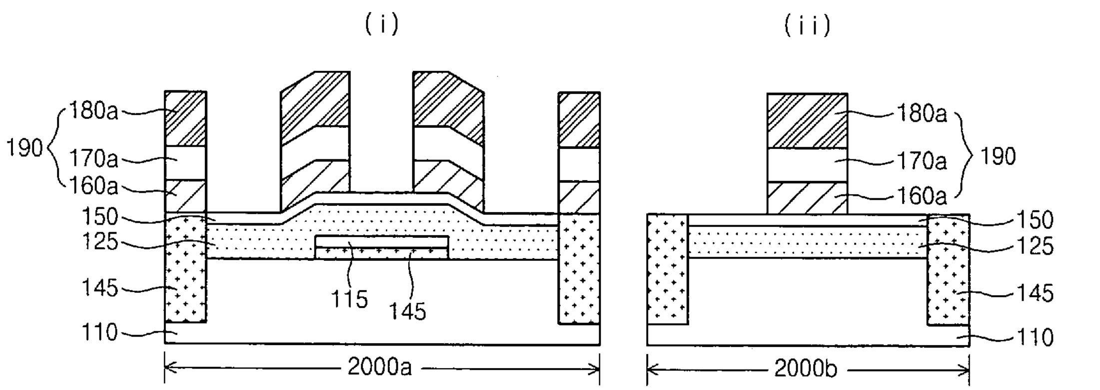

(i)
(ii)
190
180a
170a
160a
150
125
145
115
145
110
2000a
2000b

Fig.4F

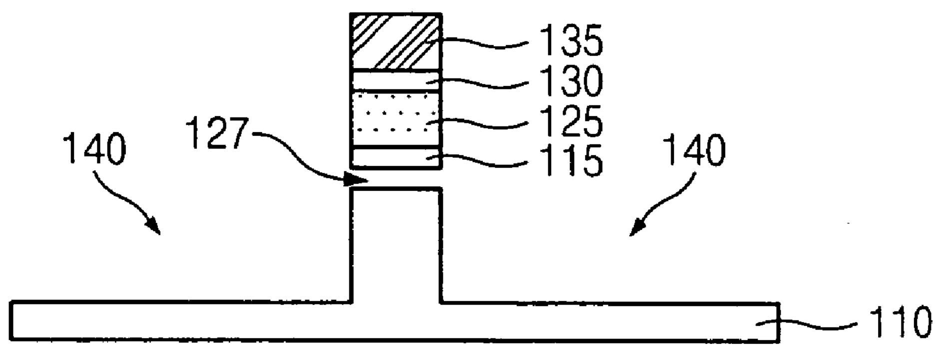


Fig.5

METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to a method for fabricating a semiconductor device, and more specifically to a method for fabricating a semiconductor device wherein a gate is formed on a stepped Si epitaxial layer in order to increase an effective length of a gate channel, and an oxide film is only formed at the interface of the Si epitaxial layer under a bit line contact and the semiconductor substrate, thereby improving a characteristic of a leakage current for a storage node junction.

[0003] 2. Description of the Related Art

[0004] **FIG. 1** is a layout illustrating a conventional method for fabricating a semiconductor device, wherein reference numerals **1000***a*, **1**, **2** and **3** denote a cell region, an active region, a first gate region and a second gate region, respectively.

[0005] **FIGS. 2***a* through **2***f* are cross-sectional views illustrating a conventional method for fabricating a semiconductor device, wherein **FIGS. 2***a*(i) through **2***f*(i) are cross-sectional views taken along the line I-I' in **FIG. 1**, and **FIGS. 2***a*(ii) through **2***f*(ii) are cross-sectional views in a core/peripheral circuit region **1000***b*.

[0006] Referring to **FIG. 2***a*, a stacked structure of a SiGe epitaxial layer (not shown), a first Si epitaxial layer (not shown), a first oxide film (not shown) and a first nitride film (not shown) is formed on a semiconductor substrate **10** having a cell region **1000***a* and a core/peripheral circuit region **1000***b* defined therein.

[0007] Next, a first photoresist film (not shown) is deposited on the entire surface of the first nitride film (not shown) in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0008] Thereafter, the first photoresist film (not shown) is exposed and developed to form a first photoresist film pattern (not shown) exposing the first gate region **2** of **FIG. 1** and cover the entire core/peripheral circuit region **1000***b*.

[0009] After that, the stacked structure is etched using the first photoresist film pattern as an etching mask to expose the semiconductor substrate **10** of the first gate region **2** and the entire core/peripheral circuit region **1000***b*.

[0010] The first photoresist film pattern is then removed.

[0011] Referring **FIG. 2***b*, a first nitride film pattern **19** and a first oxide film pattern **17** in the cell region **1000***a* are removed via a wet etching method.

[0012] Next, a second Si expitaxial layer **25** is formed on the entire surface of the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0013] Referring to **FIG. 2***c*, a second oxide film **30** and a second nitride film **35** are formed on the second Si epitaxial layer **25** in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0014] Next, a second photoresist film (not shown) is deposited on the entire surface of the second nitride film **35**. The second photoresist film is then exposed and developed to form a second photoresist film pattern (not shown) defining the active region **1** of **FIG. 1** in the cell region **1000***a*, and also an active region in the core/peripheral circuit region **1000***b*.

[0015] Thereafter, the second nitride film **35**, the second oxide film **30**, the second Si epitaxial layer **25**, the first Si epitaxial layer pattern **15**, the SiGe epitaxial layer pattern **13** and a predetermined thickness of the semiconductor substrate **10** are etched using the second photoresist film pattern as an etching mask to form a trench **40** in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0016] After that, the second photoresist film pattern (not shown) is removed. The SiGe epitaxial layer pattern **13** is then etched through a sidewall of the trench **40** via a wet etching method to form a space **27** under the first Si epitaxial layer pattern **15**.

[0017] Referring to **FIG. 2***d*, a gap-filling insulating film **45** is formed on the entire surface to fill up the space **27** and the trench **40** in the cell region **1000***a* and to fill up the trench **40** in the core/peripheral circuit region **1000***b*.

[0018] Next, the gap-filling insulating film **45** is polished until the second nitride film **35** is exposed. The gap-filling insulating film **45** serves as a device isolation film.

[0019] Thereafter, a predetermined thickness of the gap-filling insulating film **45** in the trench **40** is etched. The second nitride film **35** is then removed via a wet etching method.

[0020] After that, a well implant process and a channel implant process are performed so as to adjust impurity concentrations in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0021] Referring to **FIG. 2***e*, the second oxide film **30** in the cell region **1000***a* and the core/peripheral circuit region **1000***b* is removed via a wet etching method to expose the second Si epitaxial layer **25**. A gate oxide film **50** is then formed on the exposed second Si epitaxial layer **25**.

[0022] Next, gate conductive layers **60** and **70**, and a hard mask insulating film **80** are formed on the gate oxide film **50** and the gap-filling insulating film **45** in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0023] Referring to **FIG. 2***f*, a third photoresist film (not shown) is deposited on the hard mask insulating film **80** in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0024] Thereafter, the third photoresist film (not shown) is exposed and developed to form a third photoresist film pattern defining the second gate region **3** of **FIG. 1** and a gate region (not shown) in the core/peripheral circuit region **1000***b*. Specifically, the third photoresist film pattern exposes a bit line contact region and storage node contact regions in the cell region **1000***a* and covers a region where a gate is to be formed in the core/peripheral circuit region **1000***b*.

[0025] Next, the hard mask insulating film **80** and the gate conductive layers **70** and **60** are etched using the third photoresist film pattern as an etching mask to respectively form a gate **90** in the cell region **1000***a* and the core/peripheral circuit region **1000***b*.

[0026] However, in accordance with the above-described conventional method, the gate **90** of the active region is formed on a plane second Si epitaxial layer. As a result, a gate channel length is decreased as a design rule of the semiconductor device is reduced.

[0027] Moreover, an oxide film is formed at the interface of the Si epitaxial layer under a storage node contact and the semiconductor substrate. Accordingly, the leakage current for a storage node junction is highly depended upon an interface characteristic between the Si epitaxial layer and an oxide film.

[0028] In addition, the SiGe epitaxial layer under the storage node contact is removed for forming a device isolation film. As a result, Ge in the SiGe epitaxial layer is diffused into the first Si epitaxial layer, the second Si epitaxial layer and the semiconductor substrate due to heat treatment processes prior to the formation of the device isolation film. Accordingly, there is a problem such as increase in the leakage current for the storage node junction.

SUMMARY OF THE INVENTION

[0029] It is an object of the present invention to provide a method for fabricating a semiconductor device wherein a gate is formed on a stepped Si epitaxial layer to increase an effective length of a gate channel, and an oxide film is only formed at the interface of the Si epitaxial layer under a bit line contact and the semiconductor substrate, thereby improving a characteristic of a leakage current for a storage node junction.

[0030] In order to achieve the object of the present invention, there is provided a method for fabricating a semiconductor device comprising the steps:

[0031] (a) forming a SiGe epitaxial layer, a first Si epitaxial layer and an insulating film on a semiconductor substrate, (b) etching a predetermined region of the insulating film, the first Si epitaxial layer and the SiGe epitaxial layer to expose the semiconductor substrate, wherein the predetermined region includes a storage node contact region and a portion of a gate region adjacent thereto, (c) removing the insulating film, (d) forming a second Si epitaxial layer on the entire surface including the exposed semiconductor substrate, (e) etching the second Si epitaxial layer, the first Si epitaxial layer, the SiGe epitaxial layer and a predetermined thickness of the semiconductor substrate to form a trench defining an active region, (f) removing the SiGe epitaxial layer through a sidewall of the trench to form a space under the first Si epitaxial layer, (g) forming a gap-filling insulating film to at least fill up the space and the trench, (h) forming a gate oxide film on the second Si epitaxial layer, and (i) depositing and patterning a gate conductive layer and a hard mask layer on the entire surface to form a gate in the gate region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] **FIG. 1** is a layout illustrating a conventional method for fabricating a semiconductor device.

[0033] **FIGS. 2***a* through **2***f* are cross-sectional views illustrating a conventional method for fabricating a semiconductor device.

[0034] **FIG. 3** is a layout illustrating a method for fabricating a semiconductor device in accordance with a preferred embodiment of the present invention.

[0035] **FIGS. 4***a* through **4***f* and **FIG. 5** are cross-sectional views illustrating a method for fabricating a semiconductor device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0036] Reference will now be made in detail to exemplary embodiments of the present invention. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0037] **FIG. 3** is a layout illustrating a method for fabricating a semiconductor device in accordance with a preferred embodiment of the present invention, wherein reference numerals **2000***a*, **101**, **102** and **103** denote a cell region, an active region, a contact region and a gate region, respectively.

[0038] **FIGS. 4***a* through **4***f* illustrate a method for fabricating a semiconductor device according to a preferred embodiment of the present invention, wherein **FIGS. 4***a*(i) through **4***f*(i) are cross-sectional views taken along the line II-II' of **FIG. 3**, and **FIGS. 4***a*(ii) through **4***f*(ii) are cross-sectional views in a core/peripheral circuit region **2000***b*.

[0039] Referring to **FIG. 4***a*, a stacked structure of a SiGe epitaxial layer (not shown), a first Si epitaxial layer (not shown) and an insulating film (not shown) is formed on a semiconductor substrate **110** having a cell region **2000***a* and a core/peripheral circuit region **2000***b* defined therein. Preferably, the insulating film comprises an oxide film or a stacked structure of an oxide film and a nitride film.

[0040] Next, a first photoresist film (not shown) is deposited on the entire surface of the insulating film in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0041] Thereafter, the first photoresist film (not shown) is exposed and developed to form a first photoresist film pattern (not shown) exposing the contact region **102** of FIG. **3** and cover the entire core/peripheral circuit region **2000***b*. The contact region **102** includes a storage node contact region and a portion of the gate region **103** adjacent thereto. Preferably, the portion of the gate region **103** has a line width of M ranging from ⅓F to F, where F is a gate line width.

[0042] After that, the stacked structure is etched using the first photoresist film pattern as an etching mask to expose the semiconductor substrate **110** of the contact region **102** and the entire core/peripheral circuit region **2000***b*.

[0043] The first photoresist film pattern is then removed.

[0044] Referring to **FIG. 4***b*, an insulating film pattern **120** in the cell region **2000***a* is removed. Preferably, the removal process for the insulating film pattern **120** is performed via a wet etching method.

[0045] Next, a second Si epitaxial layer **125** is formed on the entire surface of the cell region **2000***a* and the core/peripheral circuit region **2000***b*. Preferably, a thickness of the second Si epitaxial layer **125** ranges from 10 nm to 100 nm.

[0046] The second epitaxial layer **125** in the cell region **2000***a* may have a step difference due to the first Si epitaxial layer pattern **115** and the SiGe epitaxial layer pattern **113**.

[0047] Referring to **FIG. 4***c*, a second oxide film **130** and a second nitride film **135** are formed on the second Si epitaxial layer **125** in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0048] Next, a second photoresist film (not shown) is deposited on the entire surface of the second nitride film **135**. The photoresist film is then exposed and developed to form a second photoresist film pattern (not shown) defining the active region **101** of **FIG. 3** in the cell region **2000***a* and also an active region in the core/peripheral circuit region **2000***b*.

[0049] Thereafter, the second nitride film **135**, the second oxide film **130**, the second Si epitaxial layer **125**, the first Si epitaxial layer pattern **115**, the SiGe epitaxial layer pattern **113** and a predetermined thickness of the semiconductor substrate **110** are etched using the second photoresist film pattern as an etching mask to form a trench **140** in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0050] After that, the second photoresist film pattern (not shown) is removed. The SiGe epitaxial layer pattern **113** is then etched through a sidewall of the trench **140** to form a space **127** under the first Si epitaxial layer pattern **115**.

[0051] **FIG. 5** is a cross-sectional view taken along the line III-III' of **FIG. 3** illustrating the structure of **FIG. 4***c*(i) including the space **127** having a undercut structure.

[0052] Preferably, the removal process for the SiGe epitaxial layer pattern **113** is preformed via a wet etching method utilizing a mixed etchant containing HF, H_2O_2 and CH_3CHOOH, a plasma etching method utilizing a mixed gas containing (CF_3 or CH_2F_2), N_2 and O_2, or combinations thereof. Moreover, a volume ratio of HF, H_2O_2 and CH_3COOH in the mixed etchant is preferably 1:2:3.

[0053] Referring to **FIG. 4***d*, a gap-filling insulating film **145** is formed on the entire surface to at least fill up the space **127** and the trench **140** in the cell region **2000***a* and to fill up the trench **140** in the core/peripheral circuit region **2000***b*.

[0054] Preferably, the formation process of the gap-filling insulating film **145** may include forming a thermal oxide film filling up the space **127** and forming an oxide film for a device isolation film filling up the trench **140**. A nitride film may be further formed at an interface of the thermal oxide film and the oxide film for the device isolation film.

[0055] Moreover, the formation process of the gap-filling insulating film **145** may include forming a thermal oxide film to fill up a portion of the space **127**, forming a nitride film to fill up the remaining portion of the space **127**, and forming an oxide film for the device isolation film to fill up the trench **140**.

[0056] Next, the gap-filling insulating film **145** is polished until the second nitride film **135** is exposed. The gap-filling insulating film **145** in the trench **140** serves as a device isolation film.

[0057] Thereafter, a predetermined thickness of the gap-filling insulating film **145** in the trench **140** is etched. The second nitride film **135** is then removed. Preferably, the etching process for the gap-fill insulating film **145** is performed via a wet etching method. The removal process for the second nitride film **135** is preferably preformed via a wet etching method.

[0058] After that, well implant processes and channel implant processes are performed so as to respectively adjust impurity concentrations in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0059] Referring to **FIG. 4***e*, the second oxide film **130** in the cell region **2000***a* and the core/peripheral circuit region **2000***b* is removed to expose the second Si epitaxial layer **125**. A gate oxide film **150** is then formed on the exposed second Si epitaxial layer **125**. Preferably, the removal process for the second oxide film **130** is performed via a wet etching method.

[0060] Next, a stacked structure of a gate conductive layer **175** and a hard mask layer **180** is formed on the gate oxide film **150** and the gap-filling insulating film **145** in the cell region **2000***a* and the core/peripheral circuit region **2000***b*. Preferably, the gate conductive layer **175** comprises a lower conductive layer **160** and an upper conductive layer **170**.

[0061] Referring to **FIG. 4***f*, a third photoresist film (not shown) is deposited on the hard mask layer **180** in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0062] Thereafter, the third photoresist film (not shown) is exposed and developed to form a third photoresist film pattern defining the gate region **103** of **FIG. 3** and a gate region (not shown) in the core/peripheral circuit region **2000***b*. Specifically, the third photoresist film pattern exposes a bit line contact region and storage node contact regions in the cell region **2000***a* and covers a region where a gate is to be formed in the core/peripheral circuit region **2000***b*.

[0063] Next, the stacked structure is patterned using the third photoresist film pattern as an etching mask to respectively form a gate **190** in the cell region **2000***a* and the core/peripheral circuit region **2000***b*.

[0064] In addition, subsequent processes such as an ion-implant process for forming source/drain regions in the active regions, a process for forming a spacer on a sidewall of the gate **190**, a process for forming a landing plug, a process for forming a bit line contact and a bit line, a process for forming a capacitor and a process for forming an interconnect may be done.

[0065] As described above, the method for fabricating a semiconductor device in accordance with the present invention provides exposing the contact region including the storage node contact region and a portion of the gate region adjacent thereto and only forming an oxide film at the interface of the Si epitaxial layer under both a bit line contact and the semiconductor substrate. Accordingly, capacitance for a bit line contact and a short-channel effect of a cell transistor are improved.

[0066] As shown in **FIG. 4***f*, the gate **190** in the cell region **2000***a* is formed on a structure having a step difference instead of over a plane structure to increase an effective length of the gate channel, and the storage node contact is formed on the Si epitaxial layer without the oxide film to minimize the leakage current of the storage node junction. Accordingly, a refresh characteristic of a DRAM can be improved.

[0067] The foregoing description of various embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. The embodiments were chosen and described in order to explain the principles of the invention and its practical application to enable one skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a SiGe epitaxial layer, a first Si epitaxial layer and an insulating film on a semiconductor substrate;

(b) etching a predetermined region of the insulating film, the first Si epitaxial layer and the SiGe epitaxial layer to expose the semiconductor substrate, wherein the predetermined region includes a storage node contact region and a portion of a gate region adjacent thereto;

(c) removing the insulating film;

(d) forming a second Si epitaxial layer on the entire surface including the exposed semiconductor substrate;

(e) etching the second Si epitaxial layer, the first Si epitaxial layer, the SiGe epitaxial layer and a predetermined thickness of the semiconductor substrate to form a trench defining an active region;

(f) removing the SiGe epitaxial layer through a sidewall of the trench to form a space under the first Si epitaxial layer;

(g) forming a gap-filling insulating film to at least fill up the space and the trench;

(h) forming a gate oxide film on the second Si epitaxial layer; and

(i) depositing and patterning a gate conductive layer and a hard mask layer on the entire surface to form a gate in the gate region.

2. The method according to claim 1, wherein the step (b) comprises:

forming a photoresist film on the entire surface of the semiconductor substrate;

forming a photoresist film pattern exposing the predetermined region by exposing and developing the photoresist film, wherein the portion of the gate region of the predetermined region has a line width of M; and

etching the insulating film, the Si epitaxial layer and the SiGe epitaxial layer using the photoresist film pattern as an etching mask.

3. The method according to claim 2, wherein the M ranges from ⅓F to F, wherein F is a gate line width.

4. The method according to claim 1, wherein the insulating film comprises an oxide film.

5. The method according to claim 1, wherein the insulating film comprises a stacked structure of an oxide film and a nitride film.

6. The method according to claim 1, wherein the removal process for the insulating film in the step (e) is performed via a wet etching method.

7. The method according to claim 1, wherein a thickness of the second Si epitaxial layer ranges from 10 to 100 nm.

8. The method according to claim 1, wherein the removal process for the SiGe epitaxial layer in the step (f) is performed via one method selected from the group consisting of a wet etching method utilizing a mixed etchant containing HF, H_2O_2 and CH_3COOH, a plasma etching method utilizing a mixed gas containing (CF_4 or CH_2F_2), N_2 and O_2, and combinations thereof.

9. The method according to claim 8, wherein a volume ratio of HF, H_2O_2 and CH_3COOH in the mixed etchant is 1:2:3.

10. The method according to claim 1, wherein the step (g) comprises:

forming a thermal oxide film filling up the space; and

forming an oxide film for a device isolation film to fill up the trench.

11. The method according to claim 10, further comprising

forming a nitride film at the interface of the thermal oxide film and the oxide film for the device isolation film.

12. The method according to claim 1, wherein the step (g) comprises:

forming a thermal oxide film to fill a portion of the space;

forming a nitride film to fill up a remaining portion of the space; and

forming an oxide film for the device isolation film to fill up the trench.

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