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(54) Title: VOLTAGE WAVEFORM GENERATOR FOR PLASMA PROCESSING APPARATUSES

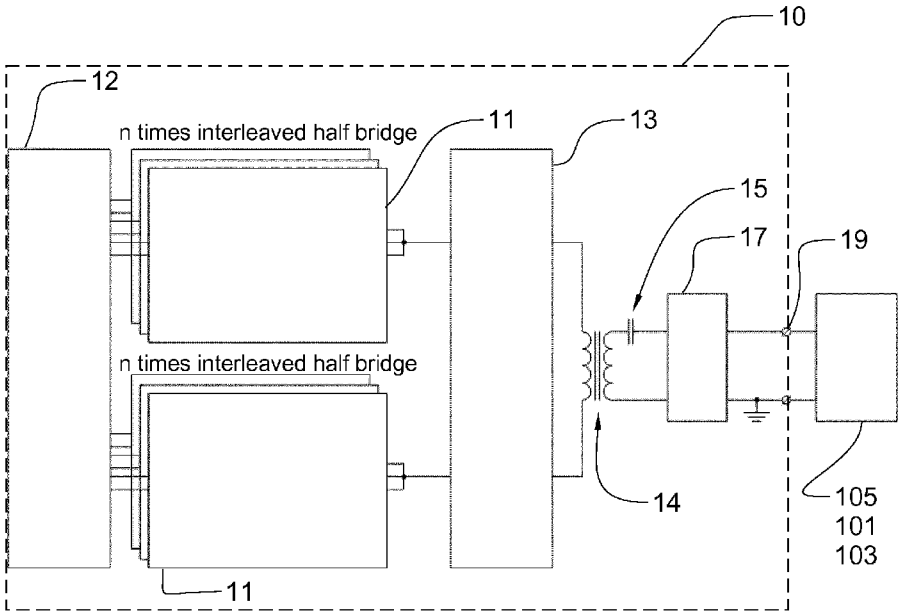

FIG 2

(57) Abstract: Plasma processing apparatus (100), comprising means for generating a plasma (103), a processing platform (105) for supporting a substrate (101) to be processed, and a voltage waveform generator (10) comprising an output (19) electrically coupled to the processing platform. The voltage waveform generator comprises a plurality of first buck converters (11) arranged in parallel and coupled to the output, the first buck converters comprising actively switchable semiconductor switches (111), and a control unit (130) configured to operate the actively switchable semiconductor switches through pulse width modulation signals. The control unit is configured to operate the plurality of first buck converters in an interleaved manner.

[Continued on next page]

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Voltage waveform generator for plasma processing apparatuses

Technical field

[0001] The present invention is related to a plasma processing apparatus comprising a voltage waveform generator, in particular for producing a voltage bias on the substrate to be plasma processed. The voltage bias is advantageously used for controlling the ion energy in plasma assisted etching or plasma assisted layer deposition.

Background art

[0002] In plasma assisted etching and plasma assisted layer deposition radio frequency (RF) generators are used to generate a bias voltage for controlling the ion energy. To improve process control, accurate control of the bias voltage and the resulting ion energy distribution is of importance. Generating this bias voltage is done with limited efficiency (wideband) linear amplifiers or with limited flexibility (narrowband) switch-mode amplifiers or dedicated pulse generating amplifiers. Most amplifiers are only indirectly controlling the output voltage waveform (e.g. controlling output power or relying on calibration). Due to non-idealities and parameter variation in the system, this approach is resulting in limited performance (the generated waveform is less close to the desired output voltage waveform, resulting in a less desired ion energy distribution) and limited reproducibility (wafer to wafer variation and system to system variation).

[0003] US 9208992 describes a plasma processing apparatus comprising a switch mode power supply for forming a periodic voltage function at an exposed surface of the substrate to be processed. The periodic voltage function effectuates a desired ion energy intensity distribution to perform etching of the substrate or plasma deposition on the substrate. The switch mode power supply can be realized by buck, boost and/or buck-boost type power technologies. The switch mode power supply comprises two switch components that are coupled in a half-bridge and are controlled based on drive signals generated by a controller.

[0004] A disadvantage of the above switch mode power supply is that it can only generate a block shape waveform with a DC current to compensate for the ion current (see Fig. 14). However, in current plasma-based processing apparatuses, there is a tendency to apply direct voltage control of the bias by a tailored waveform. Therefore, there is a need in the art of a voltage waveform generator that has a desired flexibility to provide an arbitrary waveform with possibly high bandwidth. However, to obtain such

high bandwidth with the above power supplies would impose an extremely high switching frequency on the switching components, which is unfeasible.

[0005] The RF amplifiers used to generate sinusoidal bias voltage waveform have typically a 50 Ohm output impedance. A matching network (called match box in the industry, which is placed between the amplifier and the substrate table) is used to convert the complex plasma impedance to a real 50 Ohm impedance. Depending on the process conditions, this results in high reactive current through the matching network, which result in significant losses. This makes matching boxes expensive system components.

Summary of the invention

[0006] Various chemical processes are performed through assistance of a plasma, some of which require a high precision, whereas others require a high power. Current plasma processing apparatuses do not allow sufficient flexibility to address both needs, or provide such flexibility at increased cost or at the expense of operational efficiency.

[0007] It is an aim of the present invention to overcome the above drawbacks. It is an aim of the present invention to provide a voltage waveform generator, such as in a plasma processing apparatus, which allows for generating a large variation of desired voltage waveforms with no or limited efficiency loss.

[0008] It is an aim of the present invention to provide plasma processing apparatuses that allow for being used in a variety of operational modes to address the above needs of high precision on the one hand and high power on the other.

[0009] It is an aim of the present invention to eliminate the need for a matching network for converting the plasma impedance to a 50 Ohm impedance. It is an aim to provide a plasma processing apparatus that does not require such a matching network, and hence wherein such a matching network is absent.

[0010] According to the present invention, there is therefore provided a plasma processing apparatus as set out in the appended claims. The plasma processing apparatus, which can be configured for plasma assisted etching, or for plasma assisted layer deposition, comprises means for generating a plasma, a processing platform for supporting a substrate to be processed and a voltage waveform generator comprising an output electrically coupled to the processing platform, e.g. for providing a bias voltage to the platform. The voltage waveform generator comprises a plurality of first buck converters (herein referred to as buck cells) arranged in parallel and coupled to the output, the first buck converters comprising actively switchable semiconductor switches

and a control unit configured to operate the actively switchable semiconductor switches through pulse width modulation signals. The control unit is configured to operate the plurality of first buck converters in an interleaved manner.

[0011] With a voltage waveform of the above kind, it becomes possible to generate a large variation of desired voltage waveforms, while keeping switching efficiency at high levels.

[0012] Advantageously, the voltage waveform generator comprises a plurality of second buck converters arranged in parallel and coupled to the output, the second buck converters comprising actively switchable semiconductor switches which are operated by the control unit. Advantageously, the plurality of first buck converters and the plurality of second buck converters are arranged in parallel. As a result, a parallel arrangement of multiple (two or even more) sets of n interleaved buck converters is obtained, enabling to distribute the current and therefore reduce loading on the semiconductor switches of the individual buck converters.

[0013] The buck converters can be coupled via current or voltage. In case of voltage coupling, the voltage waveform generator advantageously comprises a capacitor acting as an input filter.

[0014] Optionally, a (high frequency, such as RF) transformer is coupled between the buck converters and the output to increase, or alternatively decrease the output voltage of the buck converters.

[0015] A DC blocking capacitor is advantageously coupled between the buck converters and the output. In case a transformer is provided as indicated above, the DC blocking capacitor is advantageously coupled at the secondary side of the transformer. The DC blocking capacitor advantageously has a capacitance in the range between about 10 pF and about 200 nF, advantageously between about 100 pF and about 100 nF. Such a DC blocking capacitor advantageously prevents saturation of the transformer, and even in case the transformer is omitted, to reduce voltage stress on the semiconductor switches of the buck converter since the DC bias voltage is placed over the blocking capacitor instead of over the semiconductors, enabling the use of more economical semiconductor switches, and hence obtaining a more economical voltage waveform generator.

[0016] Advantageously, the voltage waveform generator comprises a linear power amplifier coupled to the output, advantageously in parallel with the first buck converters. Each set of interleaved buck converters (e.g., the first and second buck converters) can have a separate linear power amplifier coupled in parallel. The linear power amplifier is advantageously operated through the control unit. Such a linear power

amplifier allows to increase the bandwidth of the voltage waveform generator and/or to reduce the switching speed of the semiconductor switches of the buck converters. Hence, more economical semiconductor switches can be used and/or voltage waveforms of higher frequency can be generated.

[0017] According to another aspect, a method of controlling or operating a plasma processing apparatus is described herein.

Brief description of the figures

[0018] Aspects of the invention will now be described in more detail with reference to the appended drawings, wherein same reference numerals illustrate same features and wherein:

[0019] Figure 1 represents an example of a voltage waveform generator used as bias generator for an ICP (Inductively Coupled Plasma) reactor according to aspects of the present invention;

[0020] Figure 2 represents a block diagram of a voltage waveform generator according to the invention;

[0021] Figure 3 represents a second block diagram of another voltage waveform generator according to the invention which differs from the diagram of Fig. 2 in that linear power amplifiers are added in parallel with the interleaved buck cells;

[0022] Figure 4 represents a third block diagram of yet another voltage waveform generator according to the invention which differs from the diagram of Fig. 2 or Fig. 3 in that only one set of interleaved buck cells is provided in asymmetry with respect to the transformer;

[0023] Figure 5 represents a fourth block diagram of yet another voltage waveform generator according to the invention which differs from the diagram of Fig. 3 in that the linear power amplifiers are coupled in parallel with the interleaved buck cells and the (primary) filter;

[0024] Figure 6 represents a fifth block diagram of yet another voltage waveform generator according to the invention which differs from the diagram of Fig. 2 in that the sets of interleaved buck cells are coupled through capacitors;

[0025] Figure 7 represents an electric scheme of a single buck cell as can be used in Figs. 2-6;

[0026] Figure 8 represents a flow diagram of a control method for operating the voltage waveform generator according to various operational modes;

[0027] Figure 9 represents a block diagram of a voltage waveform generator, which can be any one of the voltage waveform generators as described in relation to Figs. 2-6, including a protection circuit for overcurrent detection;

[0028] Figure 10 represents a block diagram of a voltage waveform generator, which can be any one of the voltage waveform generators as described in relation to Figs. 2-6, including a protection circuit for current limiting;

[0029] Figure 11 represents graphs of substrate voltage, resulting arbitrary voltage waveform generator (ABVG) output current and ideal ABVG output voltage required for achieving the target substrate voltage in an optimal case;

[0030] Figure 12 represents graphs of substrate voltage, resulting ABVG output current and ABVG output voltage required for achieving the target substrate voltage in a suboptimal case.

Description of embodiments

[0031] Plasmas can be complex and different recipes (used chemicals and process settings) have different requirements on IED and hence on the desired bias voltage waveform. In this invention a flexible wideband arbitrary voltage waveform generator (ABVG) is proposed with a high efficiency switched mode architecture. The ABVG can optionally be assisted with performance increasing linear amplifiers (resulting in a higher overall system bandwidth).

[0032] Fig. 1 shows one to the typical usages of the ABVG 10 in an Inductively Coupled Plasma (ICP) apparatus 100, where the ABVG 10 is controlling the substrate 101 (typically a wafer) voltage by controlling the substrate stage voltage. In a plasma reactor 102, a plasma 103 is generated by introduction of a plasma forming gas 104 in a dielectric tube 108 surrounded by an induction coil 107. The arrangement forms a plasma torch which directs the plasma 103 towards a stage or platform 105 on which the substrate 101 is positioned. A RF voltage is applied to the induction coil 107 through a RF power supply 120, and a matching network 121 as known in the art. Optionally, a precursor 109 can be introduced in the plasma reactor 102. The RF power supply 120 and the ABVG 10 can be controlled by a system host controller 130.

[0033] The ABVG 10 can also be used in other configurations like:

- In a Capacitively Coupled Plasma (CCP) reactor;
- Direct inter connection (not via the system host) of control signals between source power generator (RF power supply) and ABVG is possible.

A different source could be used to generate the plasma (e.g. Capacitively Coupled Plasma, Electron Cyclotron Resonance, Magnetron, DC voltage, etc.).

[0034] Possible system architectures of the voltage waveform generator according to the invention are shown in Figs. 2-6. Fig. 4 is the most basic scheme.

[0035] Referring to Figs. 2-6, the desired output voltage at output terminals 19 of the voltage waveform generator 10 is generated by pulse width modulation (PWM) controlled Buck cells 11. A possible implementation of one such Buck cell 11 is a half bridge comprising actively switchable semiconductor switches 111 as represented in Fig. 7. The PWM is typically generated by a PWM generator 12; e.g. a Field Programmable Gate Array (FPGA). Multiple buck cells 11 can be placed in parallel to distribute the current. The Buck cells PWM will be applied out of phase (i.e. interleaved operation) to reduce the ripple current and increase the effective switching frequency f_{sw_eff}. The Buck cell output voltage is filtered by a filter 13 to remove harmonic components.

[0036] Buck cell current sharing can be taken care of by measuring the coil currents of the buck cell and adjusting the PWM signals that control the buck cell in such a way that the current is evenly distributed between the buck cells.

[0037] A transformer 14 is increasing (but could also decrease) the filtered Buck cell output voltage by the transformer turn ratio to the level required for the system. The DC bias voltage of the substrate table potential is automatically placed over the DC blocking capacitor 15 after the transformer 14. This is reducing the voltage stress on the transformer 14 and on the Buck cells 11. The DC blocking capacitor 15 is also preventing secondary DC current (e.g. due to a DC potential of the plasma) to saturating the transformer. Prevention of transformer saturation on the primary side can be done by measuring the current and adjusting the generated PWM signals to prevent a DC voltage over the primary side of the transformer, e.g. by controller 16. An (optional) EMC filter 17 is used to filter high frequency components generated the ABVG for normative compliance.

[0038] With more complex transformer arrangements it is possible to place more than 2 interleaved half-bridges (buck cells 11) in parallel.

[0039] With appropriate voltage levels on the Buck cell power supply and of the desired bias voltage it is possible to omit the transformer 14. Note that possible Buck cell voltage levels are limited by the available semiconductor switches 111.

[0040] The transformer output side can comprise multiple tabs enabling the user to select the turn ratio of the transformer and therefore the output voltage range. Alternatively, the ABVG can comprise (internal) relays to switch between a plurality of output voltage settings.

[0041] There are limitations to the switching speed of the available semiconductor switches 111. This can be overcome with linear amplifiers 18 which can

have a higher bandwidth. To increase the ABVG bandwidth linear power amplifiers 18 can be added for generation of some higher harmonics (which typically contain less energy) at the expense of some efficiency loss. The controller 16 in the ABVG can control both the PWM generation 12 and the (optional) linear power amplifiers 18. The digital output supplied by controller 16 is converted to an analog signal via D/A converters 28 before being fed to the linear power amplifiers 18.

[0042] To prevent DC biasing / saturation of the transformer in Fig. 4 a DC blocking capacitor 15 is provided. Alternatively, the transformer primary can be connected to a split bus (shared with the buck cells 11) instead of to ground. The EMC filter in Fig. 4 is optional.

[0043] By generation of phase shifted PWM signal for operation of multiple Buck cells in parallel the effective switching frequency f_{sw_eff} (f_{sw_eff} = n * 2 * switching frequency of one Buck cell) can be increased. With this topology any waveform can be synthesized by generation of a corresponding PWM signals. A repeating waveform can be seen as a sum of its Fourier components. As rule of thumb the highest frequency that can be generated with this ABVG topology is f_{sw_eff} / 5. The more Fourier components that can be made the better the desired voltage waveform is reproduced. With this topology any waveform with Fourier components up to approximately f_{sw_eff} / 5 can be generated.

[0044] With this topology the Buck cells can be implemented with the for the state-of-the-art best-in-class semiconductor switches (at the moment of writing GaN HEMT devices). These switches can switch very fast resulting in low turn on and turn off loss and therefore a high efficiency. To further increase the efficiency, the converter can be operated in zero voltage switching (ZVS). This can be done by reducing the inductance value of the Buck cell inductor 112.

[0045] Implementing a closed loop voltage control system with internal and optional external sensors can further improve voltage waveform generation and reproducibility. The direct control of the bias voltage and therefore the ion velocity can result in a much lower power consumption on system level, compared to what is shown by the state-of-the-art (possibly up to an order of magnitude lower).

[0046] Depending on the process in the plasma chamber 102 high accuracy (e.g. atomic layer etching) or high power (e.g. sputtering) is required. For high power processes like sputtering, a lower accuracy can be tolerated. As a result, the ABVG controller 16 requires less bandwidth in such a mode of operation, allowing for a lower effective switching frequency. According to one aspect, the controller 16 is implemented with a control program or method configured to allow for selecting different

modes of operation of the ABVG. By way of example, the flow chart of Fig. 8 shows possible selections. Advantageously, at least two, advantageously at least three modes of operation are implemented in the controller 16 corresponding to different power levels and/or different levels of switching frequency: low power, high power, and possibly medium power, corresponding to a low, high or medium switching frequency, respectively. The modes of operation can be selected on the basis of selection between at least two voltage levels and/or at least two current levels.

[0047] Selecting a low voltage results in a lower bus voltage (supply voltage of the buck cells). Selecting a low current results in a lower current level of the ABVG protection circuit. This protection circuit can be configured to behave in two ways. In a first case, referring to Fig. 9, the protection circuit 161 is configured as an overcurrent detection circuit configured to measure the output current (e.g. at the secondary side of transformer 14); when the current is too high, the protection circuit 161 will emit a disable signal to disable the ABVG power stage and an error is raised. In a second case, referring to Fig. 10, the protection circuit 162 is configured as a current limiting circuit configured to measure the output current (e.g. at the secondary side of transformer 14); when the current is too high the protection circuit 162 reduces the output voltage which lowers / limits the output current (behavior like a typical lab supply).

[0048] Referring to Figs. 9 and 10, it will be convenient to note that the controller 16, the PWM generator 12, the waveform generator 26, any D/A converters (e.g. for the linear amplifiers), the control (feedback) loops and the protection circuit(s) 161, 162 can be integrated in one or more field-programmable gate arrays (FPGA) 36. The waveform generator 26 can be configured to provide an output voltage setpoint, optionally with predistortion. Controller 16 can comprise a control loop with feedback.

[0049] For a narrow ion energy distribution (IED), the substrate voltage should advantageously be flat during t_{ON} as shown in Fig. 11. To achieve this the capacitive charging of the substrate (and holder) is advantageously compensated by adjusting the ABVG output voltage, dV_{OUT}/dt during t_{ON}. A flat substrate voltage during t_{ON} results in a continuous ion current and therefore a continuous ABVG output current during t_{ON}. This can be obtained by the ABVG, by providing a current measuring unit configured to measure the ABVG output current and coupled to the controller configured to adjusting the dV_{OUT}/dt during t_{ON}.. This is one example of an indirectly measured process parameter which is used to adjust the ABVG output voltage. This improves process performance, in this case it results in better control of the IED. Referring to Fig. 12, substrate voltage, resulting ABVG output current and ABVG output voltage required for achieving the target substrate voltage in a suboptimal case are shown.

[0050] In other examples, the ABVG is configured to measure the ION flux or IED and use this information for the control of the ABVG output voltage (setpoint).

[0051] In an aspect, a method of operating the ABVG and/or plasma processing apparatus comprises a control program implementation comprising a plurality of modes of operation. A first mode of operation can correspond to a high power mode. A second mode of operation can correspond to a high precision mode. The plurality of modes of operation can distinguish by one or a combination of: a different switching frequency, a different output voltage, a different output current.

[0052] The first mode of operation which corresponds to a high power mode advantageously corresponds to a mode in which the switching frequency is low, the output voltage and current are high, e.g. they are at a maximum level. A low switching frequency advantageously results in low switching losses, and in turn higher conduction losses may be allowed and hence, the output current level can be increased. A low switching frequency is advantageous when using a high output voltage to limit switching losses.

[0053] The second mode of operation corresponding to a high precision mode can be obtained in different ways. Possibly, each of these ways can be a different mode of operation. In a first option, the output current can be limited resulting in lower conduction losses. Lower conduction losses may allow for increasing switching frequency with respect to the first mode. In this option switching frequency and output voltage can be maintained at high levels. A high switching frequency results in a high bandwidth and therefore a higher precision.

[0054] In a second option for the second mode, the output voltage is limited. Reducing the output voltage with respect to the first mode reduces switching losses which may allow for increasing switching frequency with respect to the first mode. Therefore, a higher precision can be obtained.

[0055] In a third option for the second mode, both the output voltage and the output current is limited with respect to the first mode (high power mode). This reduces both the conduction losses (due to lower current) and the switching losses (due to the lower output voltage) and therefore allows for increasing the switching frequency to a maximum level. This option may result in a maximal precision mode of operation.

[0056] In the third option, the output power may be lowest. In the first and/or second option, the output power may be intermediate between the output power obtained in the first mode and the output power obtained in the third option.

[0057] The apparatus may comprise a user interface enabling an operator to select between different modes of operation. Any one of the first to third option can be implemented in the control unit as a distinct mode of operation of the ABVG.

[0058] A feedback may be implemented in the apparatus. Feedback may be based on current and/or voltage feedback. Advantageously, a feedback control loop may be based on a measured process parameter, such as ion energy density and/or ion current through the substrate.

CLAIMS

1. Plasma processing apparatus (100), comprising:

means for generating a plasma,

a processing platform (105) for supporting a substrate (101) to be processed, and

a voltage waveform generator (10) comprising an output (19) electrically coupled to the processing platform (105),

characterised in that the voltage waveform generator (10) comprises:

a plurality of first buck converters (11) arranged in parallel and coupled to the output (19), the first buck converters (11) comprising actively switchable semiconductor switches (111),

a control unit (16) configured to operate the actively switchable semiconductor switches (111) through pulse width modulation signals,

wherein the control unit (16) is configured to operate the plurality of first buck converters (11) in an interleaved manner.

2. Plasma processing apparatus of claim 1, wherein the actively switchable semiconductor switches in each buck converter comprise a first semiconductor switch and a second semiconductor switch arranged in a half bridge configuration.

3. Plasma processing apparatus of claim 2, wherein the control unit is configured to generate phase shifted pulse width modulation signals applied to the plurality of first buck converters.

4. Plasma processing apparatus of claim 1 or 2, wherein the voltage waveform generator comprises a plurality of second buck converters arranged in parallel and coupled to the output, the second buck converters comprising actively switchable semiconductor switches,

wherein the control unit is configured to operate the actively switchable semiconductor switches of the second buck converters through pulse width modulation signals and configured to operate the plurality of second buck converters in an interleaved manner, and

wherein the plurality of first buck converters and the plurality of second buck converters are arranged in parallel.

5. Plasma processing apparatus of claim 4, wherein the actively switchable semiconductor switches of the second buck converters comprise in each of

the second buck converters a third semiconductor switch and a fourth semiconductor switch arranged in a half bridge configuration.

6. Plasma processing apparatus of any one of the preceding claims, wherein the voltage waveform generator comprises a transformer between the plurality of first buck converters and the output.

7. Plasma processing apparatus of any one of the preceding claims, wherein the voltage waveform generator comprises a DC blocking capacitor between the first buck converters and the output.

8. Plasma processing apparatus of claim 7 in conjunction with claim 6, wherein the DC blocking capacitor is coupled between a secondary side of the transformer and the output.

9. Plasma processing apparatus of any one of the preceding claims, wherein the voltage waveform generator comprises a linear power amplifier coupled to the output.

10. Plasma processing apparatus of claim 9, wherein the control unit is operable to control operation of the linear power amplifier.

11. Plasma processing apparatus of claim 9 or 10, wherein the linear power amplifier is coupled in parallel with the first buck converters.

12. Plasma processing apparatus of claim 9 or 10, comprising a filter arranged in series with the first and/or optionally second buck converters and coupled to the output, wherein the linear power amplifier is coupled in parallel with the series of the first and/or optionally second buck converters and the filter.

13. Plasma processing apparatus of any one of the preceding claims, wherein the voltage waveform generator is operable to provide a voltage bias to an exposed surface of the substrate.

14. Plasma processing apparatus of any one of the preceding claims, wherein the control unit is configured to operate the actively switchable semiconductor switches of the first and optionally second buck converters to generate a predetermined voltage waveform at the output.

15. Plasma processing apparatus of any one of the preceding claims, wherein the voltage waveform generator is operable to generate an AC voltage at the output.

16. Plasma processing apparatus of any one of the preceding claims, wherein the control unit is implemented with a plurality of modes of operation of the voltage waveform generator.

17. Plasma processing apparatus of claim 16, wherein the plurality of modes of operation comprise modes of operation resulting in different output voltage levels.

18. Plasma processing apparatus of claim 16 or 17, wherein the plurality of modes of operation comprise modes of operation resulting in different output current levels.

19. Plasma processing apparatus of any one of the claims 16 to 18, wherein at least one mode of operation of the plurality of modes of operation comprises operating at a limited output current and/or limited output voltage.

20. Plasma processing apparatus of any one of the claims 16 to 19, wherein the plurality of modes of operation distinguish by a different switching frequency of the actively switchable semiconductor switches.

21. Plasma processing apparatus of any one of the preceding claims, arranged to measure a process parameter being one or more of an ion energy density and an ion current through the substrate, and wherein the voltage waveform generator comprises a control loop on the basis of the measured process parameter.

22. Plasma processing apparatus of any one of the preceding claims, being a dry etching apparatus.

23. Plasma processing apparatus of any one of the claims 1 to 21, being a plasma assisted layer deposition apparatus.

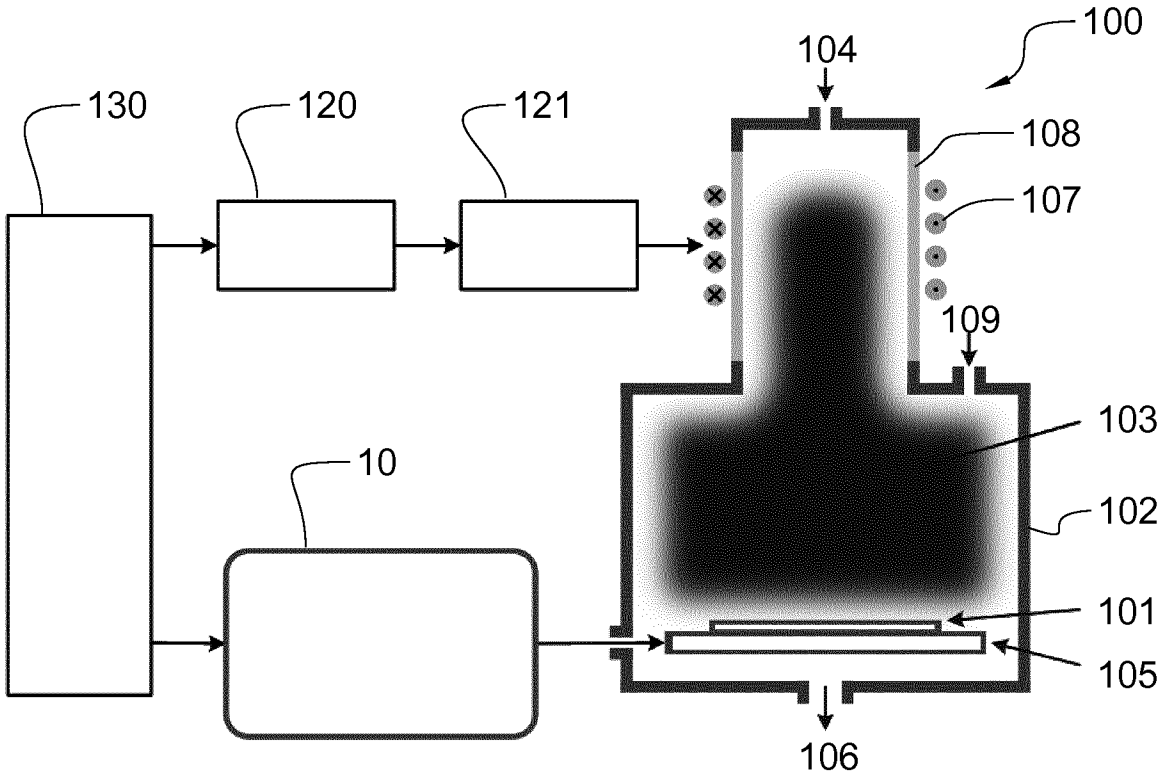
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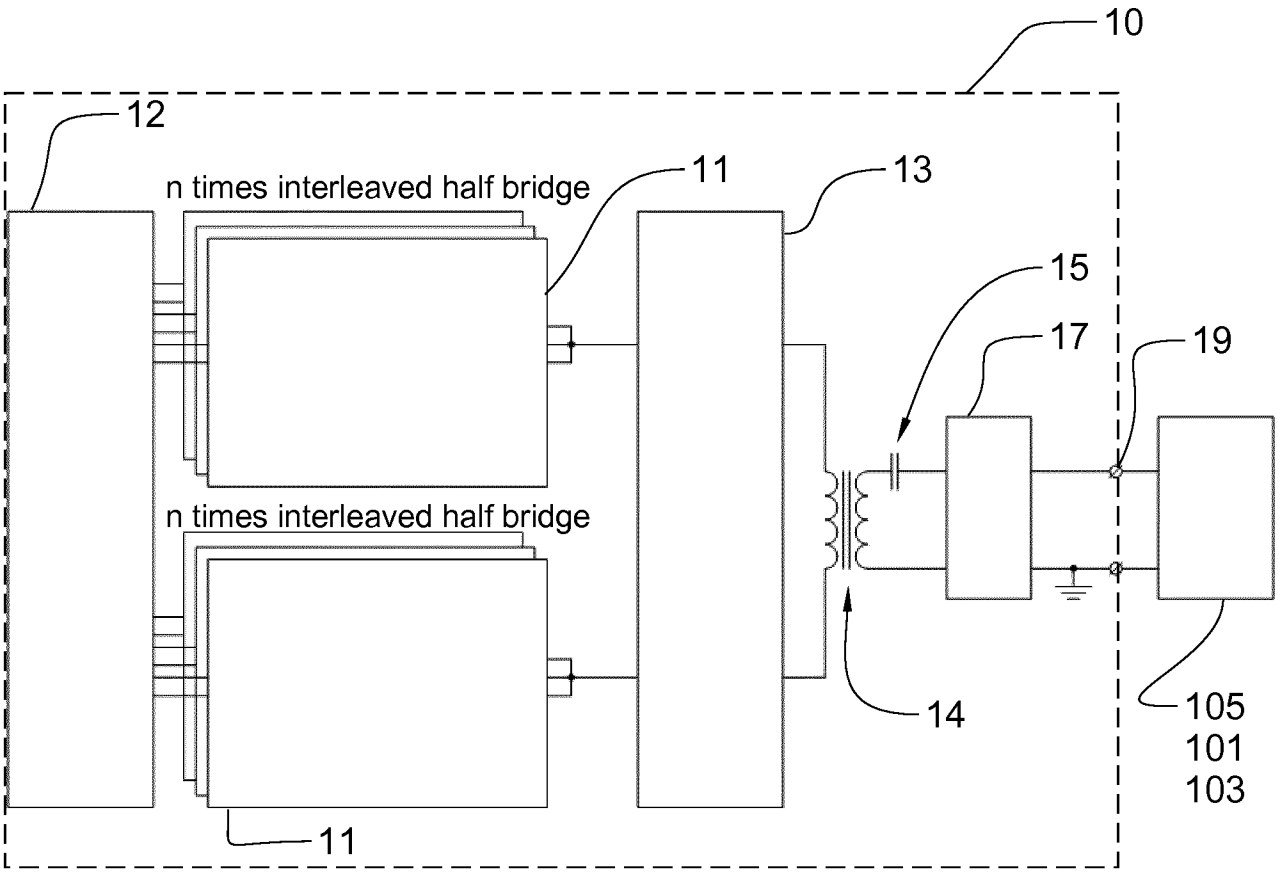
FIG 1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12
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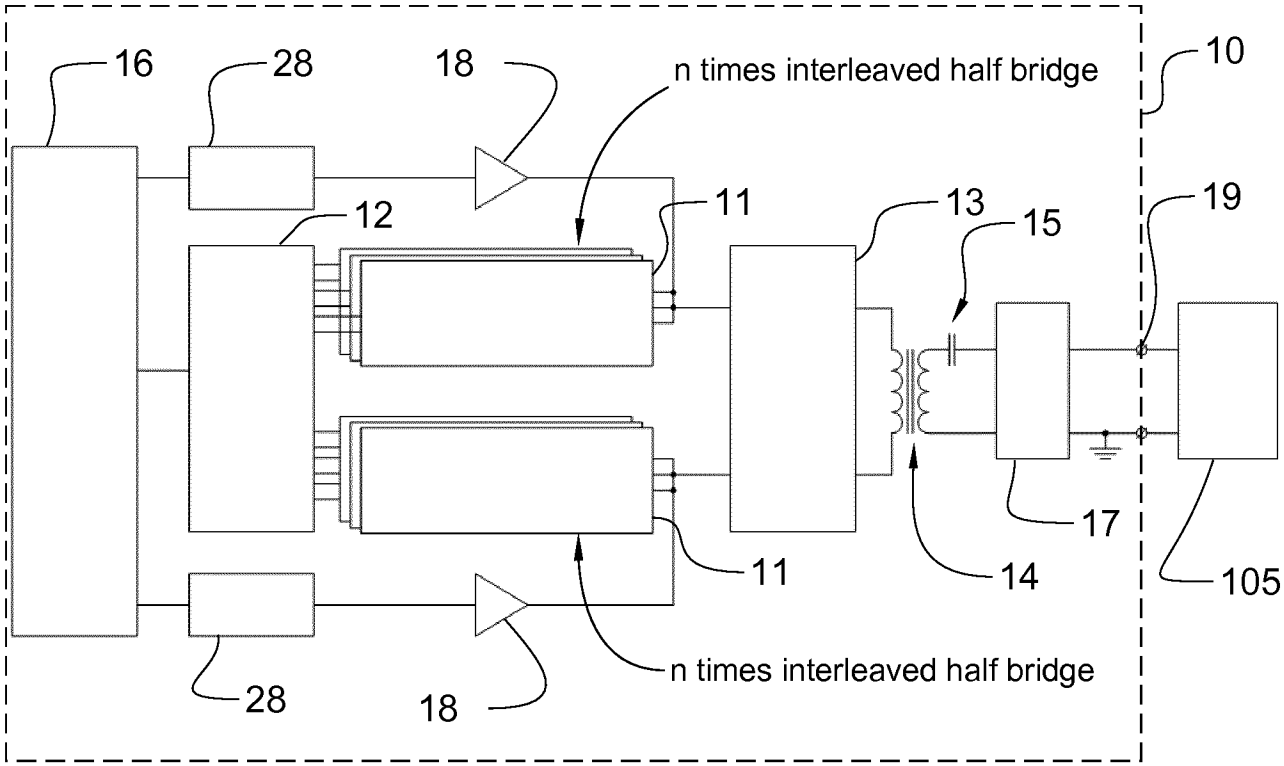
11
13
15
17
19
n times interleaved half bridge
14
105
101
103
11

FIG 2


16
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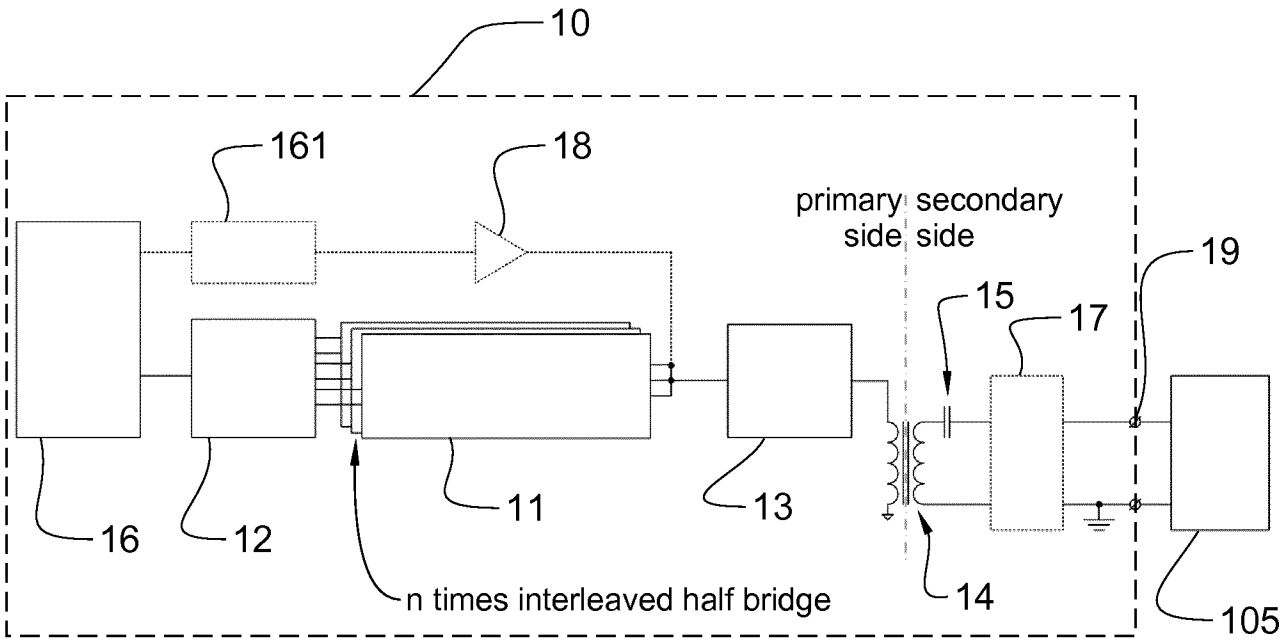
n times interleaved half bridge

FIG 3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161
18
primary side
secondary side
19
15
17
16
12
11
13
14
n times interleaved half bridge
105

FIG 4

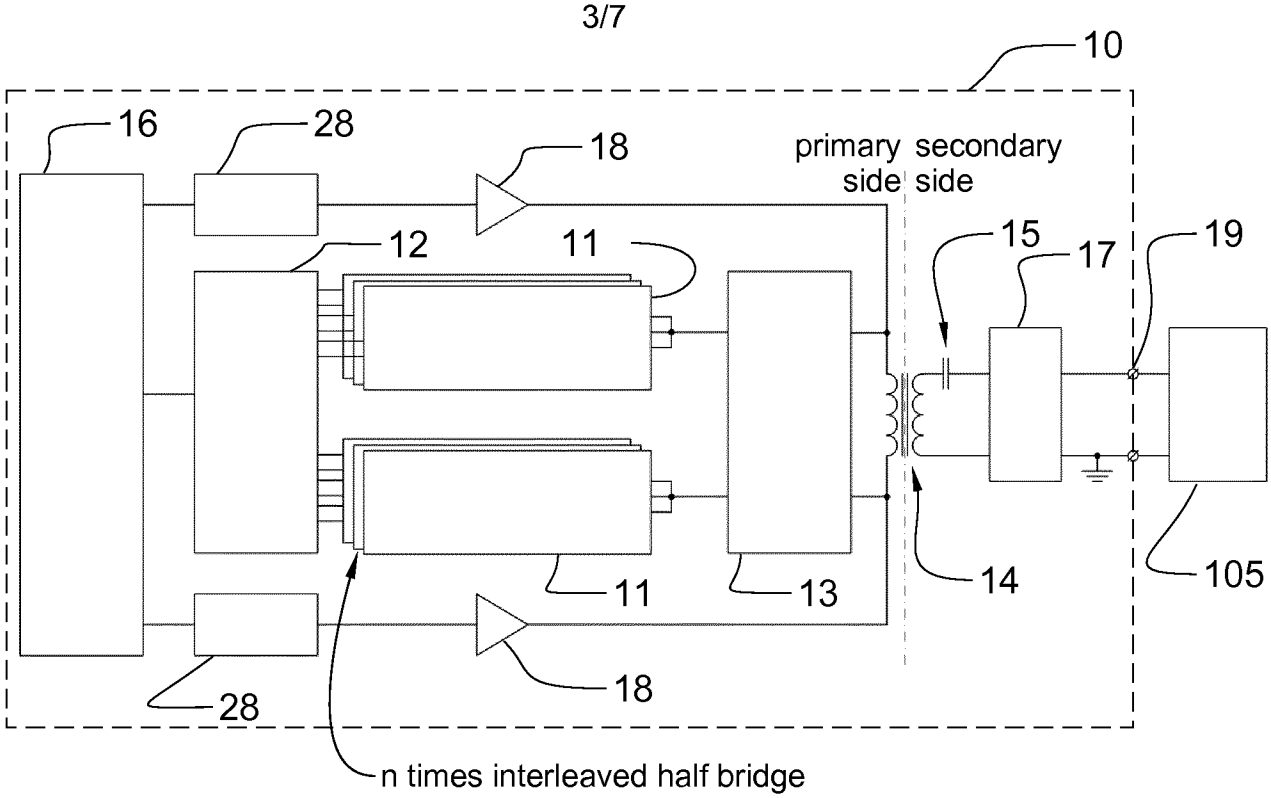
10
16
28
18
primary side
secondary side
12
11
15
17
19
11
13
14
105
28
18
n times interleaved half bridge

FIG 5

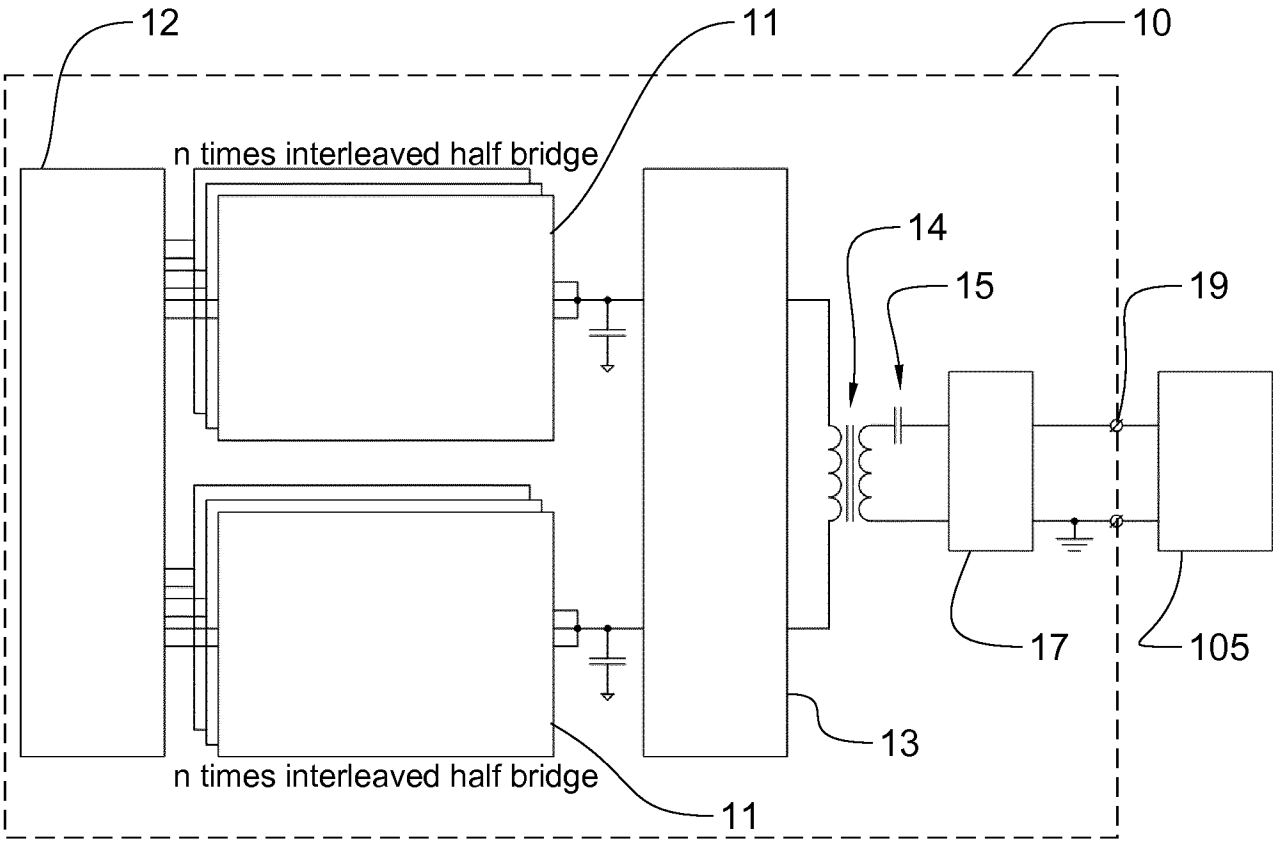
12
11
10
n times interleaved half bridge
14
15
19
17
105
13
n times interleaved half bridge
11

FIG 6

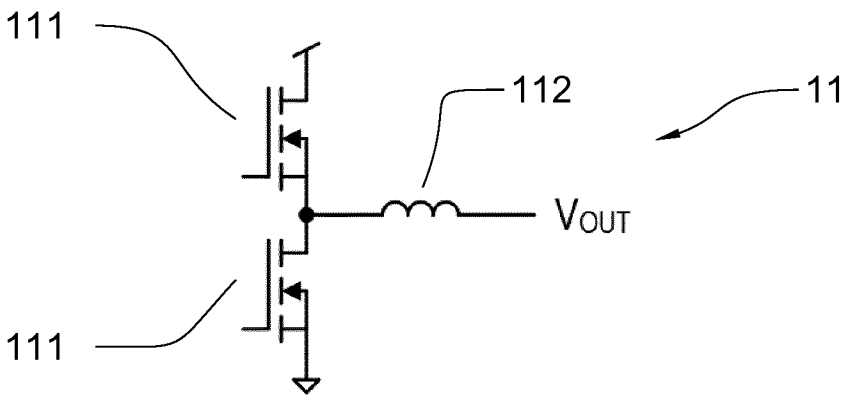
111
112
11
VOUT
111

FIG 7

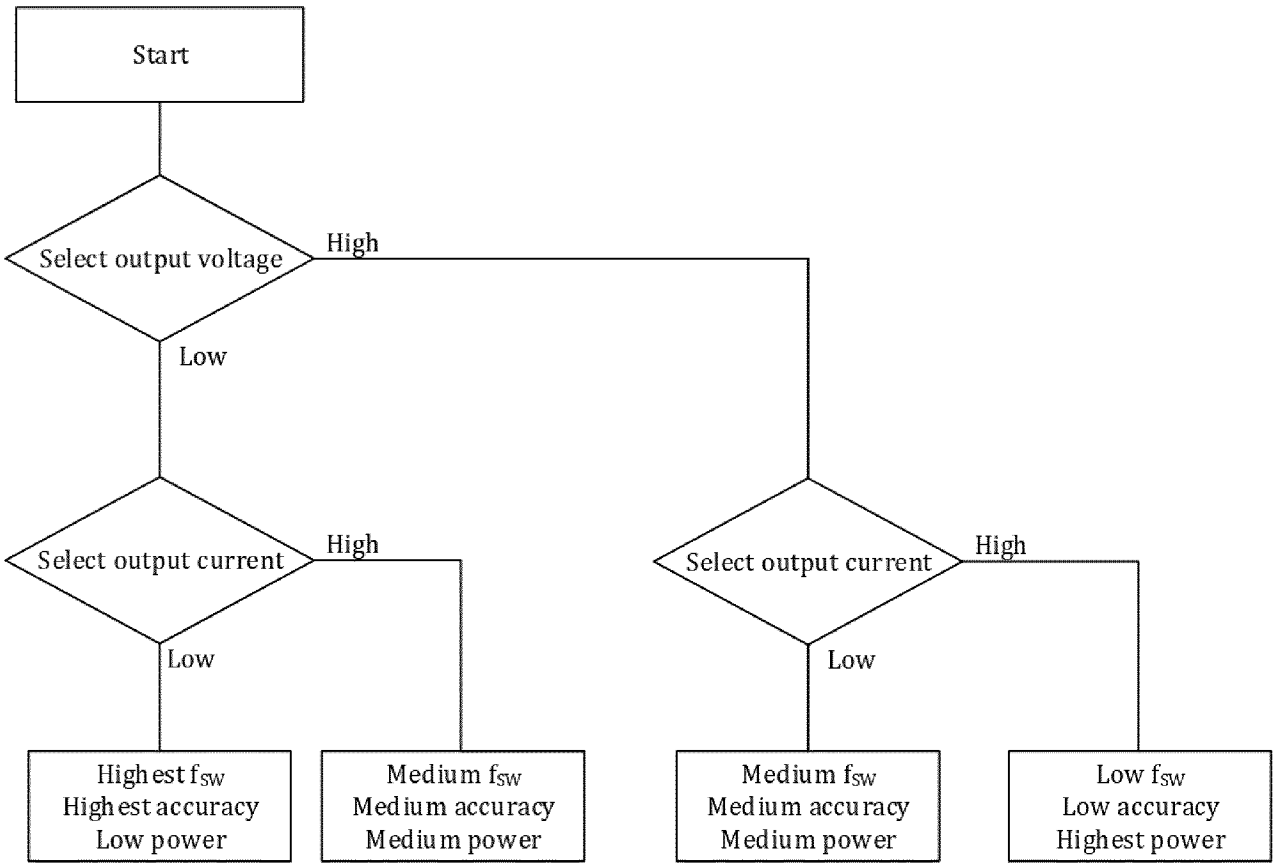
Start
Select output voltage
High
Low
Select output current
High
Low
Select output current
High
Low
Highest fSW
Highest accuracy
Low power
Medium fSW
Medium accuracy
Medium power
Medium fSW
Medium accuracy
Medium power
Low fSW
Low accuracy
Highest power

FIG 8

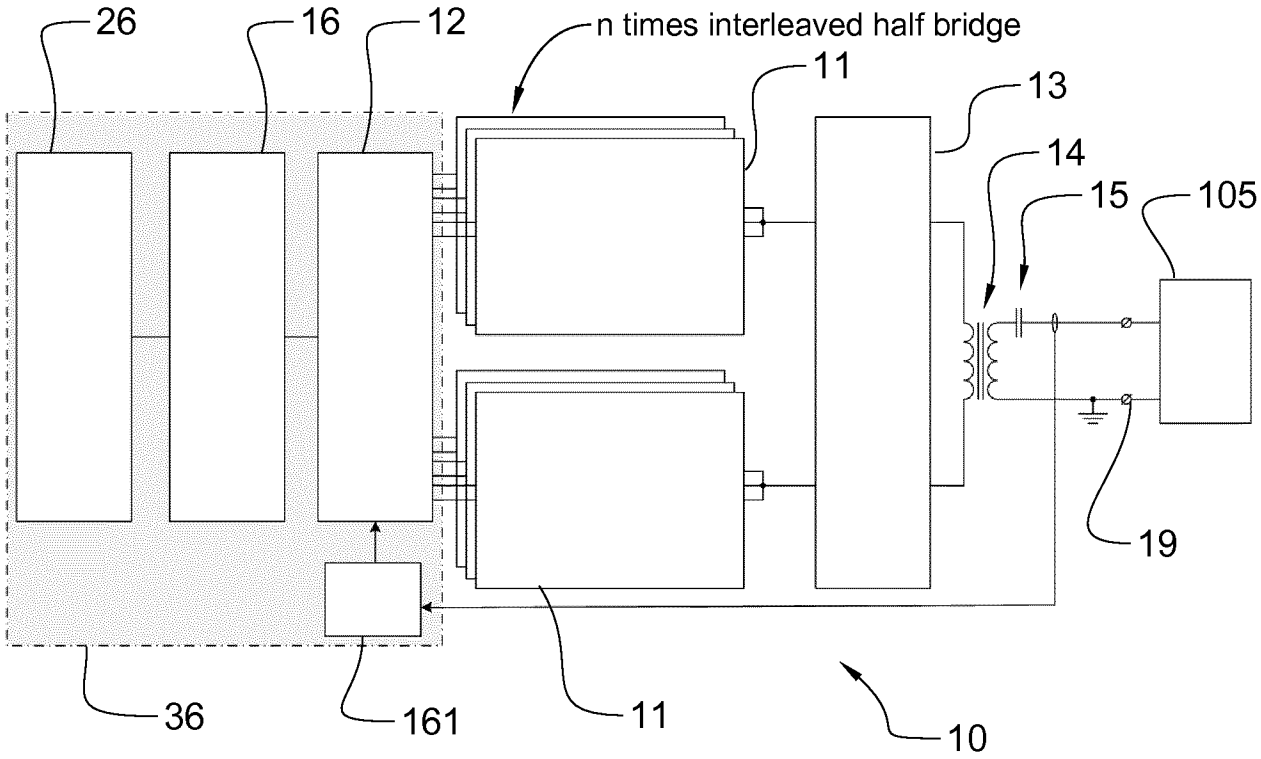
26
16
12
n times interleaved half bridge
11
13
14
15
105
19
36
161
11
10

FIG 9

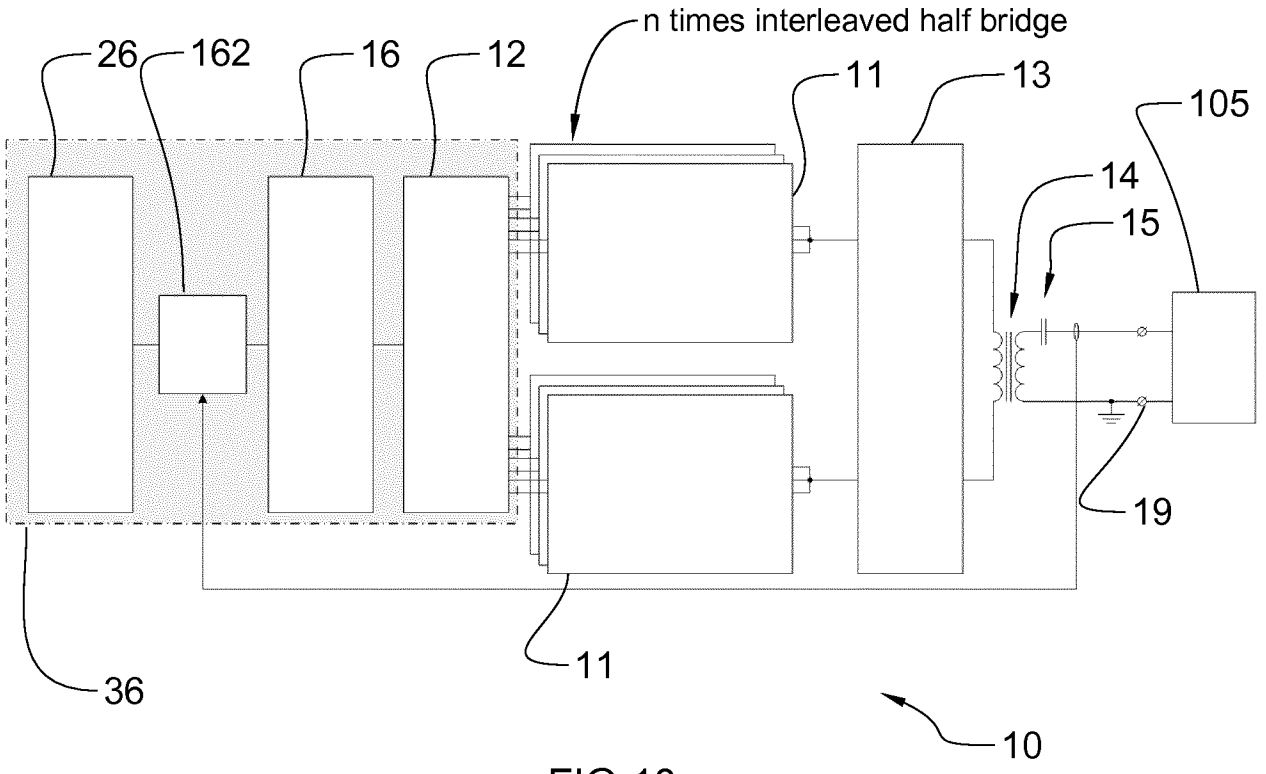
n times interleaved half bridge
26
162
16
12
11
13
105
14
15
19
36
11
10

FIG 10

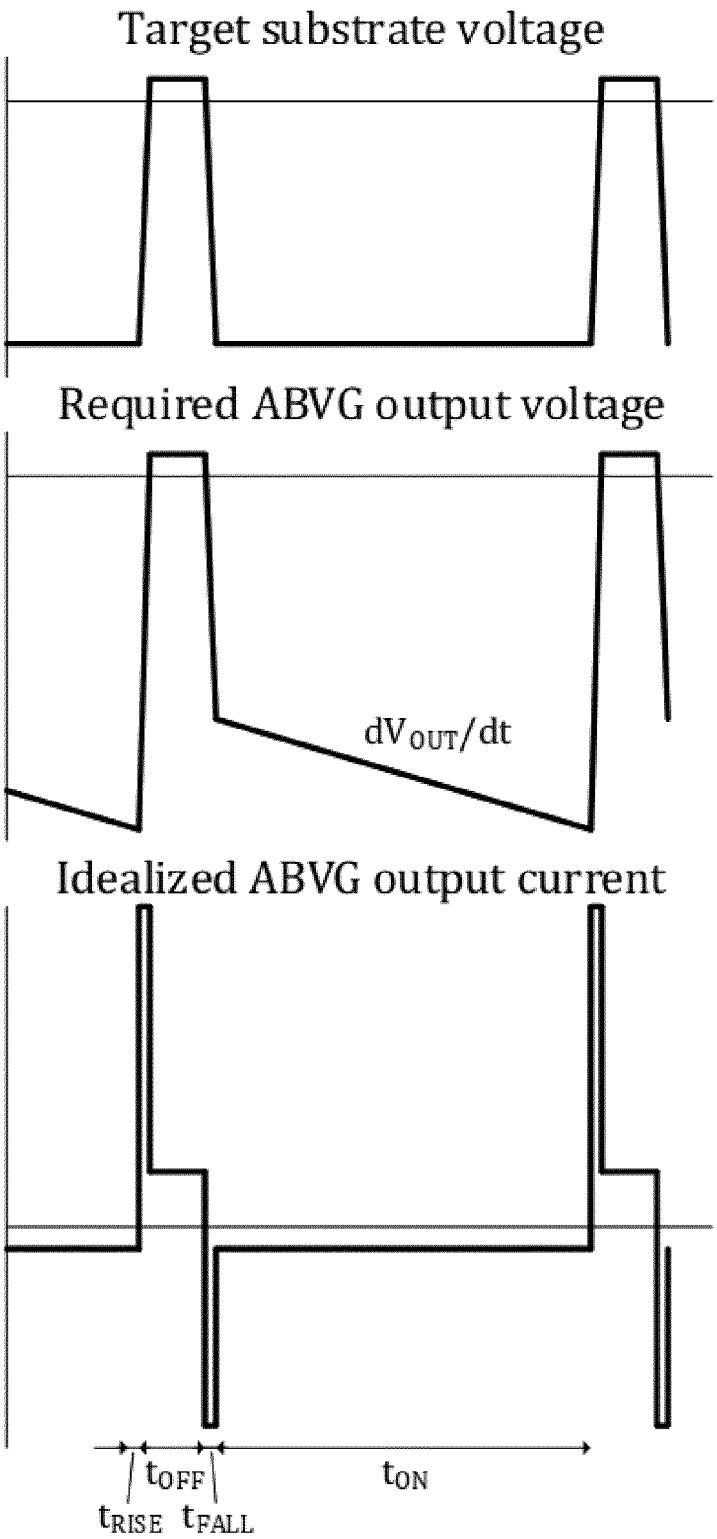
Target substrate voltage
Required ABVG output voltage
dV$_{OUT}$/dt
Idealized ABVG output current
t$_{OFF}$
t$_{ON}$
t$_{RISE}$
t$_{FALL}$

FIG 11

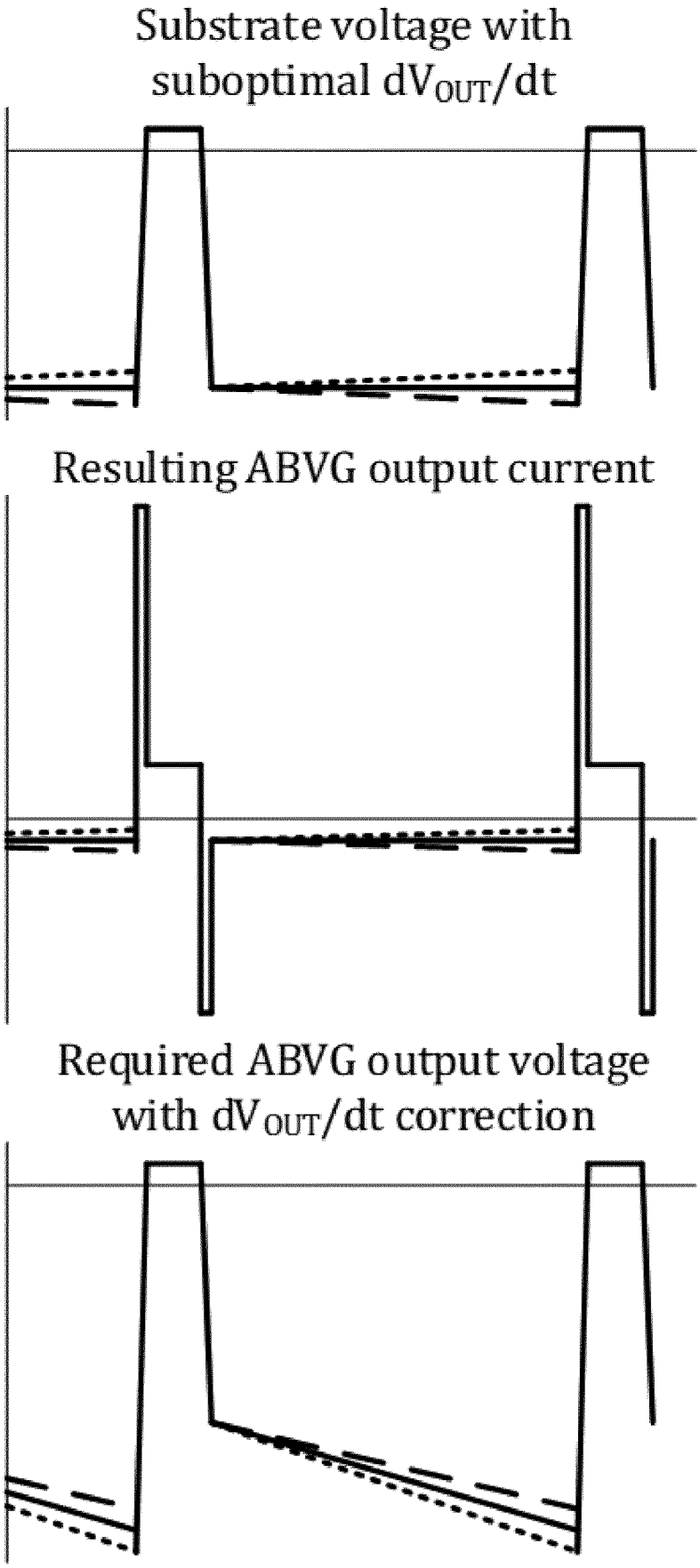
Substrate voltage with suboptimal dV_{OUT}/dt
Resulting ABVG output current
Required ABVG output voltage with dV_{OUT}/dt correction

FIG 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/080405

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01J37/32 C23C14/34 G05F3/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01J G05F C23C H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9 208 992 B2 (ADVANCED ENERGY IND INC [US]) 8 December 2015 (2015-12-08) cited in the application abstract; figures 1-6 column 1, lines 16-20, 47-57 column 4, line 19 - column 9, line 6 -----	1-3,7, 13-23
A	US 6 979 980 B1 (HESTERMAN BRYCE L [US] ET AL) 27 December 2005 (2005-12-27) abstract; figures 4,17,20,26 column 1, lines 8-12 column 2, line 64 - column 3, line 7 column 7, line 60 - column 8, line 7 column 10, lines 39-52 ----- -/--	1-4,7, 15-20

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 January 2020	17/01/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Remy, Jérôme

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/080405

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 95/15612 A1 (CROWN INT [US]) 8 June 1995 (1995-06-08) abstract; figures 2,3 page 1, lines 17-27 page 2, line 28 - page 3, line 14 page 5, line 35 - page 8, line 1	1,3,4,7, 9-12, 14-20
A	EP 0 987 818 A2 (GEN ELECTRIC [US]) 22 March 2000 (2000-03-22) abstract; figures 4,8 paragraphs [0001], [0004], [0009], [0010], [0021]	1-9, 14-20

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2019/080405

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		CA 2175800 A1	08-06-1995
		CN 1136370 A	20-11-1996
		DE 69409968 D1	04-06-1998
		DE 69409968 T2	29-10-1998
		DK 0732004 T3	15-02-1999
		EP 0732004 A1	18-09-1996
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		DE 69913454 T2	07-10-2004
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