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(54) **A capacitor for integration with copper damascene structure and manufacturing method**

Ein Kondensator für die Integration in einer Kupfer-Damaszen-Struktur und Herstellungsmethode

Condensateur pour l'intégration dans une structure à damasquinage en cuivre et son procédé de fabrication

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Description

[0001] The present invention is directed, in general, to fabricating a capacitor for use in a semiconductor device, and more specifically, to a capacitor for integration with copper damascene processes and a method of manufacture therefore.

Background Of The Invention

[0002] Capacitors have gained wide acceptance and use in today's integrated circuit technology. As is well known, a common capacitor essentially comprises two conductive plates separated by an insulator. It is normal for the conductive plates to be made of aluminum and the insulator to be a dielectric material, such as silicon dioxide (SiO_2).

[0003] Originally, capacitors were often placed upon a substrate of the integrated circuit (IC) and electrically connected to contact or via structures, as required by design. While these structures were quite effective, their presence caused a topographical aberration in the overlying dielectric material, such that the capacitor's structure would be reflected in the surface of the dielectric layer. As a result, special planarization techniques had to be performed to remove the aberration so that subsequent photolithographic processes were not adversely affected. The effect of the capacitor's aberrations in the photolithographic processes became even more acute as device sizes decreased.

[0004] Given the planarization problems associated with the earlier capacitor structures, the semiconductor manufacturing industry sought ways to form the capacitors while lessening their impact on the topography of the overlying dielectric layer. One such approach was to form the capacitor within a contact or via opening. This approach has worked very well for the larger submicron technologies. Because the capacitor was formed within the contact opening or via, its structure did not heavily influence the overlying dielectric layer. As such, the planarization problems present with previous capacitor structures were substantially reduced.

[0005] As the design rules have continued to decrease, however, difficulty has arisen with respect to forming a capacitor within these structures. Because smaller device size requires greater precision in the etching processes, the industry is moving toward an etching process known as damascene processing. Because the completed damascene structure has an upper cavity with a width larger than the lower cavity, a stair step topography results within the damascene opening. This damascene process provides more control when forming the trace openings, which in turn allows for manufacturing ICs in the submicron range.

[0006] The invention of the damascene process for forming trace openings allowed for the manufacture of ICs in the submicron range. However, because of the damascene's stair step topography, it has proven much more difficult to form capacitors within these damascene openings. One reason for this difficulty, stems from deposition problems that arise due to the deposition of the various layers needed for the capacitor, over the stair step topography. Because of the increased topography, the thickness of the layers that form the capacitor may vary significantly within the damascene structure. This variance in material thickness is difficult to control and makes it very difficult to achieve the desired degree of capacitance. Moreover, because of the number of layers that must be deposited within the smaller portion of the damascene structure, the material necessary to achieve the desired degree of conduction may not be adequately deposited within the damascene structure. Furthermore, voids may also be formed. Because of these uncertainties, the capacitor cannot be easily and consistently manufactured to the desired level.

[0007] The document US 5,998,258, discloses a capacitor formed on a damascene structure. This capacitor has only one of the electrodes connected to the underlying interconnect structure.

[0008] Accordingly, what is needed in the art is a capacitor structure and a process for forming that capacitor structure that avoids the disadvantages associated with prior art structures and processes.

Summary Of The Invention

[0009] To address the above-discussed deficiencies of the prior art, the present invention provides a capacitor according to claim 1. In one particularly advantageous embodiment, the capacitor, such as a metal-insulator-metal (MIM) capacitor, comprises a first capacitor electrode, such as copper, comprising a portion of the damascene interconnect structure. The capacitor further includes an insulator layer formed on the damascene interconnect structure wherein the insulator layer is a passivation layer, such as silicon nitride. The passivation layer may be an outermost or final passivation layer, or it may be an interlevel passivation layer within an integrated circuit. The second capacitor electrode comprises a conductive layer, such as aluminum, that is formed on at least a portion of the insulator layer.

[0010] The material selected for the capacitor may vary. For example, in one embodiment, the insulator may be silicon nitride. However, in alternative embodiments, the insulator may be tantalum pentoxide. When using certain alternative embodiments, such as tantalum pentoxide with copper, it may be necessary to include an appropriate barrier layer to prevent migration of the copper into the surrounding dielectric.

[0011] The semiconductor device includes a plurality of damascene interconnect structures that are electrically isolated from each other by a dielectric material. On any given layer on which the capacitor is to be formed, the passivation layer is formed on each of the plurality of interconnect structures.

[0012] The conductive layer is formed on at least two

of the interconnect structures. Yet in another embodiment, the damascene interconnect is an outermost or final damascene interconnect structure, the insulator layer is an outermost capping layer and the second capacitor electrode comprises a portion of an outermost conductive layer formed on at least a portion of the insulator layer. This particular embodiment is particularly advantageous because the capacitor is formed on the outermost layers of the semiconductor wafer and the planarization problems that exist at prior levels are avoided. In such embodiments, the outermost layer may also be used to form a bond pad for the semiconductor device.

[0013] In yet another aspect, the present invention provides a semiconductor device formed on a substrate of a semiconductor wafer. This particular embodiment includes transistors formed over the substrate, damascene interconnect structures formed over and electrically connected to the transistors, an insulator passivation layer formed on one of the damascene interconnect structures, a conductive layer formed over one of the damascene interconnect structures, and the capacitor as previously described above, including the various embodiments.

[0014] A method according to claim 6 is also provided.

[0015] The method embodiments also include steps of forming the variations of the devices as discussed above with respect to the capacitor. However, in those embodiments where the capacitor is formed on an interlevel dielectric, as opposed to the outermost dielectric level, the method further comprises planarizing the damascene interconnect structure prior to depositing the insulator material and further comprises planarizing a dielectric that is deposited over the capacitor once it is formed with a planarization process, such as chemical/mechanical planarization techniques.

[0016] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention.

Brief Description Of The Drawings

[0017] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a partial sectional view of one embodiment of a semiconductor device covered by the present invention;

FIGURE 2 illustrates a partial sectional view of the damascene interconnect structure as illustrated in FIGURE 1, including the insulator layer formed over the damascene interconnect structure;

FIGURE 3 illustrates a partial view of the semiconductor device shown in FIGURE 2, following patterning and etching of the insulator layer;

FIGURE 4 illustrates the damascene interconnect structure covered by portions of the insulator layer as illustrated in FIGURE 3, with a second capacitor electrode, which is preferably comprised of a conductive layer, located on at least a portion of the insulator layer; and

FIGURE 5 illustrates a partial section view of the damascene interconnect structure located at an intermediate level within the semiconductor device.

Detailed Description

[0018] Referring initially to FIGURE 1 there is illustrated a sectional view of one embodiment of a semiconductor device 100 covered by the present invention. The semiconductor device 100 shows a portion of a conventionally formed integrated circuit (IC) 110, such as a complementary metal oxide semiconductor (CMOS) device. One having skill in the art knows that the portion of the IC 110 can comprise any number of interconnects 115 and dielectric layers 120 such as to form the desired semiconductor device 100. In the illustrated embodiment of FIGURE 1, the portion of the IC 110 contains conventionally formed twin tubs, including an n-tub 123 and a p-tub 125. Also illustrated in FIGURE 1 are source regions 133 and drain regions 135 both of which are formed using conventional methods.

[0019] A conventional gate electrode structure 140 may be formed, straddling the source region 133 and drain region 135. The gate structure 140 consists of a conventionally formed gate 141, oxide layer 143 and spacers 145. Conventionally formed damascene plugs 150 or vias 152 connect the different layers of the IC 110. The damascene process is used in place of the traditional etch processes to allow for more control when forming the damascene structure. This is especially important because copper is increasingly becoming the conductor of choice, over aluminum as the conductive material, and copper is harder to etch in a controlled manner than aluminum.

[0020] The top portion 155 shown in FIGURE 1, illustrates a damascene interconnect structure 160 from which a capacitor 162 is formed. In one embodiment of the invention, the capacitor 162 is a metal-insulator-metal (MIM) capacitor. The damascene interconnect structure 160 forms a first capacitor electrode 164. In a preferred embodiment, the damascene interconnect structure 160 comprises copper. Furthermore, when the damascene interconnect structures 160 comprise copper (Cu) an optional barrier layer 161 may be conventionally formed such that the Cu damascene interconnect structures 160 are not in contact with the dielectric layer 120, which is preferably SiO_2. Thus, the barrier layer prevents the Cu from diffusing into the SiO_2 dielectric layer 120, and vice

versa. In a preferred embodiment, the barrier layer 161 includes a tantalum nitride (TaN) layer, however, one having skill in the art understands that other similar barrier layers, such as tantalum, may be used. If the copper is electroplated, a seed layer may be required to be formed on top of the barrier layer 161. Furthermore, one having skill in the art understands that other similar conductive materials known to those skilled in the art may also be used for the damascene interconnect structure 160. The capacitor 162 further includes an insulator layer 166, such as a silicon nitride layer, and a second or upper capacitor electrode 168, which may comprise conventional materials, such as aluminum, aluminum alloy or a stacked metal. When the damascene interconnect structures 160 comprise copper (Cu) and the upper capacitor electrode 168 comprises aluminum (Al), a Cu/Al barrier layer 170 should be conventionally deposited between the interconnect structure 160 and the upper capacitor electrode 168 to prevent diffusion. In the illustrated embodiment the Cu/Al barrier layer 170 comprises tantalum nitride (TaN), however one having skill in the art knows that a material having similar properties, such as titanium nitride (TiN), may be used.

[0021] The damascene interconnect structure 160 may be either a single damascene interconnect structure or a dual damascene interconnect structure. However, the dual damascene interconnect structure provides advantages over the prior techniques. For example, the dual damascene interconnect structure allows for manufacturing ICs less than .25 μm in size, a feature that was not available in the traditional trench etching or single damascene process. The illustrated damascene interconnect structure 160 may be the outermost or top damascene interconnect structure 160 of the semiconductor device 100. Alternatively, however, it may be an interlevel damascene interconnect structure. Thus, the capacitor 162 may be constructed at various levels within the semiconductor device 100. However, as explained below in a preferred embodiment, the capacitor 162 is constructed using the outermost or top damascene interconnect structure.

[0022] Turning now to FIGURE 2 with continued reference to FIGURE 1, there is illustrated a sectional view of the damascene interconnect structure 160 as illustrated in FIGURE 1. The interconnect structure 160 includes the insulator layer 166 formed over the damascene interconnect structure 160, and the barrier layer 161 separates the copper damascene interconnect structure 160 from the SiO_2 dielectric layer 120. In a preferred embodiment the barrier layer 161 is conformally deposited over the substrate surface and within the damascene interconnect structure 160, after which copper is deposited over the barrier layer 161 and within the damascene interconnect structure 160. The copper and the barrier layer 161 are polished back using conventional chemical/mechanical process so that the barrier layer 161 and the copper are located only within the damascene interconnect structure 160. In another preferred embodiment, the insulator layer 166 is deposited using conventional deposition processes, such as chemical vapor deposition (CVD) or physical vapor deposition (PVD). In an advantageous embodiment, the insulator layer 166 is typically deposited as a passivation layer. As well known, in some processes, semiconductor devices may be passivated with a capping layer at the end of the fabrication process to protect or seal the semiconductor device from deleterious environmental contaminants. Thus, in this particular embodiment, no extra steps have been necessary to fabricate either the first capacitor electrode 164 or the insulator layer 166 of the capacitor 162. As shown, the insulator or passivation layer 166, such as tantalum pentoxide, is formed over the entire surface of the planarized IC 110.

[0023] Turning now to FIGURE 3, there is illustrated a partial view of the semiconductor device 100 shown in FIGURE 2 following patterning and etching of the insulator layer 166. Conventional patterning and etching processes may be used to form openings 310 within the insulator layer 166. The portions of insulator layer 166 are removed to define the capacitor dielectric of the capacitor 162. In the embodiment illustrated in FIGURE 3, a portion of the insulator layer 166 as been removed over damascene structures 320 and 330.

[0024] Turning to FIGURE 4, illustrated is the damascene interconnect structure 160 covered by portions of the insulator layer 166 as illustrated in FIGURE 3, with a second capacitor electrode 168, comprised of a conductive layer, located on at least a portion of the insulator layer 166. The conductive layer may, if desired so, be a metal layer or a doped polysilicon layer. Not shown in FIGURE 4 is the step of conventionally depositing the conductive layer over the entire surface of the semiconductor device 100 and patterning and etching the conductive layer to end up with the capacitor 162 as shown in FIGURE 4. In a preferred embodiment the second capacitor electrode 168 may comprise aluminum, an aluminum alloy, such as aluminum/copper, or a conventional stacked metal. However, as one having ordinary skill in the art obviously knows, any material used as conductive materials in semiconductor devices may be used.

[0025] As discussed previously, the damascene interconnect structure 160 forms the first electrode 164 of the capacitor 162, and it may be formed at any level within the IC 110. FIGURE 5 illustrates the capacitor 162, discussed previously, located at a interlevel within the IC 110. When an interlevel of the device is used, planarization processes should be conducted after the deposition of conductive layer from which the capacitor's second capacitor electrode 168 is formed. A planarization process, such as chemical/mechanical processes, may be used. Planarization should be conducted to smooth the irregular topography that results from the earlier planarization of the copper damascene interconnect structure 160.

[0026] In a preferred embodiment, however, the capacitor 162 is formed from the outermost damascene in-

terconnect structure 160. The outermost damascene interconnect structure 160 is then covered by an outermost capping layer, which serves as the insulator layer 166. The outermost capping layer may act as the final capping layer of the semiconductor device 100 in some designs. The use of the outermost damascene interconnect 160 is particularly advantageous because no planarization processes are required after the formation of the second capacitor electrode 168, since no substantive, subsequent layers are present in the semiconductor device 100.

[0027] The second capacitor electrode 168 may also be formed from deposition processes used to form other parts of the semiconductor device 100. For example, in some cases a conductive layer is often deposited, patterned and etched to form a bond pad. In certain aspects of the present invention, the second capacitor electrode 168 may be formed from this bond conductive layer. Thus, no additional steps are needed to fabricate either first electrode 164, the insulator layer 166 or the second capacitor electrode 168 of the capacitor 162.

Claims

1. A capacitor (162) for use in a semiconductor device (100) having damascene interconnect structures formed over a substrate of a semiconductor wafer, the capacitor comprising:

   a first capacitor electrode comprising a portion of a first damascene interconnect structure (160);
   a second damascene interconnect structure, said first and second interconnect structures being formed in the same interconnect level;
   an insulator layer (166) formed on said first damascene interconnect structure (160);
   a second capacitor electrode (168) comprising a conductive layer formed on at least a portion of the insulator layer (166) and on said second damascene interconnect structure;
   characterized in that
   the insulating layer (166) has holes exposing said second damascene interconnect structure, and the conductive layer is in electrical and physical contact with the second damascene interconnect structure through said holes.

2. The capacitor (162) of claim 1 wherein the insulator layer (166) is silicon nitride.

3. The capacitor (162) of claim 1 wherein the first capacitor electrode comprises copper and the second capacitor electrode comprises aluminum.

4. The capacitor (162) of claim 1 wherein the insulator layer (166) is tantalum pentoxide.

5. The capacitor (162) of claim 1 wherein the first and second damascene interconnect structures are outermost damascene interconnect structures, the insulator layer (166) is an outermost capping layer and the second capacitor electrode (168) comprises a portion of an outermost conductive layer formed on at least a portion of the insulator layer (166).

6. A method of fabricating a capacitor (162) for use in a semiconductor device (100) having a plurality of damascene interconnect structures formed over a substrate of a semiconductor wafer, comprising:

   forming a first capacitor electrode comprising a portion of a first damascene interconnect structure (160) and forming a second damascene interconnect structure in the same interconnect level;
   forming an insulator layer (166) on the first and second damascene interconnect structures;
   removing a portion of the insulator layer (166) over the second damascene interconnect structures;
   forming a second capacitor electrode (168) comprising a conductive layer formed on at least a portion of the insulator layer (166), wherein the conductive layer is formed over the first and second damascene interconnect structures and is in direct and electrical contact with the second damascene interconnect structure.

7. The method of claim 6 wherein the damascene interconnect structures are outermost damascene interconnect structures, forming an insulator layer includes forming an outermost capping layer, and forming a conductive layer includes forming an outermost conductive layer on at least a portion of the insulator layer (166).

8. The method of claim 7 wherein forming a conductive layer includes forming a bond pad from a portion of the conductive layer.

Patentansprüche

1. Kondensator (162) zur Verwendung in einem Halbeiterbauelement (100) mit Damaszen-Verbindungsstrukturen, die über einem Substrat eines Halbleiter-Wafers gebildet sind, wobei der Kondensator umfasst:

   eine erste Kondensatorelektrode, die einen Teil einer ersten Damaszen-Verbindungsstruktur (160) umfasst;
   eine zweite Damaszen-Verbindungsstruktur, wobei besagte ersten und zweiten Verbindungsstrukturen in der gleichen Verbindungsebene

gebildet sind;
eine Isolatorschicht (166), die auf besagter ersten Damaszen-Verbindungsstruktur (160) gebildet ist;
eine zweite Kondensatorelektrode (168), die eine leitende Schicht umfasst, die auf zumindest einem Teil der Isolatorschicht (166) und aufbesagter Damaszen Verbindungsstruktur gebildet ist;
dadurch gekennzeichnet, dass
die Isolierschicht (166) Löcher aufweist, die besagte zweite Damaszen-Verbindungsstruktur freilegen und sich die leitende Schicht durch besagte Löcher in elektrischem und physikalischem Kontakt mit der zweiten Damaszen-Verbindungsstruktur befindet.

2. Kondensator (162) nach Anspruch 1, wobei die Isolatorschicht (166) Siliciumnitrid ist.

3. Kondensator (162) nach Anspruch 1, wobei die erste Kondensatorelektrode Kupfer und die zweite Kondensatorelektrode Aluminium umfasst.

4. Kondensator (162) nach Anspruch 1, wobei die Isolatorschicht (166) Tantalpentoxid ist.

5. Kondensator (162) nach Anspruch 1, wobei die ersten und zweiten Damaszen-Verbindungsstrukturen äußerste Damaszen-Verbindungsstrukturen sind, die Isolatorschicht (166) eine äußerste Deckschicht ist und die zweite Kondensatorelektrode (168) einen Teil einer äußersten leitenden Schicht umfasst, die auf zumindest einem Teil der Isolatorschicht (166) gebildet ist.

6. Herstellungsmethode eines Kondensators (162) zur Verwendung in einem Halbeiterbauelement (100) mit einer Mehrheit von Damaszen-Verbindungsstrukturen, die über einem Substrat eines Halbleiter-Wafers gebildet sind, umfassend:

Bilden einer ersten Kondensatorelektrode, die einen Teil einer ersten Damaszen-Verbindungsstruktur (160) umfasst und Bilden einer zweiten Damaszen-Verbindungsstruktur in der gleichen Verbindungsebene;
Bilden einer Isolatorschicht (166) auf den ersten und zweiten Damaszen-Verbindungsstrukturen;
Entfernen eines Teils der Isolatorschicht (166) über den zweiten Damaszen-Verbindungsstrukturen;
Bilden einer zweiten Kondensatorelektrode (168), die eine leitende Schicht umfasst, die auf zumindest einem Teil der Isolatorschicht (166) gebildet ist, wobei die leitende Schicht über den ersten und zweiten Damaszen-Verbindungsstrukturen gebildet ist und in direktem und elektrischem Kontakt mit der zweiten Damaszen-Verbindungsstruktur ist.

7. Methode nach Anspruch 6, wobei die Damaszen-Verbindungsstrukturen äußerste Damaszen-Verbindungsstrukturen sind, wobei Bilden einer Isolatorschicht Bilden einer äußersten Deckschicht einschließt und Bilden einer leitenden Schicht Bilden einer äußersten leitenden Schicht auf zumindest einem Teil der Isolatorschicht (166) einschließt.

8. Methode nach Anspruch 7, wobei Bilden einer leitenden Schicht Bilden einer Bondinsel aus einem Teil der leitenden Schicht einschließt.

Revendications

1. Condensateur (162) utilisable dans un dispositif semi-conducteur (100) comportant des structures d'interconnexion damassées formées au-dessus du substrat d'une galette de semi-conducteur, le condensateur comportant :

une première électrode du condensateur comprenant une partie d'une première structure d'interconnexion damassée (160) ;
une deuxième structure d'interconnexion damassée, les première et deuxième structures d'interconnexion étant formées dans le même niveau d'interconnexion ;
une couche isolante (166) formée sur la première structure d'interconnexion damassée (160) ;
une deuxième électrode du condensateur (168) comprenant une couche conductrice formée sur au moins une partie de la couche isolante (166) et sur la deuxième structure d'interconnexion damassée ;
caractérisé en ce que
la couche isolante (166) comporte des trous exposant la deuxième structure d'interconnexion damassée, et **en ce que** la couche conductrice se trouve en contact électrique et physique avec la deuxième structure d'interconnexion damassée à travers ces trous.

2. Condensateur (162) selon la revendication 1, dans lequel la couche isolante (166) est constituée de nitrure de silicium.

3. Condensateur (162) selon la revendication 1, dans lequel la première électrode du condensateur est composée cuivre et la deuxième électrode du condensateur est composée d'aluminium

4. Condensateur (162) selon la revendication 1, dans lequel la couche isolante (166) est constituée de

pentoxyde de tantale.

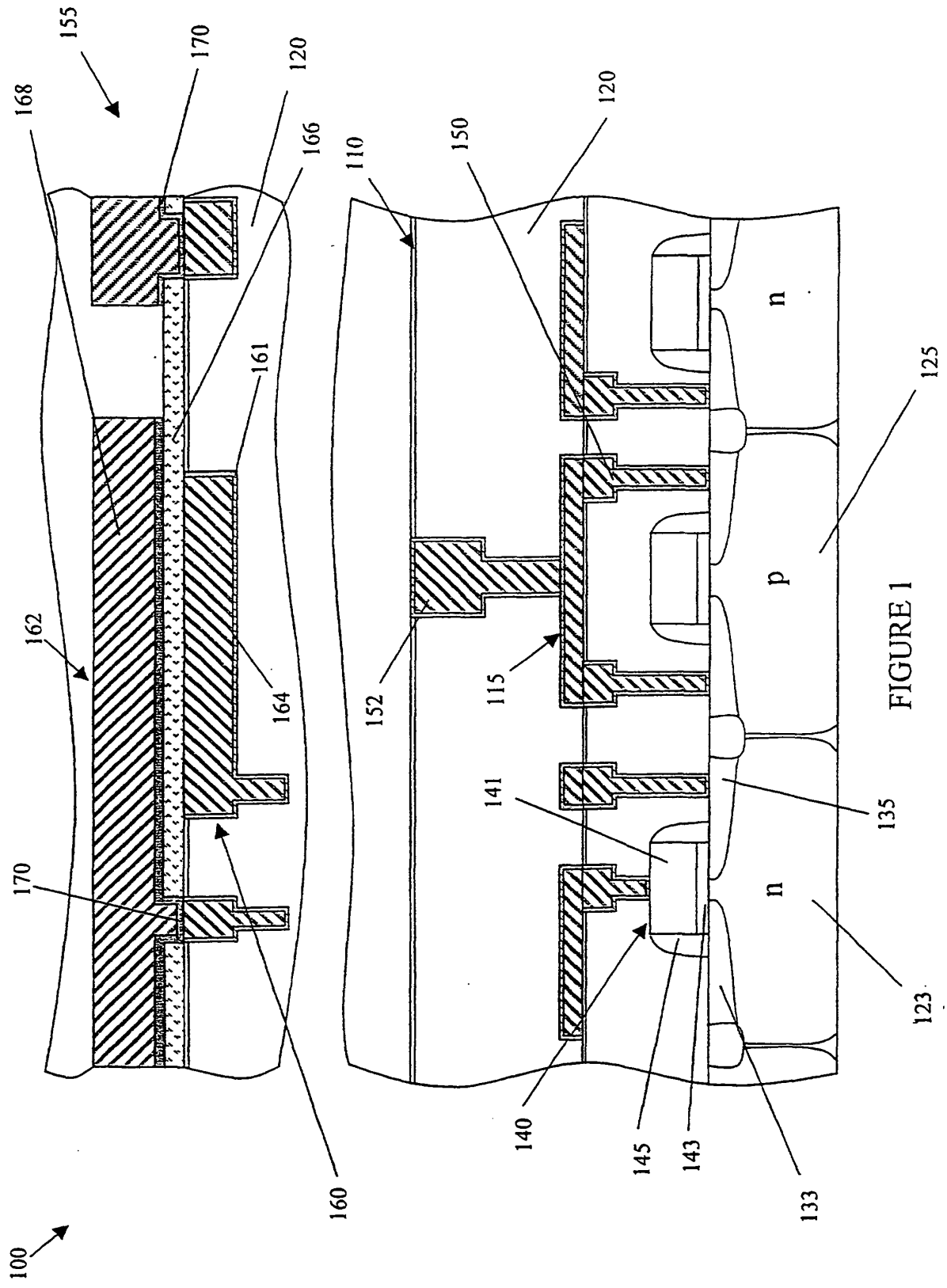
5. Condensateur (162) selon la revendication 1, dans lequel les première et deuxième structures d'interconnexion damassées sont des structures d'interconnexion damassées situées à l'extrémité, la couche isolante (166) est une couche de recouvrement située à l'extrémité, et la deuxième électrode du condensateur (168) comprend une partie d'une couche conductrice située à l'extrémité, formée sur au moins une partie de la couche isolante (166).

6. Méthode de fabrication d'un condensateur (162) utilisable dans un dispositif semi-conducteur (100) comportant des structures d'interconnexion damassées formées au-dessus du substrat d'une galette de semi-conducteur, comportant:

à former une première électrode du condensateur comprenant une partie d'une première structure d'interconnexion damassée (160) et à former une deuxième électrode du condensateur dans le même niveau d'interconnexion ;
à former une couche isolante (166) sur les première et deuxième structures d'interconnexion damassées ;
à enlever une partie de la couche isolante (166) au-dessus des deuxièmes structures d'interconnexion damassées ;
à former une deuxième électrode du condensateur comprenant une couche conductrice formée sur au moins une partie de la couche isolante (166), **caractérisée en ce que** la couche conductrice est formée au-dessus des première et deuxième structures d'interconnexion damassées et se trouve en contact électrique et physique direct avec la deuxième structure d'interconnexion damassée.

7. Méthode selon la revendication 6, dans lequel les structures d'interconnexion damassées sont des structures d'interconnexion damassées situées à l'extrémité, formant une couche isolante y compris la formation d'une couche de recouvrement située à l'extrémité, et formant une couche conductrice située à l'extrémité, formée sur au moins une partie de la couche isolante (166).

8. Méthode selon la revendication 7, dans lequel la formation d'une couche conductrice consiste entre autres à former un élément de connexion en utilisant une partie de la couche conductrice.


155
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133

FIGURE 1

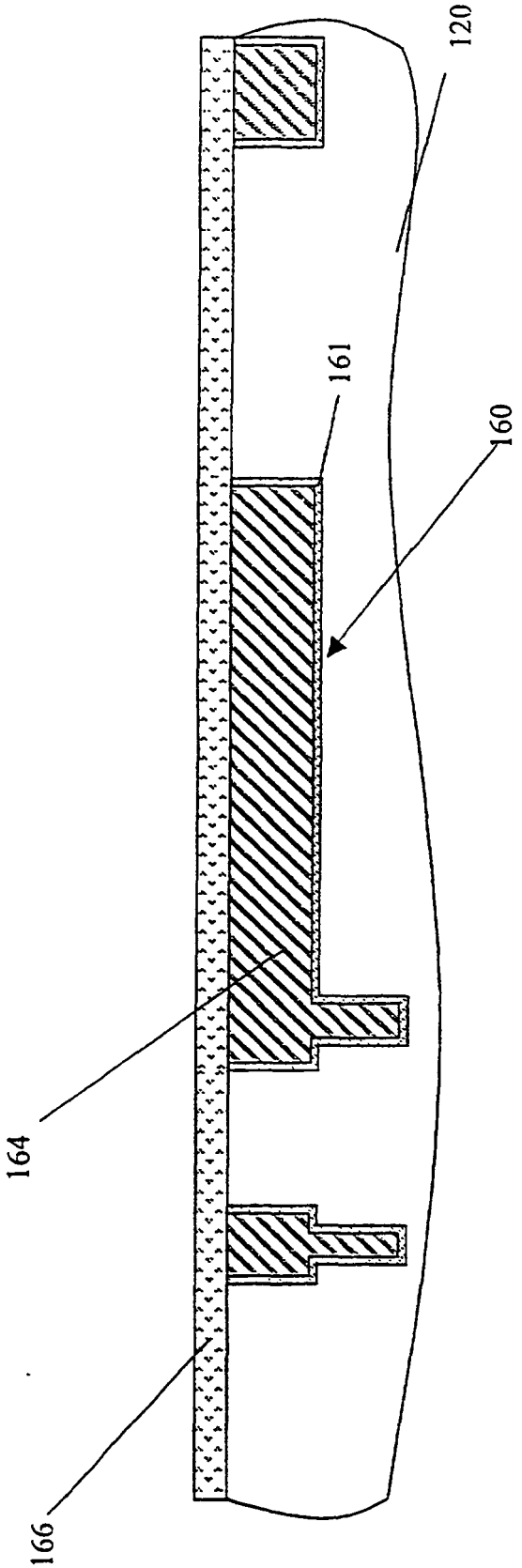


FIGURE 2

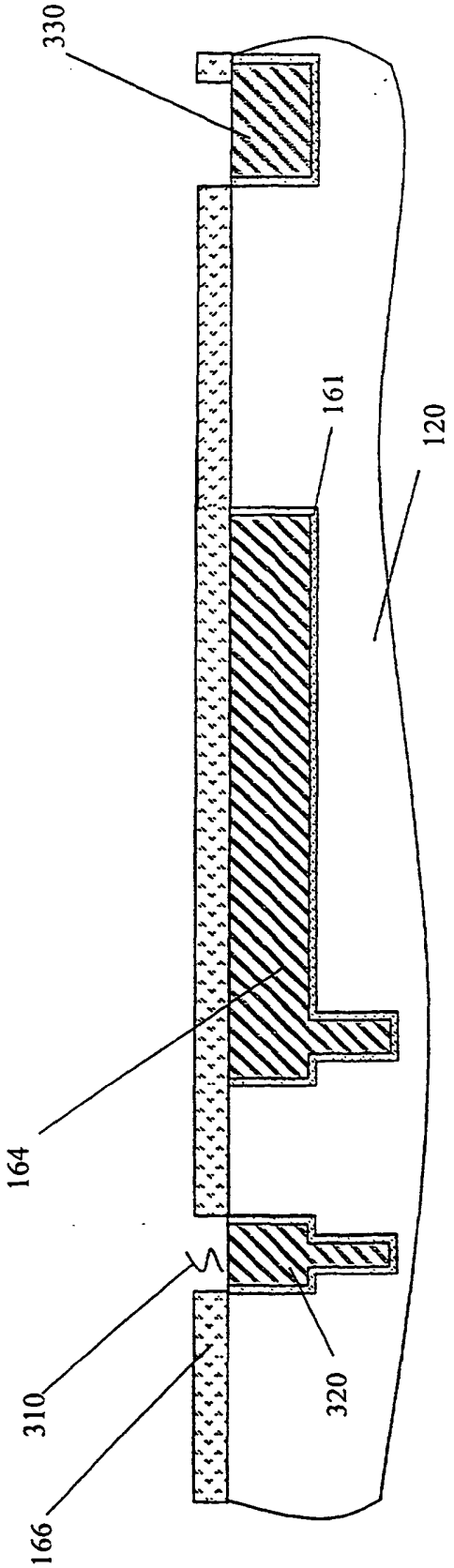


FIGURE 3

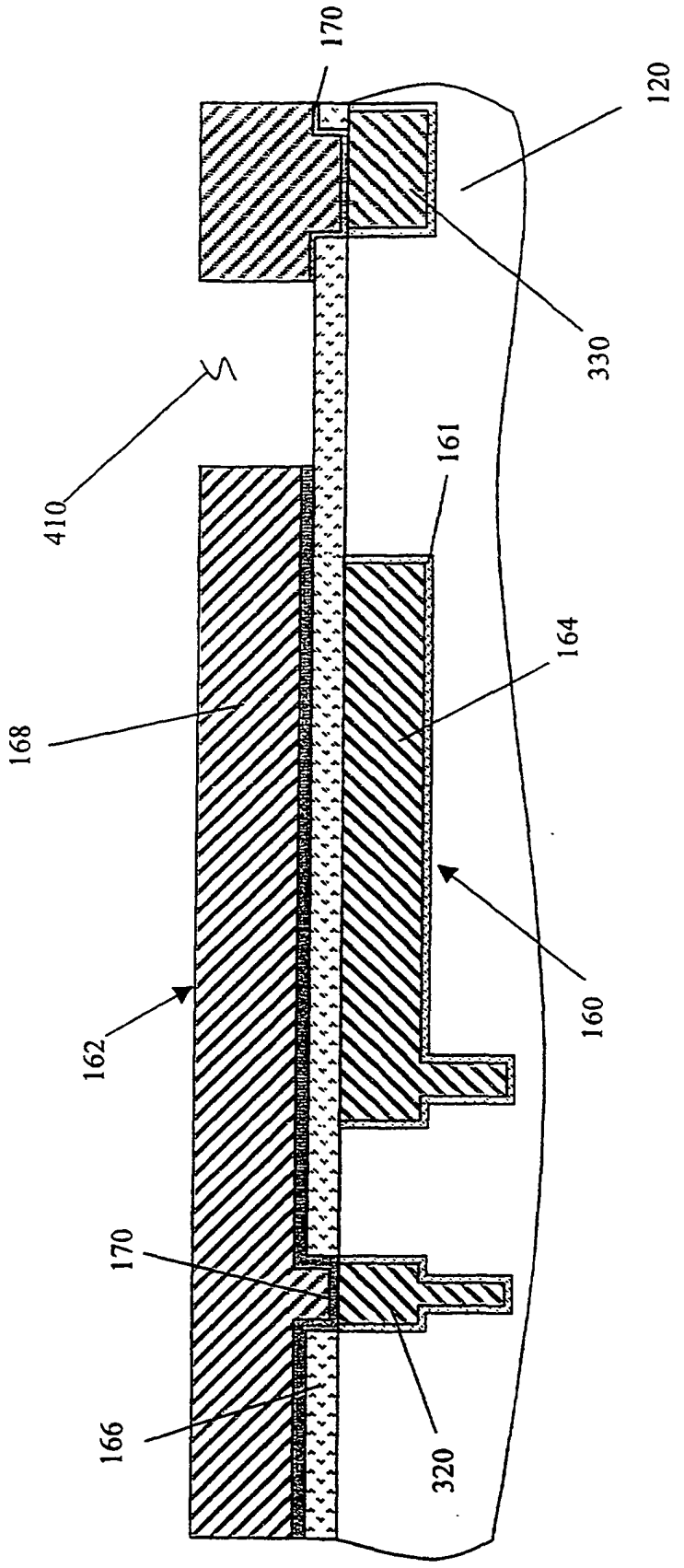
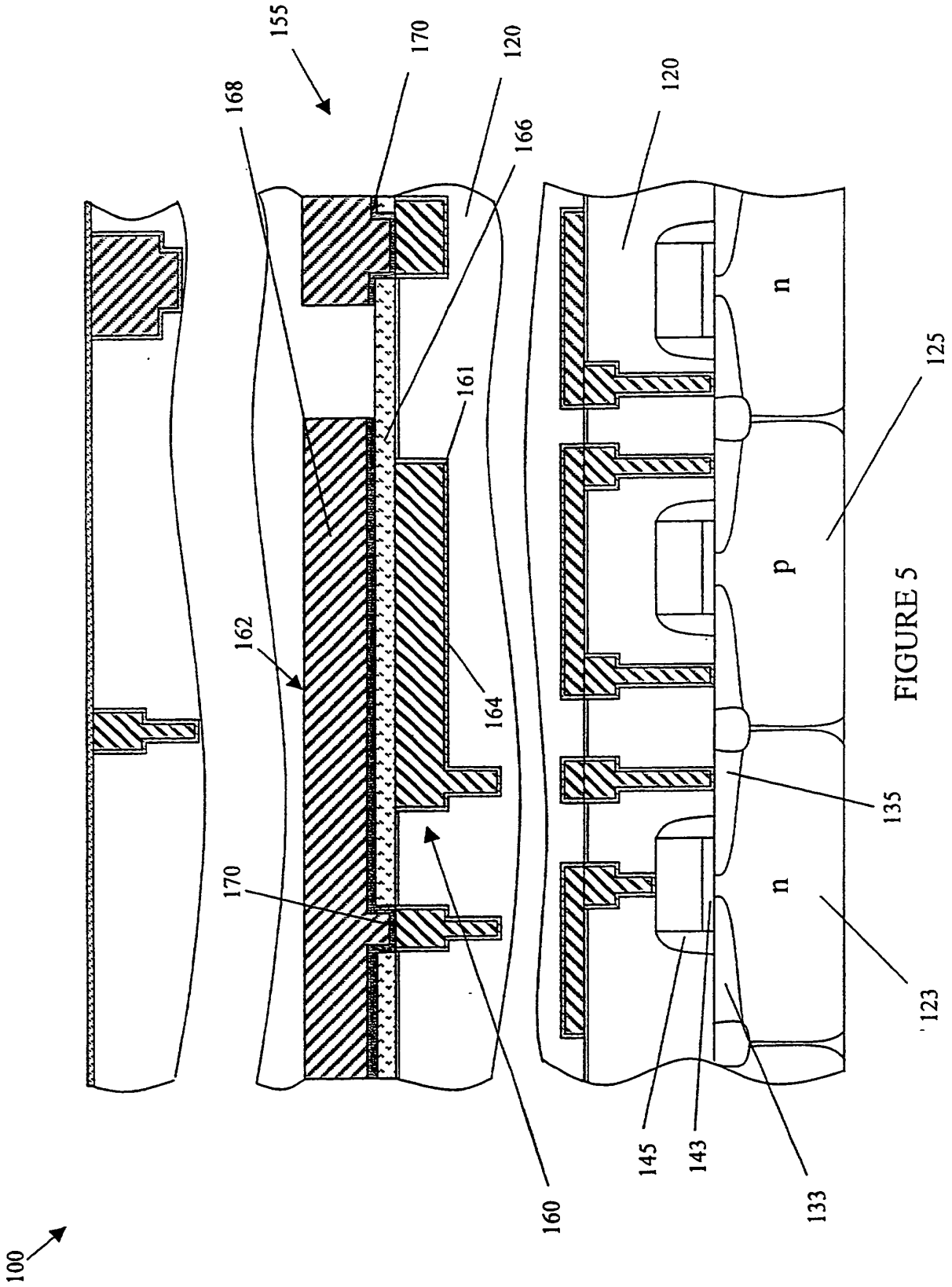


FIGURE 4


155
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161
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160
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143
133
123
100

FIGURE 5

REFERENCES CITED IN THE DESCRIPTION

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