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(54) LOGIC ARRAY ARRANGEMENTS

(71) We, NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION, a corporation organised and existing under the laws of Japan, of 6, 1, Uchisaiwai-cho, 1-chome, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to logic array arrangements, and particularly to logic array arrangements suitable for large scale logic integrated circuits (LSI).

Among prior art techniques are included a master slice type LSI and a programmable logic array (PLA). According to the former technique it is possible to design and manufacture at low costs LSI's having various logic functions by fabricating LSIs with common process steps up to the diffusion step and then with various wiring masks. However, when this method is applied to the manufacture of larger scale logic integrated circuits, the design of the wiring masks becomes more troublesome so that this method is not economical.

For this reason, the latter method has been developed. According to this latter method, the layout of the electronic circuit elements and connections required to construct such special logic circuits as a decoder, an AND array, an OR array, output buffer and the like is predetermined, and all logic circuits are realized by individually designing only one mask to program cross points of an AND array and of an OR array for fabricating all types of logic LSIs according to a desired logic circuit. This method is described, for example, in an article of the title "Programmable Logic Arrays" of Dr. William N. Carr et al "MOS/LSI Design and Application" published by McGraw Hill Book Co., 1972, pages 229—257, chapter 8. This method, however, is defective in that the use of the chip area is redundant so that even if the manufacture of fine structure LSIs becomes possible by the development of the technique of manufacturing LSI it would be impossible to realize high density and high efficiency logic LSIs but rather would result in an increase of redundancy.

Describing this defect in more detail, when designing logic circuits for various purposes, it has been impossible to fabricate desired logic circuits. For example in one application AND arrays are formed abundantly and OR arrays are deficient; whereas in another application OR arrays are surplus, but AND arrays are deficient. Furthermore, when constructing sequential circuits, it is necessary to separate the PLA output for applying it to the input of an external flip-flop circuit and to feedback the output of the flip-flop circuit to the PLA. To this end, it is necessary to provide an additional flip-flop circuit. When this flip-flop circuit is incorporated into the PLA, its efficiency of utilization would be degraded.

According to the present invention there is provided a logic array arrangement comprising a plurality of cell units formed on a semiconductor substrate, each said cell unit having an input terminal and an output terminal and comprising:

a plurality of row lines and a plurality of column lines arrangement in the form of a matrix;

a plurality of electronic elements;

a respective first conductive member connected to each of said row lines to each of said column lines and to each of said electronic elements;

a respective second conductive member connected to each of said input and output terminals; and

a plurality of nodes disposed between said conductive members, each said node comprising a point where a selected pair of said con-

ductive members are physically adjacent to one another and are either electrically connected together or are electrically isolated from one another, at least some of said nodes each being disposed at a said point of physical adjacency of one said first conductive member connected to a said row or column line and another said first conductive member connected to a said electronic element;

the arrangement of said electronic elements, said first conductive members and associated said nodes being such that at least two different types of logic circuit actual or potential can be traced through said elements, said first conductive members and said associated nodes; and

the arrangement of said first and second conductive members and associated said nodes being such that through said first and second conductive members and the relevant said associated nodes at least two different patterns of electrical connection actual or potential can be traced between said input and output terminals and a said logic circuit of each said cell and similarly also between said terminals of the respective said cells.

The electronic elements would normally comprise transistors and resistors.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram, partly in block form, showing the basic construction of a logic array arrangement embodying the invention;

Fig. 2 is a circuit diagram showing a logic circuit fabricated in programming the logic array arrangement shown in Fig. 1;

Figs. 3 and 4 are block diagrams showing systems in which arrangements according to this invention are utilized to improve logic capabilities;

Fig. 5 is a circuit diagram showing one example of an arrangement to which the invention is applied;

Fig. 6 is a sectional view taken along a line VIa—VIb . . . VII and showing the arrangement shown in Fig. 5 before forming a contact hole and through hole;

Fig. 7 is a circuit diagram showing a circuit utilizing the arrangement shown in Fig. 5 and in which a two bit decoder circuit and an array circuit are combined according to Table 1 herein;

Fig. 8 is a sectional view taken along the sme line as in Fig. 6 and showing a combination shown in Fig. 7 utilizing the arrangement shown in Fig. 5;

Figs. 9 and 10 are circuit diagrams showing a combination of an output buffer and an OR array, and a combination of a RS type flip-flop circuit and an OR array which are combined according to Table 1 herein and utilizing the arrangement shown in Fig. 5; and

Figs. 11A—11D, Figs. 12A—12D, Figs. 13A—13D, Figs. 14A—14D, Figs. 15A—15C, Fig. 16 and Figs. 17A and 17B are sectional views and top plan views showing some examples of nodes or switching elements utilized in this invention.

Fig. 1 shows the basic construction of a logic array arrangement according to this invention as comprising four cell units 11a to 11d and conductors 12 for interconnecting the cell units arrangement on a semiconductor substrate 10, each cell unit comprising a function unit 20 and an array unit 30. The detail of one of the function units is shown at A. As shown, the function unit 20 comprises a plurality of suitably arranged electronic elements such as transistors 21a to 21e and resistors 22a to 22c, conductors interconnecting these electronic circuit elements, and a group of nodes 26a, 26b . . . 26m (which may be switches) disposed between transistors 21a to 21e, resistors 22a to 22c and conductors 23a to 23h for connecting and disconnecting them Furthermore, each function unit is provided with electronic elements and connections which are necessary to form a flip-flop circuit, a decoder and output buffer circuits. A node 26i (i represents any one of a through m) is constructed to form a first metal layer through a contact hole when an LSI is fabricated. The actual construction of the nodes will be described later. Node 26i is shown as a small circle showing that this node is open.

The details of the array unit 30 are shown at B. Like the function unit 20 each array unit comprises electronic elements such as a transistor 31 and resistors 32a and 32b. Furthermore each array unit includes bit lines (row lines) 33a and 33b, product term lines (column lines) 34a to 34f which are arranged in the form of a matrix and wirings 36 adapted to determine the type of the logic circuit to be formed and the input and output conditions thereof. A group of nodes 37a through 37f are disposed between the electronic elements, bit lines, product term lines and wirings described above for constructing an AND array and an OR array when the nodes are opened or closed. Each of the nodes 37a through 37f has a construction similar to that of the node 26i of the function unit 20, the detail of the construction will be described hereinafter.

The wirings between respective cell units comprise connecting lines 40 for interconnecting the cell units 11a through 11d and input/output terminals 39a through 39h, a group of nodes 41aa through 41ij (where i and j are positive integers) and a group of nodes 43. Node 41ij is used to connect and/or disconnect a column line and a row line whereas nodes 43 are used to connect and/or disconnect sectionalized vertical wirings.

To construct a desired circuit by utilizing the arrangement shown in Fig. 1 nodes 26i,

37a through 37f, and nodes 41aa through 41ij of the function unit 20, and the array unit 30 of a cell unit and the wirings 12 between respective cell units are selectively closed.

Fig. 2 shows a connection diagram in which the function units 24a and 20b of the cell units 11a and 11b are connected to form an AND array; the function unit 20c of the cell unit 11c is connected to form a flip-flip circuit; the array unit 30c of the cell unit 11c is connected to form an OR array; the function unit 20d of the cell unit 11d is connected to form an output buffer whereas the array unit 30d of the cell unit 11d is connected to form an OR array. In Fig. 2, small black circles indicate that nodes at these portions are closed.

More particularly, to construct a decoder, transistors 21b, 21c and 21e and resistors 22a, 22b and 22c of the function units 20a and 20b of the cell units 11a and 11b are used and nodes 26b, 26e, 26g 26j, 26k and 26m are closed. When a signal applied to input line 23b is at a high level, transistor 21b is turned ON whereas transistor 21e is turned OFF so that a high level signal and a low level signal appear on lines 23k and 23m respectively. On the other hand, where the input signal is at a low level, a low level signal and a high level signal appear on lines 23k and 23m respectively. In other words, the same signal as the input signal appears on line 23k whereas a negation signal appears on line 23m.

To construct a flip-flop circuit, transistors 21a through 21e and resistors 22a through 22c of the function unit 20c of the cell unit 11c are used, and a signal is applied to lines 23k and 23m from the OR array 30c. When signals appearing on lines 23k and 23m are at high levels respectively, both transistors 21a and 21e become ON so that negation signals appear on lines 23b and 23c. On the other hand, when the signals appearing on lines 23k and 23m are at high and low levels respectively, transistors 21b and 21d are rendered OFF and ON respectively whereby signals applied to lines 23b and 23c are at low and high levels respectively. Where the signals appearing on lines 23k and 23m are at low and high levels respectively, transistors 21b and 21d are turned OFF so that signals at high and low levels appear on lines 23b and 23c respectively.

When the signals applied to lines 23k and 23m are at a low level, transistors 21b and 21d are maintained in the states previously established so that the same outputs as before appear on lines 23b and 23c.

To form an output buffer circuit, transistors 21a, 21c and 21e and resistors 22a, 22b and 22c of the function unit 20d of the cell unit 11d are used, and nodes 26a, 26c, 26d, 26f, 26j and 26m are closed. When the OR array 30d produces an OR output transistor 21a is turned ON to obtain the negation output of the OR array on line 23c and an affirmation output of the OR array on line 23b.

To form an AND array, nodes 37a and 37b of the array units 30a and 30b of the cell units 11a and 11b are closed and node 37d is selectively closed. Under these conditions a high level output is produced on a product term line when all inputs to bit lines which constitute the AND circuit become a high level.

To form an OR array, nodes 37b and 37c of the array units 30c and 30d of the cell units 11c and 11d are closed whereas node 37d is selectively closed. Under these conditions, when any one of the product term line constituting the OR circuit becomes high level a low level output is produced on a corresponding bit line.

Cell units 11a through 11d cooperate to from a logic array arrangement. The input signal applied to input terminal 39a is applied to decoder 20a via interconnecting lines. One of the two outputs of the flip-flop circuit is produced on output terminal 39f and the other output is applied to decoder 20b. The outputs of the output buffer appear on its output terminals 39g and 39h.

The arrangement shown in Fig. 2 comprises a single stage. Generally, however, it is possible to reduce the size of the semiconductor substrate that is the chip size by dividing the arrangement into a number of smaller logic function circuits for constructing a multistage arrangement as shown in Fig. 3, for example, rather than forming a large logic circuit with a single stage arrangement. In some cases, it is possible to reduce the chip size to less than 1/10. Although the logic circuit shown in Fig. 3 comprises two stages, of course it is possible to increase the number of stages as desired. When it is possible to arbitrary sectionalize the produce term lines and the bit lines of the arrangement, such division may be made so long as the sum of the numbers of the adjacent product term lines in the horizontal direction and the sum of the numbers of the adjacent bit lines in the vertical direction are less than prescribed values thus alleviating the limits on the number of product term lines and the number of the bit lines of the arrangement. With this arrangement the function of each cell unit would not be specified so that versatile design can be made. For this reason, when the cell units of the arrangement are divided as shown by solid lines in Fig. 4 it is possible to change the layout as shown by dotted lines in Fig. 4. Such versatility enables use of chips of small areas for realizing the same logic.

Fig. 5 shows the detail of one example of logic array arrangement of this invention comprising four cell units 100 each made up of a function unit 200 and an array unit 300. In this embodiment the function units 200 comprise resistors 201 through 204, NPN bipolar

transistors 205 through 212 and 225 through 232 and resistors 213 through 224 and 233 through 236, whereas the array units 300 comprise NPN transistors 337 through 348 and resistors 350 through 352. These electronic circuit elements are formed on a single semiconductor substrate which may be, for example, a silicon wafer, or a silicon substrate formed on a germanium, gallium, sapphire or other insulators. In Fig. 5, there are also shown wiring lines 101 through 129 for interconnecting the electronic elements of the function units 200 and the array units 300. Of these wiring lines straight lines show first metal layer wiring of multilayer construction while wavy lines the second metal layer wiring small circles show the position of through holes and squares the positions of the contact holes. The through holes or contact holes are formed at these positions depending upon the functions of the logic circuits to be formed.

The functions of respective wiring lines are as follows. Wiring lines 101 and 102 are signal lines utilized as the wirings between multistage arrangements, as the wirings to bonding pads or as the wiring for feedback. As shown in Fig. 5, these signal lines are formed on the second metal layer except portions 116 and 117 which are formed on the first metal layer. Each wiring line described above is connected or disconnected whether through holes are provided or not for the nodes located between the portions 116 and 117 and wiring lines 101a, 101b, 102a and 102b on both sides thereof.

Line 103 acts as a $-V_{EE2}$ line connected to a source of voltage having a voltage of $-V_{EE2}$, lines 104 and 110 act as $-V_{EE}$ lines connected to a source of voltage having a voltage of $-V_{EE}$, line 105 acts as a V_{cs} line connected to a source of voltage having a voltage of V_{cs}, lines 118 and 106 act as V_{ref2} line connected to a source of voltage having a voltage of V_{ref2}, line 107 acts as a V_{ref2} line connected to a source of voltage having a voltage of V_{ref2}, and lines 108 and 109 are grounded lines.

Lines 111, 112 and 113 are product term or column lines utilized to pass product signals of the AND array. When not utilized to pass product term lines they can be used as connecting lines between the arrangements of a multistage arrangement. Most of these product term lines comprise the first layer wires except portions 111a, 112a and 113a which are constructed as the second layer wires. Accordingly, it is possible to connect to and disconnect from the product term lines of other cell units depending upon whether through holes are provided or not for the nodes defined between the opposed ends of the portions 111a, 112a and 113a and of the remaining portions 111b, 112b and 113b.

Where a Fig. 5 cell unit is used as the AND array of the uppermost stage of the arrangement like the cell unit 11a shown in Fig. 2, the lines 114 and 115 can be used as the grounded conductors, but as signal lines in other cases.

Lines 121 through 124 which constitute a matrix together with the product term lines 111, 112 and 113 act as bit lines which are also formed on the second metal layer and when through holes are provided for nodes interposed between the second layer portions 121a, 122a 123a and 124a and the first layer portions 121b, 122b, 123b and 124b it is possible to integrally form the bit lines 121a through 124a with corresponding bit lines of a cell unit disposed on the back of the cell unit 110.

Resistors 350 through 352 are connected in the uppermost stage of an AND array, and in the illustrated embodiment, one end of these resistors are connected to the product term lines 111, 112 and 113 respectively.

Lines 119, 120, 128 and 129 constitute input or output terminals of the four cell units 100.

Fig. 6 is a longitudinal sectional view of the Fig. 5 arrangement taken along a line VIa—VIb . . . VII and not provided with any through hole and contact hole. In Fig. 6 reference numeral 400 designates a P type semiconductor substrate, 401 the first layer wiring line, 402 the second layer wiring line, and 403 and 404 insulators. Table 1 below shows the ON and OFF conditions of the through holes and the contact holes comprising respective nodes when the cell units 100 are shown in Fig. 5 are used to fabricate various logic circuits.

TABLE 1

No.	Combined Arrangement	ON OFF Conditions of Nodes						
		a	b	c	d	e	f	g
A	two bit decoder and AND array		0		0		0	0
B	output buffer and OR array			0		0	0	0
C	RS flip-flop circuit and OR array	0			0	0		0

Remarks:

0 mark ..... ON state of the node

no mark ..... OFF state of the node

Where a combination of a two bit decoder circuit and an AND array is to be formed, the first layer lines and the second layer lines are interconnected through holes b, d, f and g according to item A shown in Table 1. The circuit completed by this connection is shown in Fig. 7 in which reference numerals 119 and 120 show the input lines of a two bit decoder constituted by two stage cascade connected emitter coupled logic circuit (ECL). Denoting the input signals applied to these lines Y and X, corresponding signals $(\overline{X}+\overline{Y})$, $(X+\overline{Y})$, $(X+Y)$ and $(\overline{X}+Y)$ are produced respectively on lines 121, 122, 123 and 124. In this case, resistors 350, 351, and 352 are connected in only the uppermost stage of the AND array. The actual sectional construction corresponding to Fig. 6 is shown by Fig. 8.

The two bit decoder system utilized in this embodiment is more advantageous than a conventional one bit decoder system in that it requires smaller number of the product term lines. This tendency becomes more remarkable when an arithmetic logic such as an adder is contemplated and the number of the product term lines can be reduced to about 1/10 of the one bit decoder system in some cases.

Where a combination of an output buffer and an OR array is to be formed, the first metal layer and the second metal layer are interconnected through holes c, e, f and g according to item B of Table 1. Fig. 9 shows a circuit constructed by such connections and by utilizing 1/4 of the four cell units of Fig. 5. In this case, the logical sum signal of the output signals on product term lines 111, 112 and 113 is produced on line 121 and this signal is applied to the base electrode of a transistor 225 and is then sent to an output terminal 128 through the collector electrode of transistor 209. When this combination of an output buffer and an OR array is applied to all cell units 100 shown in Fig. 5, four identical combinations are formed.

In this example, the output signal of the output buffer, that is the signal appearing on the output terminal 128 is at the level of V_{ref2}. However, where it is desired to produce an output at the level of V_{rf1}, the resistor 217 shown in Fig. 7 is removed and the V_{ref2} line 106 connected to the base electrode of transistor 209 should be connected to V_{rf1} line 107.

To form a combination of a RS type flip-flop circuit and an OR array, the first metal layer and the second metal layer of respective nodes are interconnected through holes, a, d, e and g according to item C of Table 1. The circuit formed by this connection is shown in Fig. 10. As can be noted from Fig. 10 this circuit is constructed by using 1/2 of the four cell units shown in Fig. 5. The flip-flop circuit constructed in this manner is a simple RS type flip-flop circuit, but other types of flip-flop circuits such as a clock gated RS flip-flop circuit, a set preference flip-flop circuit, a D flip-flop circuit and a T flip-flop circuit can be realized by constructing the circuit such that the combination logic is computed by the AND array and the OR array and that the output thereof is applied to the input of the RS flip-flop circuit. Figs. 11 through 17 show examples of the nodes which connect and interrupt the metal layers. Figs. 11A—11D show a case in which a first metal layer and a second metal layer are interconnected or interrupted at nodes by

the presence or absence of through holes. Figs. 11A and 11B show an interrupted state, while Figs. 11C and 11D an interconnected state. In the state shown by Figs. 11A and 11B a first metal layer 401 formed on the upper surface of a semiconductor substrate 400 via a dielectric layer 404, and a second metal layer formed on the first metal layer 401 through a dielectric layer 403 are separated by the dielectric layer 403 so that the first and second metal layers 401 and 402 are electrically interrupted. This means that a node at this position is open.

Figs. 11C and 11D shows a state in which the first and second metal layers shown in Figs. 11A and 11B are interconnected by providing a through hole 410 for the dielectric layer 403 interposed between these metal layers. This means that the node at this position is closed. To interconnect or not the first and second metal layers is determined whether the through opening 410 is formed or not through the dielectric layer 403. Such through opening can be formed or not by changing a mask that determines the pattern of the dielectric layer 403.

Figs. 12A through 12D show a modification of the node shown in Figs. 11A through 11D in which Figs. 12A and 12B show an interrupted state and Figs. 12B and 12C an interconnected state. In this case, in order to electrically isolate first and second metal layers 401 and 402, as shown in Figs. 12A and 12B, the first metal layer 401 is formed on the first dielectric layer 404 such that it terminates a short distance from a through hole 411 of the second dielectric layer 403 on which the second metal layer 402 is formed subsequent to the formation of the first metal layer. With this construction, although the second metal layer 402 extends through the through hole 411, since the first metal layer 401 does not reach the through hole, the first and second metal layers are positively isolated. Thus, this node is open. Conversely, in the construction shown in Fig. 12C and 12D, as the first metal layer 401 extends immediately beneath the through hole 412, the first and second metal layers 401 and 402 are electrically interconnected. Consequently, this node is closed. In the cases shown in Figs. 12—12D, the design of the mask pattern for forming the first metal layer 401 is changed depending upon whether the node is to be closed or open.

In the cases shown in Figs. 13A—13D a diffusion layer 420 formed on the semiconductor substrate and the first metal layer 401 are interconnected or disconnected depending upon the presence or absence of a contact hole 421. Figs. 13A and 13B show a case wherein metal layers 420 and 401 are disconnected whereas Figs. 13C and 13D show a case wherein the metal layers 420 and 401 are interconnected. It should be understood that Figs. 13A and 13C are shown with dielectric layer 403 removed. In the case shown in Figs. 13A and 13B, a dielectric layer 404 is formed on the diffusion layer 420 on the semiconductor substrate 400 and the first metal layer 401 is formed on the dielectric layer 402. A second dielectric layer 403 is formed on the first metal layer 401. As a consequence, the diffusion layer 420 and the first metal layer 401 are electrically isolated, meaning that the node at this position is open. On the other hand, Figs. 13C and 13D show a case wherein the diffusion layer 420 and the first metal layer 401 are interconnected through contact hole 421 provided for the dielectric layer 404. This means that the node formed at this position is closed. In this case, a mask pattern for forming the contact hole 421 through the dielectric layer 404 is changed depending upon whether the dielectric layer 404 is changed depending upon whether the node is to be closed or open.

Figs. 14A—14D show cases wherein a diffusion layer 420 formed on the semiconductor substrate 400 is connected to or disconnected from the first metal layer 401 depending upon the presence or absence of a contact hole 412. Figs. 14A and 14B show a disconnected state, while Figs. 14C and 14D show an interconnected state. Figs. 14A and 14C are shown with the dielectric layer 403 removed. Different from the cases shown in Figs. 13A—13D, in which the diffusion layer 420 and the metal layer 401 are interconnected or disconnected depending upon the presence or absence of the contact hole, in the cases shown in Figs. 14A—14D a contact hole 412 is formed through a dielectric layer 404 formed on a diffusion layer 420, and where it is necessary to disconnect the diffusion layer 420 from the first metal layer 401 this layer is terminated short of the contact hole 412. Then the dielectric layer 403 overlying the first metal layer 401 fills the contact hole 412 thus preventing other metal layer from reaching the diffusion layer 420 through the contact hole 412. On the contrary, in the case shown in Figs. 14C and 14D, the first metal layer 401 is formed to reach the contact hole 412 thereby connecting the first metal layer 401 to the diffusion layer 420 through the contact hole 412. Accordingly, in the cases shown in Figs. 14—14D, the mask pattern for forming the first metal layer 401 is changed depending upon whether the node is to be closed or open.

In the foregoing embodiments nodes are closed or open by means of contact holes and through holes, but other well known nodes can also be used. Figs. 15, 16 and 17 illustrate examples of such other nodes.

Figs. 15A, 15B and 15C show diode nodes. In the case of Fig. 15A, two diodes 440 and 441 connected in series opposition are formed

at programmed positions corresponding to the contact holes and the through holes described above. With this arrangement, terminals A and B are electrically isolated. When an overvoltage which make terminal A to be negative and terminal B to be positive, lefthand diode 440 would be ruptured, thus forming a short circuit condition. Consequently, an electric path which is conductive for the current flowing from terminal A to terminal B but not conductive for the current flowing in the opposite direction, as shown in Fig. 15B. Conversely, when an overvoltage of the opposite polarity is impressed across terminals A and B there is formed an electric path which is conductive for the current flowing from terminal B to terminal A but not conductive for the current flowing in the opposite direction, as shown in Fig. 15C. When the diode node described above is used it is not necessary to change the design of the mask pattern. Accordingly, it is possible to programme the arrangement after completion of manufacture.

Fig. 16 shows another example, wherein a fuse 450 is provided at a predetermined node position. In this case, the circuit between terminals A and B is normally conductive, but will be interrupted when the fuse 450 is blown out. Again, it is possible to programme the arrangement after completion of manufacture.

Figs. 17A and 17B show a case wherein a floating gate 460 comprising a FAMOS (floating gate avalanche injection MOS) is provided at a predetermined node position. Where electrons are not accumulate in the floating gate 460 as shown in Figs. 17A terminals A and B are isolated. Conversely, when a high voltage is impressed across terminals A and B, electrons are accumulated in the floating gate 460 with the result that an inversion layer, or a channel 461 is formed at the interface of the semiconductor substrate 466 beneath the floating gate 460, thereby connecting terminal A with terminal B through a metal layer 462, diffusion layer 463, channel 461, diffusion layer 464, and metal layer 465. In Figs. 17A and 17B, reference numerals 467 through 469 designate dielectric layers.

Arrangements according to this invention have the following advantages.

(1) Since electronic circuit elements such as transistors and resistors of the function unit and the array unit which constitute a cell unit are connected to wiring lines through nodes, instead of being connected to some extent to the wiring line for manifesting specific functions as in the prior art arrangement it is free to change the logical functions, thereby greatly improving the logic capabilities.

To more clearly demonstrate this advantage, an arrangement according to this invention is compared with a prior art PLA. Let us consider package devices I and II having gates, flip-flop circuits (FF) input terminals and output terminals of the numbers as shown in Tables 2 and 3. To fabricate device II of the packages A—N and A—F, PLAs having sizes shown in the lowermost rows are necessary. These sizes show the maximum values required to fabricate package A—N. The data regarding the size of the particular arrangements according to this invention are derived from the data wherein the sum of the number of the AND array bit lines and the number of the OR array bit lines of each package is a maximum whereas the data regarding the size of commercial PLAs are derived from respective maximum values of the bit numbers of the AND array and the OR array.

TABLE 2

Device I

Package Code	Package				Arrangement of this invention		Commercial PLA	
	gate number	FF number	input terminal number	output terminal number	AND array bit line number	OR array bit line number	AND array bit line number	OR array bit line number
A	111	13	60	21	73	38	87	38
B	97	8	47	16	50	26	60	26
C	127	9	45	38	59	24	59	26
D	199	26	34	66	63	44	101	44
E	195	24	32	50	68	61	141	61
F	211	0	43	37	56	36	83	36
G	133	0	58	26	65	26	65	28
H	159	16	45	32	55	36	83	36
I	156	19	37	29	62	30	69	30
J	249	30	15	15	45	19	45	20
K	154	11	44	37	62	42	97	42
L	223	27	52	33	91	43	99	43
M	136	11	49	33	43	23	53	23
N	165	2	47	27	54	22	54	23
Necessary Size (pieces)	249	30	60	50	91	43	141	61

TABLE 3

Device II

Package Code	Package				Arrangement of this invention		Commercial PLA	
	gate number	FF number	input terminal number	output terminal number	AND array bit line number	OR array bit line number	AND array bit line number	OR array bit line number
A	170	0	8	8	16	8	18	8
B	122	0	16	9	32	9	32	14
C	46	0	8	5	16	5	16	7
D	46	0	9	5	18	5	18	8
E	46	0	6	4	12	4	12	5
F	3	0	2	1	4	1	4	2
Necessary Size (pieces)	170	0	16	9	32	9	32	14

From these data it can be noted that in order to fabricate device I by a prior art PLA technique it is necessary to use 61 OR array bit lines and 141 AND array bit lines (total 202). However, when device I is designed according to this invention the total number of bit lines is only 134.

To fabricate device II by a prior art technique it is necessary to use 32 AND array bit lines and 14 OR array bit lines (total 46) whereas when the device is designed in accordance with this invention, the total number of the bit lines is 41.

These data show that the logic array arrangement can increase its logic capability by 10 to fifty percent over that prior art arrangement.

Considering a case in which a plurality of

PLAs are fabricated on the same semiconductor substrate and supposing now that each package A—N of device I contains one PLA, the prior art PLA technique requires 1974 AND array bit lines and 854 OR array bit lines (total 2828) whereas a particular arrangement of this invention requires only 846 AND array bit lines and 470 OR array bit lines (total 1316).

With reference to device II, in a case wherein each PLA contains four A and each one of B, C, D, E and F, the prior art PLA techniques requires 188 AND array bit lines and 81 OR array bit lines (total 369) whereas a particular arrangement of this invention requires only 146 AND array bit lines and 56 OR array bit lines (total 202).

As can be noted from the foregoing description, in a case wherein a plurality of arrangements are fabricated on the same semiconductor substrate it is also possible to increase the logical capability by 180 to 210 per cent than the prior art arrangement.

(2) Furthermore, it is possible to use various well known methods of increasing the capabilities of PLA, for example a two decoder system, multistage PLA system, division of the product lines and the bit lines. For this reason, according to this invention it is possible to obtain arrangements having higher capabilities than the prior art PLAs having the maximum capabilities realized by using various methods of increasing the capability of PLAs.

(3) Actually, however, according to this invention, it is necessary to individually design various metal layer masks as well as wiring masks for preparing function units and array units. However, the latter masks comprises only few types of definite patterns and since the mask patterns can be processed with a computer, no hand work is necessary for their design. Accordingly, it is possible to manufacture larger scale logic integrated circuit at low cost and simple design.

It should be understood that the invention is not limited to the specific embodiments described above. Thus, for example, although the invention has been described in terms of optical exposure method utilizing mask patterns, electron beam exposure method can also be used in which case the mask pattern is replaced by electron beam exposure pattern.

WHAT WE CLAIM IS:—

1. A logic array arrangement comprising a plurality of cell units formed on a semiconductor substrate, each said cell unit having an input terminal and an output terminal and comprising:

a plurality of row lines and a plurality of column lines arranged in the form of a matrix;

a plurality of electronic elements;

a respective first conductive member connected to each of said row lines to each of said column lines and to each of said electronic elements;

a respective second conductive member connected to each of said input and output terminals; and

a plurality of nodes disposed between said conductive members, each said node comprising a point where a selected pair of said conductive members are physically adjacent to one another and are either electrically connected together or are electrically isolated from one another, at least some of said nodes each being disposed at a said point of physical adjacency of one said first conductive member connected to a said row or column line and another said first conductive member connected to a said electronic element;

the arrangement of said electronic elements, said first conductive members and associated said nodes being such that at least two different types of logic circuit actual or potential can be traced through said elements, said first conductive members and said associated nodes; and

the arrangement of said first and second conductive members and associated said nodes being such that through said first and second conductive members and the relevant said associated nodes at least two different patterns of electrical connection actual or potential can be traced between said input and output terminals and a said logic circuit of each said cell and similarly also between said terminals of the respective said cells.

2. An arrangement according to claim 1 wherein the relevant pair of conductive members at each said node are either permanently electrically connected together or are permanently electrically isolated from one another in a predetermined pattern, whereby said actual type of said logic circuit and said actual pattern of electrical connection are determined during manufacture of said arrangement to provide a programmed logic array.

3. An arrangement according to claim 1 wherein the relevant pair of conductive members at each said node are electrically connected together in a manner susceptible to subsequent individual selective disconnection to isolate that pair of conductive members from one another, whereby the arrangement is a programmable logic array arrangement.

4. An arrangement according to claim 1 wherein the relevant pair of conductive members at each said node are electrically isolated from one another in a manner susceptible to subsequent individual selective connection to connect that pair of conductive members to one another, whereby the arrangement is a programmable logic array arrangement.

5. An arrangement as claimed in claim 1 wherein the relevant pair of conductive

members at each said node are either in a mutually electrically connected state or are in a mutually electrically isolated state in a manner susceptible to subsequent individual selective switching from one said state to the other, whereby the arrangement is a programmable logic array arrangement.

6. An arrangement according to claim 2 wherein the first and second conductive members comprise metal layers on a layer of dielectric material, and wherein each said node of permanent electric isolation is provided by a portion of the dielectric material, and wherein each said node of permanent electrical connection is formed by conductive material which extends through a hole formed through said dielectric layer and into contact with a said selected pair of said conductive members.

7. An arrangement according to claim 6 wherein each said node comprises a point where respective metal layer portions of a selected pair of said conductive members lie in register on opposite faces of said dielectric layer.

8. An arrangement according to claim 6 wherein each said node of permanent electrical isolation is provided by a portion of the dielectric material disposed between laterally spaced physically adjacent metal layer portions of a selected pair of said conductive members.

9. An arrangement according to claim 3 wherein the relevant pair of conductive members at each said node are electrically connected together by means of a fusible element susceptible to subsequent blowing by the passage of an overcurrent.

10. An arrangement according to claim 4 wherein the relevant pair of conductive members at each said node are electrically isolated from one another by means of a pair of diodes connected in series opposition between said pair of members, said diodes being susceptible to subsequent selective individual rupture by the impression across said series pair of an over voltage of one or other polarity whereby to render said anode conductive for a selected direction of conduction.

11. An arrangement according to claim 5 wherein the relevant pair of conductive members at each said node are connected to one another by means of a floating gate avalanche junction field effect transistor, said transistor being susceptible to subsequent switching from an open to a closed switch state by accumulation of electrons in its floating gate.

12. An arrangement according to any one of claims 1 to 11 wherein each said cell unit comprises a function unit and an array unit, said function unit including such electronic elements, first conductive members and nodes, and said array unit including said matrix, such electronic elements, first conductive members and nodes.

13. An arrangement according to claim 12 wherein the arrangement of said electronic elements, said first conductive members and associated said nodes is such that for each of said function unit and said array unit at least two different types of logic circuit actual or potential can be traced through said elements, said first conductive members and said associated nodes.

14. An arrangement according to claim 13 wherein said different types of logic circuit for said function unit comprise a flip-flop circuit and a decoder, and wherein said different types of logic circuit for said array unit comprise an AND array and an OR array.

15. A programmable logic array arrangement substantially as described herein with reference to Figure 1, or Figure 5, or Figures 5 and 6, in each case together with Figures 15A to 15C, or Figure 16, or Figures 17A and 17B, of the accompanying drawings.

16. A programmed logic array arrangement made by programming an arrangement as claimed in any one of claims 3 to 5, 9 to 11 and 15.

17. A programmed logic array arrangement as claimed in claim 2 and substantially as described herein with reference to the accompanying drawings.

18. A logic array arrangement as claimed in claim 1 and substantially as described herein with reference to the accompanying drawings.

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Agents for the Applicants.

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FIG.1

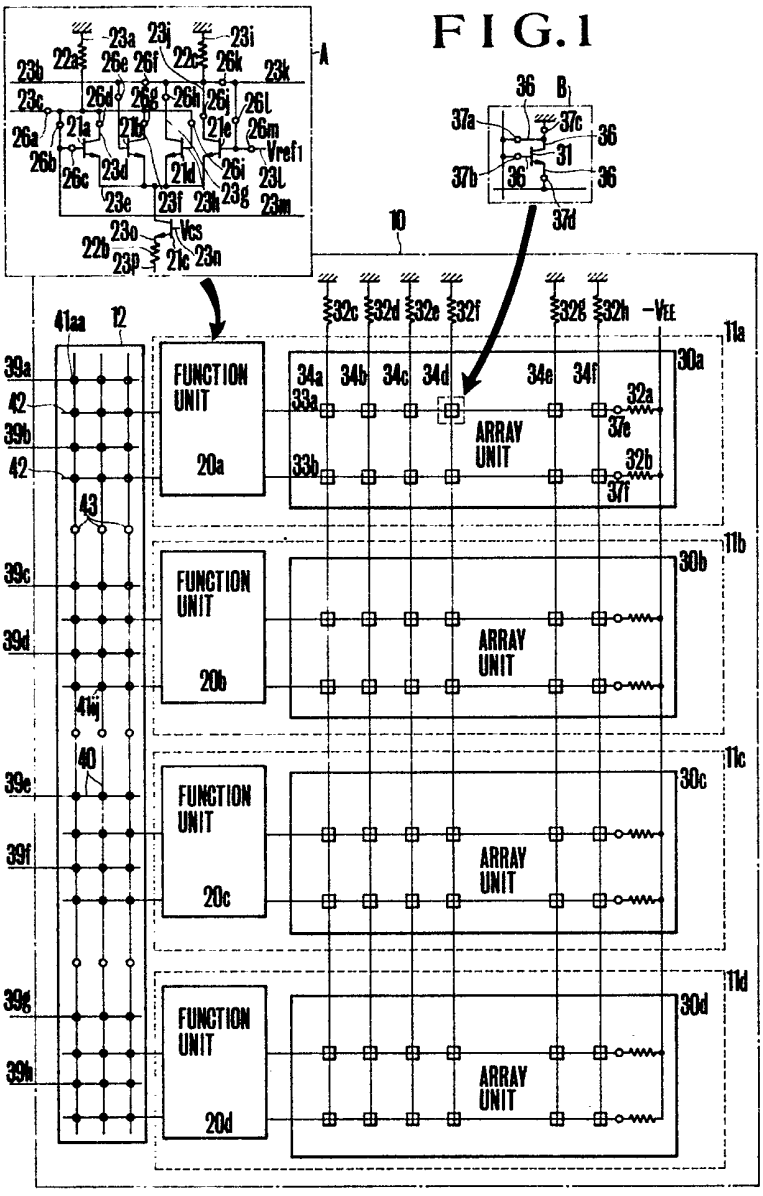

A
B
10
FUNCTION UNIT
20a
20b
20c
20d
ARRAY UNIT
11a
11b
11c
11d
30a
30b
30c
30d
-VEE

FIG.2

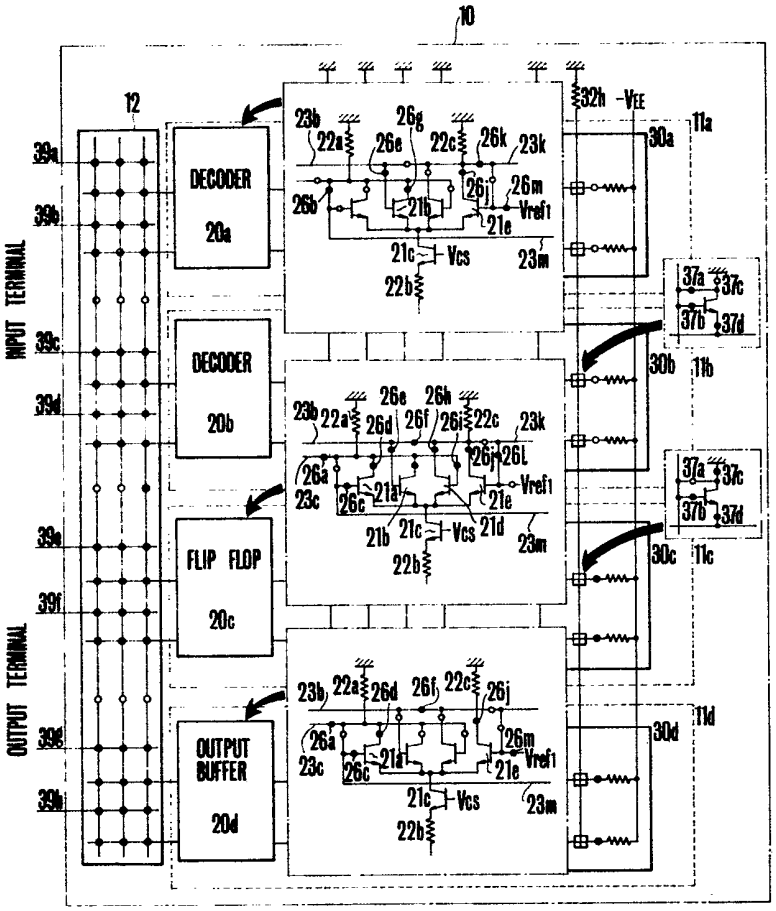

10
12
INPUT TERMINAL
OUTPUT TERMINAL
39a
39b
39c
39d
39e
39f
39g
39h
DECODER 20a
DECODER 20b
FLIP FLOP 20c
OUTPUT BUFFER 20d
11a
11b
11c
11d
30a
30b
30c
30d
32h -VEE
Vref1
Vcs

FIG.3

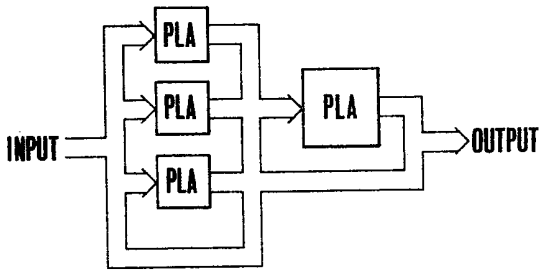

PLA
PLA
PLA
PLA
INPUT
OUTPUT

FIG.4

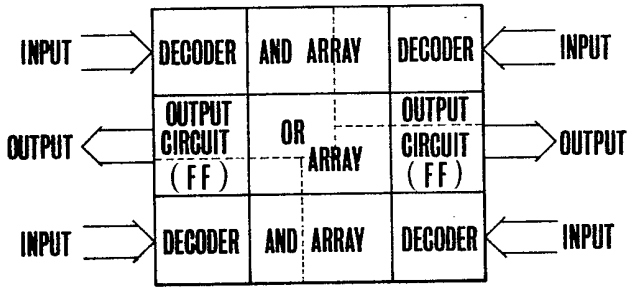
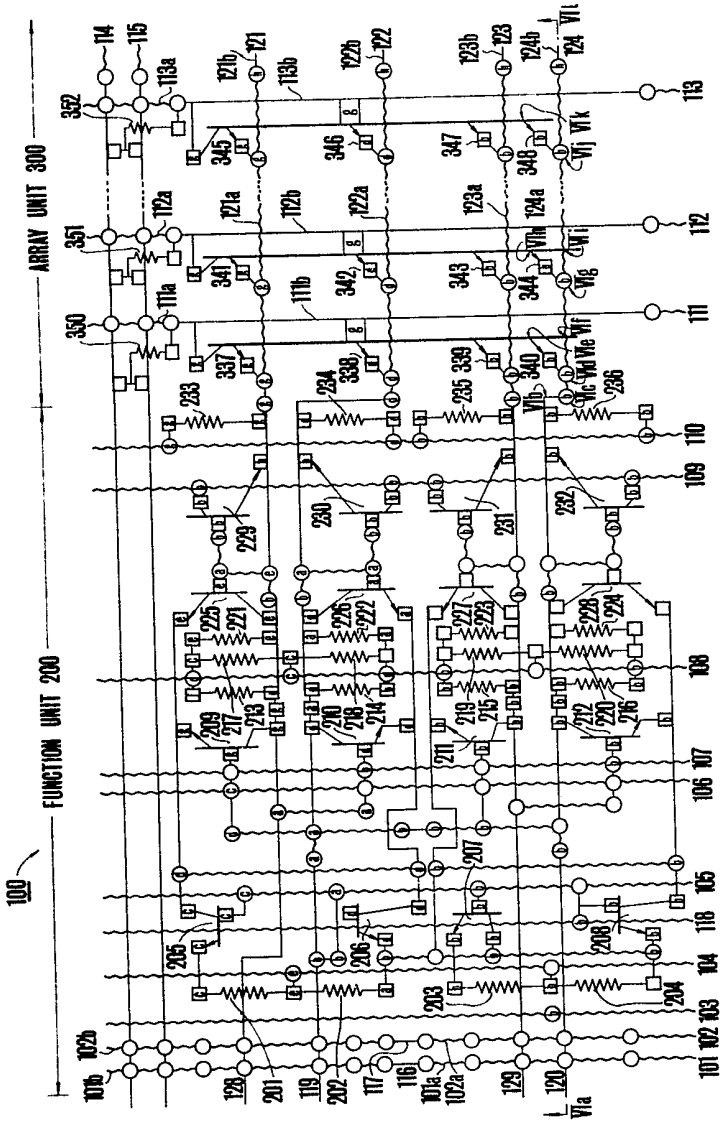

INPUT
DECODER
AND ARRAY
DECODER
INPUT
OUTPUT
OUTPUT CIRCUIT (FF)
OR ARRAY
OUTPUT CIRCUIT (FF)
OUTPUT
INPUT
DECODER
AND ARRAY
DECODER
INPUT

FIG.5



1600623 COMPLETE SPECIFICATION
10 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 5

FIG.6

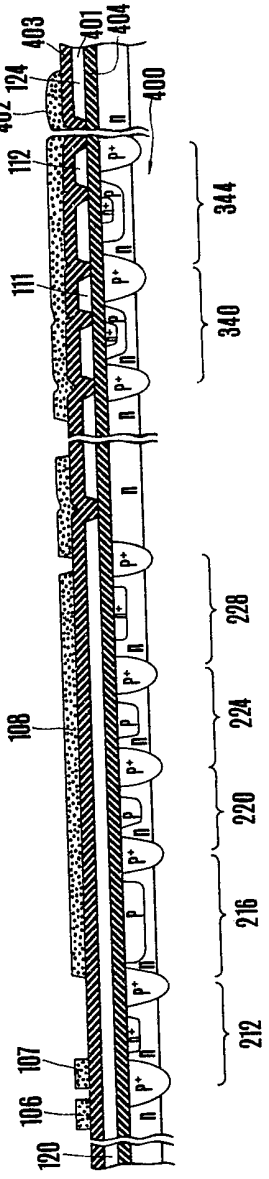


FIG.8

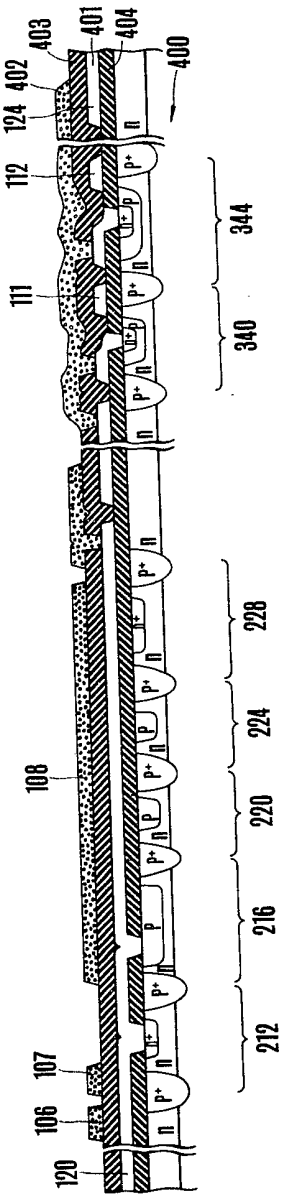


FIG.7

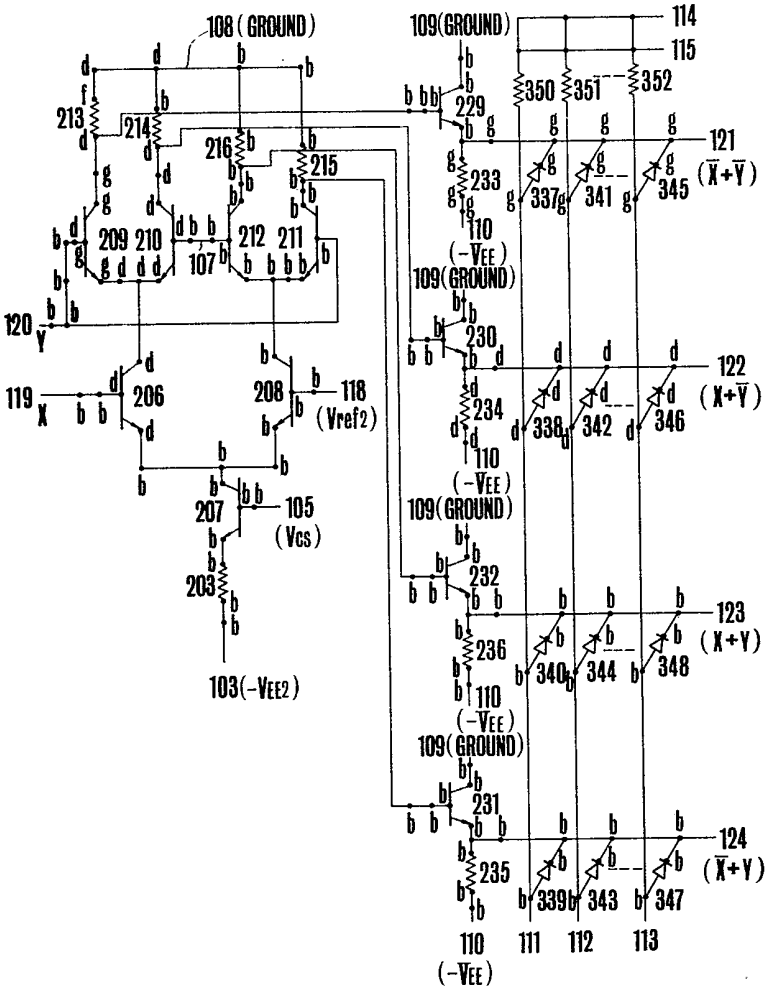

108 (GROUND)
109(GROUND)
114
115
213
214
216
215
229
350
351
352
121
(X̄+Ȳ)
233
337
341
345
110
(-VEE)
209
210
212
211
107
120
Y
230
122
(X+Ȳ)
234
338
342
346
119
X
206
208
118
(Vref2)
232
123
(X+Y)
236
340
344
348
207
105
(Vcs)
203
231
124
(X̄+Y)
235
339
343
347
103(-VEE2)
110
111
112
113
(-VEE)

FIG.9

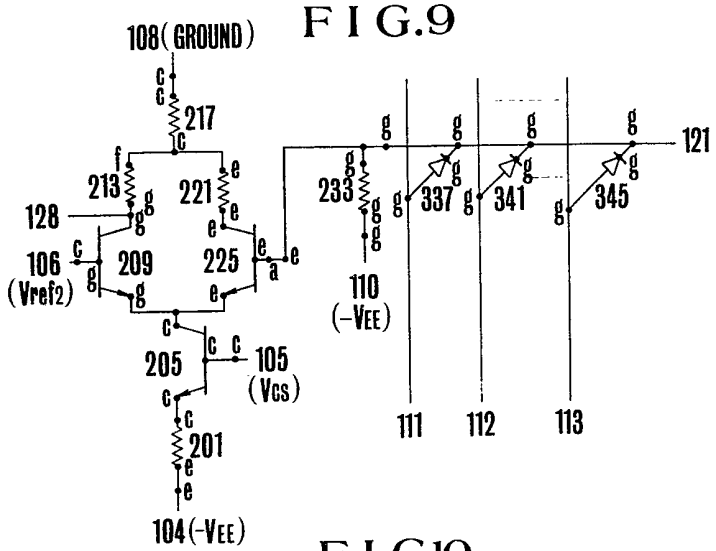
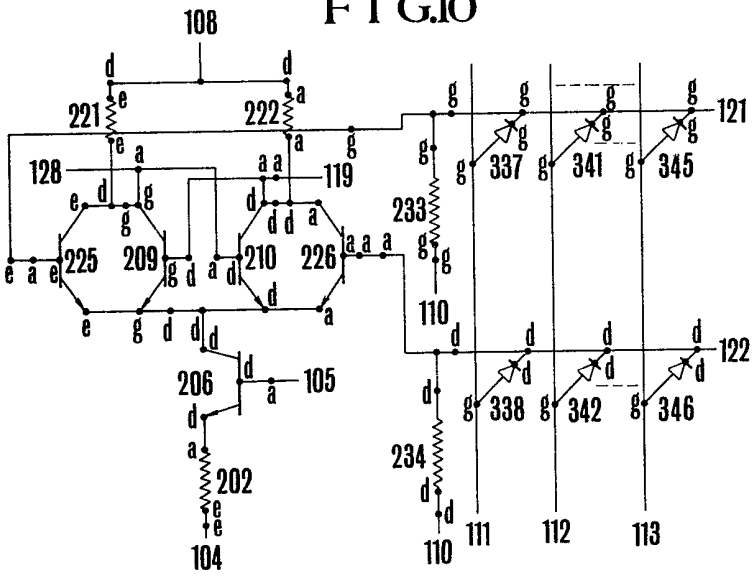

108(GROUND)
217
213
221
128
106
(Vref2)
209
225
205
105
(Vcs)
201
104(-VEE)
233
110
(-VEE)
337
341
345
121
111
112
113

FIG.10


108
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226
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342
346
122
234
111
112
113

FIG.11A

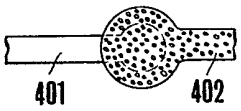


FIG.12A

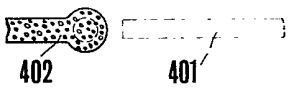


FIG.11B

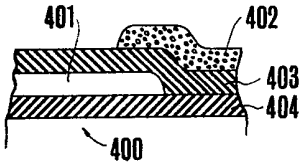


FIG.12B

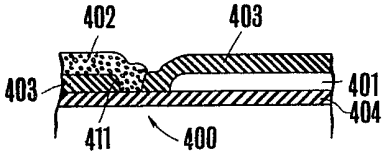


FIG.11C

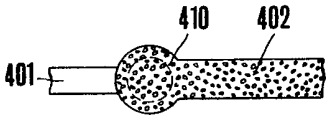


FIG.12C

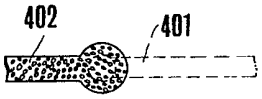


FIG.11D

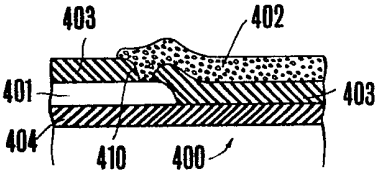


FIG.12D

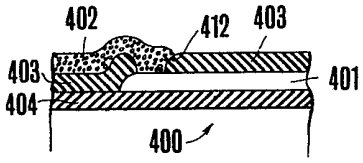


FIG.13A

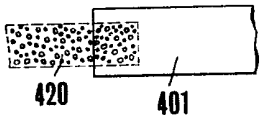


FIG.13B

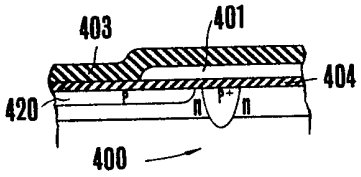


FIG.13C

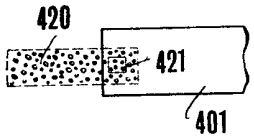


FIG.13D

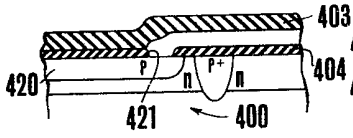


FIG.14A

FIG.14B

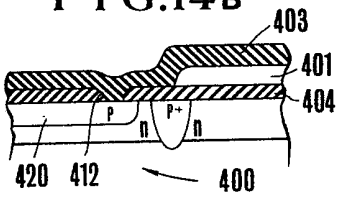


FIG.14C

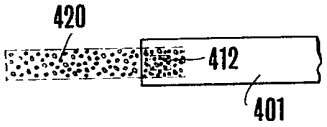


FIG.14D

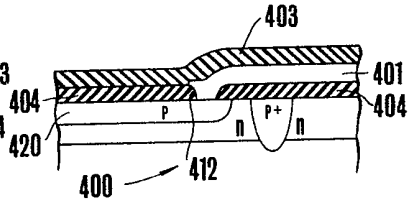


FIG.15A 

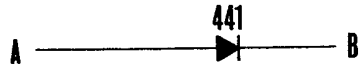
FIG.15B 

FIG.15c 

FIG.16 

FIG.17A

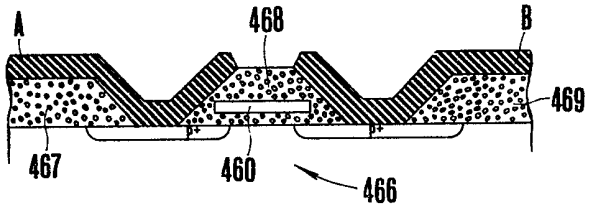


FIG.17B