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(54) Title: PHOTOCONDUCTIVE SEMICONDUCTOR SWITCH LATERALLY FABRICATED ALONGSIDE GaN ON Si FIELD-EFFECT TRANSISTORS

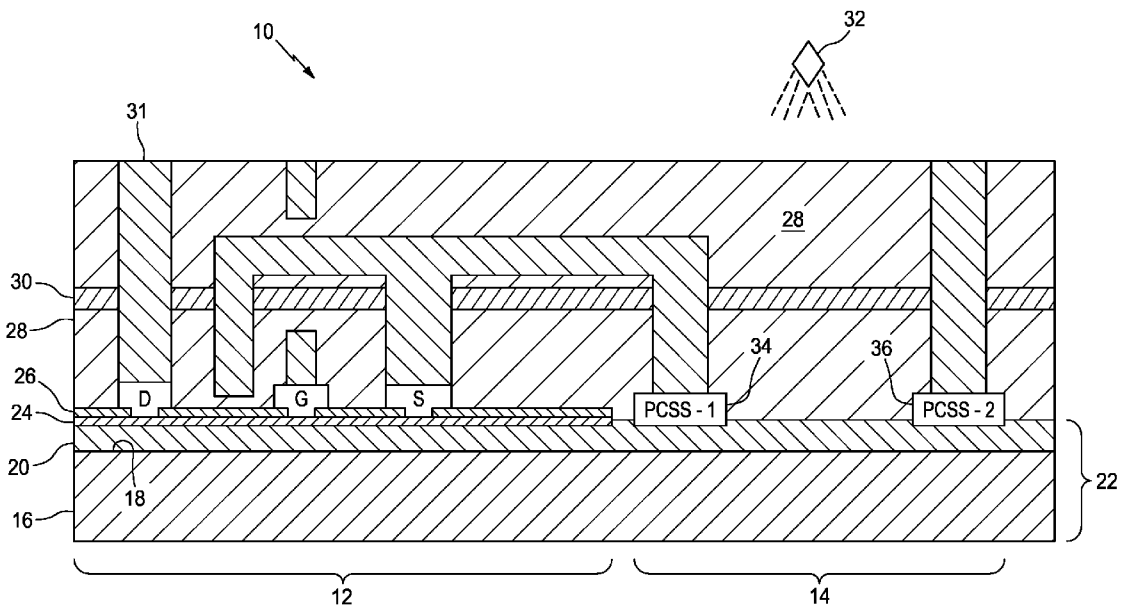


FIG. 1

(57) Abstract: An integrated circuit structure comprising a substrate having an upper surface; a gallium nitride layer disposed on the upper surface of the substrate; and a photoconductive semiconductor switch laterally disposed alongside a transistor on the gallium nitride layer integrated into the integrated circuit structure wherein a regrown gallium nitride material is disposed on the photoconductive semiconductor switch and operatively coupled with the wafer.



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PHOTOCONDUCTIVE SEMICONDUCTOR SWITCH LATERALLY FABRICATED  
ALONGSIDE GaN ON Si FIELD-EFFECT TRANSISTORS

BACKGROUND

[0001] The present disclosure is directed to the improved gallium nitride (GaN) integrated circuit technology, particularly, a structure that includes both GaN photoconductive semiconductor switch (PCSS) and/or photoconductively switched transistor and GaN transistors and accompanying integrated circuit structures.

[0002] Currently on-chip GaN on Si High Electron Mobility Transistor (HEMT) switches and RF devices are controlled through electrical signals and are limited by the constraints of traditional semiconductor device design, and fabrication. For example, switching speed is limited to device geometry, and the on-off current ratio. Another example includes the breakdown voltage of the device, which is the maximum voltage the device can handle before catastrophic device failure. This voltage is determined by the breakdown of the HEMT semiconductor material and/or dielectric when electric field peak at the drain side, which is a function of the applied drain bias and gate to drain distance, exceed the breakdown fields of the materials. The maximum operating voltage of current state of the art GaN HEMT switches, operating in a safe operating region below the breakdown voltage, is approximately 650 V. Photoconductive Semiconductor Switches (PCSS) and photoconductively switched transistors are different devices that offer high voltage switching capabilities, ultra-fast switching speeds, or rapid energy pulses that are switched by light instead of by biases applied by metal gates. As such, they offer the potential for increased

operating voltages relative to traditional GaN HEMT switches and RF devices.

[0003] Further, existing GaN PCSS structures are stand-alone devices, fabricated through nonplanar liftoff based processing, that are connected with transistors, integrated circuits (ICs), and light sources (e.g. lasers and light emitting diodes), as part of a larger module, either through wire bonding or circuit board design.

[0004] What is needed for maximum performance and functional density is compact integration photoconductive semiconductor switches and photoconductively switched transistors.

#### SUMMARY

[0005] In accordance with the present disclosure, there is provided an integrated circuit structure comprising a substrate having an upper surface; a gallium nitride layer disposed on the upper surface of the substrate, wherein the substrate and the gallium nitride layer comprise a wafer; and a photoconductive semiconductor switch laterally disposed alongside a transistor on the gallium nitride layer integrated into the integrated circuit structure; wherein a regrown gallium nitride material is disposed on the photoconductive semiconductor switch and operatively coupled with the wafer.

[0006] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the substrate comprises at least one of a silicon material and a silicon carbide material.

[0007] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the transistor comprises a field-effect transistor.

[0008] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch comprises a first electrical contact and a second electrical contact disposed on the GaN layer.

[0009] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch comprises an aluminum gallium nitride layer disposed on a gallium nitride on silicon wafer; the first electrical contact and second electrical contact are laterally arranged off-mesa on the gallium nitride layer of the wafer, wherein the regrown gallium nitride material is deposited over each of the first electrical contact and the second electrical contact and disposed on the gallium nitride between the first electrical contact and the second electrical contact.

[0010] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include at least one of the regrown gallium nitride material and the gallium nitride layer forms a photoconductive circuit.

[0011] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch comprises an aluminum gallium nitride layer disposed on a gallium nitride on silicon wafer; the first electrical contact and the second electrical contact are on-mesa being disposed on the aluminum gallium nitride layer, wherein an AlGa<sub>N</sub>-Ga<sub>N</sub> two dimensional electron gas interface is present; a window etched into the AlGa<sub>N</sub> layer; and the regrown Ga<sub>N</sub> layer deposited in the window.

[0012] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include

the regrown GaN layer is disposed on the exposed gallium nitride layer in the window.

[0013] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the integrated circuit structure further comprising a transparent silicon dioxide dielectric insulation layer configured to insulate each of the first electrical contact and the second electrical contact of the photoconductive semiconductor switch and the transistor.

[0014] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the integrated circuit structure further comprising a light source optically coupled to the photoconductive semiconductor switch.

[0015] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch and the transistor are each configured to be utilized separately or interdependently.

[0016] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch is homogeneously integrated with the transistor on a gallium nitride on silicon wafer and configured to control the transistor.

[0017] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include the photoconductive semiconductor switch is homogeneously integrated with the transistor in a gallium nitride on silicon wafer and configured to be controlled by the transistor.

[0018] A further embodiment of any of the foregoing embodiments may additionally and/or alternatively include a

dielectric and an interlayer are transparent to a light source utilized to trigger the photoconductive semiconductor switch.

[0019] Other details of the GaN on Si heterogeneous technology are set forth in the following detailed description and the accompanying drawings wherein like reference numerals depict like elements.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Fig. 1 is a cross-sectional schematic diagram of an exemplary laterally integrated circuit structure.

[0021] Fig. 2 is a cross-sectional schematic diagram of an exemplary GaN PCSS.

[0022] Fig. 3 is a cross-sectional schematic diagram of an exemplary GaN PCSS.

#### DETAILED DESCRIPTION

[0023] Referring Fig. 1, there is illustrated a laterally integrated circuit structure 10. The laterally integrated circuit structure 10 includes a transistor 12 electrically coupled with a PCSS 14 each laterally integrated and supported on a common substrate 16. The transistor 12 can be a FET, for example, GaN transistors, Si transistors and accompanying integrated circuit structures. The PCSS 14 can include a GaN PCSS. The substrate 16 can include a silicon (Si) or silicon carbide (SiC) material. The substrate 16 includes an upper surface 18.

[0024] A gallium nitride (GaN) layer is disposed on the upper surface 18 of the substrate 16 to form a GaN on Si wafer 22. The GaN layer 20 supports the transistor 12 and the PCSS 14 in tandem such that the transistor 12 and PCSS 14 are laterally integrated and incorporated in the same integrated circuit.

[0025] The FET 12 includes an aluminum gallium nitride (AlGaN) layer 24 disposed on the GaN layer 20. The FET 12 includes silicon nitride dielectric (SiN/dielectric) layer 26 disposed on the AlGaN layer 24 proximate each of the drain D, gate G and source S of the FET 12. A silicon dioxide dielectric (SiO<sub>2</sub>/dielectric) layer 28 insulates the transistor 12 circuitry as well as an interlayer 30, here for example SiNx, and conductive interconnects 31 disposed within the silicon dioxide dielectric layer 28. The dielectrics 28, 26 and interlayer 30 can be transparent to a light source 32 utilized to trigger the PCSS 14 conduction path. In an exemplary embodiment, in the event of the dielectric or interlayer not being transparent, a window can be opened in the films to allow for light transmission.

[0026] The PCSS 14 can include a first electrical contact 34 (PCSS-1) and a second electrical contact 36 (PCSS-2) disposed on the GaN layer. In an exemplary embodiment, the silicon dioxide dielectric layer 28 insulates each of the first electrical contact 34 and second electrical contact 36 of the photoconductive semiconductor switch 14. In exemplary embodiments, the dielectric layer 28 can be silicon nitride, or silicon dioxide material, and the like. In other exemplary embodiments, the first electrical contact 34 and second electrical contact 36 do not have dielectric insulation. A photoconductive semiconductor switch 14 is a region of semiconductor material (such as GaN) that is normally very highly resistive, here for example unintentionally doped or doped with a deep level such as carbon or iron. This allows the material to block a substantial amount of voltage with very low leakage. However, when illuminated with a light

source 32 that has an energy above or near the band gap energy, a plethora of excited carriers are generated. These excited carriers now form a low-resistance conduction path used for switching. The PCSS 14 offers high voltage switching capabilities, ultra-fast switching speeds, or rapid energy pulses. An input voltage to the transistor 12 can be controlled by the on-off state of the PCSS 14 or the other way around.

[0027] Referring also to Fig. 2, Fig. 3, the GaN PCSS 14 can be fabricated in a variety of ways on the wafer 22.

[0028] As shown in Fig. 2, in an exemplary embodiment, the PCSS 14 can include the substrate 16 with the GaN layer 20 disposed on the substrate 16 that comprises the wafer 22. The first electrical contact 34 and second electrical contact 36 are laterally arranged off-mesa on the GaN layer 20 of the wafer 22. A regrown GaN material 40 is deposited over each of the first electrical contact 34 and the second electrical contact 36 and over the gallium nitride layer 20 between the first electrical contact 34 and second electrical contact 36, such that either the regrown GaN 40 and/or the GaN layer 20 forms a photoconductive circuit 42.

[0029] As shown in Fig. 3, in an exemplary embodiment, the PCSS 14 can include the substrate 16 with the GaN layer 20 disposed on the substrate 16 that comprises the wafer 22. The first electrical contact 34 and the second electrical contact 36 are on-mesa, being disposed on the AlGaN layer 24, such that the AlGaN-GaN two dimensional interface (2DEG interface) is present. The AlGaN layer 24 can be etched to form a GaN window 38 in the 2DEG layer 24. Regrown GaN 40 can be deposited in the window 38 instead of a gate metal (not shown). The regrown GaN 40 is formed on

the exposed GaN layer 20 in the window 38 etched out of the AlGaN layer 24.

[0030] The disclosure provides for photoconductive semiconductor switches and photoconductively switched transistors integrated monolithically or through wafer to wafer bonding or die stacking with transistors and light sources. To accomplish this, subtractive planar processing techniques are needed.

[0031] A technical advantage of the disclosure includes integration of optically gated switches directly with the GaN on Si process flow to enable intrinsic high voltage capabilities and rapid response times of optically gated switches.

[0032] Another technical advantage of the disclosure includes a structure that includes a single chip/wafer that contains both GaN on Si transistor devices and GaN PCSS devices wherein the final device has the functions of GaN transistors, Si transistors, and GaN PCSS, utilized separately or interpedently.

[0033] Another technical advantage of the disclosure includes a PCSS device that controls, or is controlled by, a GaN plus Si device homogenously integrated in the same wafer.

[0034] Another technical advantage of the disclosure includes a structure that has multiple options for photoconductive materials, such as, an AlGaN/GaN based substrate with regrown AlGaN/GaN either independent or combined; or an AlGaN/GaN 2DEG connected by a narrow region of photosensitive AlGaN/GaN material.

[0035] Another technical advantage of the disclosure includes the regrown AlGaN/GaN which can be configured and tuned independently from the epitaxial GaN in the

substrate. Configuring and tuning parameters can include geometry/thickness, doping, and concentration/stoichiometry.

[0036] Another technical advantage of the disclosure includes methods of fabricating the GaN PCSS can be layer-subtraction based, utilizing techniques traditional to Si foundries.

[0037] Another technical advantage of the disclosure includes both GaN PCSS and GaN/Si transistors are fabricated at the same time using the same processing steps.

[0038] Another technical advantage of the disclosure includes adding PCSS to a GaN on a Si device which is a nontrivial addition, as it utilizes layers and structure that would not be used in a standalone GaN on Si or standalone PCSS device.

[0039] Another technical advantage of the disclosure includes the 2DEG layer must be completely recessed through, unlike in GaN on Si devices.

[0040] Another technical advantage of the disclosure includes the substrate of an AlGaIn/GaN high electron mobility transistor (HEMPT) epi being used, as opposed to a bulk substrate optimized for photosensitivity, unlike typical PCSS devices.

[0041] There has been provided a GaN on Si heterogeneous technology. While the GaN on Si heterogeneous technology has been described in the context of specific embodiments thereof, other unforeseen alternatives, modifications, and variations may become apparent to those skilled in the art having read the foregoing description. Accordingly, it is intended to embrace those alternatives, modifications, and

variations which fall within the broad scope of the appended claims.

WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:
  - a substrate having an upper surface;
  - a gallium nitride layer disposed on said upper surface of the substrate, wherein said substrate and said gallium nitride layer comprise a wafer; and
  - a photoconductive semiconductor switch laterally disposed alongside a transistor on said gallium nitride layer integrated into the integrated circuit structure; wherein a regrown gallium nitride material is disposed on said photoconductive semiconductor switch and operatively coupled with said wafer.
2. The integrated circuit structure according to claim 1, wherein said substrate comprises at least one of a silicon material and a silicon carbide material.
3. The integrated circuit structure according to claim 1, wherein said transistor comprises a field-effect transistor.
4. The integrated circuit structure according to claim 1, wherein said photoconductive semiconductor switch comprises a first electrical contact and a second electrical contact disposed on the GaN layer.
5. The integrated circuit structure according to claim 4, wherein said photoconductive semiconductor switch comprises an aluminum gallium nitride layer disposed on a gallium nitride on silicon wafer; the first electrical contact and

second electrical contact are laterally arranged off-mesa on the gallium nitride layer of the wafer, wherein the regrown gallium nitride material is deposited over each of the first electrical contact and the second electrical contact and disposed on the gallium nitride between the first electrical contact and the second electrical contact.

6. The integrated circuit structure according to claim 5, wherein at least one of the regrown gallium nitride material and the gallium nitride layer forms a photoconductive circuit.

7. The integrated circuit structure according to claim 4, wherein said photoconductive semiconductor switch comprises an aluminum gallium nitride layer disposed on a gallium nitride on silicon wafer; the first electrical contact and the second electrical contact are on-mesa being disposed on the aluminum gallium nitride layer, wherein an AlGaN-GaN two dimensional electron gas interface is present; a window etched into the AlGaN layer; and the regrown GaN layer deposited in the window.

8. The integrated circuit structure according to claim 7, wherein said regrown GaN layer is disposed on the exposed gallium nitride layer in the window.

9. The integrated circuit structure according to claim 1 further comprising:

a transparent silicon dioxide dielectric insulation layer configured to insulate each of the first electrical contact and the second electrical contact of the photoconductive semiconductor switch and the transistor.

10. The integrated circuit structure according to claim 1 further comprising:

a light source optically coupled to said photoconductive semiconductor switch.

11. The integrated circuit structure according to claim 1, wherein said photoconductive semiconductor switch and said transistor are each configured to be utilized separately or interdependently.

12. The integrated circuit structure according to claim 1, wherein said photoconductive semiconductor switch is homogeneously integrated with said transistor on a gallium nitride on silicon wafer and configured to control said transistor.

13. The integrated circuit structure according to claim 1, wherein said photoconductive semiconductor switch is homogeneously integrated with said transistor in a gallium nitride on silicon wafer and configured to be controlled by said transistor.

14. The integrated circuit structure according to claim 1, wherein a dielectric and an interlayer are transparent to a light source utilized to trigger the photoconductive semiconductor switch.



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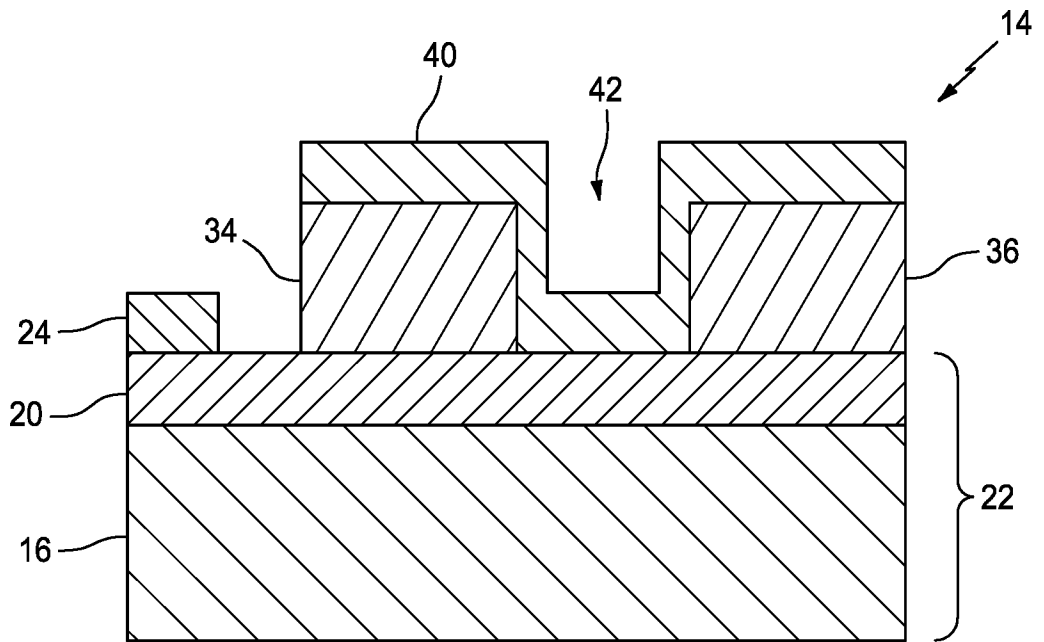


FIG. 2

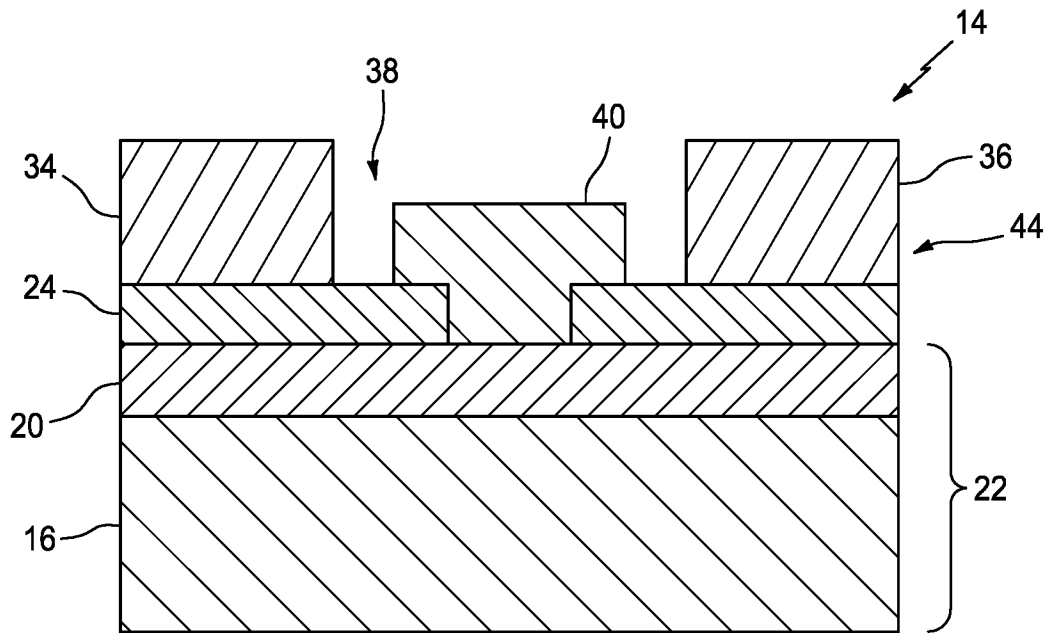


FIG. 3

**INTERNATIONAL SEARCH REPORT**

International application No  
**PCT/US2022/022523**

**A. CLASSIFICATION OF SUBJECT MATTER**  
**INV. H01L31/09 H01L31/0304 H01L27/144 H01L27/146**  
**ADD.**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**  
 Minimum documentation searched (classification system followed by classification symbols)  
**H01L**

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
**EPO-Internal, WPI Data**

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
<b>X</b>	<b>US 2010/019279 A1 (CHEN JING [CN] ET AL)</b> <b>28 January 2010 (2010-01-28)</b> <b>the whole document</b>	<b>1-14</b>
<b>X</b>	<b>"Ultrafast characterization of an in-plane gate transistor integrated with photoconductive switches", APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS, 2 HUNTINGTON QUADRANGLE, MELVILLE, NY 11747, vol. 66, no. 10, 6 March 1995 (1995-03-06), pages 1228-1230, XP012012312, ISSN: 0003-6951, DOI: 10.1063/1.113245</b> <b>the whole document</b>	<b>1-14</b>
<b>X</b>	<b>EP 0 235 029 A1 (THOMSON CSF [FR])</b> <b>2 September 1987 (1987-09-02)</b> <b>the whole document</b>	<b>1-14</b>

Further documents are listed in the continuation of Box C.       See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search <b>15 June 2022</b>	Date of mailing of the international search report <b>24/06/2022</b>
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  <b>Voignier, Vincent</b>
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## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2022/022523

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>KOEHLER ANDREW D. ET AL: "High Voltage GaN Lateral Photoconductive Semiconductor Switches",  ECS JOURNAL OF SOLID STATE SCIENCE AND TECHNOLOGY,  vol. 6, no. 11,  1 January 2017 (2017-01-01), pages  S3099-S3102, XP055930756,  US  ISSN: 2162-8769, DOI: 10.1149/2.0231711jss  Retrieved from the Internet:  URL:https://iopscience.iop.org/article/10.1149/2.0231711jss/pdf&gt;  the whole document</p> <p>-----</p>	1-14
A	<p>US 2009/072240 A1 (SUH CHANG SOO [US] ET AL) 19 March 2009 (2009-03-19)  the whole document</p> <p>-----</p>	1-14
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A	<p>SAMIZADEH NIKOO MOHAMMAD ET AL: "On the Dynamic Performance of Laterally Gated Transistors",  IEEE ELECTRON DEVICE LETTERS, IEEE, USA,  vol. 40, no. 7, 1 July 2019 (2019-07-01),  pages 1171-1174, XP011732080,  ISSN: 0741-3106, DOI:  10.1109/LED.2019.2920116  [retrieved on 2019-06-25]  the whole document</p> <p>-----</p>	1-14

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No

**PCT/US2022/022523**

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