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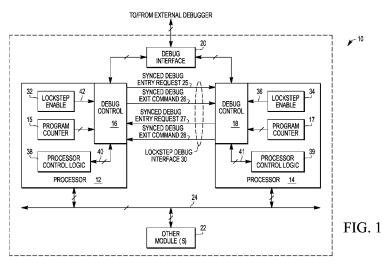
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(54) Title: DEBUG SIGNALING IN A MULTIPLE PROCESSOR DATA PROCESSING SYSTEM



(57) Abstract: A system includes a first processor (12), a second processor (14), a first clock (54) coupled to the first processor, and a third clock (56) coupled to the first processor and to the second processor. The first processor includes debug circuitry (58) coupled to receive the third clock, synchronization circuitry (48, 43) coupled to receive the first clock, wherein the synchronization circuitry receives a first request to enter a debug mode and provides a first synced debug entry request signal (51 or 25) and wherein the first synced debug entry request signal is synchronized with respect to the first clock, and an input for receiving a second synced debug entry request signal (27) from the second processor wherein the first processor waits to enter the debug mode until the first synced debug entry request signal and the second synced debug entry request signal are both asserted.



#### INTERNATIONAL SEARCH REPORT

International application No. **PCT/US2010/028300** 

#### A. CLASSIFICATION OF SUBJECT MATTER

G06F 9/46(2006.01)i, G06F 9/06(2006.01)i, G06F 15/163(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

#### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols) G06F 9/46; G06F 15/16; G06F 1100; G06F 11/34; G06F 15/20; G06F 1/12; G06F 11/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: multiprocessor, debug, synchronization,

#### C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Internet data, eXpressDSP Software and Development Tools (-) http://focus.ti .com/lit/ml/sprue40/sprue40.pdf(2004) See page 5.	1-20
Α	US 2007-0130492 A1 (JAMKHANDI, P.) 07 June 2007 See abstract, paragraph [0008], figure 1, and claim 1.	1-20
Α	US 5452437 A1 (RICHEY, J.M. et al.) 19 September 1995 See column 14 line 11 - line 64, and figure 9.	1-20
A	US 6826717 B1 (DRAPER, A. et al.) 30 November 2004 See abstract.	1-20
A	US 6145100 A1 (MADDURI, V.R.) 07 November 2000 See abstract and fig 1.	1-20

		Further	documents	are li	isted i	in the	continuation	ı of Box	С.
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See patent family annex.

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Date of the actual completion of the international search

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Information on patent family members

Information on	PCT/US2010/028300		
Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0130492 A1	07.06.2007	None	
JS 5452437 A1	19.09.1995	None	
JS 6826717 B1	30.11.2004	None	
JS 6145100 A1	07.11.2000	None	