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(54) Title: COMPRESSIVE INTERLAYER HAVING A DEFINED CRACK-STOP EDGE EXTENSION

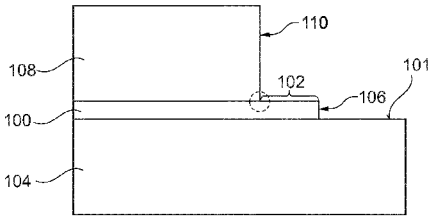

Fig. 1

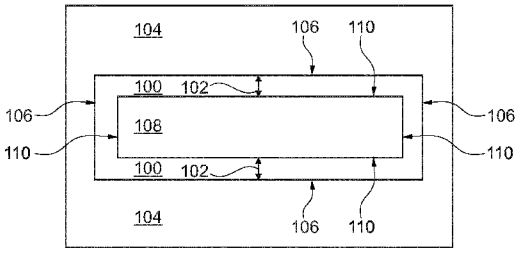

Fig. 2

(57) Abstract: A semiconductor device includes a substrate, a structured interlayer on the substrate and having defined edges, and a structured metallization on the structured interlayer and also having defined edges. Each defined edge of the structured interlayer neighbors one of the defined edges of the structured metallization and runs in the same direction as the neighboring defined edge of the structured metallization. Each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns so that each defined edge of the structured metallization terminates before reaching the neighboring defined edge of the structured interlayer. The structured interlayer has a compressive residual stress at room temperature.

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COMPRESSIVE INTERLAYER HAVING A DEFINED CRACK-STOP EDGE EXTENSION

[0001] The present application relates to semiconductor devices, in particular preventing crack propagation from metallization edges of a semiconductor device.

[0002] When thick (e.g. >5 µm) and stiff (high E-modulus / high yield stress) metallization stacks such as thick Cu, Al and Au power metals are introduced into a semiconductor device e.g. to enable particular interconnect solutions or improve thermal performance, high stresses occur near any film-terminating free-edge of the metal layer as a result of any sufficiently large temperature change. Such stresses occur due to the mismatch in the coefficients of thermal expansion (CTE) between the metal film and the underlying substrate (e.g. semiconductor materials or interlevel dielectrics). Temperature changes can occur during device processing (e.g. during cool-down to room temperature after an annealing step) or during use of the final device (e.g. power dissipation during switching operation under overload conditions). Free edges are created by the requirement of a patterned power metallization having defined lines and plates of limited size.

[0003] Whenever tensile stresses occur below the metal edge and hence in the substrate (e.g. SiO2- or Si3N4-based interlevel dielectrics, or the semiconductor substrate itself), cracks can result in the underlying brittle layers. This is in general the case during cool-down phases, e.g. from annealing at typically 400°C down to room-temperature, if the CTE of the film is larger than that of the substrate, which is practically always the case.

[0004] To avoid cracks during production, either the temperature budget is reduced after deposition of the metal (e.g., to 300°C anneal), or metals with reduced stiffness are utilized (e.g. aluminum with lower yield stress instead of harder copper). Both measures severely limit the technology, and may result in adverse side effects. Hence, improved crack-stop measures are desired.

[0005] According to an embodiment of a semiconductor device, the semiconductor device comprises a substrate, a structured interlayer on the substrate and a structured metallization on the structured interlayer. The structured interlayer has defined edges, as does the structured metallization. Each defined edge of the structured interlayer neighbors one of the defined edges of the structured metallization and runs in the same direction as the neighboring defined edge of the structured metallization. Each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns so that each defined edge of the structured metallization terminates before reaching the neighboring defined edge of the structured interlayer. The structured interlayer has a compressive residual stress at room temperature.

[0006] According to an embodiment of a method of manufacturing a semiconductor device, the method comprises: forming a structured interlayer on a substrate, the structured interlayer having defined edges; and forming a structured metallization on the structured interlayer, the structured metallization having defined edges, wherein the structured interlayer is formed so that each defined edge of the structured interlayer neighbors one of the defined edges of the structured metallization and runs in the same direction as the neighboring defined edge of the structured metallization, wherein the

structured interlayer is formed so that each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns and each defined edge of the structured metallization terminates before reaching the neighboring defined edge of the structured interlayer, and wherein the structured interlayer has a compressive residual stress at room temperature.

[0007] Those skilled in the art will recognize additional features and advantages upon reading the following detailed description, and upon viewing the accompanying drawings.

[0008] The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts. The features of the various illustrated embodiments can be combined unless they exclude each other. Embodiments are depicted in the drawings and are detailed in the description which follows.

[0009] Figure 1 illustrates a partial sectional view of an embodiment of a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0010] Figure 2 shows a corresponding top-down plan view of the part of the semiconductor device shown in Figure 1.

[0011] Figure 3 illustrates a partial sectional view of another embodiment of a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0012] Figure 4 illustrates a partial sectional view of yet another embodiment of a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0013] Figures 5A through 5D illustrate an embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0014] Figures 6A through 6E illustrate another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0015] Figures 7A through 7E illustrate yet another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0016] Figures 8A through 8E illustrate still another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension.

[0017] The embodiments described herein provide a structured, compressive interlayer having a defined crack-stop edge extension. The structured interlayer reduces crack probability without necessitating a change in temperature profile of the device manufacturing process, the properties of the overlying metallization, or the topology of the underlying substrate. This is achieved by placing a robust, high-fracture strength structured interlayer of suitable thickness and compressive residual stress at room

temperature between the overlying metal and the underlying brittle layers. The structured interlayer extends by a defined amount, also referred to herein as overlap, beyond the defined edges of the overlying metal. The structured interlayer spreads the tensile stress emanating from the defined edges of the metallization, thereby reducing the peak stress in the underlying substrate. The compressive residual stress of the structured interlayer counteracts the tensile stress caused by cool-down, and thus acts against cracking (the fracture strength of brittle materials being generally much larger under compression than under tension). The structured interlayer effectively decouples the metallization edge from the substrate and the substrate topology by a fixed extension (overlap). Hence, a crack-critical topology (e.g. a substrate surface with grooves) is either covered and hence protected by the stress-distributing layer, or when not covered, is provided with a safe overlap distance from the free metal edge.

[0018] Figure 1 illustrates a partial sectional view of a semiconductor device having a structured, compressive interlayer 100 with a defined crack-stop edge extension 102.

[0019] Figure 2 shows a corresponding top-down plan view of the part of the semiconductor device shown in Figure 1.

[0020] The structured interlayer 100 is formed on a substrate 104, and has defined edges 106. In one embodiment, the underlying substrate 104 is a semiconductor substrate such as Si, GaN on Si, GaN on SiC, GaN on sapphire, SiC, etc. In another embodiment, the underlying substrate 104 is an interlevel dielectric such as an SiO_2-based interlevel dielectric, an Si_3N_4-based interlevel dielectric, etc. In either case, the semiconductor device also has a structured metallization 108 on the structured interlayer

100. The metallization 108 can be structured (patterned) as desired, and has defined edges 110. The structured metallization 108 together with the structured interlayer 100 can be applied over the front or back side of the substrate 104. The structured metallization 108 can comprise a single layer or multiple (more than one) layers of metal. In some cases, the structured metallization 108 is a thick (e.g. >5 μm) and stiff (high E-modulus / high yield stress) metallization such as thick Cu, Al or Au power metal for a power semiconductor device. However, the structured metallization 108 need not be a power metallization layer of a power semiconductor device, but may instead be thinner e.g. in the case of advanced CMOS designs.

[0021] Various metallization / interlayer combinations are contemplated. For example, the structured metallization 108 can comprise Cu and the structured interlayer 100 can comprise at least one of Ti, TiW, W and Ta. In another embodiment, the structured metallization 108 comprises Al or an Al alloy and the structured interlayer 100 comprises at least one of Ti, TiN and W. In yet another embodiment, the structured metallization 108 comprises Au and the structured interlayer 100 comprises any suitable barrier layer and/or adhesion promotion layer compatible with Au. A common barrier layer for at least Cu and Al metal systems is TiW, which can be compressive or tensile depending on the choice of deposition parameters. Hence, if the structured interlayer 100 comprises a single layer of TiW, the TiW layer should be deposited so as to have a compressive residual stress at room temperature. Still other metallization / interlayer combinations are possible.

[0022] In each case, the structured interlayer 100 has an overall compressive residual stress at room temperature. For example, the structured interlayer 100 can comprise a single layer having a compressive residual stress at room temperature. In another

embodiment, the structured interlayer 100 can comprise a combination of tensile and compressive layers but in total has an overall compressive residual stress at room temperature. For example, at least one layer can have a compressive residual stress at room temperature and at least one other layer can have a tensile residual stress at room temperature. However, the overall residual stress of such a composite structured interlayer 100 is still compressive at room temperature despite the presence of one or more tensile layers.

[0023] Regardless of the metallization / interlayer combination and type of semiconductor device (power device, logic device, etc.), each defined edge 106 of the structured interlayer 100 neighbors one of the defined edges 110 of the structured metallization 108 and runs in the same direction as the neighboring defined edge 110 of the structured metallization 108. Each defined edge 106 of the structured interlayer 100 extends beyond the neighboring defined edge 110 of the structured metallization 108 by at least 0.5 microns, so that each defined edge 110 of the structured metallization 108 terminates before reaching the neighboring defined edge 106 of the structured interlayer 100. Hence, the structured interlayer 100 looks like a flange in the top plan view of Figure 2 in that the structured interlayer 100 projects further outward laterally than the structured metallization 108 and each defined edge 110 of the structured metallization 108 terminates before reaching the neighboring edge 106 of the structured interlayer 100.

[0024] The amount by which each defined edge 106 of the structured interlayer 100 extends beyond the neighboring defined edge 110 of the structured metallization 108 is a function of the thickness and yield stress of the structured metallization 108. In one embodiment, each defined edge 106 of the structured interlayer 100 extends beyond the

neighboring defined edge 110 of the structured metallization 108 by more than 0.5 microns and less than 15 microns. For example, each defined edge 106 of the structured interlayer 100 can extend beyond the neighboring defined edge 110 of the structured metallization 108 by at least 1 micron. In the case of a planar substrate surface 101 on which the structured interlayer 100 is formed, each defined edge 106 of the structured interlayer 100 can extend beyond the neighboring defined edge 110 of the structured metallization 108 by at least 0.5 microns and less than 5 microns, or by at least 0.5 microns and less than 10 microns, etc. In the case of a nonplanar substrate surface 101 on which the structured interlayer 100 is formed, each defined edge 106 of the structured interlayer 100 can extend beyond the neighboring defined edge 110 of the structured metallization 108 by at least 2 microns and less than 15 microns, or by at least 2 microns and less than 30 microns, etc. For example, each defined edge 106 of the structured interlayer 100 can extend beyond the neighboring defined edge 110 of the structured metallization 108 by at least 4 microns and less than 15 microns. Even larger extensions for planar and non-planar substrate surfaces are contemplated.

[0025] The length of the defined crack-stop edge extension 102 of the structured interlayer 100 can differ depending on whether the structured interlayer 100 in combination with the structure metallization 108 are applied to the front or back side of the substrate 108. Figures 3 and 4 described later herein show the structured interlayer 100 in combination with the structure metallization 108 applied to the front side of the substrate 108. In the case of being applied to the back side of the substrate 104, the structured metallization 108 may comprise metal plates such as copper plates on the substrate back side. Alignment precision for such metal plates is poor, since the back-side lithography is commonly aligned to front-side structures, resulting in large tolerance e.g. in the range of

10 microns to 30 microns. Each defined edge 106 of the structured interlayer 100 can extend by a sufficiently large amount beyond the edges 110 of the structured metallization 108 on the substrate back side to mitigate cracking. For example, each defined edge 106 of the structured interlayer 100 can extend by 2 microns to 15 microns, 10 microns to 100 microns, or up to 10% of the lateral dimension of the structured metallization 108 in the direction perpendicular to the defined edges 110 of the structured metallization 108, etc. In the case of relatively large metal plates e.g. typically 500x1000um^2 metal plates, the structured interlayer 100 could overlap by about 50 microns to 100 microns.

[0026] The structured metallization 108 and the structured interlayer 100 are illustrated with simple rectangular shapes for ease of illustration in the top-down plan view of Figure 2. In general, the structured metallization 108 and the structured interlayer 100 may have any shape such as, but not limited to, square, rectangular, linear, rectilinear, curved, meandering, etc. Also in Figure 2, the defined crack-stop edge extension 102 of the structured interlayer 100 need not be equal size along all defined edges 110 of the structured metallization 108, thus allowing for area optimization (less extension) at less critical locations and maximum crack-risk prevention (more extension) at more critical locations. For example, the defined crack-stop edge extension 102 of the structured interlayer 100 may be smaller (less overlap) along edges 110 of the structured metallization 108 less likely to cause cracking and larger (more overlap) along edges 110 of the structured metallization 108 more likely to cause cracking. The size of the defined crack-stop edge extension 102 along the defined edges 110 of the structured metallization 108 can also depend on the topology of the substrate 104. For example, the defined crack-stop edge extension 102 of the structured interlayer 100 may be smaller (less

overlap) over planar portions of the substrate surface and larger (more overlap) over non-planar portions of the surface.

[0027] Because of the compressive nature of the structured interlayer 100 and the 0.5 micron or greater lateral extension 102 beyond the defined edges 110 of the structured metallization 108, the interlayer 100 reduces crack probability in the underlying substrate 104. During cooling of the structured metallization 108, the metallization 108 becomes tensile and pulls back, imparting stress. The greatest degree of stress occurs along the edge interface with the structured interlayer 100 which is indicated by the dashed curved line in Figure 1. However, the defined crack-stop edge extension 102 of the structured interlayer 100 combined with the compressive nature of the interlayer 100 at room temperature yields a counter stress. As a result, tensile stresses underneath the metallization-interlayer terminating edge are significantly reduced. Significant stress reduction is realized for both planar and non-planar substrate surfaces.

[0028] Figure 3 illustrates a partial sectional view of another semiconductor device having a structured, compressive interlayer 200 with a defined crack-stop edge extension 202. According to this embodiment, the substrate 204 has a non-planar surface 205 on which the structured interlayer 200 is formed and some of the defined edges 206 of the structured metallization 208 terminate between raised features 210 of the non-planar surface 205. Each defined edge 212 of the structured interlayer 200 neighboring a defined edge 206 of the structured metallization 208 that terminates between raised features 210 of the non-planar surface 205 extends beyond that neighboring defined edge 206 of the structured metallization 208 by at least 3 microns, e.g. by at least 4 microns.

[0029] Figure 4 illustrates a partial sectional view of yet another semiconductor device having a structured, compressive interlayer 300 with a defined crack-stop edge extension 302. According to this embodiment, the substrate 304 has a non-planar surface on which the structured interlayer 300 is formed and some of the defined edges 306 of the structured metallization 308 terminate over raised features 310 of the non-planar surface instead of between the raised features 310. Each defined edge 312 of the structured interlayer 300 neighboring a defined edge 306 of the structured metallization 308 that terminates over a raised feature 310 of the non-planar surface extends beyond that neighboring defined edge 306 of the structured metallization 308 by at least 3 microns, e.g. by at least 4 microns. In some cases, each defined edge 312 of the structured interlayer 300 neighboring a defined edge 306 of the structured metallization 308 that terminates over a raised feature 310 of the non-planar surface extends beyond that raised feature 310 of the non-planar surface as indicated by reference number 314 in Figure 4.

[0030] Figures 5A through 5D illustrate an embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension. According to this embodiment, the compressive interlayer is structured by selective metal etch after metal deposition and patterning. In Figure 5A, an interlayer material system 400 is deposited on a substrate 402. The interlayer material system 400 comprises one or more material layers and has an overall compressive residual stress at room temperature. In Figure 5B, metal 404 such as Cu, Al, Au, etc. is deposited and patterned (e.g. by standard lithography) on the interlayer material system 400. In Figure 5C, the deposited and structured metal 404 is used as a mask to remove the part of the interlayer material system 400 unprotected by the deposited and structured metal 404. Any standard selective etching process can be used to remove the exposed

parts of the interlayer material system 400. In Figure 5D, the deposited and structured metal 404 is etched laterally selective to the interlayer material system 400 as indicated by the inward-facing dashed lines, so that each defined edge 406 of the interlayer material system 400 extends beyond the neighboring defined edge 408 of the deposited and structured metal 404 by at least 0.5 microns. Here, the degree of lateral etch-back of the deposited and structured metal 404 determines the length of crack-stop edge extension 410 as shown in Figure 5D. Any standard selective metallization etching process can be used to form the crack-stop edge extension 410 of the structured interlayer 402.

[0031] Figures 6A through 6E illustrate another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension. According to this embodiment, the compressive interlayer is structured by dedicated interlayer-lithography before metal deposition. In Figure 6A, an interlayer material system 500 is deposited on a substrate 502. The interlayer material system 500 comprises one or more material layers and has an overall compressive residual stress at room temperature. In Figure 6B, a mask 504 such as a photoresist mask is formed on the interlayer material system 500. In Figure 6C, the exposed part of the interlayer material system 500 is etched selective to the mask 504 to form the structured interlayer before depositing any metal of the structured metallization. The mask 504 is then removed. In Figure 6D, a second mask 506 such as a photoresist mask is formed on the structured interlayer 500. The second mask 506 covers at least a 0.5 micron periphery 508 around the perimeter of the structured interlayer 500 and has an opening 510 which exposes the structured interlayer 500 inward from the periphery 508. Here, the amount of mask coverage on the periphery 508 of the structured interlayer 500 determines the length of crack-stop edge extension as shown in Figure 6D. Metal 512 is

then deposited in the opening 510 of the second mask 506 to form the structured metallization 518. The mask 506 prevents the metal 512 from being deposited on the periphery 508 of the structured interlayer 500. Figure 6E shows the resulting device after structure metallization formation.

[0032] Figures 7A through 7E illustrate yet another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension. According to this embodiment, the compressive interlayer is structured by dedicated interlayer-lithography after metal deposition. In Figure 7A, an interlayer material system 600 is deposited on a substrate 602. The interlayer material system 600 comprises one or more material layers and has an overall compressive residual stress at room temperature. In Figure 7B, a structured metallization 604 is formed on the interlayer material system 600 e.g. by standard deposition and lithographic patterning of metal. In Figure 7C, the structured metallization 604 is covered with a mask 606 such as a photoresist mask. This interlayer-lithography is aligned to the structured metallization 604. The mask 606 is wider than the structured metallization 604, so that the mask 606 extends onto the interlayer material system 600 by at least 0.5 microns beyond the perimeter of the structured metallization 604 as indicated by reference number 608 in Figure 7C. In Figure 7D, the part of the interlayer material system 600 unprotected by the mask 606 is removed e.g. by standard selective etching. Figure 7E shows the device after interlayer material system etching. Here, the length of defined crack-stop edge extension is a function of the amount 608 by which the mask 606 extends onto the interlayer material system 600 as shown in Figures 7C and 7D.

[0033] Figures 8A through 8E illustrate still another embodiment of a method of manufacturing a semiconductor device having a structured, compressive interlayer with a defined crack-stop edge extension. According to this embodiment, the compressive interlayer comprises two layers of different materials. In Figure 8A, a first interlayer material 700 such as a barrier layer is deposited on a substrate 702 and a second interlayer material 704 such as a seed layer is formed on the first interlayer material 700 to yield a bilayer interlayer 706 having an overall compressive residual stress at room temperature. In Figure 8B, a mask 708 such as a photoresist mask is formed on the compressive bilayer interlayer 706. In Figure 8C, the exposed part of the second interlayer material 704 is etched selective to the mask 708 and the first interlayer material 700 before depositing any metal of the structured metallization. The mask 708 is then removed. In Figure 8D, a second mask 710 such as a photoresist mask is formed on the etched second interlayer material 704. The second mask 710 covers at least a 0.5 micron periphery 712 around the perimeter of the etched second interlayer material 704 and has an opening 714 which exposes the etched second interlayer material 704 inward from the periphery 712. Here, the amount of mask coverage on the periphery 712 of the etched second interlayer material 704 determines the length of crack-stop edge extension. Metal 716 is then deposited in the opening 714 of the second mask 710 to form the structured metallization. The mask 710 prevents the metal 716 from being deposited on the periphery 712 of the etched second interlayer material 704. In Figure 8E, the second mask 710 is removed and the first (bottom) interlayer material 700 is etched selective to the second (upper) interlayer material 704 and to the metal 716 to form the structured interlayer.

[0034] Terms such as “first”, “second”, and the like, are used to describe various elements, regions, sections, etc. and are also not intended to be limiting. Like terms refer to like elements throughout the description.

[0035] As used herein, the terms “having”, “containing”, “including”, “comprising” and the like are open ended terms that indicate the presence of stated elements or features, but do not preclude additional elements or features. The articles “a”, “an” and “the” are intended to include the plural as well as the singular, unless the context clearly indicates otherwise.

[0036] It is to be understood that the features of the various embodiments described herein may be combined with each other, unless specifically noted otherwise.

[0037] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

CLAIMS

1. A semiconductor device, comprising:

a substrate;

a structured interlayer on the substrate, the structured interlayer having defined edges; and

a structured metallization on the structured interlayer, the structured metallization having defined edges,

wherein each defined edge of the structured interlayer neighbors one of the defined edges of the structured metallization and runs in the same direction as the neighboring defined edge of the structured metallization,

wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns so that each defined edge of the structured metallization terminates before reaching the neighboring defined edge of the structured interlayer,

wherein the structured interlayer has a compressive residual stress at room temperature.

2. The semiconductor device of claim 1, wherein the substrate is an interlevel dielectric.

3. The semiconductor device of claim 1, wherein the substrate is a semiconductor substrate.

4. The semiconductor device of claim 3, wherein the semiconductor substrate comprises one of Si, GaN on Si, GaN on SiC, GaN on sapphire, and SiC.

5. The semiconductor device of any one of the preceding claims, wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 1 micron.

6. The semiconductor device of any one of the preceding claims, wherein the structured interlayer and the structured metallization are applied over a front side of the substrate, and wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by more than 0.5 microns and less than 30 microns.

7. The semiconductor device of any one of claims 1 to 6, wherein the substrate has a non-planar surface on which the structured interlayer is formed, and wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 2 microns and less than 30 microns.

8. The semiconductor device of claim 7, wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 4 microns and less than 15 microns.

9. The semiconductor device of any one of claims 1 to 6, wherein the substrate has a non-planar surface on which the structured interlayer is formed, wherein some of the

defined edges of the structured metallization terminate between raised features of the non-planar surface, and wherein each defined edge of the structured interlayer neighboring a defined edge of the structured metallization that terminates between raised features of the non-planar surface extends beyond that neighboring defined edge of the structured metallization by at least 3 microns.

10. The semiconductor device of claim 9, wherein each defined edge of the structured interlayer neighboring a defined edge of the structured metallization that terminates between raised features of the non-planar surface of the substrate extends beyond that neighboring defined edge of the structured metallization by at least 4 microns.

11. The semiconductor device of any one of claims 1 to 6, wherein the substrate has a non-planar surface on which the structured interlayer is formed, wherein some of the defined edges of the structured metallization terminate over raised features of the non-planar surface, and wherein each defined edge of the structured interlayer neighboring a defined edge of the structured metallization that terminates over a raised feature of the non-planar surface extends beyond that neighboring defined edge of the structured metallization by at least 3 microns.

12. The semiconductor device of claim 11, wherein each defined edge of the structured interlayer neighboring a defined edge of the structured metallization that terminates over a raised feature of the non-planar surface of the substrate extends beyond that neighboring defined edge of the structured metallization by at least 4 microns.

13. The semiconductor device of any one of claims 1 to 6, wherein the substrate has a non-planar surface on which the structured interlayer is formed, wherein some of the defined edges of the structured metallization terminate over raised features of the non-planar surface, and wherein each defined edge of the structured interlayer neighboring a defined edge of the structured metallization that terminates over a raised feature of the non-planar surface extends beyond that raised feature of the non-planar surface.

14. The semiconductor device of any one of claims 1 to 6, wherein the substrate has a planar surface on which the structured interlayer is formed, and wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns and less than 10 microns.

15. The semiconductor device of any one of the preceding claims, wherein the structured metallization comprises multiple layers of metal.

16. The semiconductor device of any one of the preceding claims, wherein the amount by which each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization is a function of the thickness and yield stress of the structured metallization.

17. The semiconductor device of any one of claims 1 to 16, wherein the structured metallization comprises Cu, and wherein the structured interlayer comprises at least one of TiW and W.

18. The semiconductor device of any one of claims 1 to 16, wherein the structured metallization comprises Al, and wherein the structured interlayer comprises at least one of TiN and W.

19. The semiconductor device of any one of claims 1 to 16, wherein the structured metallization comprises Au.

20. The semiconductor device of any one of the preceding claims, wherein the structured interlayer comprises a plurality of layers, wherein at least one of the layers has a compressive residual stress at room temperature, wherein at least one of the layers has a tensile residual stress at room temperature, and wherein the structured interlayer has an overall compressive residual stress at room temperature.

21. The semiconductor device of any one of the preceding claims, wherein the structured interlayer and the structured metallization are applied over a back side of the substrate, and wherein each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by between 2 microns and 100 microns, or up to 10% of a lateral dimension of the structured metallization in a direction perpendicular to the defined edges of the structured metallization.

22. A method of manufacturing a semiconductor device, the method comprising:

forming a structured interlayer on a substrate, the structured interlayer having defined edges; and

forming a structured metallization on the structured interlayer, the structured metallization having defined edges,

wherein the structured interlayer is formed so that each defined edge of the structured interlayer neighbors one of the defined edges of the structured metallization and runs in the same direction as the neighboring defined edge of the structured metallization,

wherein the structured interlayer is formed so that each defined edge of the structured interlayer extends beyond the neighboring defined edge of the structured metallization by at least 0.5 microns and each defined edge of the structured metallization terminates before reaching the neighboring defined edge of the structured interlayer, wherein the structured interlayer has a compressive residual stress at room temperature.

23. The method of claim 22, wherein forming the structured interlayer and forming the structured metallization comprises:

depositing an interlayer material system on the substrate, the interlayer material system having an overall compressive residual stress at room temperature;

depositing and patterning metal on the interlayer material system;

using the deposited and structured metal as a mask to remove the part of the interlayer material system unprotected by the deposited and structured metal; and

laterally etching the deposited and structured metal selective to the interlayer material system so that each defined edge of the interlayer material system extends beyond the neighboring defined edge of the deposited and structured metal by at least 0.5 microns.

24. The method of claim 22, wherein forming the structured interlayer comprises:

depositing an interlayer material system on the substrate, the interlayer material system having an overall compressive residual stress at room temperature; and

patterning the interlayer material system to form the structured interlayer before depositing any metal of the structured metallization.

25. The method of claim 24, wherein forming the structured metallization comprises:

forming a mask on the structured interlayer, the mask covering at least a 0.5 micron periphery around the perimeter of the structured interlayer and having an opening which exposes the structured interlayer inward from the periphery; and

depositing metal in the opening of the mask to form the structured metallization, wherein the mask prevents the metal from being deposited on the periphery of the structured interlayer.

26. The method of claim 22, wherein forming the structured interlayer and forming the structured metallization comprises:

depositing a first interlayer material on the substrate and a second interlayer material on the first interlayer material, the first and the second interlayer materials forming a bilayer interlayer having an overall compressive residual stress at room temperature;

etching an exposed part of the second interlayer material selective to the first interlayer material before depositing any metal of the structured metallization;

forming a mask on the etched second interlayer material, the mask covering at least a 0.5 micron periphery around the perimeter of the etched second interlayer material

and having an opening which exposes the etched second interlayer material inward from the periphery;

depositing metal in the opening of the mask to form the structured metallization, wherein the mask prevents the metal from being deposited on the periphery of the etched second interlayer material; and

etching an exposed part of the first interlayer material selective to the second interlayer material after depositing the metal, to form the structured interlayer.

27. The method of claim 22, wherein forming the structured interlayer comprises:

depositing an interlayer material system on the substrate, the interlayer material system having an overall compressive residual stress at room temperature;

forming the structured metallization on the interlayer material system;

covering the structured metallization with a mask, the mask being wider than the structured metallization so that the mask extends onto the interlayer material system by at least 0.5 microns beyond the perimeter of the structured metallization; and

removing the part of the interlayer material system unprotected by the mask.

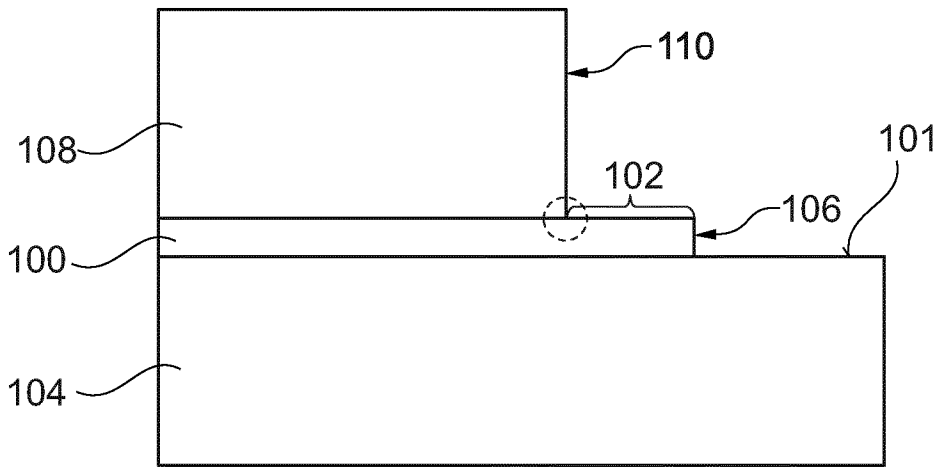

Fig. 1

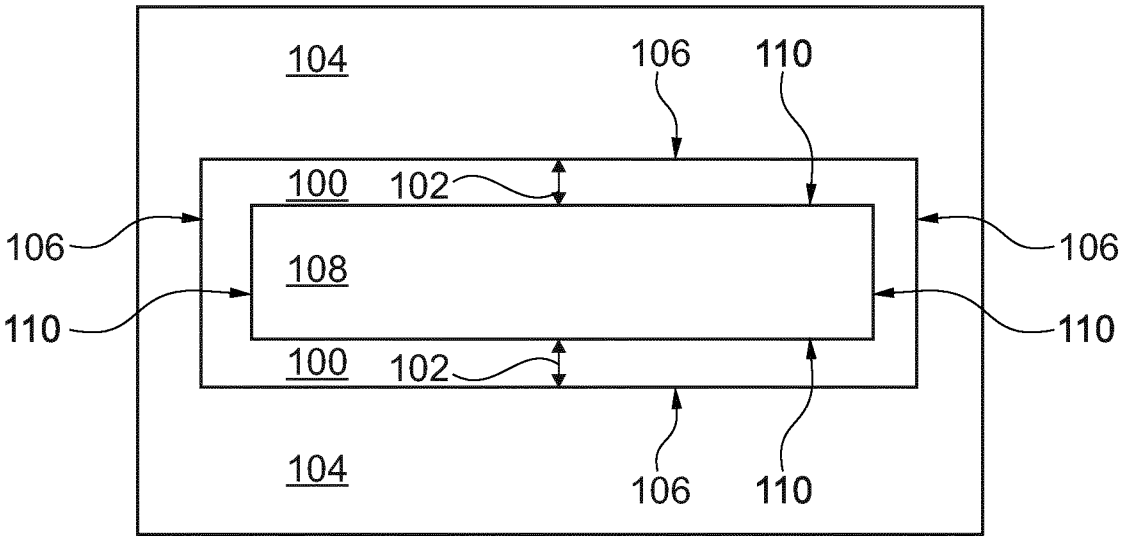

Fig. 2

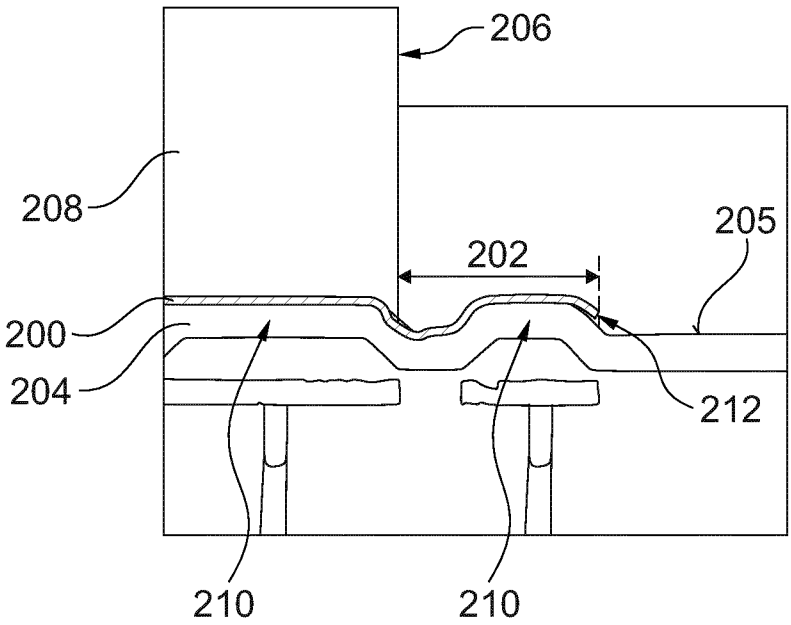
206
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Fig. 3

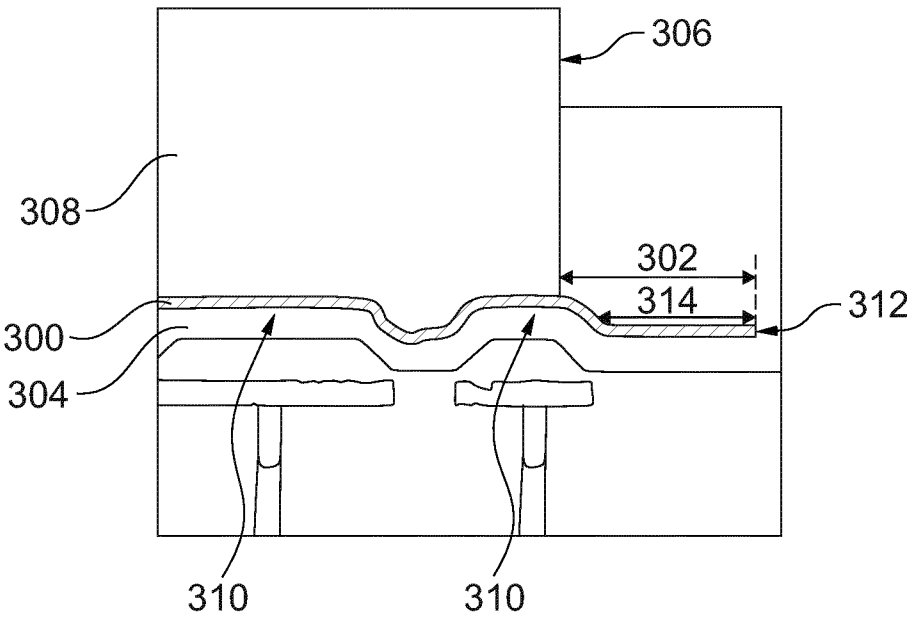
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Fig. 4

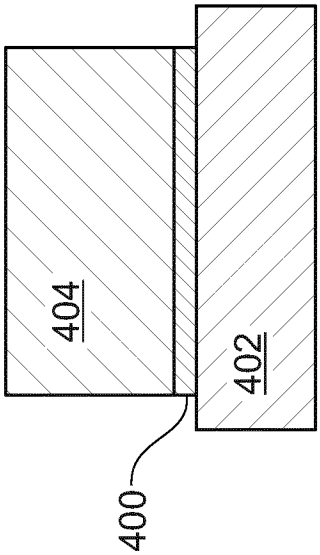

Fig. 5C

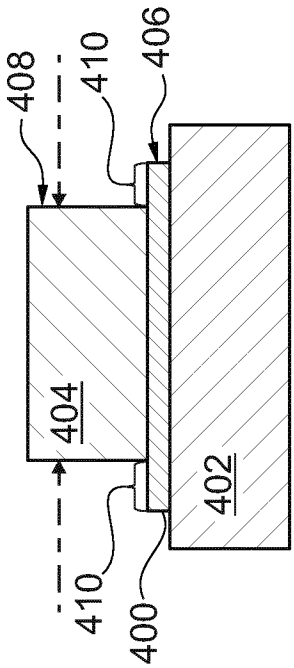

Fig. 5D

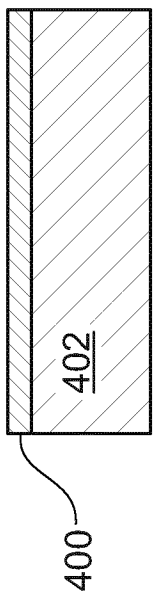

Fig. 5A

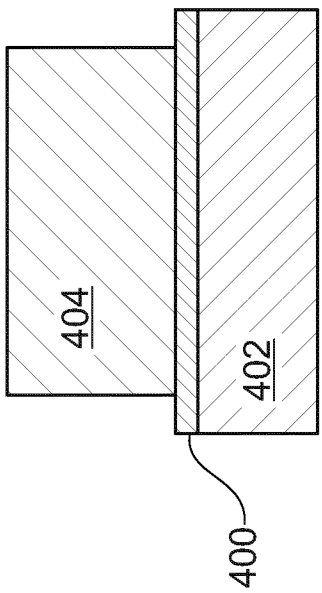

Fig. 5B

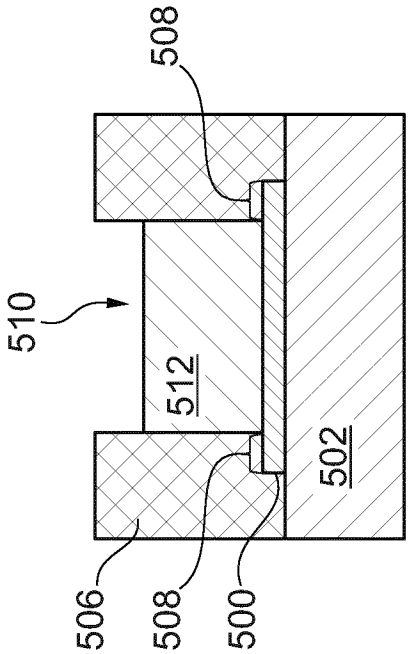

Fig. 6D

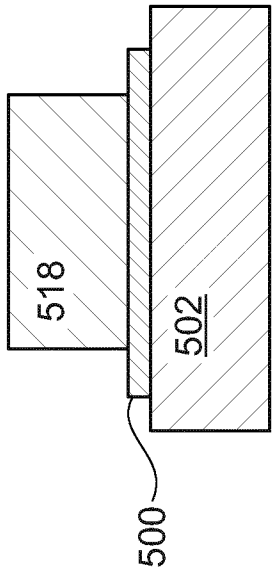

Fig. 6E

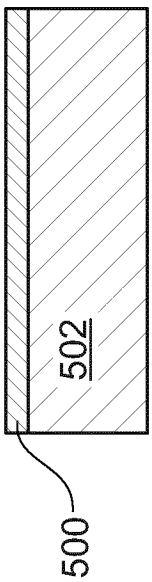

Fig. 6A

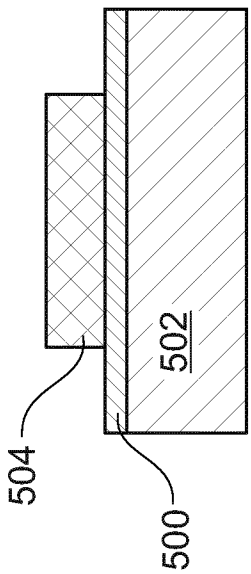

Fig. 6B

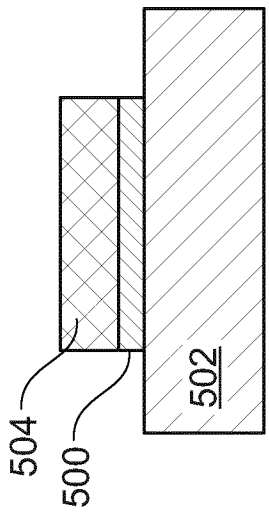

Fig. 6C

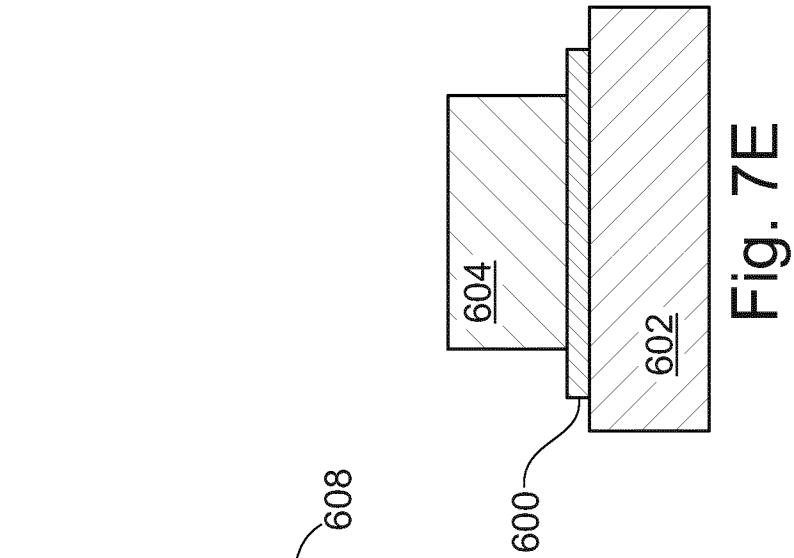

Fig. 7E

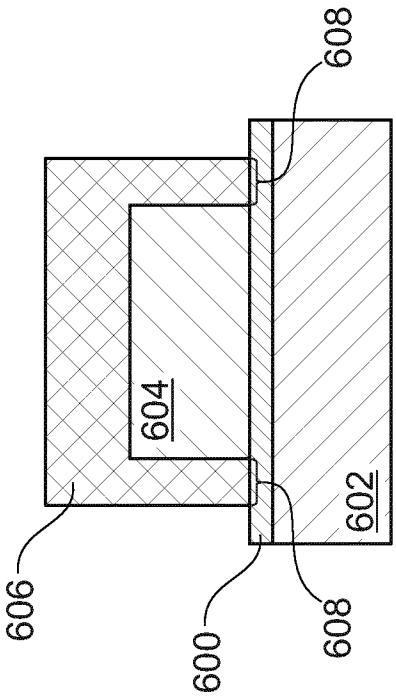

Fig. 7C

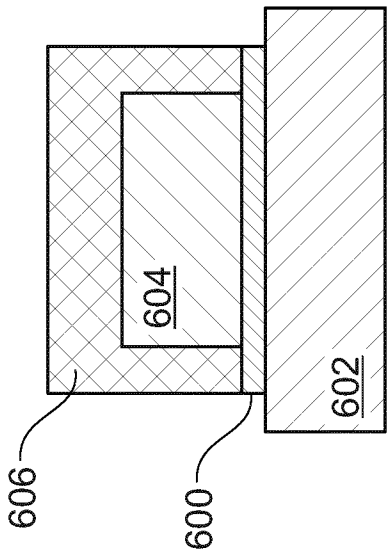

Fig. 7D

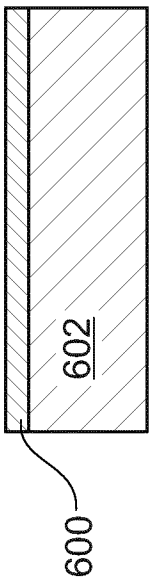

Fig. 7A

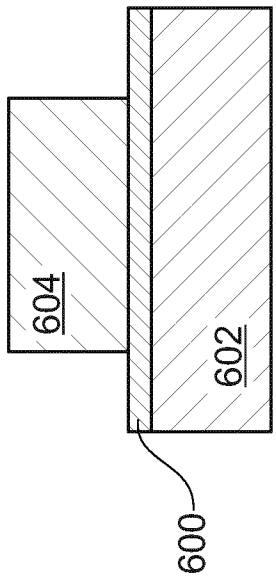

Fig. 7B

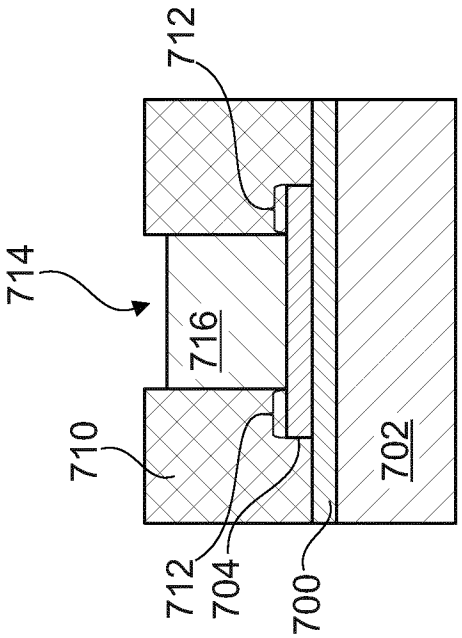

Fig. 8D

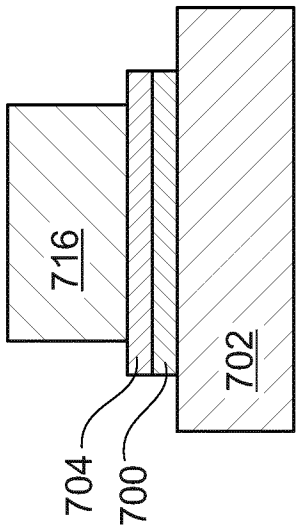

Fig. 8E

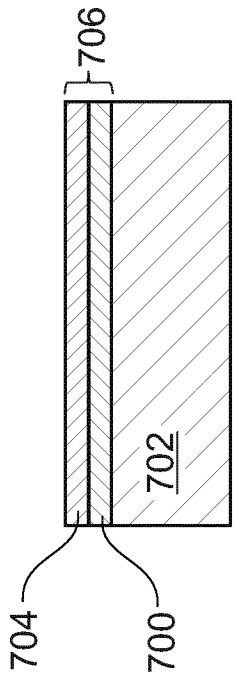

Fig. 8A

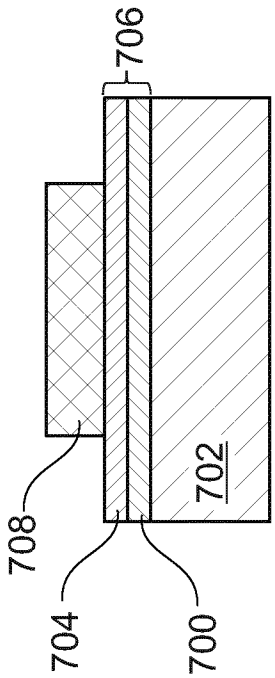

Fig. 8B

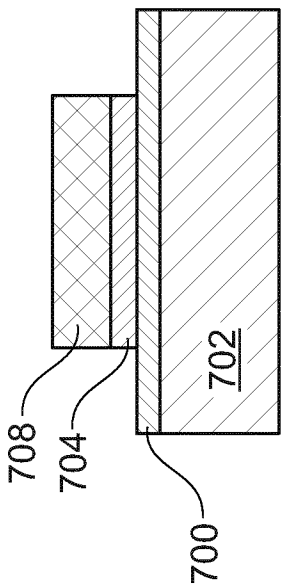

Fig. 8C

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/072712

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/00 H01L23/58 B81B3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L B81B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/061823 A1 (KAM SHIAN-YEU [SG] ET AL) 6 March 2014 (2014-03-06)	1,3-5, 15,19, 20,22
A	paragraph [0002] - paragraph [0008]; figures 1,5,10 paragraph [0023] - paragraph [0028] paragraph [0040] - paragraph [0046] -----	17
X	WO 2016/024946 A1 (RAYTHEON CO [US]) 18 February 2016 (2016-02-18) paragraph [0008]; figures 3-5 paragraph [0018] - paragraph [0019] paragraph [0031] - paragraph [0045] -----	1-27
A	US 2010/207237 A1 (YAO ALFRED [SG] ET AL) 19 August 2010 (2010-08-19) paragraph [0041] - paragraph [0048]; figures 5E-F -----	7-13
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 October 2018	30/10/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hirsch, Alexander

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/072712

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/314725 A1 (GU SHIQUN [US] ET AL) 16 December 2010 (2010-12-16) paragraph [0033] paragraph [0038] - paragraph [0041]; figure 5 -----	21

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/072712

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