



(51) International Patent Classification:

H01L 21/02 (2006.01) C23C 16/50 (2006.01)
C23C 16/36 (2006.01)

(21) International Application Number:

PCT/US2024/049179

(22) International Filing Date:

30 September 2024 (30.09.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

18/376,287 03 October 2023 (03.10.2023) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **YAO, Shanshan**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **LU, Xinyi**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **XIE, Bo**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **LANG, Chi-I**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **XIA, Li-Qun**; 3050 Bowers Avenue, Santa Clara, California 95054 (US).

(74) Agent: **CAMPBELL, Quinten M.** et al.; 1100 Peachtree Street NE, Suite 2800, Mailstop: IP Docketing - 22, Atlanta, Georgia 30309 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,

(54) Title: METHODS FOR FORMING LOW-K DIELECTRIC MATERIALS WITH REDUCED DIELECTRIC CONSTANT AND ENHANCED ELECTRICAL PROPERTIES

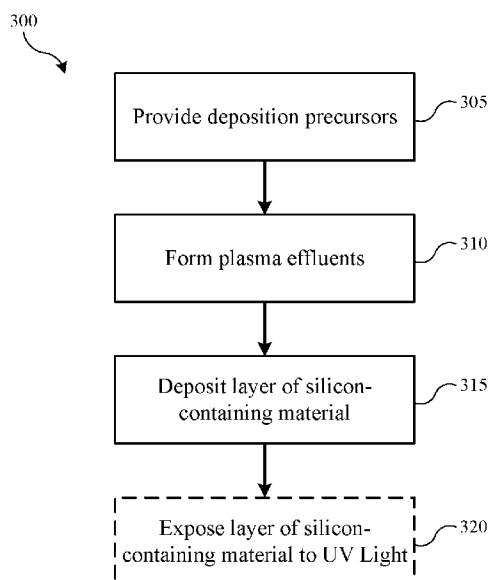


FIG. 3

(57) Abstract: Exemplary semiconductor processing methods may include providing deposition precursors to a processing region of a semiconductor processing chamber. The deposition precursors may include a silicon-carbon-and-nitrogen-containing precursor. A substrate may be disposed within the processing region. The methods may include forming plasma effluents of the deposition precursors. The methods may include depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a dielectric constant of less than or about 4.0. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a leakage current at 2 MV/cm of less than or about $3\text{E-}08\text{ A/cm}^2$.

SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

METHODS FOR FORMING LOW-K DIELECTRIC MATERIALS WITH REDUCED DIELECTRIC CONSTANT AND ENHANCED ELECTRICAL PROPERTIES

CROSS-REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This application claims the benefit and priority of U.S. Patent Application No. 18/376,287, filed October 3, 2023, entitled “METHODS FOR FORMING LOW-K DIELECTRIC MATERIALS WITH REDUCED DIELECTRIC CONSTANT AND ENHANCED ELECTRICAL PROPERTIES”, which is hereby incorporated by reference in its entirety.

10

TECHNICAL FIELD

[0002] The present technology relates to deposition processes and chambers. More specifically, the present technology relates to methods of producing low- κ materials.

BACKGROUND

15 **[0003]** Integrated circuits are made possible by processes which produce intricately patterned material layers on substrate surfaces. Producing patterned material on a substrate requires controlled methods for forming and removing material. Material characteristics may affect how the device operates, and may also affect how the materials are removed relative to one another. Plasma-enhanced deposition may produce materials having certain characteristics, which may affect the performance of the device. The characteristics of the material may be adjusted or enhanced by modifying the deposition conditions, such as the chemistry of precursors provided during deposition and/or processing conditions during deposition.

20 **[0004]** Thus, there is a need for improved systems and methods that can be used to produce high quality devices and structures. These and other needs are addressed by the present
25 technology.

SUMMARY

[0005] Exemplary semiconductor processing methods may include providing deposition precursors to a processing region of a semiconductor processing chamber. The deposition precursors may include a silicon-carbon-and-nitrogen-containing precursor. A substrate may be disposed within the processing region. The methods may include forming plasma effluents of the deposition precursors. The methods may include depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a dielectric constant of less than or about 4.0. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a leakage current at 2 MV/cm of less than or about $3\text{E-}08\text{ A/cm}^2$.

[0006] In some embodiments, the silicon-carbon-and-nitrogen-containing precursor may include greater than or about four methyl groups. The silicon-carbon-and-nitrogen-containing precursor may be or include hexamethyl cyclotrisilazane (HMCTZ), hexamethyldisilazane (HMDS), bis(dimethylamino)-dimethylsilane (BDMADMS), bis(vinyldimethylsilyl) amine (BVDMSA), 1,3,5-trivinyl-1,3,5-trimethyl cyclotrisilazane (3V3MCTZ), tris(dimethylamino) silane (TDMAS), bis(trimethylsilyl)methane, 1,1,3,3-tetramethyl-1,3-disilacyclobutane, trimethylsilane, or a combination thereof. The deposition precursors may further include a nitrogen-containing precursor. The nitrogen-containing precursor may be or include ammonia (NH_3). The methods may include providing helium, argon, or both with the deposition precursors. A flow rate of the silicon-carbon-and-nitrogen-containing precursor may be greater than or about 500 sccm. The plasma effluents may be formed at a plasma power of less than or about 1,500 W. A temperature in the semiconductor processing chamber may be maintained at greater than or about 200 °C. A pressure in the semiconductor processing chamber may be maintained at less than or about 15 Torr. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a breakdown voltage at 0.001 A/cm^2 of greater than or about 5.5 MV/cm. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a dielectric constant of less than or about 3.5.

[0007] Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing deposition precursors to a processing region of a semiconductor processing chamber. The deposition precursors may include a silicon-containing precursor having greater than or about four methyl groups. A

substrate may be disposed within the processing region. The methods may include forming plasma effluents of the deposition precursors. The methods may include depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate. The layer of silicon-containing material may be characterized by a dielectric constant of less than or about 4.0.

5 [0008] In some embodiments, the silicon-containing precursor may further include nitrogen. The deposition precursors further include a nitrogen-containing precursor, a hydrogen-containing precursor, or both. The plasma effluents may be formed at a plasma power of less than or about 1,000 W. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a breakdown voltage at 0.001 A/cm² of greater than or
10 about 7.5 MV/cm. A temperature within the processing region may be maintained at less than or about 600 °C.

[0009] Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing deposition precursors to a processing region of a semiconductor processing chamber. The deposition precursors may
15 include a silicon-carbon-and-nitrogen-containing precursor. The silicon-carbon-and-nitrogen-containing precursor may include greater than or about three methyl groups. A substrate may be disposed within the processing region. The methods may include forming plasma effluents of the deposition precursors at a plasma power of less than or about 1,500 W. The methods may include depositing a layer of silicon-carbon-and-nitrogen-containing material
20 on the substrate. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a dielectric constant of less than or about 4.0. The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a leakage current at 2 MV/cm of less than or about 1E-08 A/cm².

[0010] In some embodiments, the silicon-carbon-and-nitrogen-containing precursor may be
25 or include hexamethyl cyclotrisilazane (HMCTZ).

[0011] Such technology may provide numerous benefits over conventional processing methods. For example, utilizing silicon-containing precursors, such as silicon-carbon-and-nitrogen-containing precursors, that may include increased methyl group during deposition may modify atomic structure of the material to increase methyl groups, decrease Si-C-Si
30 crosslinking, and/or decrease Si-H bonding in the material. Additionally, the modified atomic structure of the material may reduce dielectric constant, decrease leakage current, and/or increase breakdown voltage. These and other embodiments, along with many of their

advantages and features, are described in more detail in conjunction with the below description and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0012] A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

[0013] FIG. 1 shows a top plan view of an exemplary processing system according to some embodiments of the present technology.

[0014] FIG. 2 shows a schematic cross-sectional view of an exemplary plasma system
10 according to some embodiments of the present technology.

[0015] FIG. 3 shows operations of an exemplary method of semiconductor processing according to some embodiments of the present technology.

[0016] Several of the figures are included as schematics. It is to be understood that the figures are for illustrative purposes, and are not to be considered of scale unless specifically
15 stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include exaggerated material for illustrative purposes.

[0017] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by
20 following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

DETAILED DESCRIPTION

25 [0018] During back-end-of-line semiconductor processing, structures may be produced to facilitate metallization, such as dual-damascene structures. These structures may be produced with several processing steps utilizing masking and low- κ films, which may be processed and removed. Conventional technologies have struggled with balancing dielectric constant with other electrical properties, such as leakage current and breakdown voltage. As feature sizes,

such as dimensions of metallization structures, continue to reduce, films with decreased dielectric constant, decrease leakage current, and increased breakdown voltage are more important. Conventional technologies may not currently be able to meet the demands of future devices.

5 **[0019]** The present technology may overcome these issues by providing low- κ films that, as deposited, may be characterized by reduced dielectric constants with decreased leakage currents and/or increased breakdown voltages. By performing the deposition with specific precursors, such as silicon-containing precursors with embedded nitrogen and/or increased methyl moieties, additional methyl, reduced Si-H bonds and/or reduced Si-C-Si crosslinking
10 may be incorporated into the as-deposited material. The increased amount of methyl in the as-deposited material may increase Si-CH₃ bonding within the film to lower dielectric constant, while reducing Si-H bonds and/or Si-C-Si crosslinking to address desired electrical properties. This may overcome the natural tendency of dielectric constant and electrical properties, such as leakage current, to be a tradeoff. Further, the present technology may not
15 require subsequent processing after deposition, including UV exposure, plasma treatment, or other processing operations to post-treat the film to improve mechanical properties, such as dielectric constant or density. However, subsequent processing after deposition may still be performed to further reduce dielectric constant and/or increase density.

[0020] Although the remaining disclosure will routinely identify specific deposition
20 processes utilizing the disclosed technology, it will be readily understood that the systems and methods are equally applicable to other deposition chambers, as well as processes as may occur in the described chambers. Accordingly, the technology should not be considered to be so limited as for use with these specific deposition processes or chambers alone. The disclosure will discuss one possible system and chamber that may be used to perform
25 deposition processes according to embodiments of the present technology before additional details according to embodiments of the present technology are described.

[0021] **FIG. 1** shows a top plan view of one embodiment of a processing system 100 of deposition, etching, baking, and UV treatment chambers according to embodiments. In the figure, a pair of front opening unified pods 102 supply substrates of a variety of sizes that are
30 received by robotic arms 104 and placed into a low pressure holding area 106 before being placed into one of the substrate processing chambers 108a-f, positioned in tandem sections 109a-c. A second robotic arm 110 may be used to transport the substrate wafers from the

holding area 106 to the substrate processing chambers 108a-f and back. Each substrate processing chamber 108a-f, can be outfitted to perform a number of substrate processing operations including plasma-enhanced chemical vapor deposition, atomic layer deposition, physical vapor deposition, etch, UV treatments, pre-clean, degas, orientation, and other substrate processes including, annealing, ashing, etc.

[0022] The substrate processing chambers 108a-f may include one or more system components for depositing, annealing, UV treating and/or etching a dielectric or other material on the substrate. In one configuration, two pairs of the processing chambers, e.g., 108c-d and 108e-f, may be used to deposit dielectric material on the substrate, and the third pair of processing chambers, e.g., 108a-b, may be used to etch the deposited dielectric. In another configuration, all three pairs of chambers, e.g., 108a-f, may be configured to deposit stacks of alternating dielectric materials on the substrate. Any one or more of the processes described may be carried out in chambers separated from the fabrication system shown in different embodiments. It will be appreciated that additional configurations of deposition, etching, annealing, and UV treatment chambers for dielectric materials are contemplated by system 100.

[0023] FIG. 2 shows a schematic cross-sectional view of an exemplary plasma system 200 according to some embodiments of the present technology. Plasma system 200 may illustrate a pair of processing chambers 108 that may be fitted in one or more of tandem sections 109 described above, and which may include lid stack components according to embodiments of the present technology, and as may be explained further below. The plasma system 200 generally may include a chamber body 202 having sidewalls 212, a bottom wall 216, and an interior sidewall 201 defining a pair of processing regions 220A and 220B. Each of the processing regions 220A-220B may be similarly configured, and may include identical components.

[0024] For example, processing region 220B, the components of which may also be included in processing region 220A, may include a pedestal 228 disposed in the processing region through a passage 222 formed in the bottom wall 216 in the plasma system 200. The pedestal 228 may provide a heater adapted to support a substrate 229 on an exposed surface of the pedestal, such as a body portion. The pedestal 228 may include heating elements 232, for example resistive heating elements, which may heat and control the substrate temperature

at a desired process temperature. Pedestal 228 may also be heated by a remote heating element, such as a lamp assembly, or any other heating device.

5 [0025] The body of pedestal 228 may be coupled by a flange 233 to a stem 226. The stem 226 may electrically couple the pedestal 228 with a power outlet or power box 203. The power box 203 may include a drive system that controls the elevation and movement of the pedestal 228 within the processing region 220B. The stem 226 may also include electrical power interfaces to provide electrical power to the pedestal 228. The power box 203 may also include interfaces for electrical power and temperature indicators, such as a thermocouple interface. The stem 226 may include a base assembly 238 adapted to
10 detachably couple with the power box 203. A circumferential ring 235 is shown above the power box 203. In some embodiments, the circumferential ring 235 may be a shoulder adapted as a mechanical stop or land configured to provide a mechanical interface between the base assembly 238 and the upper surface of the power box 203.

[0026] A rod 230 may be included through a passage 224 formed in the bottom wall 216 of
15 the processing region 220B and may be utilized to position substrate lift pins 261 disposed through the body of pedestal 228. The substrate lift pins 261 may selectively space the substrate 229 from the pedestal to facilitate exchange of the substrate 229 with a robot utilized for transferring the substrate 229 into and out of the processing region 220B through a substrate transfer port 260.

20 [0027] A chamber lid 204 may be coupled with a top portion of the chamber body 202. The lid 204 may accommodate one or more precursor distribution systems 208 coupled thereto. The precursor distribution system 208 may include a precursor inlet passage 240 which may deliver reactant and cleaning precursors through a dual-channel showerhead 218 into the processing region 220B. The dual-channel showerhead 218 may include an annular
25 base plate 248 having a blocker plate 244 disposed intermediate to a faceplate 246. A radio frequency ("RF") source 265 may be coupled with the dual-channel showerhead 218, which may power the dual-channel showerhead 218 to facilitate generating a plasma region between the faceplate 246 of the dual-channel showerhead 218 and the pedestal 228. The dual-channel showerhead 218 and/or faceplate 246 may include one or more openings to permit
30 the flow of precursors from the precursor distribution system 208 to the processing regions 220A and/or 220B. In some embodiments, the openings may include at least one of straight-shaped openings and conical-shaped openings. In some embodiments, the RF source may be

coupled with other portions of the chamber body 202, such as the pedestal 228, to facilitate plasma generation. A dielectric isolator 258 may be disposed between the lid 204 and the dual-channel showerhead 218 to prevent conducting RF power to the lid 204. A shadow ring 206 may be disposed on the periphery of the pedestal 228 that engages the pedestal 228.

5 [0028] An optional cooling channel 247 may be formed in the annular base plate 248 of the precursor distribution system 208 to cool the annular base plate 248 during operation. A heat transfer fluid, such as water, ethylene glycol, a gas, or the like, may be circulated through the cooling channel 247 such that the base plate 248 may be maintained at a predefined temperature. A liner assembly 227 may be disposed within the processing region 220B in
10 close proximity to the sidewalls 201, 212 of the chamber body 202 to prevent exposure of the sidewalls 201, 212 to the processing environment within the processing region 220B. The liner assembly 227 may include a circumferential pumping cavity 225, which may be coupled to a pumping system 264 configured to exhaust gases and byproducts from the processing region 220B and control the pressure within the processing region 220B. A plurality of
15 exhaust ports 231 may be formed on the liner assembly 227. The exhaust ports 231 may be configured to allow the flow of gases from the processing region 220B to the circumferential pumping cavity 225 in a manner that promotes processing within the system 200.

[0029] FIG. 3 shows operations of an exemplary method 300 of semiconductor processing according to some embodiments of the present technology. The method may be performed in
20 a variety of processing chambers, including system 200 described above, as well as any other chamber in which plasma deposition may be performed. Method 300 may include a number of optional operations, which may or may not be specifically associated with some embodiments of methods according to the present technology.

[0030] Method 300 may include plasma-enhanced chemical-vapor-deposition (PECVD)
25 processing operations to form as-deposited low- κ materials. The method 300 may include optional operations prior to initiation of method 300, or the method 300 may include additional operations after the deposition of the low- κ material. In embodiments, method 300, as shown in FIG. 3, may include providing deposition precursors into a processing region of a semiconductor processing chamber at operation 305. A substrate may be housed
30 in the processing region of the semiconductor processing chamber as the deposition precursors are provided into the chamber. Plasma effluents of the deposition precursors may be formed at operation 310. At operation 315, a layer of silicon-carbon-and-nitrogen-

containing material may be deposited on the substrate. In embodiments, at the layer of silicon-carbon-and-nitrogen-containing material may be exposed to ultraviolet (UV) light at optional operation 320.

[0031] In embodiments, the deposition precursors may include a silicon-containing precursor, such as a silicon-carbon-and-nitrogen-containing precursor. Silicon-carbon-and-nitrogen-containing precursors that may be used may be or include, but are not limited to, hexamethyl cyclotrisilazane (HMCTZ), hexamethyldisilazane (HMDS), bis(dimethylamino)-dimethylsilane (BDMADMS), bis(vinyl dimethylsilyl) amine (BVDMSA), 1,3,5-trivinyl-1,3,5-trimethyl cyclotrisilazane (3V3MCTZ), tris(dimethylamino) silane (TDMAS), bis(trimethylsilyl)methane, 1,1,3,3-tetramethyl-1,3-disilacyclobutane, trimethylsilane, or a combination thereof. In embodiments, the silicon-containing precursor may include greater than or about four methyl (CH_3) groups, greater than or about five CH_3 groups, or more. By utilizing silicon-containing precursors also including nitrogen and/or an increased amount of CH_3 groups, an increased amount of C-H bonds in CH_3 groups may be present in the deposition precursors and plasma effluents. As such, an increased amount of C-H bonds in CH_3 groups may be present in the as-deposited layer of silicon-carbon-and-nitrogen-containing material. The increased amount of C-H bonds in CH_3 groups bonding may reduce the dielectric constant of the material while also decreasing the leakage current of the material and/or increasing the breakdown voltage of the material.

[0032] The deposition precursors may further include a nitrogen-containing precursor and/or a hydrogen-containing precursor. Nitrogen-containing precursors that may be used may include, but are not limited to, diatomic nitrogen (N_2), ammonia (NH_3), hydrazine (N_2H_4), as well as any other nitrogen-containing precursors that may be used in silicon-containing material formation. Hydrogen-containing precursors that may be used may include, but are not limited to, diatomic hydrogen (H_2), ammonia (NH_3), hydrazine (N_2H_4), hydrogen peroxide (H_2O_2), as well as any other nitrogen-containing precursors that may be used in silicon-containing material formation. In embodiments, a flow rate of the nitrogen-containing precursor and/or a flow rate of the hydrogen-containing precursor relative to the flow rate of the silicon-carbon-and-nitrogen-containing precursor may be maintained and/or adjusted at a flow rate ratio that assists in forming a low- κ materials with a low dielectric constant (κ value). The deposition precursors may also include one or more carrier gases such as helium, argon, and nitrogen. Although the one or more carrier gases may be delivered with other deposition precursors, the carrier gases may be considered inert gases

that do not react to form part of the as-deposited material. The one or more carrier gases may be delivered with other deposition precursors to serve as a diluent.

[0033] A flow rate of the silicon-carbon-and-nitrogen-containing precursor may be greater than or about 50 sccm, greater than or about 60 sccm, greater than or about 70 sccm, greater than or about 80 sccm, greater than or about 90 sccm, greater than or about 100 sccm, greater than or about 125 sccm, greater than or about 150 sccm, greater than or about 175 sccm, greater than or about 200 sccm, greater than or about 250 sccm, greater than or about 300 sccm, greater than or about 350 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 1,250 sccm, greater than or about 1,500 sccm, greater than or about 1,750 sccm, greater than or about 2,000 sccm, or more. At increased flow rates of the silicon-carbon-and-nitrogen-containing precursor, such as greater than 500 sccm, Si-C-Si crosslinking may decrease, which may lower the dielectric constant and/or increase density of the material. Conversely, at lower flow rates, N-H bonding may decrease and, therefore, hermeticity of the material may decrease.

[0034] A flow rate of the nitrogen-containing precursor, if present, may be greater than or about 50 sccm, greater than or about 60 sccm, greater than or about 70 sccm, greater than or about 80 sccm, greater than or about 90 sccm, greater than or about 100 sccm, greater than or about 125 sccm, greater than or about 150 sccm, greater than or about 175 sccm, greater than or about 200 sccm, greater than or about 225 sccm, greater than or about 250 sccm, greater than or about 275 sccm, greater than or about 300 sccm, greater than or about 400 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 1,250 sccm, greater than or about 1,500 sccm, greater than or about 2,500 sccm, greater than or about 5,000 sccm, greater than or about 10,000 sccm, or more. The flow rate of the nitrogen-containing precursor may also be less than or about 7,500 sccm, less than or about 5,000 sccm, less than or about 2,500 sccm, less than or about 2,250 sccm, less than or about 2,000 sccm, less than or about 1,750 sccm, less than or about 1,250 sccm, less than or about 1,000 sccm, less than or about 750 sccm, less than or about 500 sccm, less than or about 250 sccm, or less.

[0035] A flow rate of the one or more carrier gases may be greater than or about 200 sccm, greater than or about 300 sccm, greater than or about 400 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about

2,000 sccm, greater than or about 3,000 sccm, greater than or about 3,000 sccm, greater than or about 4,000 sccm, greater than or about 5,000 sccm, or more.

5 [0036] Embodiments of method 300 may include forming plasma effluents from the deposition precursors at operation 310. The plasma effluents may be generated from the deposition precursors within the processing region, such as by providing RF power to the faceplate to generate a plasma within the processing region of the semiconductor processing chamber. In embodiments, the plasma effluents may be formed at a plasma power of less than or about 2,000 W. At increased plasma powers, such as greater than 2,000 W, increased decomposition of the silicon-carbon-and-containing precursor may result, and methyl may be
10 pulled out of the deposited material. At plasma powers of less than or about 2,000 W, conversely, less decomposition may occur, and Si-CH₃ bonding may be preserved in the deposited material. However, lower plasma powers may also reduce Si-C-Si crosslinking which may maintain lower dielectric constants and/or increased densities. Accordingly, the plasma effluents may be formed at a plasma power of less than or about 1,750 W, less than or
15 about 1,500 W, less than or about 1,400 W, less than or about 1,300 W, less than or about 1,200 W, less than or about 1,100 W, less than or about 1,000 W, less than or about 900 W, less than or about 800 W, less than or about 700 W, less than or about 600 W, less than or about 500 W, less than or about 400 W, less than or about 300 W, less than or about 200 W, or less.

20 [0037] In embodiments, a bias power may be applied while forming plasma effluents from the deposition precursors at operation 310 and/or depositing the silicon-carbon-and-nitrogen-containing material on the substrate at operation 315. The application of bias power, which may be continuous or pulsed, may control the ion and radical ratio. The bias power may increase density of the silicon-carbon-and-nitrogen-containing material.

25 [0038] Embodiments of method 300 may include depositing the silicon-carbon-and-nitrogen-containing material on the substrate at operation 315. As previously discussed, the substrate may be present in the processing region of the semiconductor processing chamber, and the silicon-carbon-and-nitrogen-containing material may be formed from plasma effluents generated by the deposition plasma also present in the processing region. The
30 processing region and, therefore, the substrate may be characterized by a temperature less than or about 600 °C, less than or about 580 °C, less than or about 560 °C, less than or about 540 °C, less than or about 520 °C, less than or about 500 °C, less than or about 480 °C, less

than or about 460 °C, less than or about 440 °C, less than or about 420 °C, less than or about 400 °C, less than or about 380 °C, less than or about 360 °C, less than or about 340 °C, less than or about 320 °C, less than or about 300 °C, less than or about 280 °C, less than or about 260 °C, or less during the deposition. Additionally, the processing region and, therefore, the substrate may be characterized by a temperature greater than or about 200 °C, greater than or about 225 °C, greater than or about 250 °C, greater than or about 275 °C, greater than or about 300 °C, greater than or about 325 °C, greater than or about 350 °C, greater than or about 375 °C, greater than or about 400 °C, greater than or about 425 °C, greater than or about 450 °C, greater than or about 475 °C, greater than or about 500 °C, or more during the deposition. At increased temperatures, such as greater than or about 250 °C, density of the silicon-carbon-and-nitrogen-containing material may increase. At increased temperatures, absorbed molecules in the material may diffuse greater distances to join already formed nuclei rather than forming a new nucleus. Therefore, at increased temperatures, the absorbed molecules may have more thermal energy to arrange in the material and a denser material may be formed. Additionally, at increased temperatures, methyl incorporation may decrease whereas lower temperatures may further reduce Si-C-Si crosslinking.

[0039] During method 300, a pressure in the semiconductor processing chamber may be greater than or about 1 Torr, greater than or about 2 Torr, greater than or about 3 Torr, greater than or about 4 Torr, greater than or about 5 Torr, greater than or about 6 Torr, greater than or about 7 Torr, greater than or about 8 Torr, greater than or about 9 Torr, greater than or about 10 Torr, greater than or about 15 Torr, greater than or about 20 Torr, or more during the deposition. However, at increased pressures, increased residence time of the deposition precursors may result, which may allow for more reaction time and reduced methyl incorporation in the deposited material. Additionally, a pressure in the semiconductor processing chamber may be less than or about 15 Torr, less than or about 14 Torr, less than or about 13 Torr, less than or about 12 Torr, less than or about 11 Torr, less than or about 10 Torr, less than or about 9 Torr, less than or about 8 Torr, less than or about 7 Torr, less than or about 6 Torr, less than or about 5 Torr, less than or about 4 Torr, less than or about 3 Torr, less than or about 2 Torr, less than or about 1 Torr, or less during the deposition.

[0040] A deposition rate of the layer of silicon-carbon-and-nitrogen-containing material may be greater than or about 500 Å/min, and may be greater than or about 525 Å/min, greater than or about 550 Å/min, greater than or about 575 Å/min, greater than or about 600 Å/min,

greater than or about 625 Å/min, greater than or about 650 Å/min, greater than or about 675 Å/min, greater than or about 700 Å/min, greater than or about 725 Å/min, greater than or about 750 Å/min, greater than or about 775 Å/min, greater than or about 700 Å/min, or more.

[0041] In embodiments, the layer of silicon-carbon-and-nitrogen-containing material may be characterized by a leakage current at 2 MV/cm of less than or about 3E-08 A/cm². The reduced Si-H bonding in the material may lower the leakage current of the material due to the reduced amount of dangling hydrogen bonds. In embodiments, the leakage current at 2 MV/cm may be less than or about 2E-08 A/cm², less than or about 1E-08 A/cm², less than or about 9E-09 A/cm², less than or about 8E-09 A/cm², less than or about 7E-09 A/cm², less than or about 6E-09 A/cm², less than or about 5.9E-09 A/cm², less than or about 5.8E-09 A/cm², less than or about 5.7E-09 A/cm², or less.

[0042] The layer of silicon-carbon-and-nitrogen-containing material may be characterized by a breakdown voltage at 0.001 A/cm² of greater than or about 6.5 MV/cm. The increased Si-CH₃ bonding in the material may be stronger than other possible bonds, such as Si-H bonding, and may result in an increased breakdown voltage. In embodiments, the breakdown voltage at 0.001 A/cm² may be greater than or about 5.5 MV/cm, greater than or about 6.0 MV/cm, greater than or about 6.5 MV/cm, greater than or about 7.0 MV/cm, greater than or about 7.5 MV/cm, greater than or about 8.0 MV/cm, greater than or about 8.1 MV/cm, greater than or about 8.2 MV/cm, greater than or about 8.3 MV/cm, greater than or about 8.4 MV/cm, or more.

[0043] As explained above, the methods of the present technology include embodiments that utilize deposition precursors and processing conditions that form low-κ materials having a low dielectric constant. A reduced amount of Si-C-Si crosslinking in the material may reduce the dielectric constant. In embodiments of method 300, as-deposited low-κ materials may be formed as silicon-carbon-and-nitrogen-containing materials with dielectric constants less than or about 5.0, less than or about 4.8, less than or about 4.6, less than or about 4.4, less than or about 4.2, less than or about 4.0, less than or about 3.9, less than or about 3.8, less than or about 3.7, less than or about 3.6, less than or about 3.5, less than or about 3.4, less than or about 3.3, less than or about 3.2, less than or about 3.1, less than or about 3.0, or less.

[0044] The methods of the present technology include embodiments that utilize deposition precursors and processing conditions that may also form low-κ materials having an increased density. In embodiments of method 300, as-deposited low-κ materials may be formed as

silicon-carbon-and-nitrogen-containing materials with densities greater than or about greater than or about 2.0 g/cm³, greater than or about greater than or about 2.05 g/cm³, greater than or about 2.1 g/cm³, greater than or about 2.15 g/cm³, greater than or about 2.2 g/cm³, greater than or about 2.25 g/cm³, greater than or about 2.3 g/cm³, greater than or about 2.35 g/cm³,
5 greater than or about 2.4 g/cm³, greater than or about 2.45 g/cm³, greater than or about 2.5 g/cm³, or more.

[0045] Embodiments of the method 300 may further include exposing the as-deposited silicon-carbon-and-nitrogen-containing material to an ultraviolet (UV) treatment at optional operation 320. In embodiments, the UV treatment may be performed in the semiconductor
10 processing chamber used for the deposition of the low- κ material. However, it is also contemplated that the substrate with the as-deposited low- κ material may be transferred to another semiconductor processing chamber where the UV treatment operation is performed. In embodiments, the UV treatment at optional operation 320 may expose the layer of silicon-carbon-and-nitrogen-containing material to ultraviolet light to provide a cured layer of
15 silicon-carbon-and-nitrogen-containing material. The treatment may produce a cured low- κ material characterized by an increased porosity and/or lower dielectric constant (κ value) than the as-deposited material.

[0046] In some embodiments, the as-deposited silicon-carbon-and-nitrogen-containing material may be deposited to a thickness of greater than or about 750 Å, greater than or about
20 800 Å, greater than or about 850 Å, greater than or about 900 Å, greater than or about 950 Å, greater than or about 1,000 Å, greater than or about 1,100 Å, greater than or about 1,200 Å, greater than or about 1,300 Å, or more. The as-deposited silicon-carbon-and-nitrogen-containing material may be deposited in two or more deposition and UV-treatment cycles to build up the final, UV-treated, low- κ material. For example, the number of deposition and
25 treatment cycles may be greater than or about three cycles, greater than or about five cycles, greater than or about ten cycles, greater than or about 15 cycles, greater than or about 20 cycles, greater than or about 30 cycles, greater than or about 40 cycles, greater than or about 50 cycles, or more.

[0047] In the preceding description, for the purposes of explanation, numerous details have
30 been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

[0048] Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present technology. Accordingly, the above description should not be taken as limiting the scope of the technology.

[0049] Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

[0050] As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a layer” includes a plurality of such layer, and reference to “the precursor” includes reference to one or more precursors and equivalents thereof known to those skilled in the art, and so forth.

[0051] Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

CLAIMS:

1. A semiconductor processing method comprising:
providing deposition precursors to a processing region of a semiconductor processing chamber, wherein the deposition precursors comprise a silicon-carbon-and-nitrogen-containing precursor, and wherein a substrate is disposed within the processing region;
forming plasma effluents of the deposition precursors; and
depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate, wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a dielectric constant of less than or about 4.0, and wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a leakage current at 2 MV/cm of less than or about $3\text{E-}08\text{ A/cm}^2$.
2. The semiconductor processing method of claim 1, wherein the silicon-carbon-and-nitrogen-containing precursor comprises greater than or about four methyl groups.
3. The semiconductor processing method of claim 1, wherein the silicon-carbon-and-nitrogen-containing precursor comprises hexamethyl cyclotrisilazane (HMCTZ), hexamethyldisilazane (HMDS), bis(dimethylamino)-dimethylsilane (BDMADMS), bis(vinyldimethylsilyl) amine (BVDMSA), 1,3,5-trivinyl-1,3,5-trimethyl cyclotrisilazane (3V3MCTZ), tris(dimethylamino) silane (TDMAS), bis(trimethylsilyl)methane, 1,1,3,3-tetramethyl-1,3-disilacyclobutane, trimethylsilane, or a combination thereof.
4. The semiconductor processing method of claim 1, wherein the deposition precursors further comprise a nitrogen-containing precursor.
5. The semiconductor processing method of claim 4, wherein the nitrogen-containing precursor comprises ammonia (NH_3).
6. The semiconductor processing method of claim 1, further comprising: providing helium, argon, or both with the deposition precursors.
7. The semiconductor processing method of claim 1, wherein a flow rate of the silicon-carbon-and-nitrogen-containing precursor is greater than or about 500 sccm.

8. The semiconductor processing method of claim 1, wherein the plasma effluents are formed at a plasma power of less than or about 1,500 W.

9. The semiconductor processing method of claim 6, wherein a temperature in the semiconductor processing chamber is maintained at greater than or about
5 200 °C.

10. The semiconductor processing method of claim 1, wherein a pressure in the semiconductor processing chamber is maintained at less than or about 15 Torr.

11. The semiconductor processing method of claim 1, wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a breakdown voltage at
10 0.001 A/cm² of greater than or about 5.5 MV/cm.

12. The semiconductor processing method of claim 1, wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a dielectric constant of less than or about 3.5.

13. A semiconductor processing method comprising:
15 providing deposition precursors to a processing region of a semiconductor processing chamber, wherein the deposition precursors comprise a silicon-containing precursor comprising greater than or about four methyl groups, and wherein a substrate is disposed within the processing region;
forming plasma effluents of the deposition precursors; and
20 depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate, wherein the layer of silicon-containing material is characterized by a dielectric constant of less than or about 4.0.

14. The semiconductor processing method of claim 13, wherein the silicon-containing precursor further comprises nitrogen.

15. The semiconductor processing method of claim 13, wherein the deposition precursors further comprise a nitrogen-containing precursor, a hydrogen-containing precursor, or both.

16. The semiconductor processing method of claim 15, wherein the plasma effluents are formed at a plasma power of less than or about 1,000 W.

17. The semiconductor processing method of claim 13, wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a breakdown voltage at 0.001 A/cm^2 of greater than or about 7.5 MV/cm .

18. The semiconductor processing method of claim 13, wherein a
5 temperature within the processing region is maintained at less than or about 600°C .

19. A semiconductor processing method comprising:
providing deposition precursors to a processing region of a semiconductor processing chamber, wherein the deposition precursors comprise a silicon-carbon-and-nitrogen-containing precursor, wherein the silicon-carbon-and-nitrogen-containing precursor
10 comprises greater than or about three methyl groups, and wherein a substrate is disposed within the processing region;

forming plasma effluents of the deposition precursors at a plasma power of less than or about $1,500 \text{ W}$; and

15 depositing a layer of silicon-carbon-and-nitrogen-containing material on the substrate, wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a dielectric constant of less than or about 4.0 , and wherein the layer of silicon-carbon-and-nitrogen-containing material is characterized by a leakage current at 2 MV/cm of less than or about $1\text{E-}08 \text{ A/cm}^2$.

20 20. The semiconductor processing method of claim 19, wherein the silicon-carbon-and-nitrogen-containing precursor comprises hexamethyl cyclotrisilazane (HMCTZ).

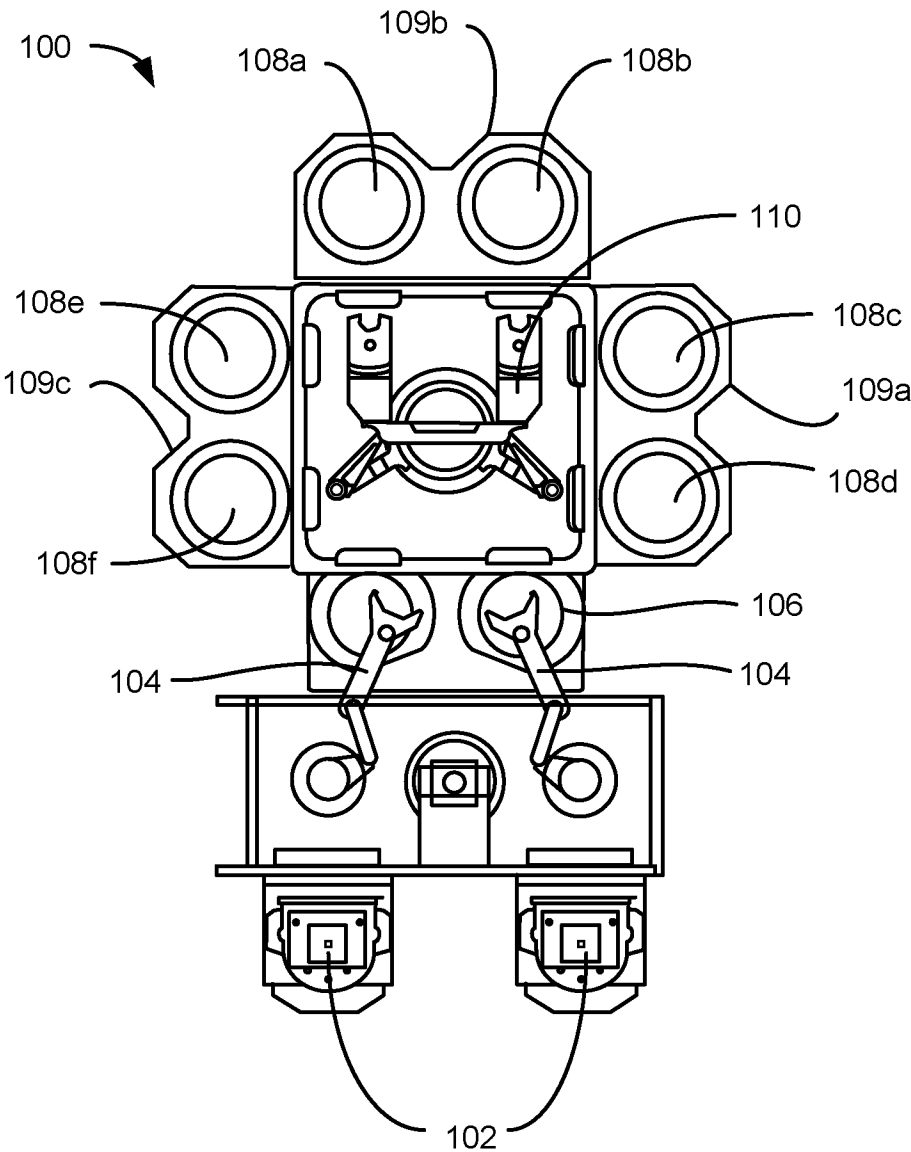


FIG. 1

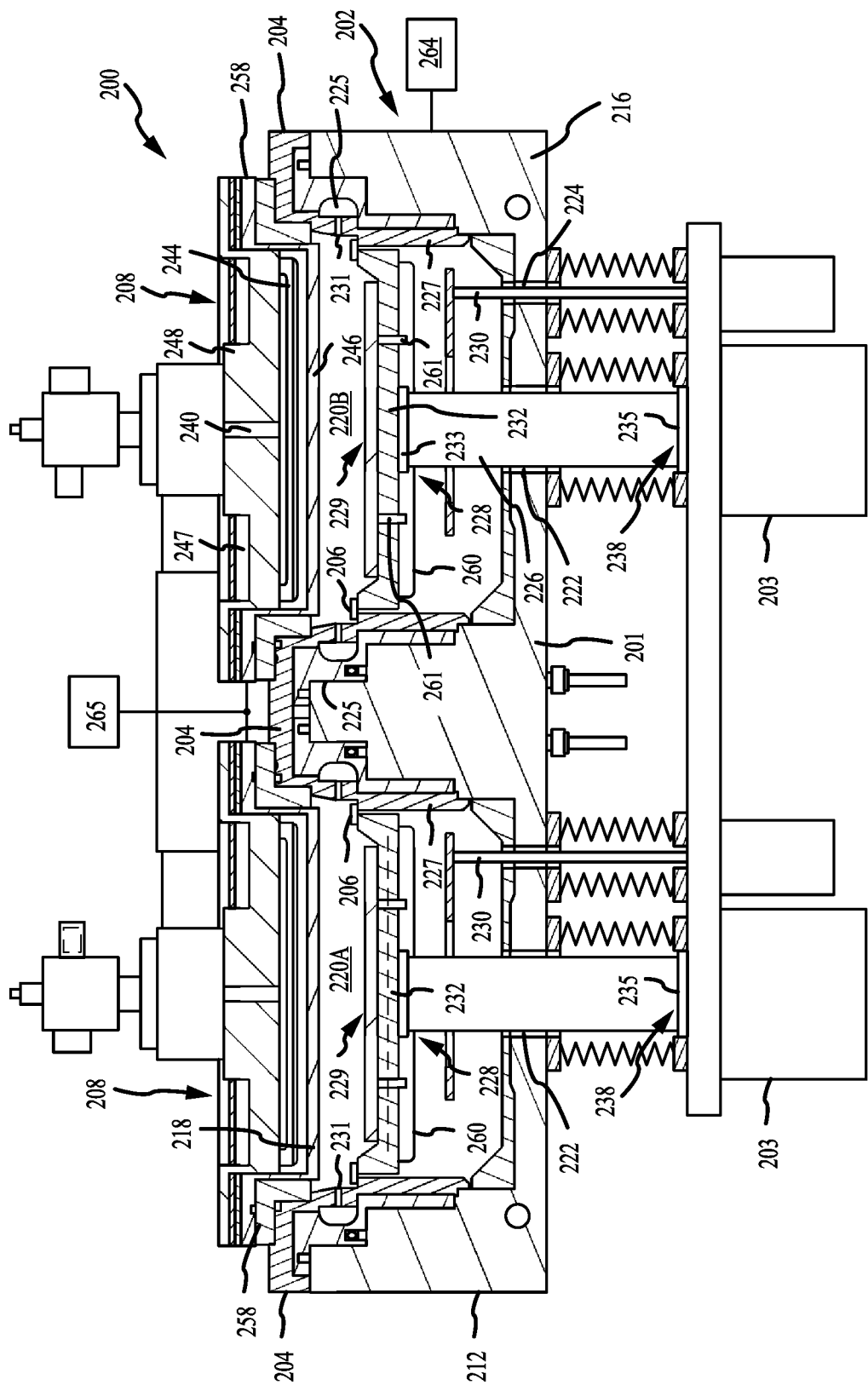
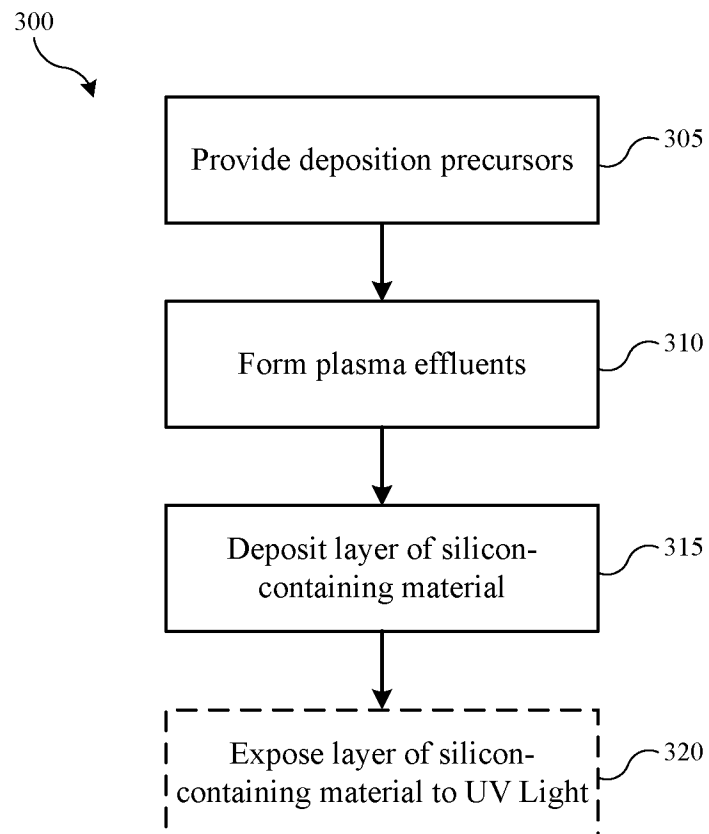


FIG. 2

3/3**FIG. 3**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/049179

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/02**(2006.01)i; **C23C 16/36**(2006.01)i; **C23C 16/50**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/02(2006.01); C23C 16/34(2006.01); C23C 16/455(2006.01); H01L 21/31(2006.01); H01L 21/768(2006.01);
H01L 29/16(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: plasma, deposition, leakage-current, dielectric-constant, hexamethylcyclotrisilazane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0042610 A1 (LI-QUN XIA et al.) 22 February 2007 (2007-02-22) Paragraphs [0012]-[0064]; and claims 1-8.	1-10,12-16,18-20
Y		11,17
Y	US 2014-0273516 A1 (APPLIED MATERIALS, INC.) 18 September 2014 (2014-09-18) Figure 5.	11,17
A	WO 2023-147382 A1 (VERSUM MATERIALS US, LLC) 03 August 2023 (2023-08-03) The entire document.	1-20
A	WO 2018-111570 A1 (LAM RESEARCH CORPORATION) 21 June 2018 (2018-06-21) The entire document.	1-20
A	US 2005-0042858 A1 (LIHUA LI et al.) 24 February 2005 (2005-02-24) The entire document.	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“D” document cited by the applicant in the international application

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

07 January 2025

Date of mailing of the international search report

07 January 2025

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon
35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Kang Ha

Telephone No. +82-42-481-5687

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2024/049179

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)		Publication date (day/month/year)	
US	2007-0042610	A1	22 February 2007	US	2003-0068881	A1	10 April 2003
				US	2004-0198070	A1	07 October 2004
				US	6759327	B2	06 July 2004
				US	7125813	B2	24 October 2006
				US	7319068	B2	15 January 2008
				WO	03-043073	A2	22 May 2003
				WO	2003-043073	A3	29 January 2004

US	2014-0273516	A1	18 September 2014	None			

WO	2023-147382	A1	03 August 2023	EP	4448835	A1	23 October 2024
				IL	314388	A	01 September 2024
				KR	10-2024-0141801	A	27 September 2024
				TW	202330559	A	01 August 2023

WO	2018-111570	A1	21 June 2018	CN	110313051	A	08 October 2019
				CN	110313051	B	09 June 2023
				CN	113707542	A	26 November 2021
				JP	2020-502797	A	23 January 2020
				KR	10-2019-0088069	A	25 July 2019
				KR	10-2022-0085847	A	22 June 2022
				KR	10-2022-0134787	A	05 October 2022
				KR	10-2023-0137503	A	04 October 2023
				KR	10-2446511	B1	23 September 2022
				KR	10-2447498	B1	23 September 2022
				KR	10-2582838	B1	26 September 2023
				TW	201835374	A	01 October 2018
				US	9837270	B1	05 December 2017

US	2005-0042858	A1	24 February 2005	EP	1588410	A1	26 October 2005
				KR	10-1119297	B1	15 March 2012
				KR	10-2005-0092430	A	21 September 2005
				US	2004-0137756	A1	15 July 2004
				US	6790788	B2	14 September 2004
				US	7049249	B2	23 May 2006
				WO	2004-064136	A1	29 July 2004
