(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 May 2006 (11.05.2006)

PCT

(10) International Publication Number
WO 2006/050017 A2

(51) International Patent Classification:
H04N 5/217 (2006.01)

(21) International Application Number:
PCT/US2005/038744

(22) International Filing Date: 27 October 2005 (27.10.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/975,865 28 October 2004 (28.10.2004) US

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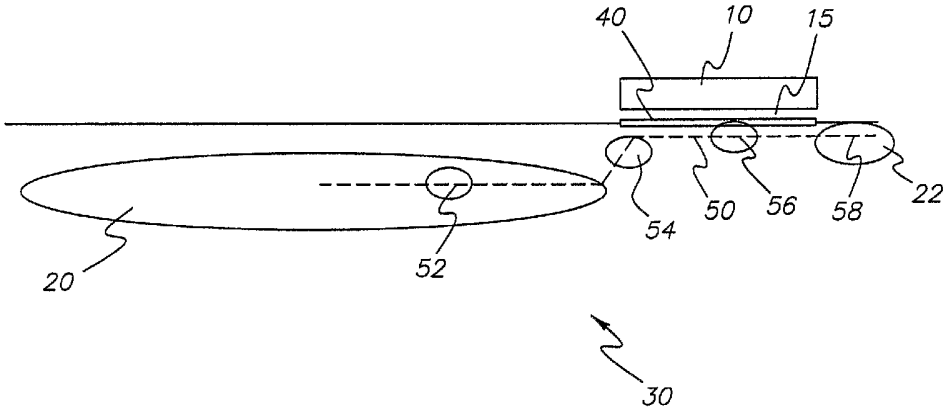
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR DECREASING UNDESIRABLE DARK CURRENT



(57) Abstract: A method for lowering dark current in an image sensor pixel, the method includes the steps of providing a photosensitive area for receiving incident light which is converted into a charge; providing a gate for transferring charge from the photosensitive area; wherein the gate is held at a voltage which will accumulate majority carriers at a semiconductor-dielectric interface during integration for the photosensitive area. Alternatively, a potentail profile can be provided under the gate to drain the dark current away from the photogeneration diffusion.

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METHOD FOR DECREASING UNDESIRABLE DARK CURRENT

FIELD OF THE INVENTION

The invention relates generally to the field of image sensors and, more particularly, to such image sensors in which undesirable dark current is substantially eliminated.

BACKGROUND OF THE INVENTION

As is well known in the art, dark current is a significant limitation of the performance of image sensors, particularly CMOS image sensors. A typical image sensor includes a substrate having a photosensitive area or charge collection area for collecting charge, and a transfer gate for transferring charge from the photosensitive area to either a charge-to-voltage conversion mechanism, such as a floating diffusion in a CMOS image sensor, a transfer mechanism in a charge-coupled device image sensor or to a reset mechanism. A dielectric is positioned between the gate and the substrate, and the area of contact between the two areas is generally referred to in the art as the semiconductor/dielectric interface. During certain stages of image capture, such as integration, electrons not associated with the photosensitive process that captures the electronic representation of the image, i.e., the photo-generation process, accumulate in certain portions of the sensor, such as adjacent gates, and inherently migrate into the photosensitive area. These electrons, a portion of what is called dark current, are undesirable as they degrade the quality of the captured image.

It is known that a pinned photodiode includes substantially all the above-described devices except as described hereinbelow. In this regard, pinned photodiodes include a photosensitive area with a pinned layer spanning the photosensitive area. Pinned photodiodes are known to decrease dark current in photosensitive areas. However, dark current still exists from adjacent gates.

Consequently, a need exists for substantially eliminating dark current associated with adjacent gates and other similar structures.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the invention resides in a method for lowering dark current in an image sensor pixel, the method comprising the steps of providing a photosensitive area for receiving incident light which is converted into a charge; providing a gate for transferring charge from the photosensitive area; wherein the gate is held at a voltage which will accumulate majority carriers at a semiconductor-dielectric interface during integration for the photosensitive area.

An alternative means to overcoming one or more of the problems set forth above is presented where the potential profile under the adjoining gate is created so that dark current related to the gate is drained away from the photogeneration diffusion.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect Of The Invention

The present invention has the advantage of substantially eliminating dark current adjacent gates and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of a typical art image sensor pixel;

Fig. 2 is a side view in cross section of Fig. 1;

Fig. 3 is a side view in cross section of the image sensor pixel of Fig. 1 with a pinned-photodiode;

Fig. 4 is a side view in cross section of an image sensor pixel showing the charge transfer channel from the photogeneration diffusion;

Fig. 5A is a potential profile along the charge transfer channel during signal integration in the photogeneration in the prior art;

Fig. 5B is a potential profile along the charge transfer channel during charge transfer from the photogeneration in the present invention;

Fig. 5C is a potential profile along the charge transfer channel during signal integration in the photogeneration with negative voltage;

Fig. 5D is a potential profile along the charge transfer channel during signal integration in the photogeneration in the present invention;

Fig. 5E is a potential profile along the charge transfer channel during signal integration in the photogeneration in an alternate embodiment of the present invention;

Fig. 6 is a top view of the image sensor including some on-chip and off-chip circuitry; and

Fig. 7 is a camera for illustrating a typical commercial embodiment for the image sensor of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figs. 1 and 2, there is shown the top and side view of a pixel of an image sensor of the present invention. Although only one pixel 70 is shown, as is well known in the art, a plurality of such pixels exists on an image sensor and only one is shown for clarity of understanding. The image sensor includes a substrate 30, preferably silicon, having a photosensitive area or charge collection area 20 therein; the photogeneration takes place in the charge collection area 20. The photosensitive area 20 receives incident light and consequently converts the incident light into charge packets during image integration, as is well known in the art. The photosenstive area 20 is electrically isolated from other areas of the pixel and other associated circuitry. A gate 10 having a dielectric 15 spanning its lower portion provides a portion of this isolation, and the gate 10 can be electrically biased to isolate the photosensitive area 20 or to permit the charge collected in the photosensitive area 20 to flow into an adjoining charge-to-voltage conversion node 22 (or referred to alternatively as diffusion or charge sensing node) for purposes of measurement of charge or resetting the charge collection area 20. The gate-controlled charge transfer is along a path 50 that is formed by creating a trough of potential minimum.

Undesirable dark current is generated both in the photosensitive area 20 and along the charge transfer channel 50. Typically, a high rate of dark current generation occurs both at the semiconductor/dielectric interface 42 adjacent to the photosensitive area 20 and at the semiconductor/dielectric interface 40 under the gate 10 due to the high rate of generation resulting from interface states. The dark current from the interfaces 40 and 42 is the dominant source of dark current flowing into the charge sensing node 22. It is noted that the charge sensing node 22 may be replaced by a reset node resulting in the same behavior. For purposes of brevity in the present invention, the implementation with the charge sensing node 22 will be discussed.

Referring to Fig. 3, there is shown the side view of a pixel where a heavily doped diffusion 32 opposite in type to that in the charge collection area 20 is used to shield the charge collection area 20 from the interface 42. This is generally referred to in the art as a pinned photodiode pixel. The photogeneration and charge transfer is along path 50 as before. The diffusion 32, among other benefits, has the effect to suppress dark current generation at the semiconductor/ dielectric interface 42 adjacent to the charge collection area 20.

In this configuration, a dominant source of dark current is at the semiconductor/dielectric interface or surface 40 under the gate 10. The present invention presents a means of surpressing this dark current by biasing the gate 10 to a potential so that the semiconductor at the interface 40 becomes accumulated with free carriers of the majority doping type. The dark current generation occurs because the defects are in an non-equilibrium state, and this accumulation supresses this generation by returning the region where the highest quantity of defects occur to local equilibrium.

Referring to Fig. 4, there is shown a side view in cross section of the image sensor of the present invention as in Fig. 2. In the prior art, the interface 40 is biased in a non-equilibrium state resulting in the generation of dark current. The charge generated by photogeneration (desirable charge generated by the incident light for capturing the image) and by dark current (undesirable charge generated by other means well known in the art) is collected within the charge

collection area 20 at a potential extremum 52. This signal charge is isolated during integration by a barrier created either at the charge-to-transfer potential transition 54 located between the potential extremum 52 and the gate-associated charge transfer channel 56, or at the gate-associated charge transfer channel 56. The existence of either of these barriers is a result of the doping in the semiconductor 30 and the bias on the gate 10.

Referring to Fig. 5A, there is in the prior art the potential in the gate-associated channel or gate channel potential 56 where the potential on gate 10 forms a barrier that isolates the collection potential 52 from the destination potential 58 and where dark current charge can flow both through the collection-to-transfer potential transition 54 to add to dark current in the collection potential 52 that adds to the signal charge, and along the charge transfer path 50 to the destination potential 58. The result is that some of the dark current generated in the interface under the gate 40 will contribute to the dark current in the signal charge located at the destination potential 58.

Referring to Fig. 5B, there is shown that the potential profile of the present invention where the potential on gate 10 removes a barrier that isolated the collection potential 52 from the destination potential 58 and whereby signal charge is readout or reset from the charge collection area 20 along the path 50 to the destination potential 58. Before this is accomplished and while the barrier is still present , however, the charge in the destination potential 58 is removed by means commonly known in the art so that any dark current collected here is kept separate from signal charge.

Referring to Fig. 5C, in a manner in the present invention, a mechanism is disclosed where the gate 10 is used to adjust the potential in the gate-associated channel 56, for example by applying a negative voltage, to the point where the potential on gate 10 forms a barrier that isolates the collection potential 52 from the destination potential 58 and whereby the semiconductor interface 40 is held in an equilibrium condition. The equilibrium condition suppresses dark current from this interface 40 so that it does not contribute to signal dark current collected in the collection volume 52 and does not eventually be transferred along the channel to the destination potential 58.

In the present invention, an additional mechanism, in addition to the above described biasing, is disclosed to eliminate the contribution of dark current from the interface under the gate 10 and the charge transfer channel under the gate 56. Referring to Fig. 5D, there is shown that this dark charge can be directed toward the destination potential 58 if a potential barrier to charge flow is formed at the collection-to-transfer potential transition 54. The dark charge will flow to destination potential 58 where it can be removed before the gate bias is changed to transfer the signal charge (for example the image signal) along the potential path 50 to the destination potential 58 or is otherwise read out. Therefore, this dark current is kept separate from the signal charge collected at the destination potential 58. Such a barrier can be created as a result of the doping in the semiconductor 30 and the bias on the gate 10.

Referring to Fig. 5E, as an additional embodiment of the present invention, the same result can be achieved if a potential gradient is formed along the transfer channel potential 56 causing the dark current charge generated at the interface under the gate 10 to preferentially flow to the destination potential 58 during the signal integration. Therefore, this dark current is kept separate from the signal charge or image signal collected at the destination potential 58. Such a barrier can be created as a result of the doping in the semiconductor 30 the bias on the gate 10 and the bias on the destination potential 58.

Referring to Fig. 6, there is shown a top view of an image sensor 75 having a plurality of pixels 70 and additional, on-chip circuitry or generation source 80 which includes circuitry that enables operation of the above-described, more specifically biasing of the gates 10. Alternatively, this circuitry may be implemented by off-chip or external circuitry 90.

Referring to Fig. 7, there is shown a camera 200 that includes the image sensor 75 of the present invention for illustrating a typical commercial embodiment.

PARTS LIST

10	gate
15	dielectric
20	photosensitive or charge collection area
22	charge-to-voltage conversion node (or referred to alternatively as diffusion or charge sensing node)
30	substrate/semiconductor
32	heavily doped diffusion
40	semiconductor/dielectric interface
42	semiconductor/dielectric interface
50	path or gate controlled charge transfer channel
52	potential extremium or collection potential
54	charge-to-transfer potential transition or collection-to-transfer potential transition
56	gate-associated charge transfer channel or gate channel potential
58	destination potential
70	pixels
75	image sensor
80	on-chip circuitry or generation source
90	off-chip or external circuitry
200	camera

CLAIMS:

1. A method for lowering dark current in an image sensor pixel, the method comprising the steps of:

(a) providing a photosensitive area for receiving incident light which is converted into a charge; and

(b) providing a gate for transferring charge from the photosensitive area; wherein the gate is held at a voltage which will accumulate majority carriers at a semiconductor-dielectric interface associated with the gate during integration for the photosensitive area.

2. The method as a claim 1 for comprising the step of providing a charge-to-voltage conversion node that receives the charge from the photosensitive area.

3. The method as a claim 1, wherein step (b) comprises providing an on-chip generation source for generating the voltage.

4. The method as a claim 1, wherein step (b) comprises providing an external voltage source for generating the voltage.

5. The method as a claim 1 further comprising the step of providing a gate channel potential so that charge generated at a surface adjacent the gate is directed away from the photosensitive area.

6. The method as a claim 1 for comprising the step of providing a negative voltage as the voltage that will accumulate carriers at a semiconductor-dielectric interface.

7. The step as a claim 1 further comprising the step of providing silicon as the semiconductor and silicon dioxide as the dielectric.

8. A method for lowering dark current in an image sensor pixel, the method comprising the steps of:

(a) providing a substrate;

(b) providing a photosensitive area in the substrate for receiving incident light that is converted into a charge; and

(c) providing a gate for transferring charge from the photosensitive area; wherein step (a) includes providing the substrate substantially adjacent the gate with an impurity concentration that transfers dark current away from the photosensitive area and into a diffusion on an opposite side from the photosensitive area during integration for the photosensitive area.

9. An image sensor pixel that substantially eliminates dark current, the sensor comprising:

(a) a photosensitive area for receiving incident light that is converted into a charge; and

(b) a gate for transferring charge from the photosensitive area; wherein the gate, when at a predetermined voltage, will accumulate majority carriers substantially at a semiconductor-dielectric interface associated with the gate during integration for the photosensitive area.

10. The image sensor as in claim 9 further comprising a charge-to-voltage conversion node that receives the charge from the photosensitive area.

11. The image sensor as in claim 9, further comprising an on-chip generation source for generating the voltage as the predetermined voltage.

12. The image sensor as in claim 9 further comprising an external voltage source for generating the voltage.

13. The image sensor as in claim 9, wherein the predetermined voltage is a negative voltage that will accumulate carriers at a semiconductor-dielectric interface.

14. The image sensor as in claim 9, wherein silicon is provided as the semiconductor and silicon dioxide is provided as the dielectric.

15. An image sensor pixel comprising:

(a) a substrate;

(b) a photosensitive area in the substrate for receiving incident light that is converted into a charge; and

(c) a gate for transferring charge from the photosensitive area; wherein the substrate substantially adjacent the gate includes an impurity concentration that transfers dark current away from the photosensitive area and into a diffusion on an opposite side from the photosensitive area during integration for the photosensitive area.

16. A camera comprising:

an image sensor pixel that substantially eliminates dark current, the sensor comprising:

(a) a photosensitive area for receiving incident light that is converted into a charge; and

(b) a gate for transferring charge from the photosensitive area; wherein the gate, when at a predetermined voltage, will accumulate majority carriers substantially at a semiconductor-dielectric interface during integration for the photosensitive area.

17. The camera as in claim 16 further comprising a charge-to-voltage conversion node that receives the charge from the photosensitive area.

18. The camera as in claim 16, further comprising an on-chip generation source for generating the voltage as the predetermined voltage.

19. The camera as in claim 16 further comprising an external voltage source for generating the voltage.

20. The camera as in claim 16, wherein the predetermined voltage is a negative voltage that will accumulate carriers at a semiconductor-dielectric interface.

21. The camera as in claim 16, wherein silicon is provided as the semiconductor and silicon dioxide is provided as the dielectric.

22. An image sensor pixel comprising:

(a) a substrate;

(b) a photosensitive area in the substrate for receiving incident light that is converted into a charge; and

(c) a gate for transferring charge from the photosensitive area; wherein the substrate substantially adjacent the gate includes an impurity concentration that transfers dark current away from the photosensitive area and into a diffusion on an opposite side from the photosensitive area during integration for the photosensitive area.

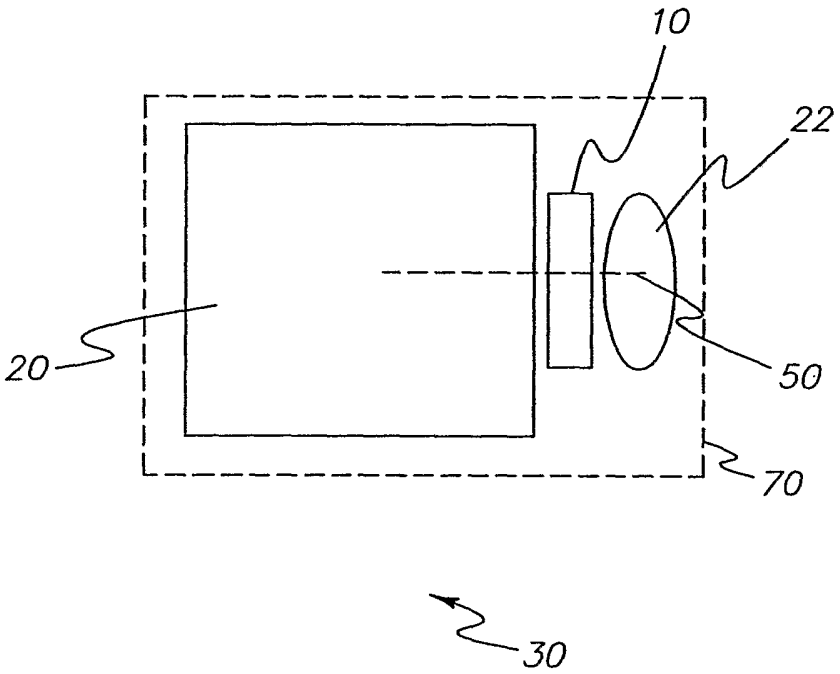


FIG. 1

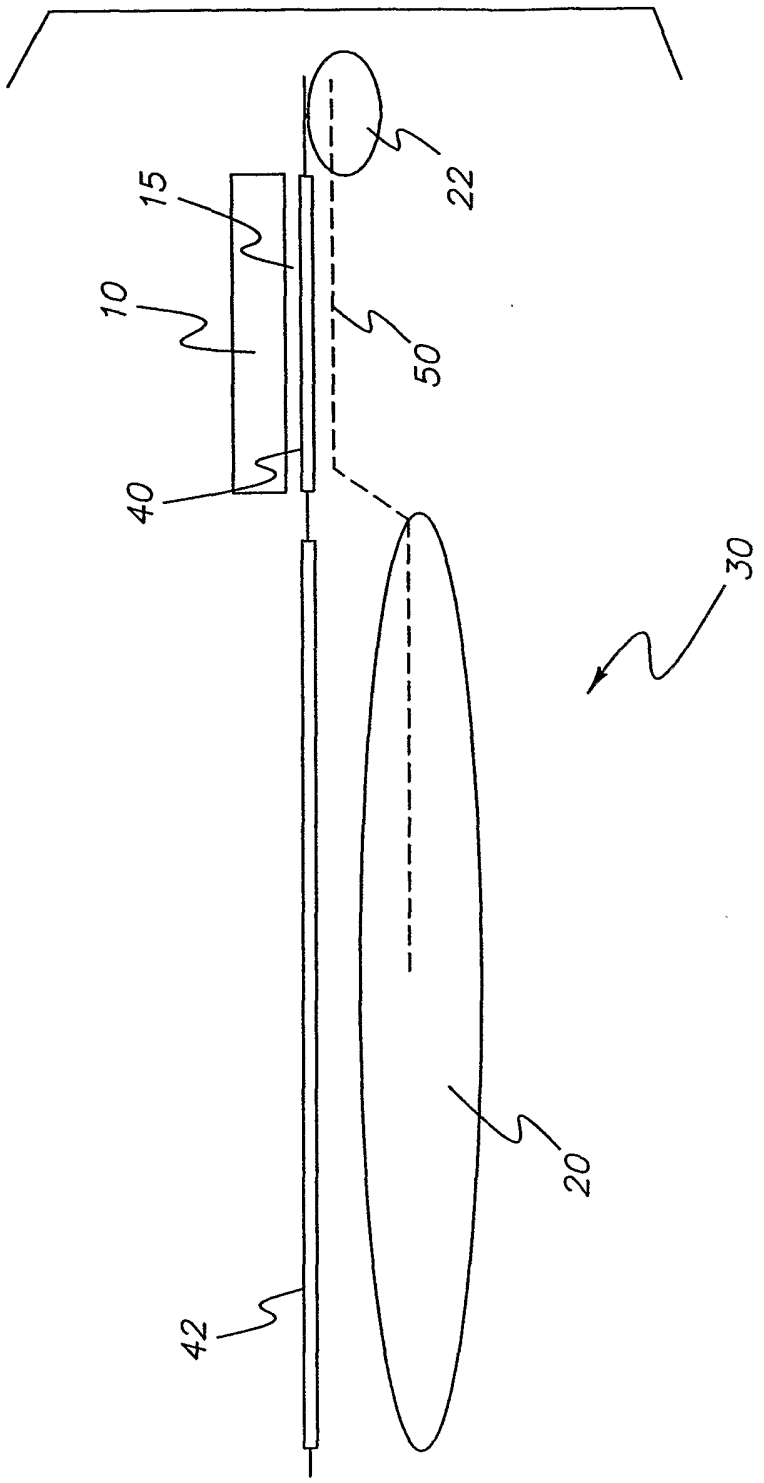


FIG. 2

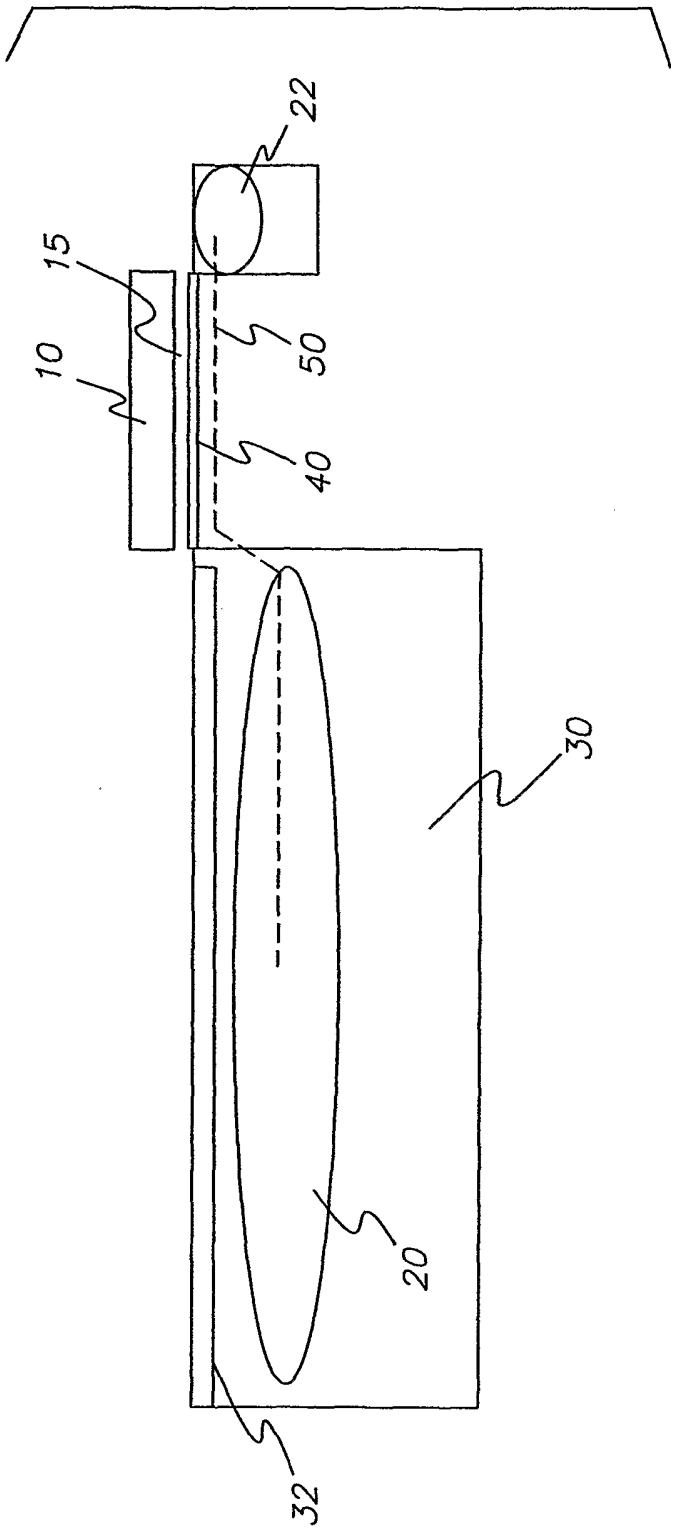


FIG. 3

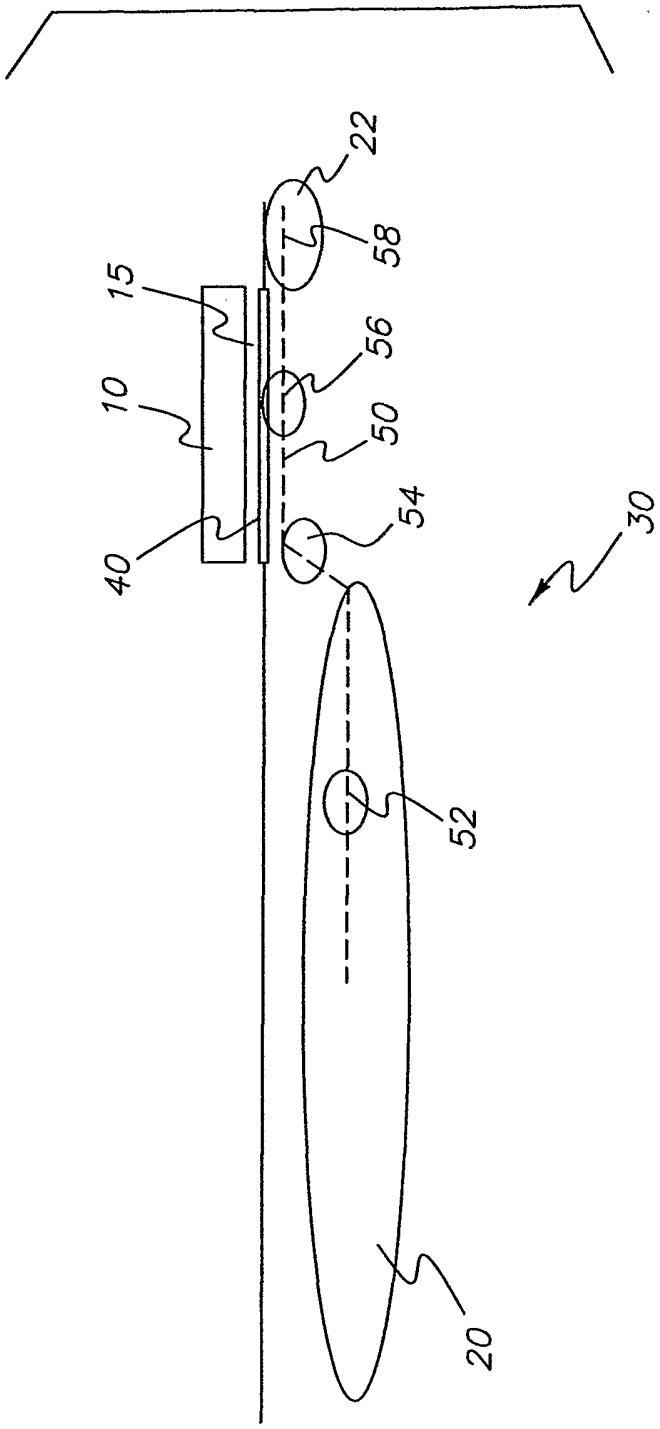


FIG. 4

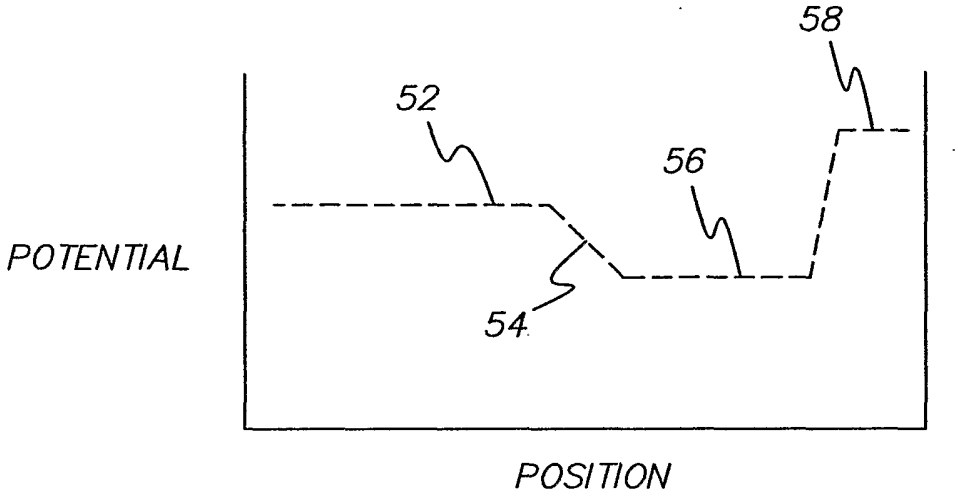

58
52
56
POTENTIAL
54
POSITION

FIG. 5A

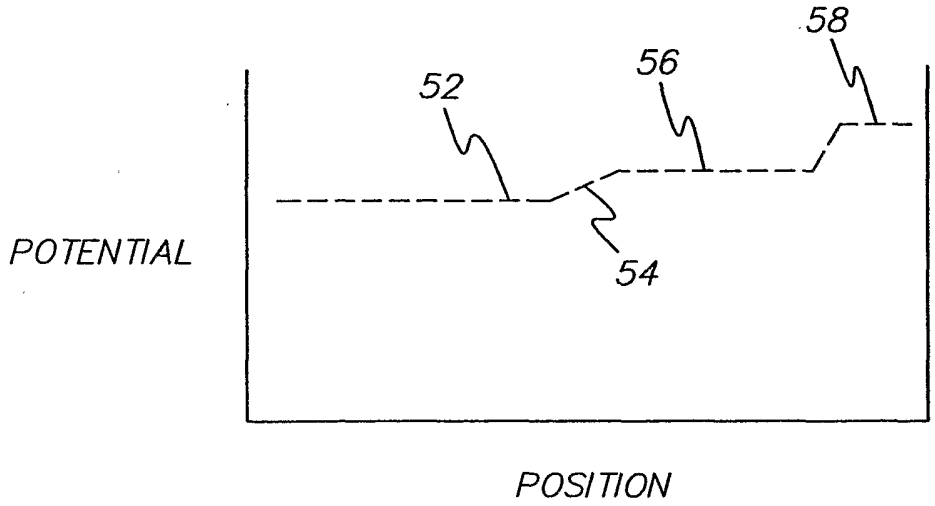

58
56
52
POTENTIAL
54
POSITION

FIG. 5B

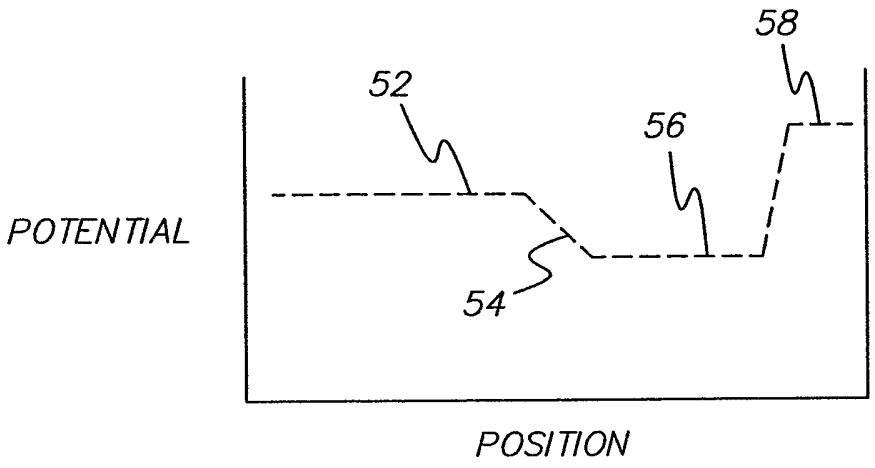

58
52
56
POTENTIAL
54
POSITION

FIG. 5C

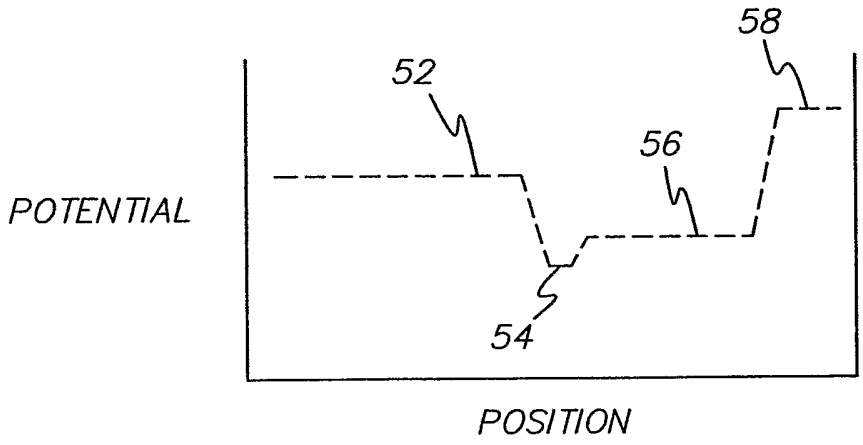

58
52
56
POTENTIAL
54
POSITION

FIG. 5D

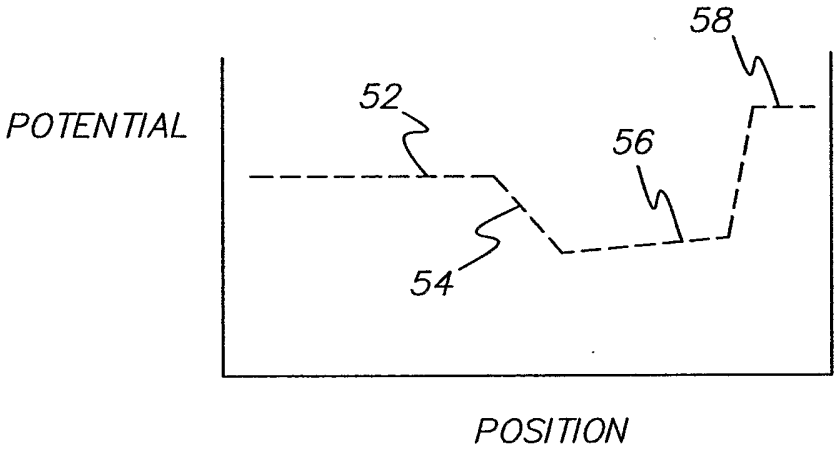


FIG. 5E

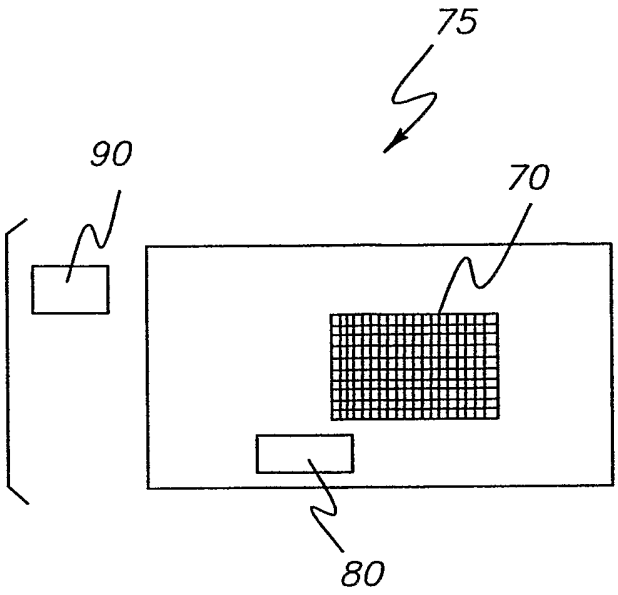


FIG. 6

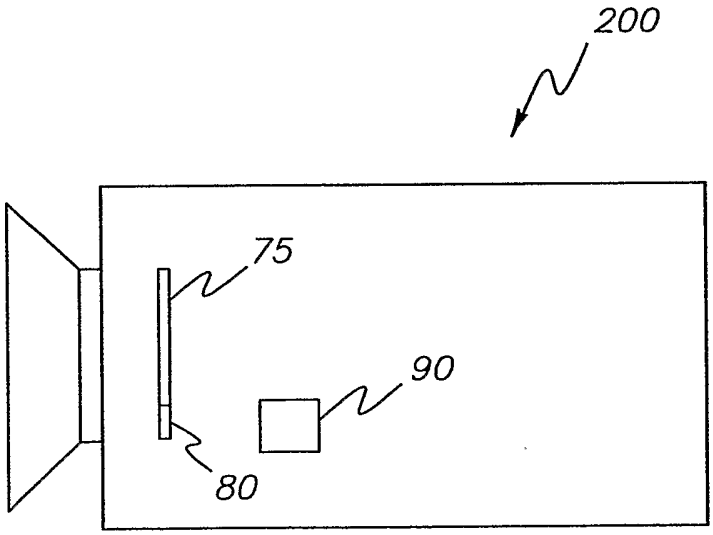


FIG. 7