United States Patent [19]

Grazebrook

[11] **3,865,368**

[45] **Feb. 11, 1975**

[54] **GAMING MACHINES GAMES OF SKILL**

[76] Inventor: **Robert Francis Needs Grazebrook,** Farm Cottage, Colinswood Rd. Farnham Common, Slough, England

[22] Filed: **Feb. 21, 1974**

[21] Appl. No.: **444,490**

[52] **U.S. Cl.** ..... **273/1 E,** 35/22 R, 273/138 A

[51] **Int. Cl.** **A63f 9/00**

[58] **Field of Search** ..... 273/1 R, 1 E, 138 A; 35/22 R

[56] **References Cited**

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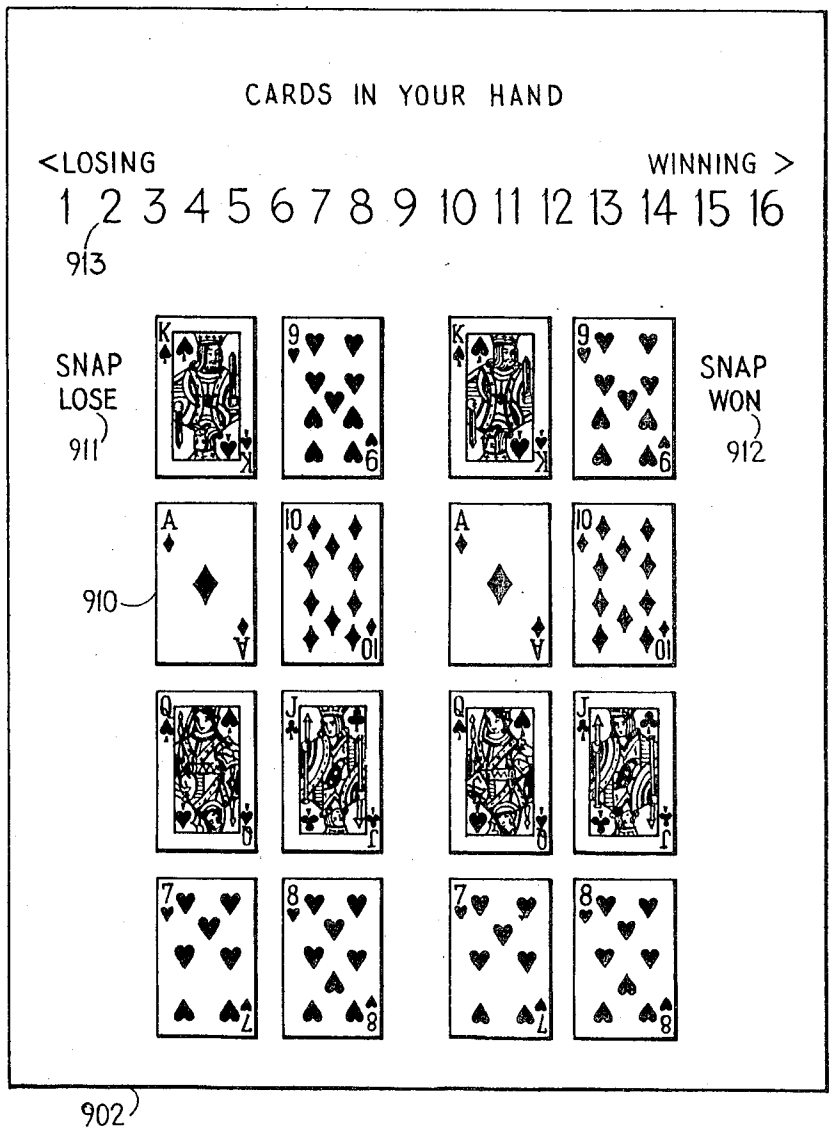
Primary Examiner—Paul E. Shapiro

Attorney, Agent, or Firm—Lawrence E. Laubscher

[57] **ABSTRACT**

The invention provides a machine which simulates the game of snap. Two symbols representing the cards thrown by the two players are displayed at random from two groups of symbols. The snap call which is given when the two symbols displayed are the same is simulated by the player pressing a button. In the case of the player playing the machine the machine snap signal is controlled by a variable time delay circuit, and in the case of the player playing a second player the second players snap signal is controlled by the second player pressing a second button. The machine determines the first to call snap and effectively transfers cards to the winner. The machine may be provided with a prize or token dispenser, or may give free games in a coin controlled embodiment.

8 Claims, 32 Drawing Figures



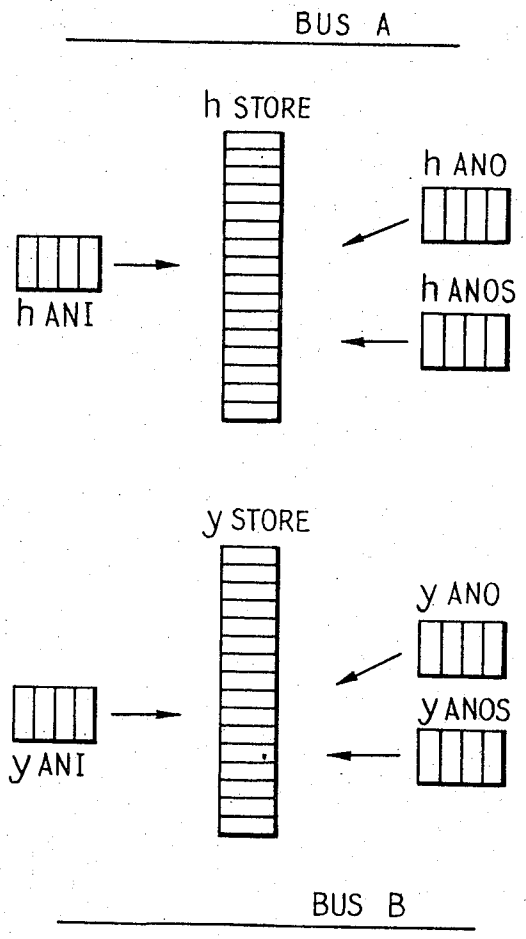


FIG. 1

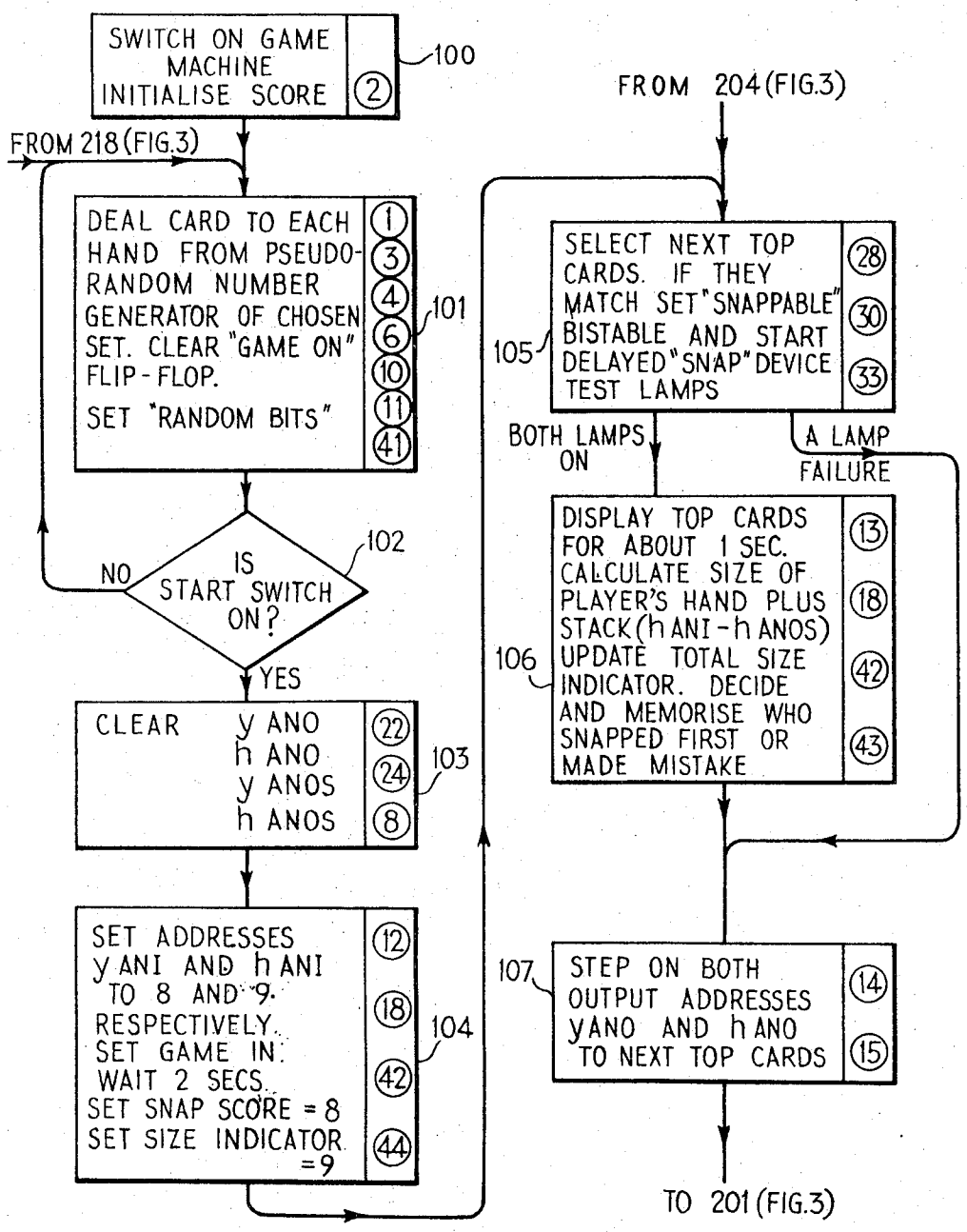

SWITCH ON GAME MACHINE INITIALISE SCORE
2
100
FROM 218 (FIG.3)
DEAL CARD TO EACH HAND FROM PSEUDO-RANDOM NUMBER GENERATOR OF CHOSEN SET. CLEAR "GAME ON" FLIP-FLOP.
SET "RANDOM BITS"
1
3
4
6
10
11
41
101
IS START SWITCH ON?
102
NO
YES
CLEAR y ANO h ANO y ANOS h ANOS
22
24
8
103
SET ADDRESSES y ANI AND h ANI TO 8 AND 9 RESPECTIVELY. SET GAME IN. WAIT 2 SECS. SET SNAP SCORE = 8 SET SIZE INDICATOR =9
12
18
42
44
104
FROM 204 (FIG.3)
SELECT NEXT TOP CARDS. IF THEY MATCH SET "SNAPPABLE" BISTABLE AND START DELAYED "SNAP" DEVICE TEST LAMPS
28
30
33
105
BOTH LAMPS ON
A LAMP FAILURE
DISPLAY TOP CARDS FOR ABOUT 1 SEC. CALCULATE SIZE OF PLAYER'S HAND PLUS STACK (h ANI - h ANOS) UPDATE TOTAL SIZE INDICATOR. DECIDE AND MEMORISE WHO SNAPPED FIRST OR MADE MISTAKE
13
18
42
43
106
STEP ON BOTH OUTPUT ADDRESSES y ANO AND h ANO TO NEXT TOP CARDS
14
15
107
TO 201 (FIG.3)

FIG. 2

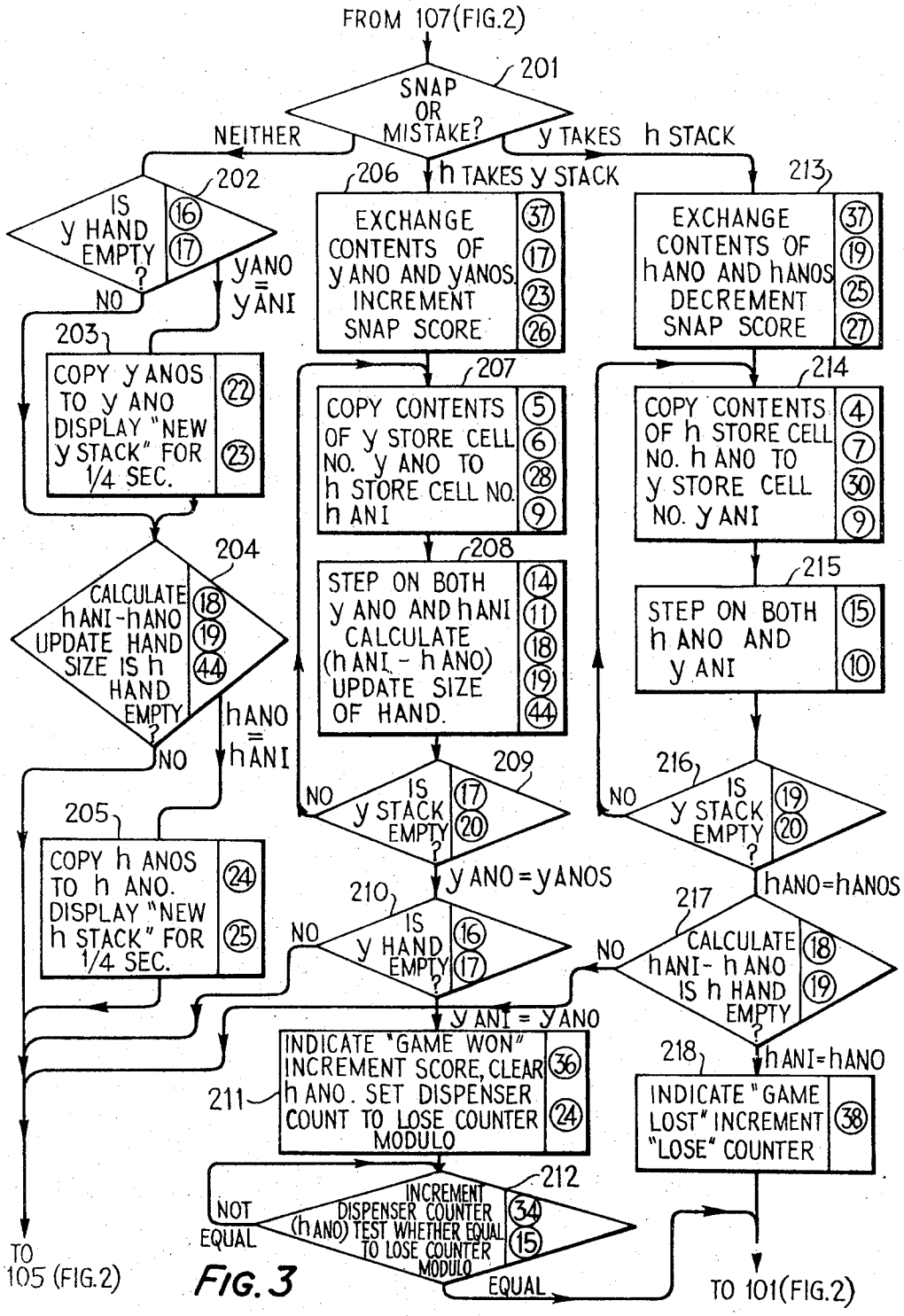

FROM 107(FIG.2)
201
SNAP OR MISTAKE?
NEITHER
y TAKES h STACK
h TAKES y STACK
202
IS y HAND EMPTY ? 16 17
NO
yANO = yANI
203
COPY yANOS TO y ANO DISPLAY "NEW y STACK" FOR 1/4 SEC. 22 23
204
CALCULATE hANI-hANO UPDATE HAND SIZE IS h HAND EMPTY ? 18 19 44
NO
hANO = hANI
205
COPY h ANOS TO h ANO. DISPLAY "NEW h STACK" FOR 1/4 SEC. 24 25
206
EXCHANGE CONTENTS OF y ANO AND yANOS INCREMENT SNAP SCORE 37 17 23 26
207
COPY CONTENTS OF y STORE CELL NO. y ANO TO h STORE CELL NO. h ANI 5 6 28 9
208
STEP ON BOTH y ANO AND hANI CALCULATE (hANI - h ANO) UPDATE SIZE OF HAND. 14 11 18 19 44
209
NO
IS y STACK EMPTY ? 17 20
y ANO = yANOS
210
NO
IS y HAND EMPTY ? 16 17
y ANI = yANO
211
INDICATE "GAME WON" INCREMENT SCORE, CLEAR h ANO. SET DISPENSER COUNT TO LOSE COUNTER MODULO 36 24
212
INCREMENT DISPENSER COUNTER (hANO) TEST WHETHER EQUAL TO LOSE COUNTER MODULO 34 15
NOT EQUAL
EQUAL
TO 105 (FIG.2)
213
EXCHANGE CONTENTS OF hANO AND hANOS DECREMENT SNAP SCORE 37 19 25 27
214
COPY CONTENTS OF h STORE CELL NO. h ANO TO y STORE CELL NO. y ANI 4 7 30 9
215
STEP ON BOTH h ANO AND y ANI 15 10
216
NO
IS y STACK EMPTY ? 19 20
hANO = hANOS
217
NO
CALCULATE hANI- h ANO IS h HAND EMPTY ? 18 19
hANI = hANO
218
INDICATE "GAME LOST" INCREMENT "LOSE" COUNTER 38
TO 101(FIG.2)

FIG. 3

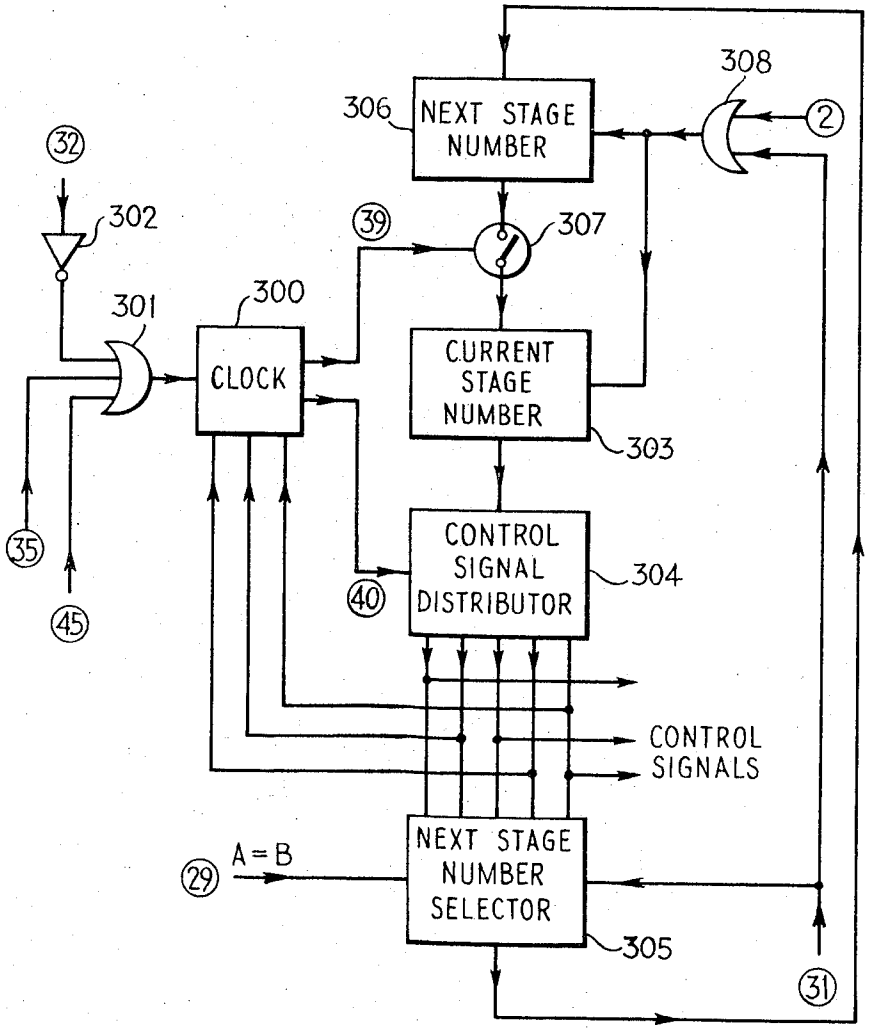

308
306
NEXT STAGE NUMBER
2
32
302
39
307
301
300
CLOCK
CURRENT STAGE NUMBER
303
35
45
40
CONTROL SIGNAL DISTRIBUTOR
304
CONTROL SIGNALS
A=B
29
NEXT STAGE NUMBER SELECTOR
305
31

FIG. 4

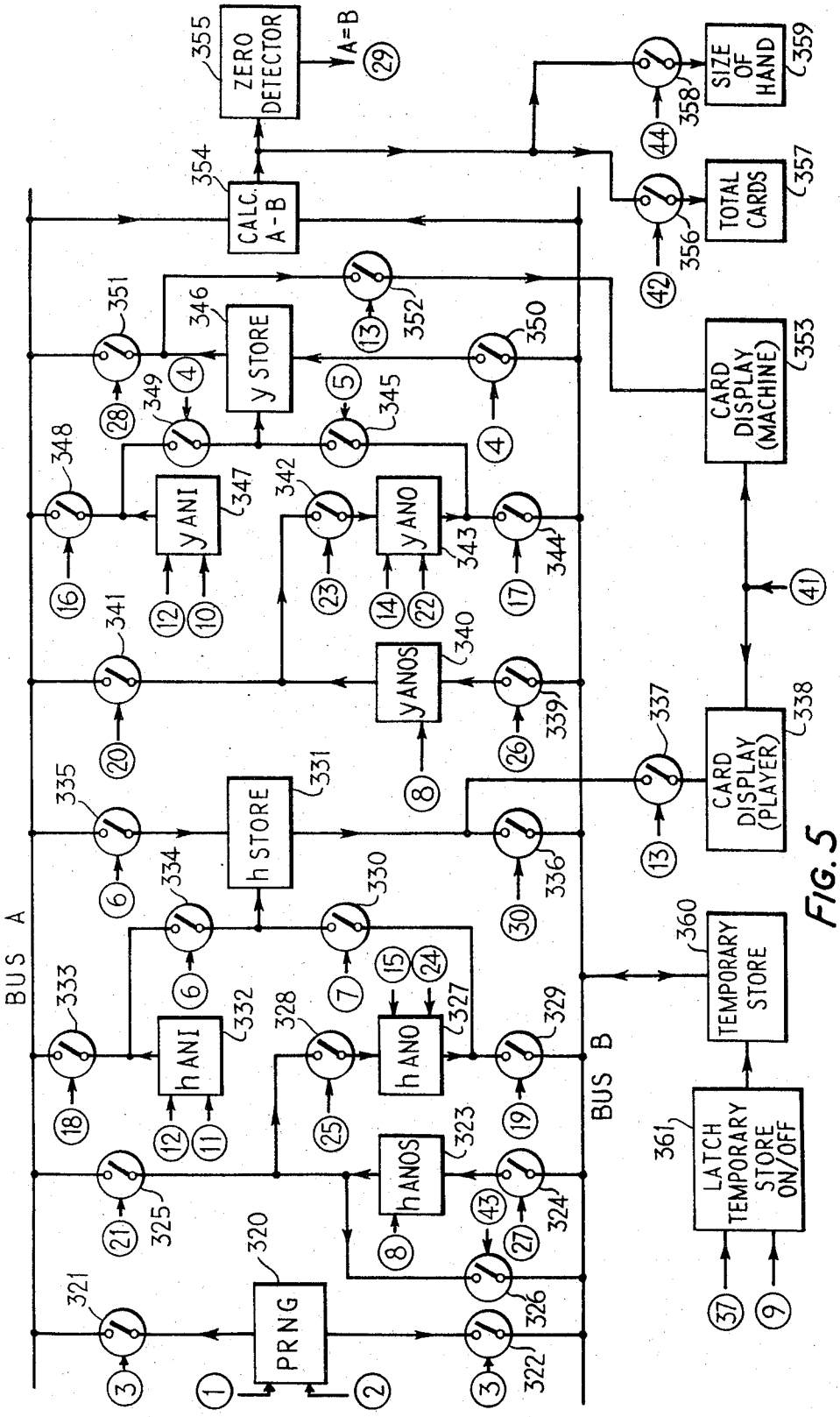

BUS A
BUS B
PRNG
320
321
322
326
h STORE
331
h ANI
332
333
334
h ANO
327
328
329
330
h ANOS
323
324
325
y STORE
346
y ANI
347
348
y ANO
342
343
344
345
y ANOS
340
341
339
CALC. A-B
354
ZERO DETECTOR
355
A=B
29
CARD DISPLAY (MACHINE)
353
CARD DISPLAY (PLAYER)
338
337
TOTAL CARDS
357
SIZE OF HAND
359
TEMPORARY STORE
360
LATCH TEMPORARY STORE ON/OFF
361

FIG. 5

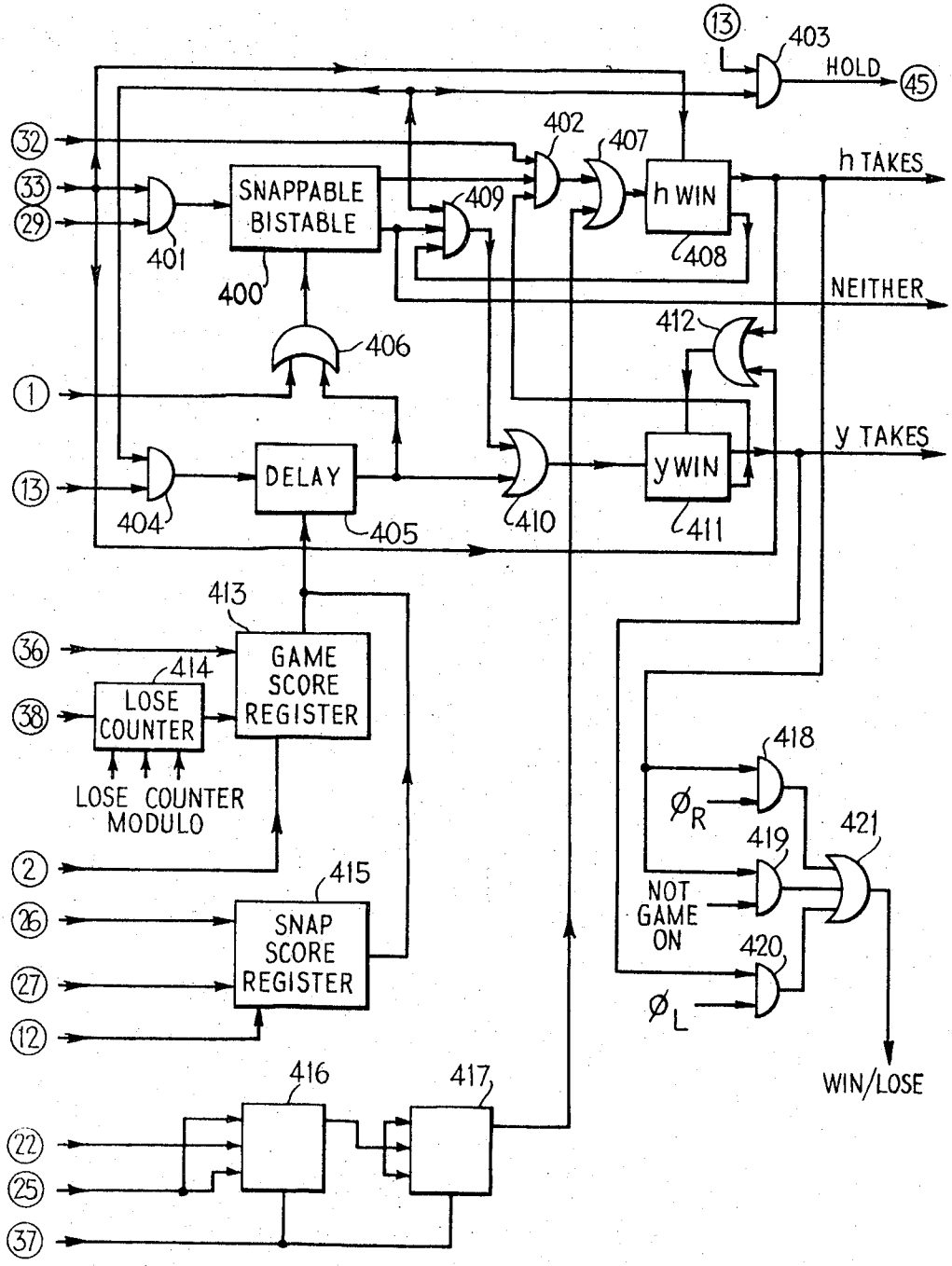

13
403
HOLD
45
32
33
29
401
SNAPPABLE BISTABLE
400
402
407
409
h WIN
408
h TAKES
NEITHER
406
412
1
13
404
DELAY
405
410
y WIN
411
y TAKES
413
36
38
414
LOSE COUNTER
GAME SCORE REGISTER
LOSE COUNTER MODULO
2
26
27
12
415
SNAP SCORE REGISTER
418
ϕ_R
419
NOT GAME ON
420
ϕ_L
421
WIN/LOSE
416
417
22
25
37

FIG. 6

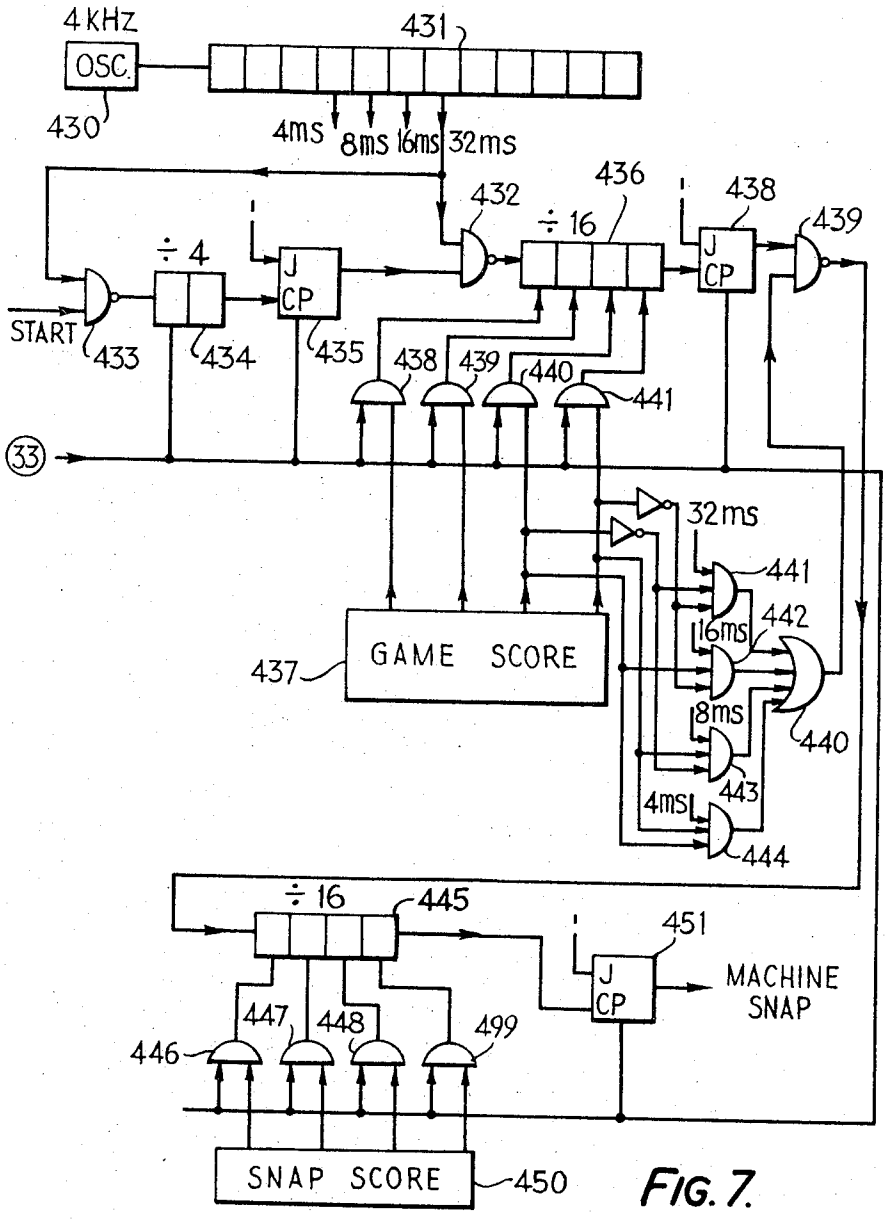

4 KHz
OSC.
430
431
4ms
8ms
16ms
32ms
÷ 4
÷ 16
J
CP
START
433
434
435
436
438
439
440
441
432
(33)
32ms
442
GAME SCORE
437
443
444
÷ 16
445
451
MACHINE SNAP
446
447
448
499
SNAP SCORE
450

FIG. 7.

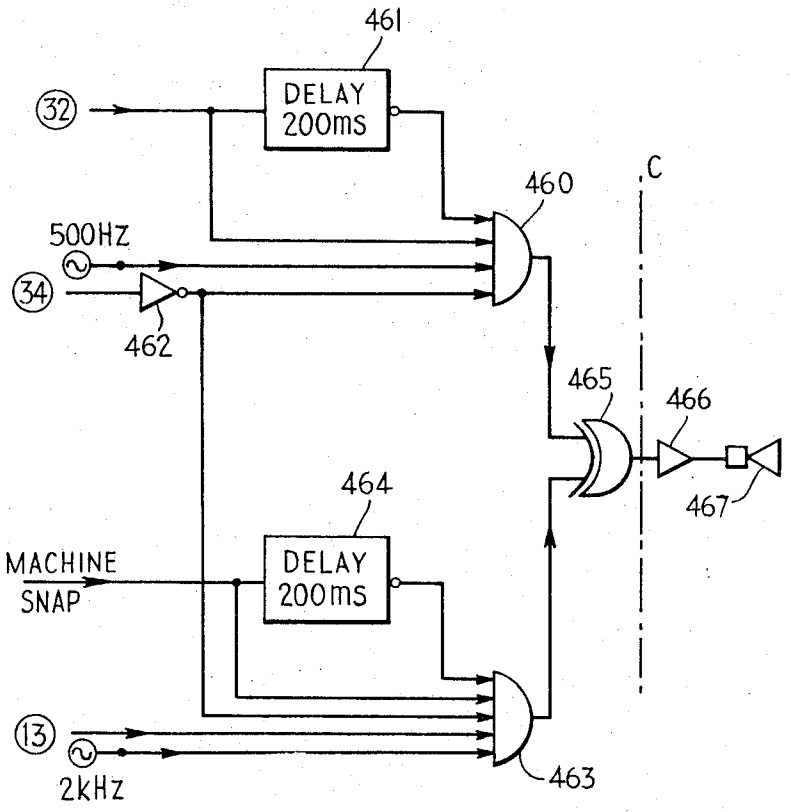

461
DELAY
200ms
32
500HZ
34
462
460
C
465
466
467
464
MACHINE
SNAP
DELAY
200ms
13
2kHz
463

FIG. 8

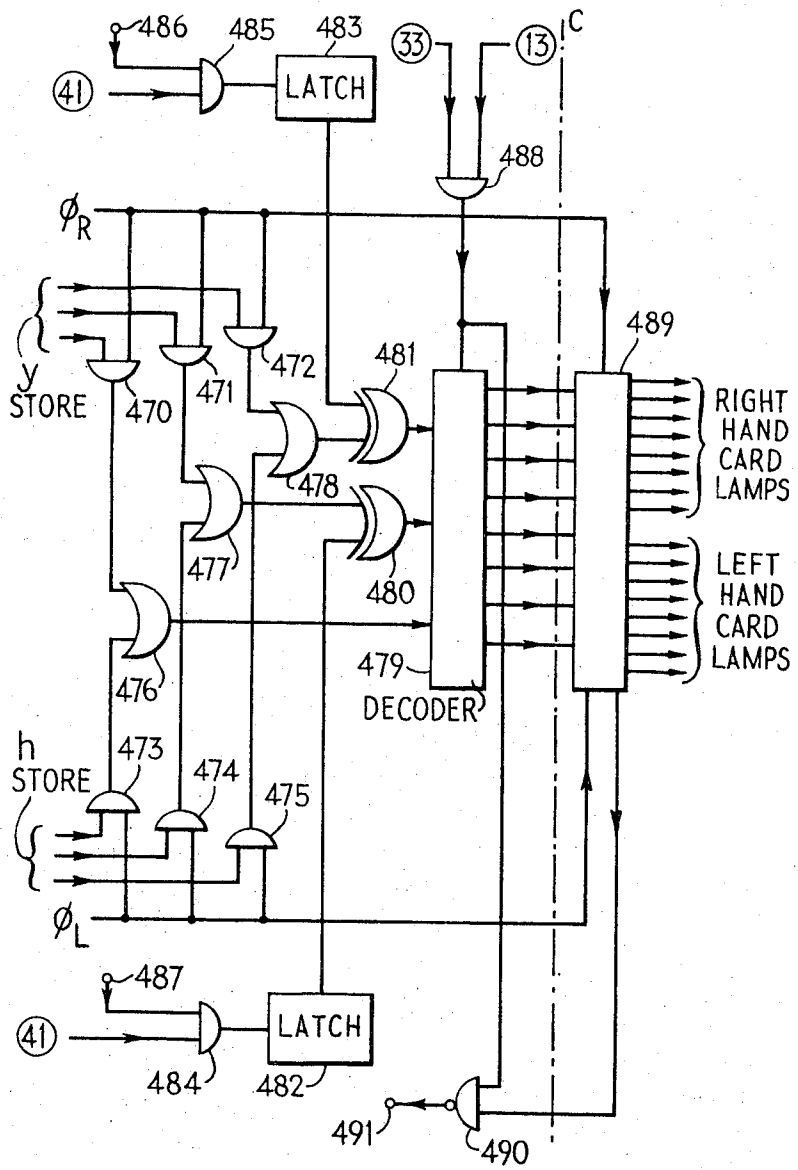

486
485
483
LATCH
41
33
13
C
488
ϕ_R
489
y
STORE
470
471
472
481
478
477
480
476
479
DECODER
RIGHT HAND CARD LAMPS
LEFT HAND CARD LAMPS
h
STORE
473
474
475
ϕ_L
487
41
LATCH
484
482
491
490

FIG. 9

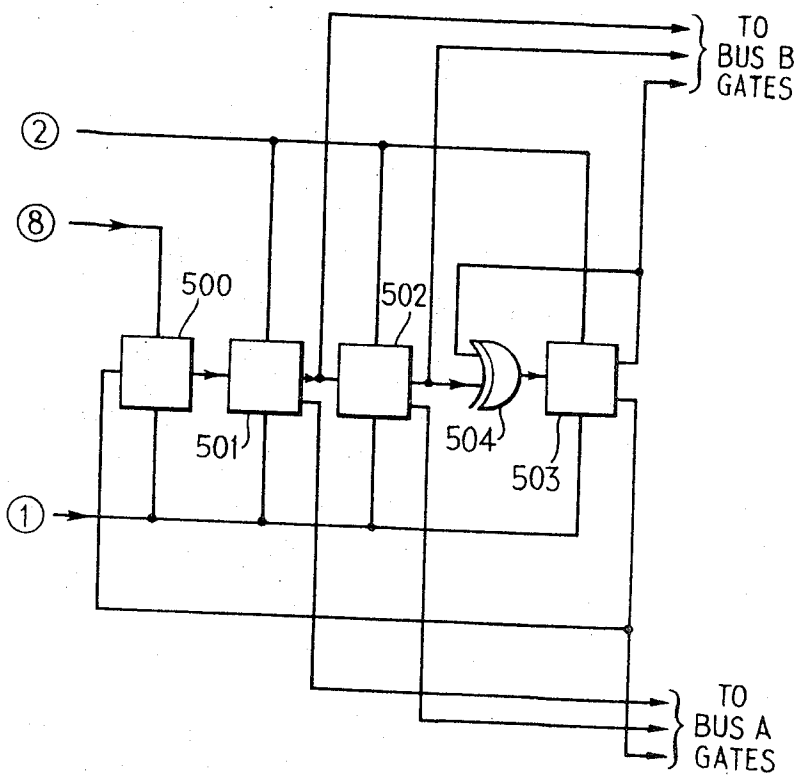


FIG. 10

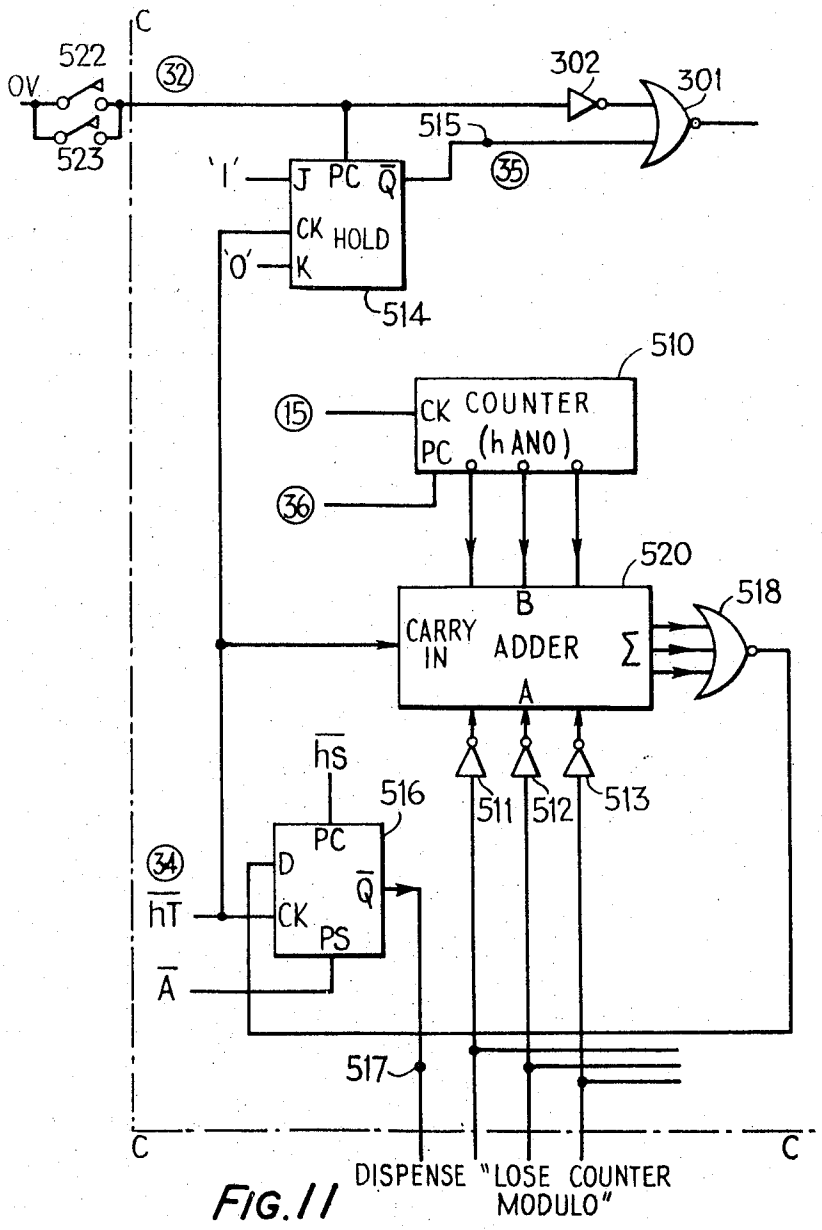

C
522
OV
32
523
302
301
515
35
'1'
J PC Q
CK HOLD
'0'
K
514
510
15
CK COUNTER
PC (h ANO)
36
520
B
CARRY IN
ADDER
Σ
A
518
hS
516
511
512
513
PC
34
D
hT
CK
Q
PS
A
517
C
C
DISPENSE "LOSE COUNTER MODULO"

FIG. 11

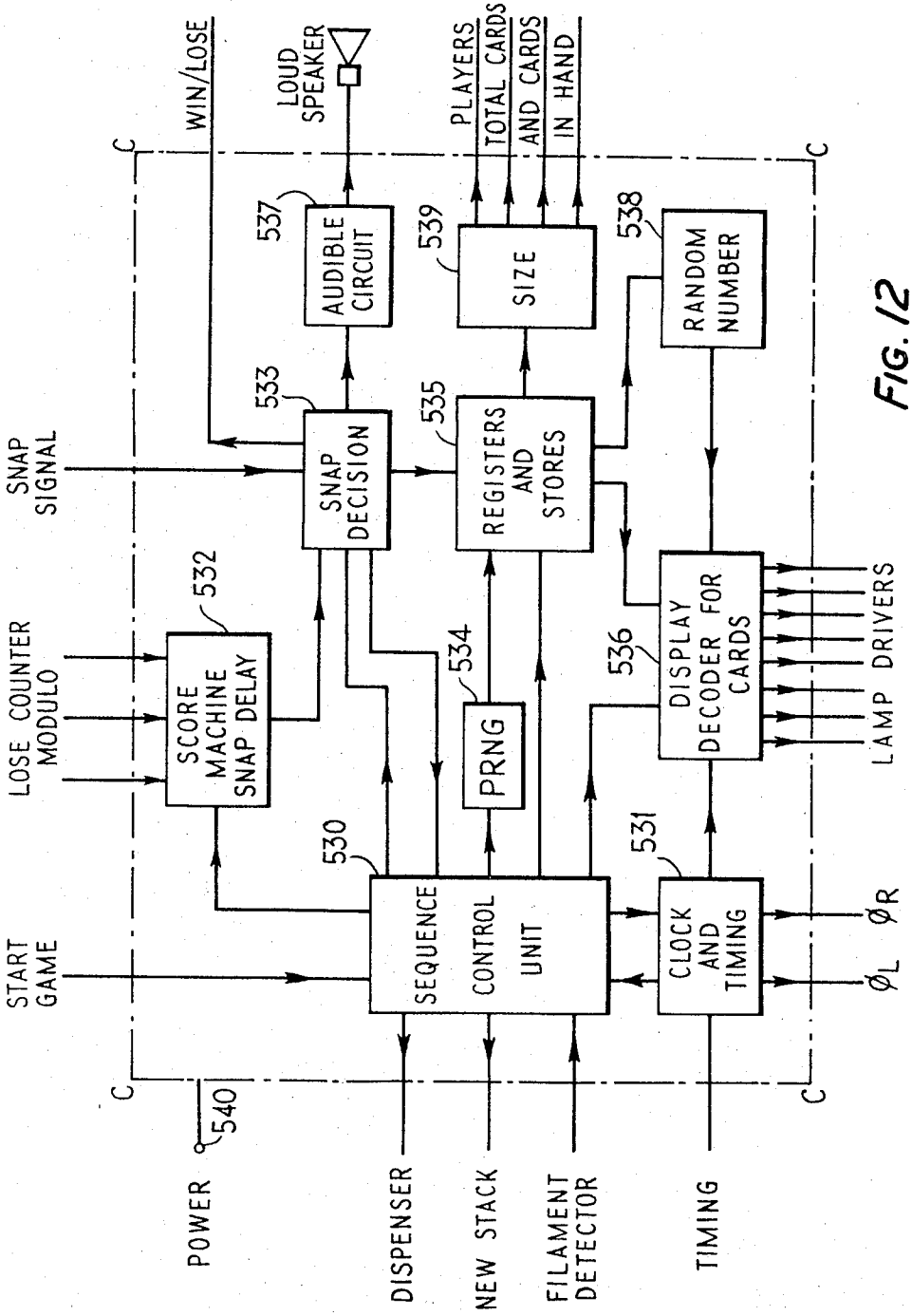

WIN/LOSE
LOUD SPEAKER
PLAYERS
TOTAL CARDS AND CARDS IN HAND
537
AUDIBLE CIRCUIT
539
SIZE
538
RANDOM NUMBER
533
SNAP DECISION
535
REGISTERS AND STORES
SNAP SIGNAL
LOSE COUNTER MODULO
532
SCORE MACHINE SNAP DELAY
534
PRNG
536
DISPLAY DECODER FOR CARDS
LAMP DRIVERS
530
SEQUENCE CONTROL UNIT
531
CLOCK AND TIMING
START GAME
ϕ_R
ϕ_L
C
C
C
C
540
POWER
DISPENSER
NEW STACK
FILAMENT DETECTOR
TIMING

FIG. 12

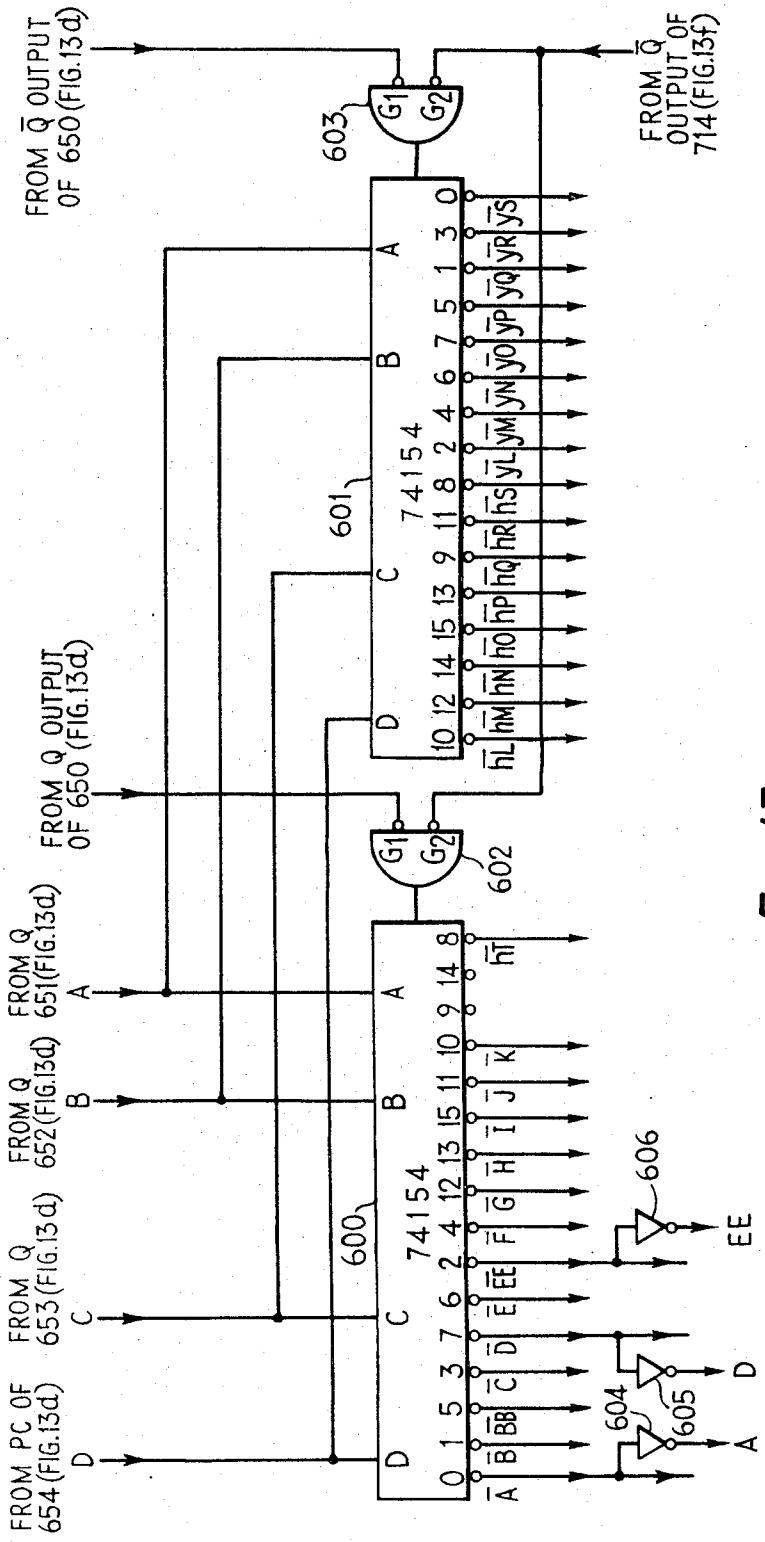

FROM $\bar{Q}$ OUTPUT OF 650 (FIG.13d)
603
FROM $\bar{Q}$ OUTPUT OF 714 (FIG.13f)
FROM Q OUTPUT OF 650 (FIG.13d)
601
FROM Q 651 (FIG.13d)
602
FROM Q 652 (FIG.13d)
FROM Q 653 (FIG.13d)
600
606
EE
FROM PC OF 654 (FIG.13d)
604
605
D
A

FIG. 13a

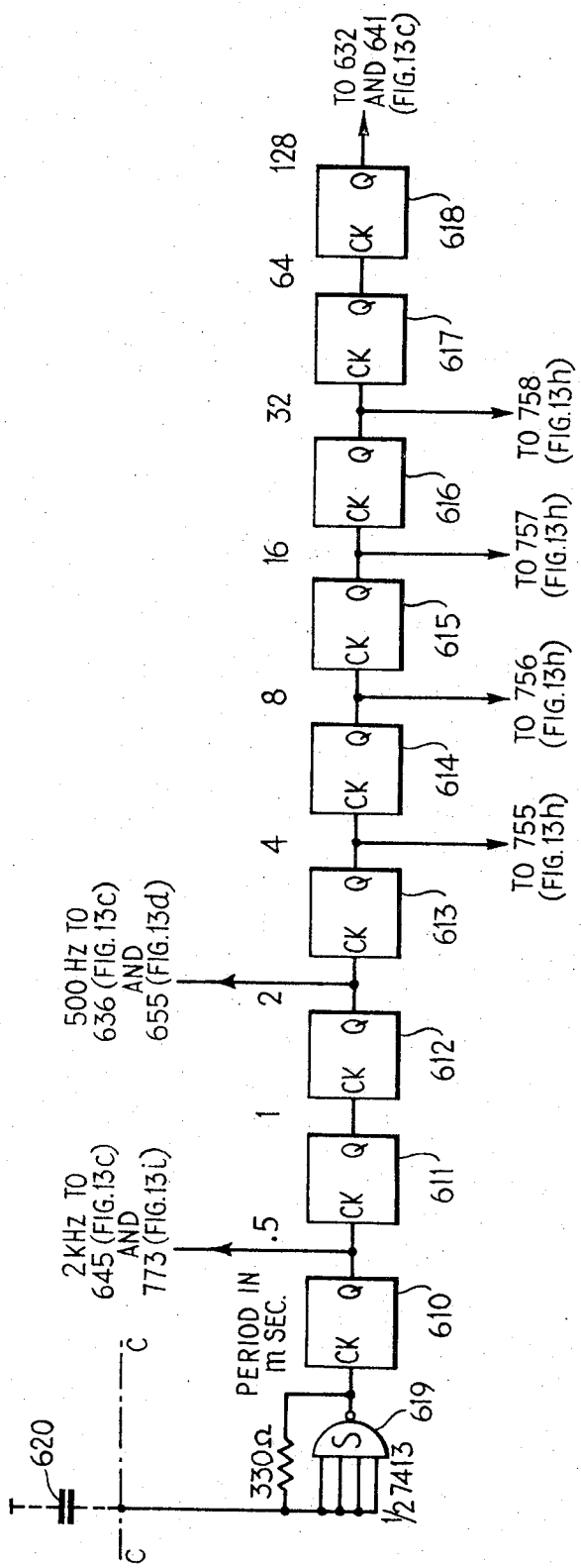

620
330Ω
½ 7413
619
PERIOD IN m SEC.
2KHz TO 645 (FIG.13c) AND 773 (FIG.13i)
500 Hz TO 636 (FIG.13c) AND 655 (FIG.13d)
.5
1
2
4
8
16
32
64
128
610
611
612
613
614
615
616
617
618
CK
Q
TO 632 AND 641 (FIG.13c)
TO 758 (FIG.13h)
TO 757 (FIG.13h)
TO 756 (FIG.13h)
TO 755 (FIG.13h)

FIG. 13b

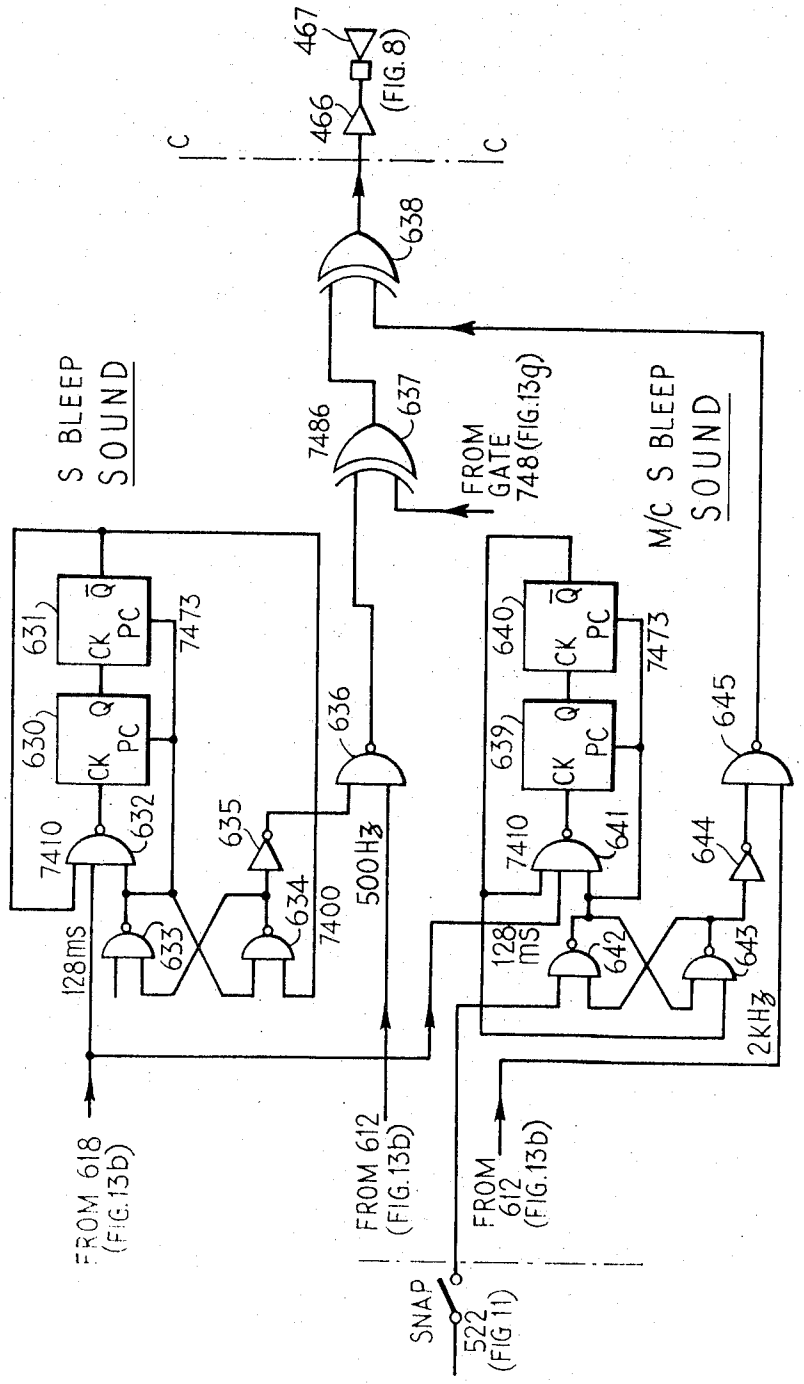

467
(FIG. 8)
466
C
C
638
7486
637
FROM GATE 748 (FIG. 13g)
S BLEEP SOUND
M/C S BLEEP SOUND
631
630
632
7410
633
128ms
635
634
7400
636
500Hz
640
639
641
644
642
643
645
2KHz
7473
FROM 618 (FIG. 13b)
FROM 612 (FIG. 13b)
FROM 612 (FIG. 13b)
SNAP
522 (FIG 11)

FIG. 13c

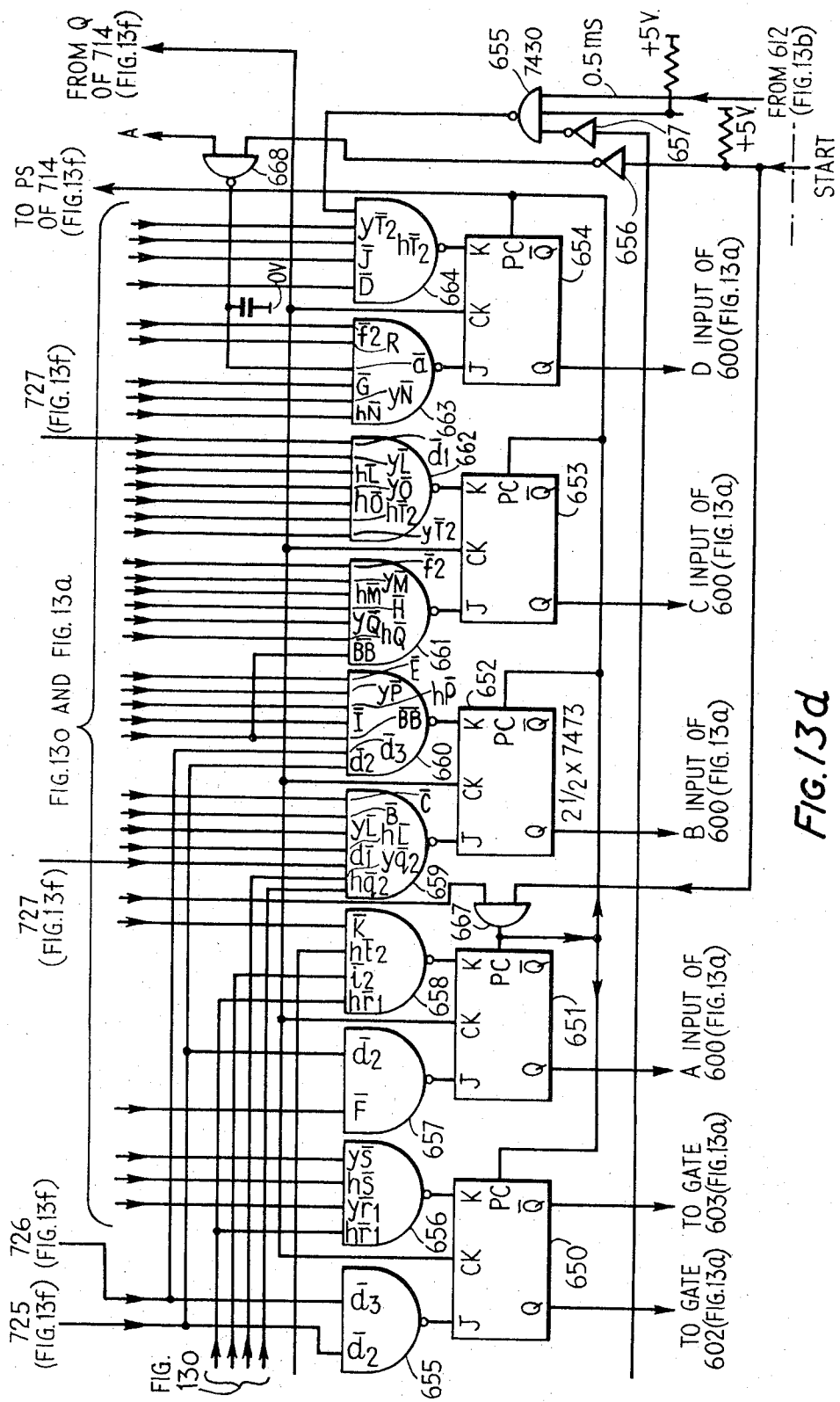

FROM Q OF 714 (FIG.13f)
TO PS OF 714 (FIG.13f)
727 (FIG.13f)
FIG.13a AND FIG.13a
727 (FIG.13f)
726 (FIG.13f)
725 (FIG.13f)
FIG. 130
655 7430
0.5 ms
+5V
FROM 612 (FIG.13b)
START
656
657
668
667
654
653
652
651
650
D INPUT OF 600(FIG.13a)
C INPUT OF 600(FIG.13a)
B INPUT OF 600(FIG.13a)
A INPUT OF 600(FIG.13a)
TO GATE 603(FIG.13a)
TO GATE 602(FIG.13a)
2½ x 7473

FIG. 13d

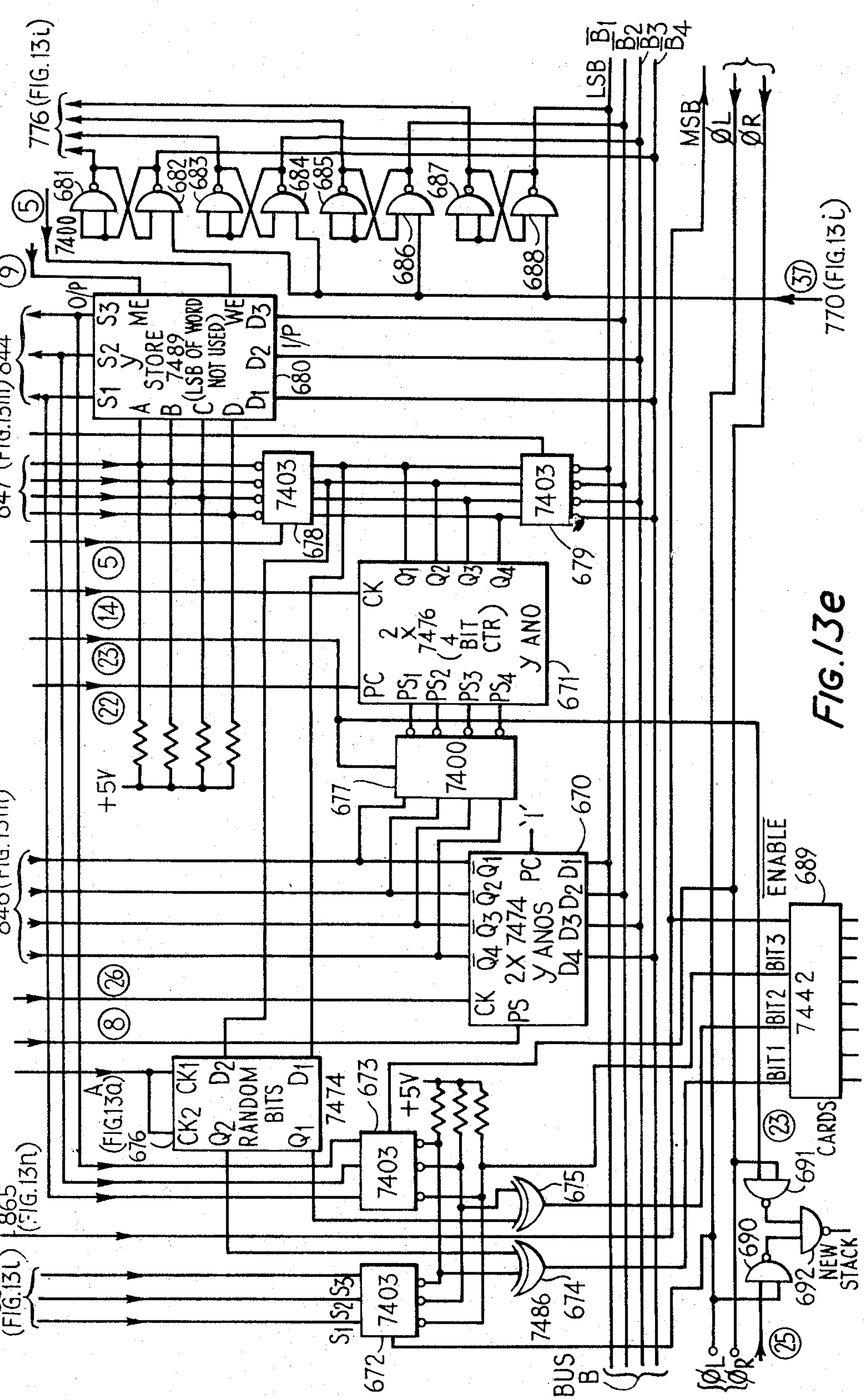

776 (FIG.13L)
LSB
$\overline{B_1}$
$\overline{B_2}$
$\overline{B_3}$
$\overline{B_4}$
MSB
ØL
ØR
7400
681
682
683
684
685
686
687
688
770 (FIG.13L)
O/P
S1 S2 S3
A STORE ME
B 7489
C (LSB OF WORD NOT USED)
D
D1 D2 D3
WE
I/P
680
844 (FIG.13m)
847 (FIG.13m)
7403
678
679
CK
Q1 Q2 Q3 Q4
2 X 7476 (4 BIT CTR) Y AND
PC
PS1 PS2 PS3 PS4
671
+5V
7400
677
846 (FIG.13m)
Q̄4 Q̄3 Q̄2 Q̄1
2X 7474 Y ANDS
D4 D3 D2 D1
PS
PC
'1'
670
ENABLE
BIT1 BIT2 BIT3
7442
689
CARDS
CK2 CK1
Q2 RANDOM BITS D2
Q1 D1
7474
676
A (FIG.13Q)
673
675
865 (FIG.13n)
830 (FIG.13L)
S1 S2 S3
672
7486
674
691
690
692
NEW STACK
BUS B

FIG. 13e

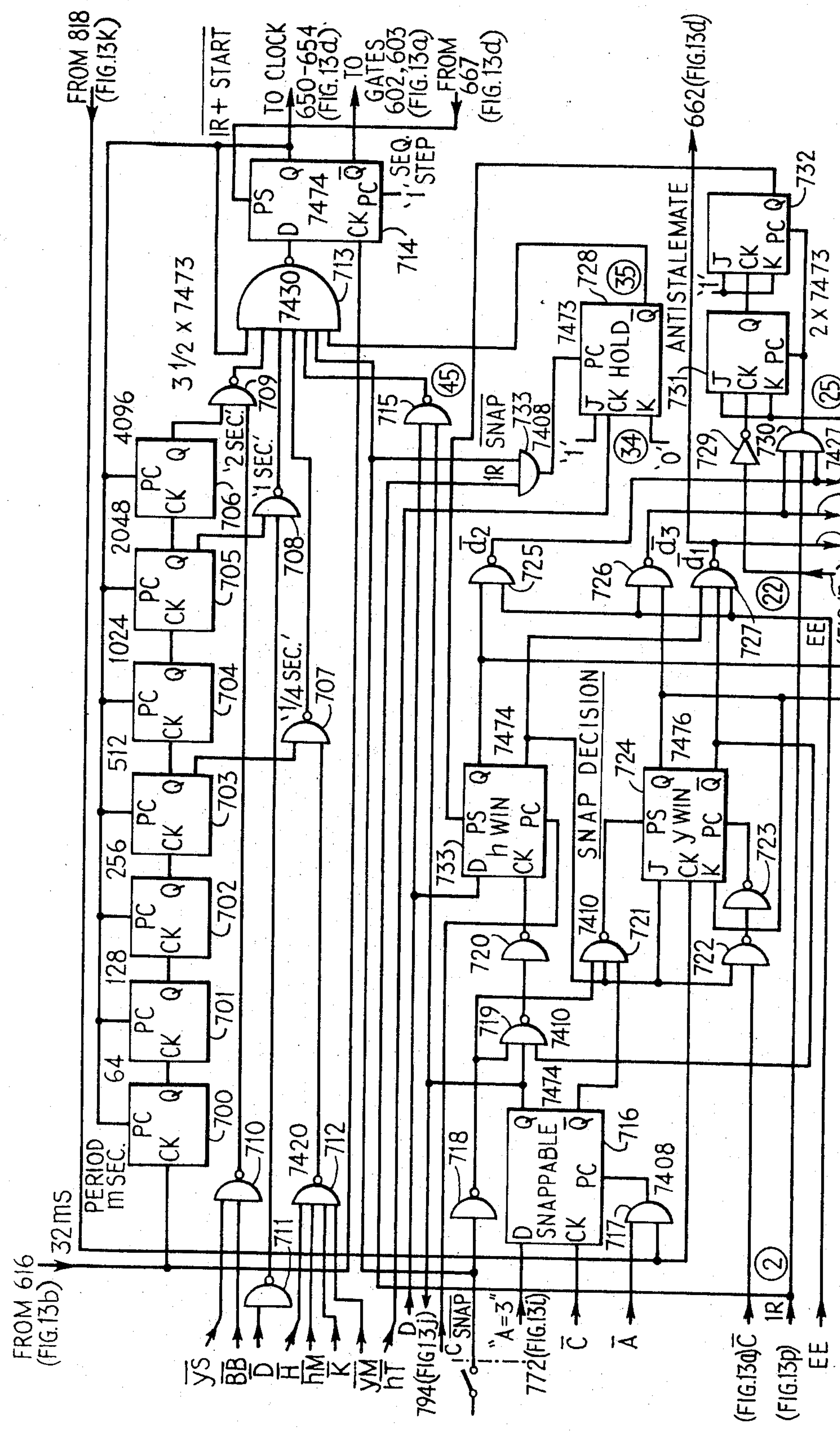

FROM 818 (FIG.13k)
IR + START
TO CLOCK 650-654 (FIG.13d)
TO GATES 602,603 (FIG.13a)
FROM 667 (FIG.13d)
662 (FIG.13d)
PS D Q 7474 Q̄ CK PC
'1' SEQ. '1' STEP
7430
3 1/2 x 7473
4096
2048
1024
512
256
128
64
PERIOD mSEC.
'2 SEC.'
'1 SEC.'
'1/4 SEC.'
7420
SNAP
7408
7473 PC J CK HOLD Q K
ANTISTALEMATE
2 x 7473
SNAP DECISION
h WIN
y WIN
7474
7476
7410
SNAPPABLE
784 (FIG.13l)
(FIG 13l) 785
(FIG.13c)
655 FIG.13d
FROM 616 (FIG.13b)
32 ms
"A=3"
772 (FIG.13l)
794 (FIG13j)
(FIG.13a) C̄
(FIG.13p) IR
EE

FIG. 13f

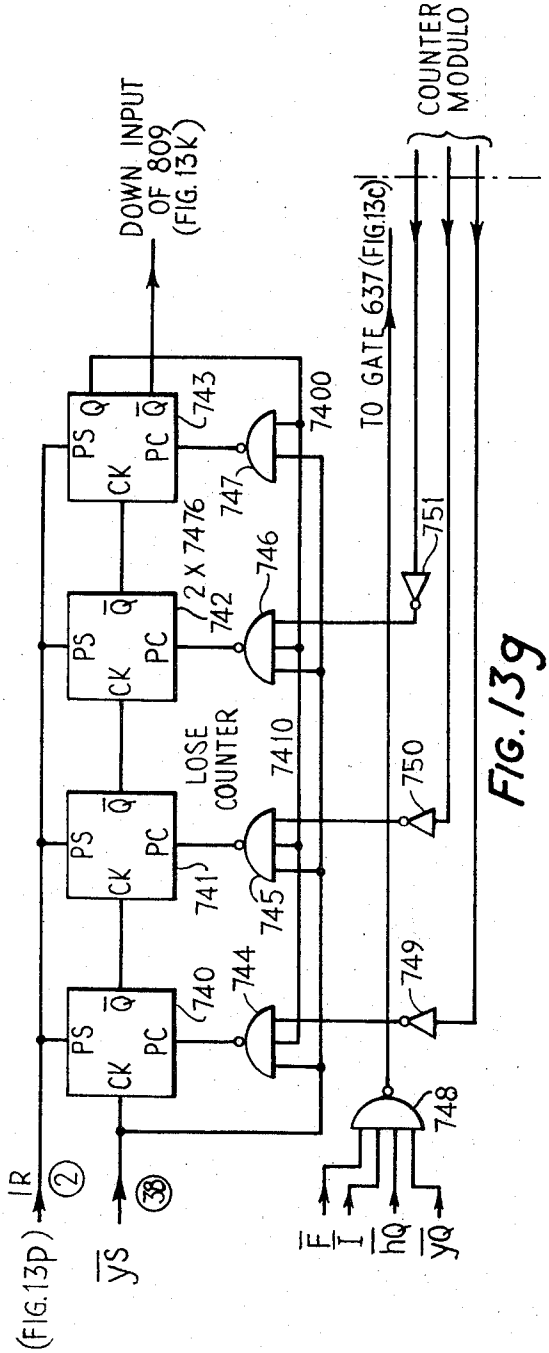


FIG. 13g

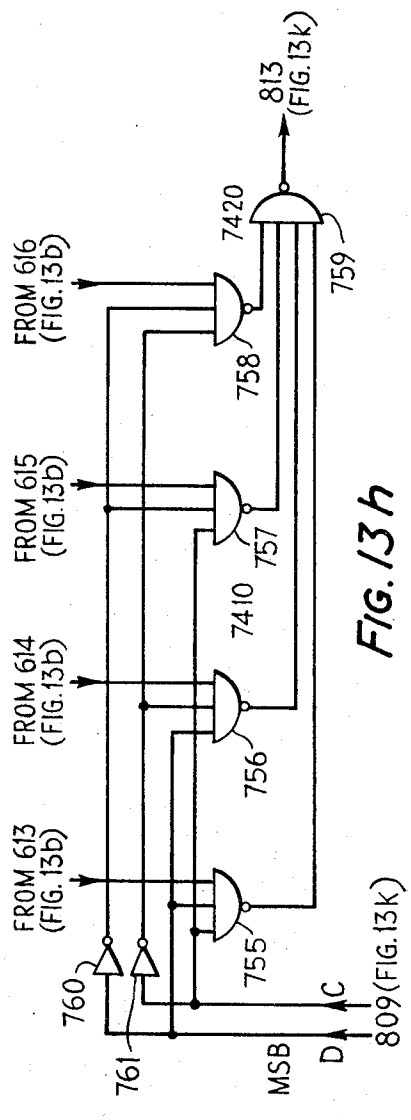


FIG. 13h

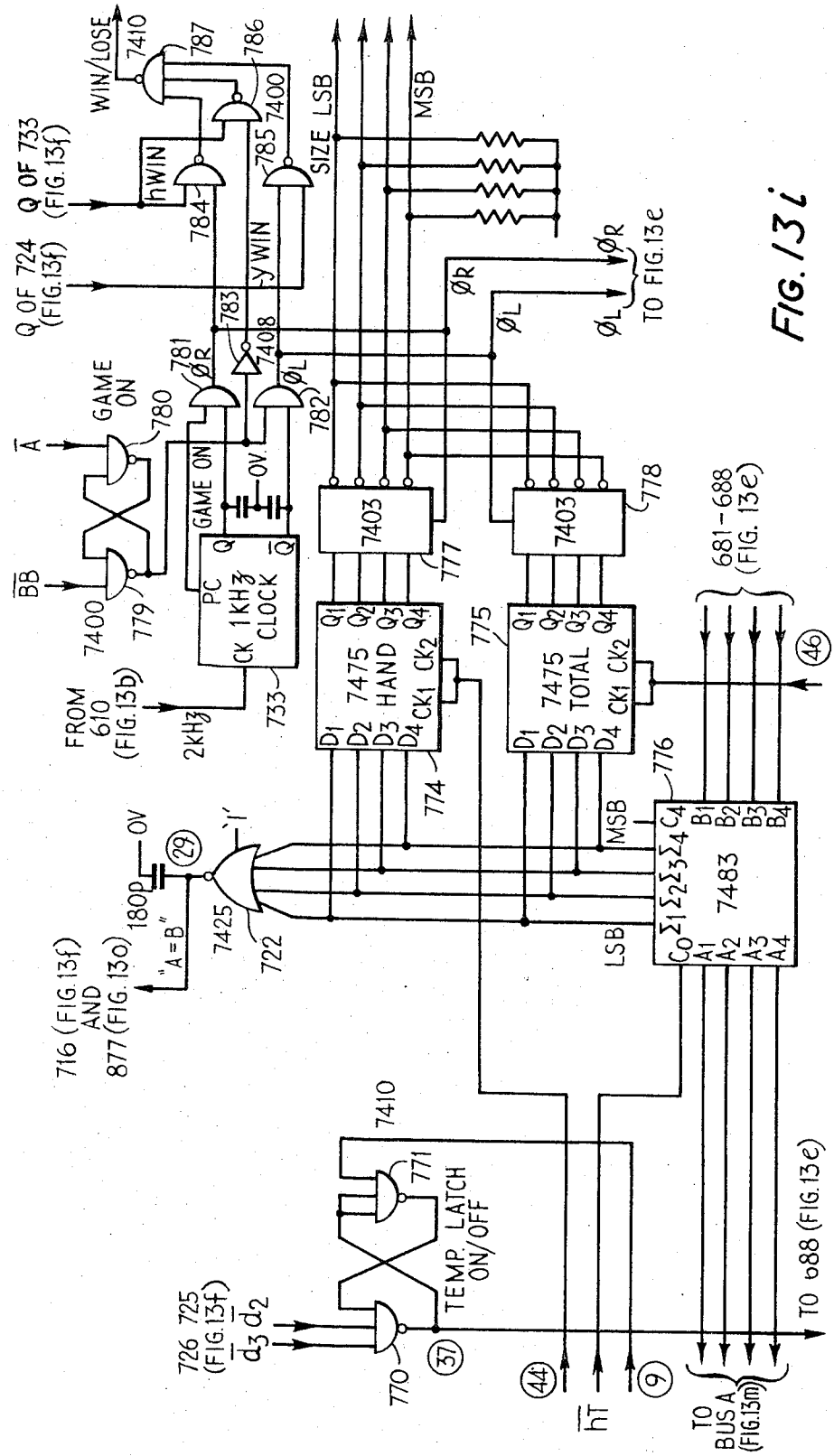

WIN/LOSE
7410
787
786
7400
785
784
hWIN
yWIN
Q OF 733 (FIG. 13f)
Q OF 724 (FIG. 13f)
SIZE LSB
MSB
TO FIG. 13e
783
7408
781
782
GAME ON
780
A
B
7400
779
PC 1KHz CLOCK
733
FROM 610 (FIG. 13b)
2KHz
7403
777
778
681-688 (FIG. 13e)
7475 HAND
7475 TOTAL
775
774
776
7483
722
7425
180p
716 (FIG. 13f) AND 877 (FIG. 13o)
"A=B"
TEMP. LATCH ON/OFF
7410
771
770
726 725 (FIG. 13f)
TO BUS A (FIG. 13m)
TO 688 (FIG. 13e)

FIG. 13i

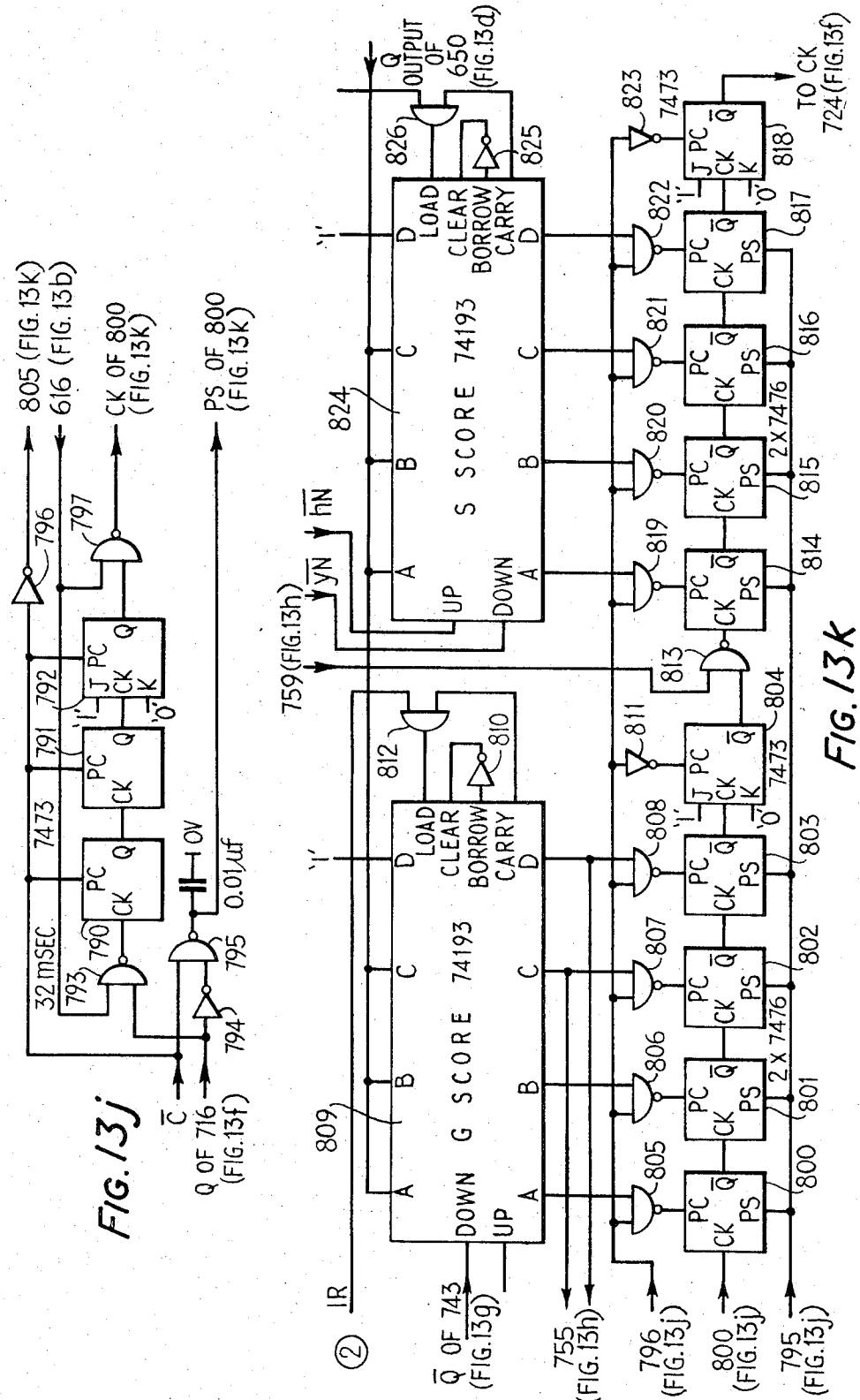


FIG. 13j

FIG. 13K

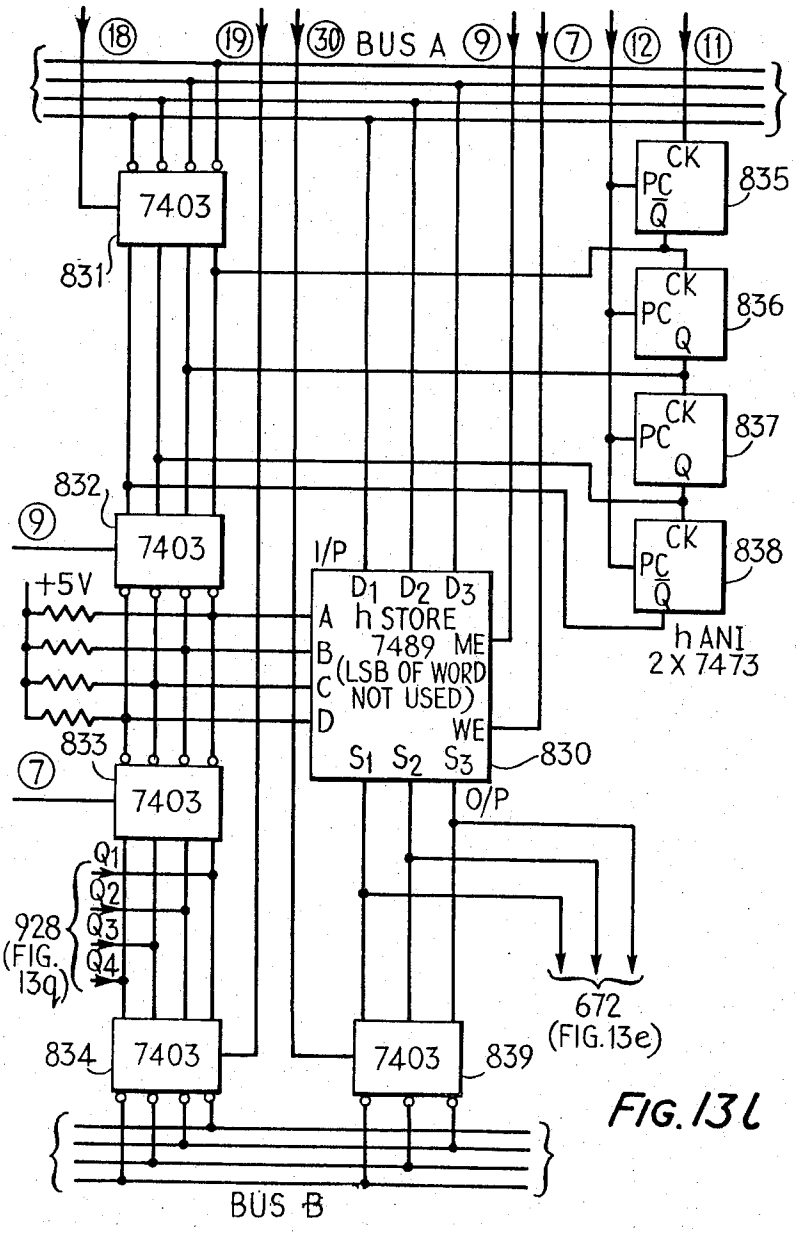

18
19
30
BUS A
9
7
12
11
7403
831
CK
PC
Q
835
836
837
838
832
9
7403
+5V
I/P
D1 D2 D3
A h STORE
B 7489 ME
C (LSB OF WORD
D NOT USED)
WE
S1 S2 S3
830
h ANI
2 X 7473
833
7
7403
O/P
Q1
Q2
Q3
Q4
928
(FIG. 13q)
672
(FIG. 13e)
834
7403
7403
839
BUS B

FIG. 13l

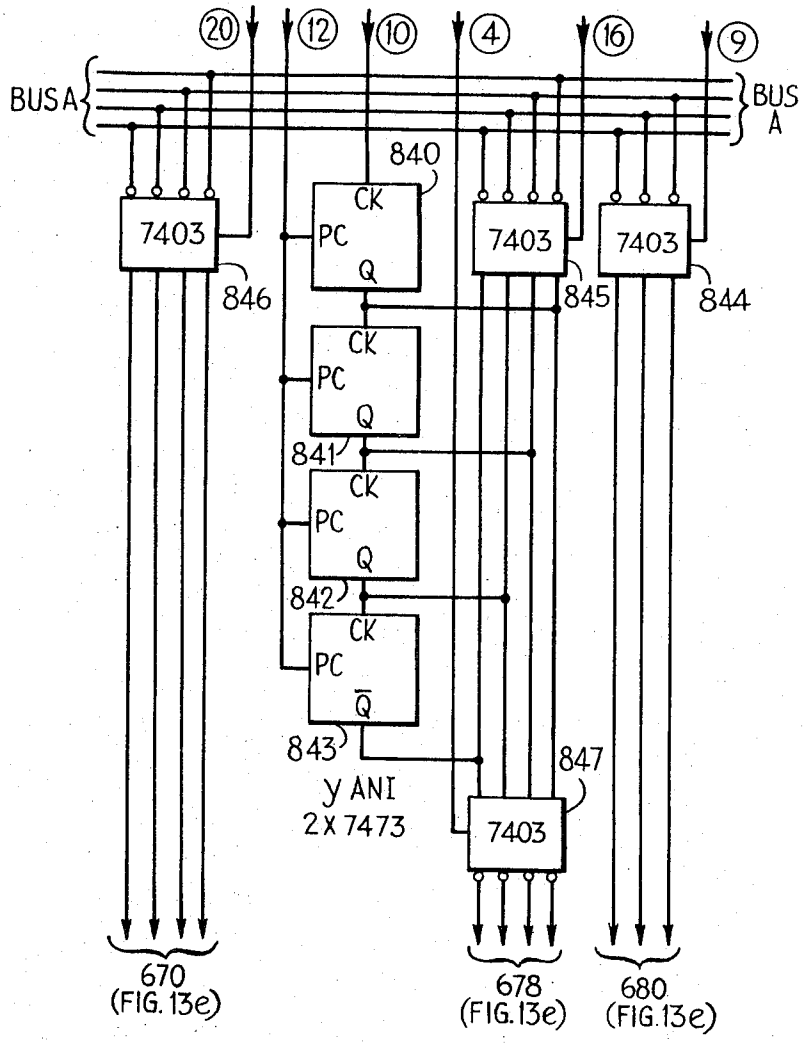

20
12
10
4
16
9
BUS A
BUS A
840
7403
CK
PC
Q
846
845
844
841
842
843
$\overline{Q}$
y ANI
2X7473
847
670
(FIG. 13e)
678
(FIG. 13e)
680
(FIG. 13e)

FIG. 13m

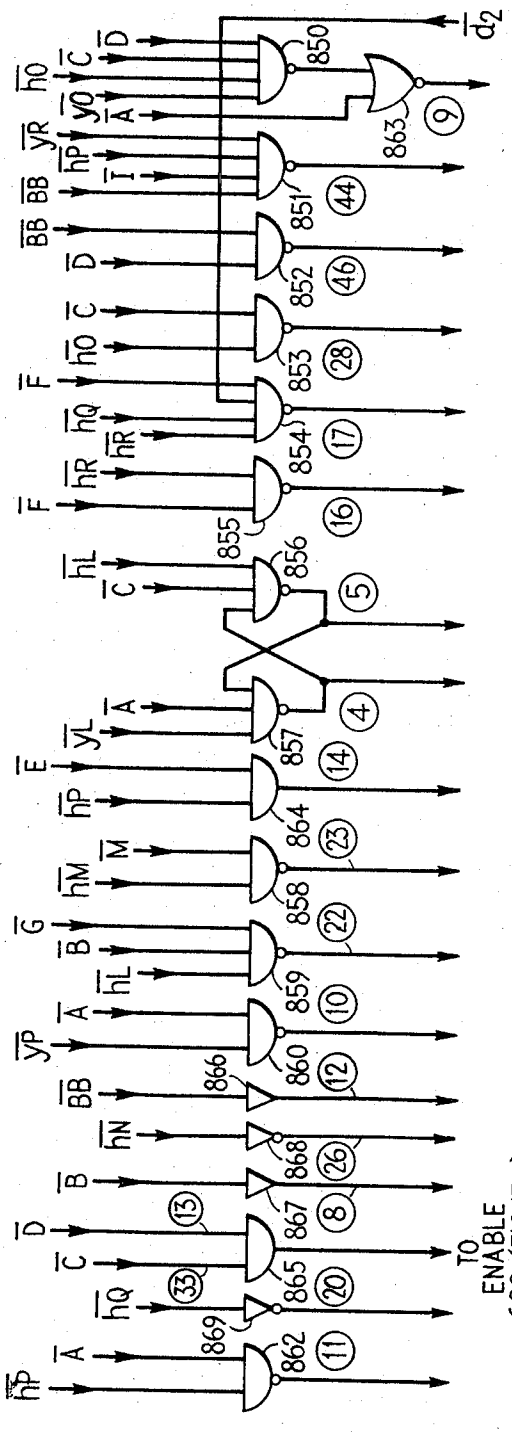

$\overline{d_2}$
850
863
9
851
44
852
46
853
28
854
17
16
855
856
5
4
857
14
864
23
858
22
859
10
860
12
866
868
26
867
8
865
20
869
862
11
13
33
TO ENABLE 689 (FIG. 13e)

FIG. 13n

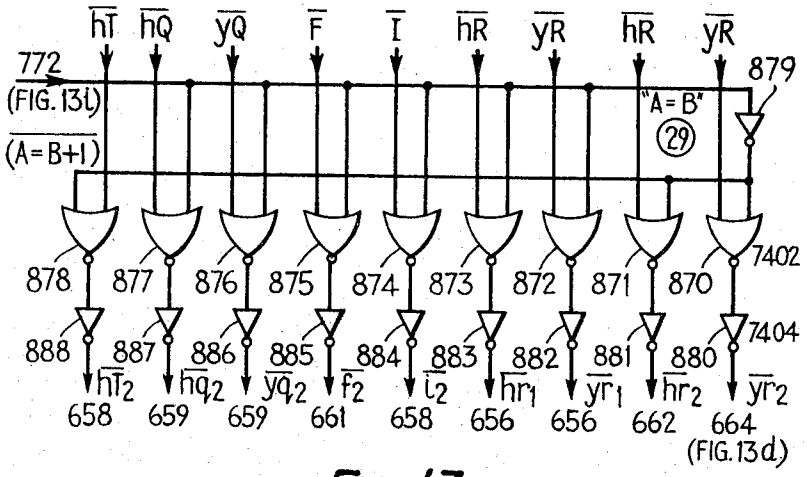


FIG. 13o

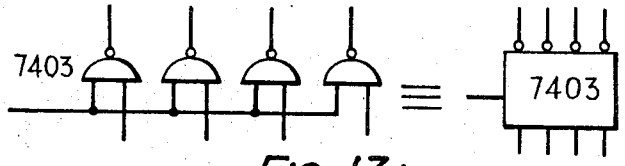


FIG. 13r

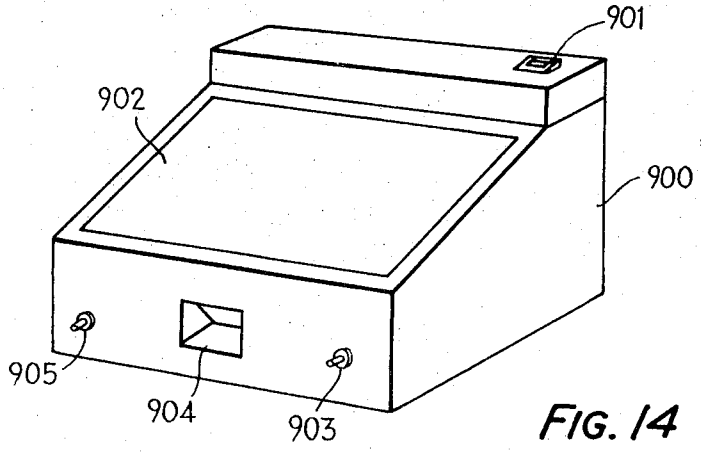


FIG. 14

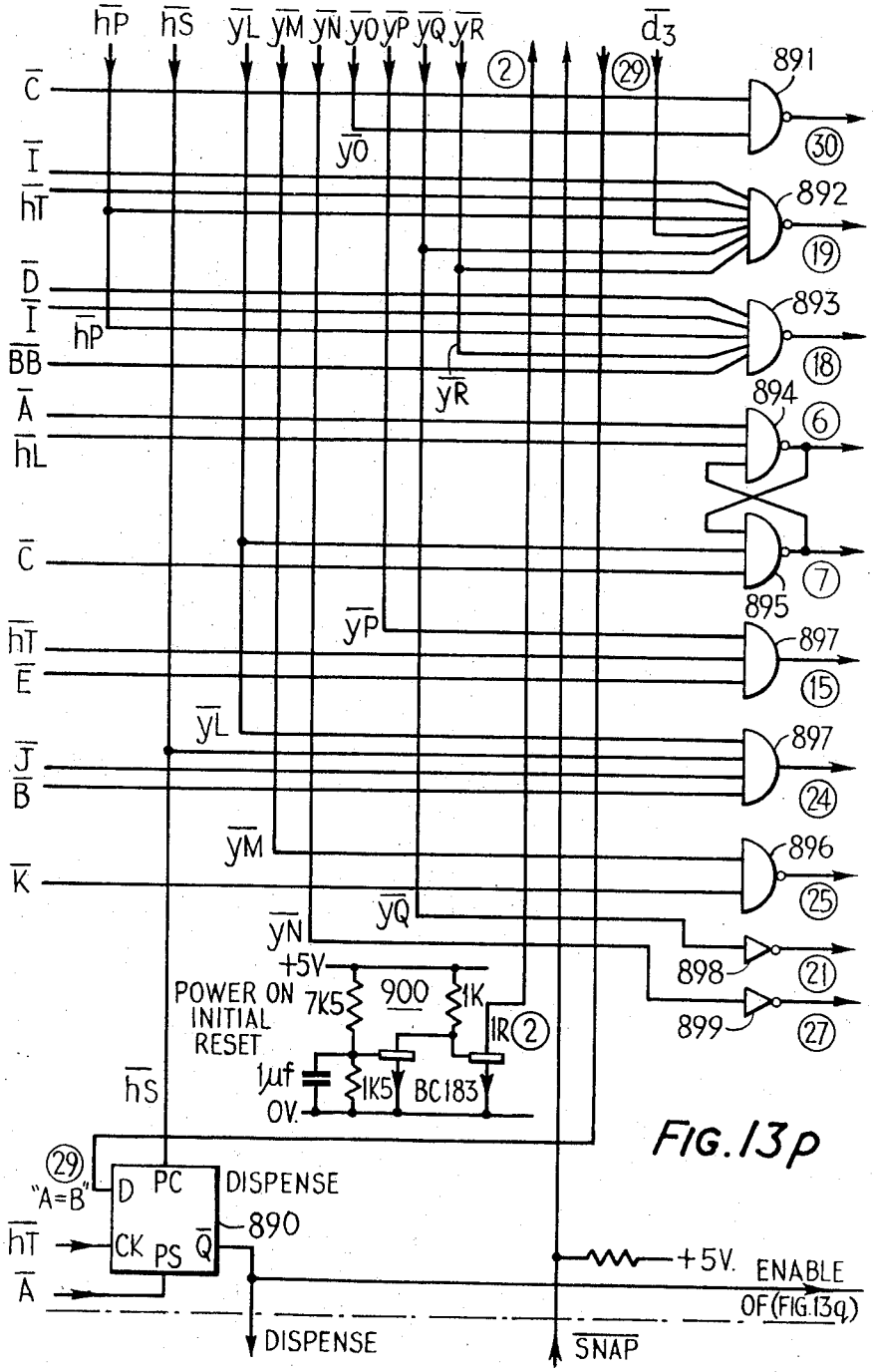

hP hS yL yM yN yO yP yQ yR
d3
C
I
hT
D
I
BB
A
hL
C
hT
E
J
B
K
hS
hP
yO
yR
yP
yL
yM
yN
yQ
+5V
POWER ON INITIAL RESET
7K5
900
1K
1R
1µf
1K5
BC183
0V.
891
892
893
894
895
897
897
896
898
899
29
"A=B"
D
PC
DISPENSE
890
CK
PS
Q
hT
A
+5V.
ENABLE OF (FIG.13q)
DISPENSE
SNAP

FIG. 13p

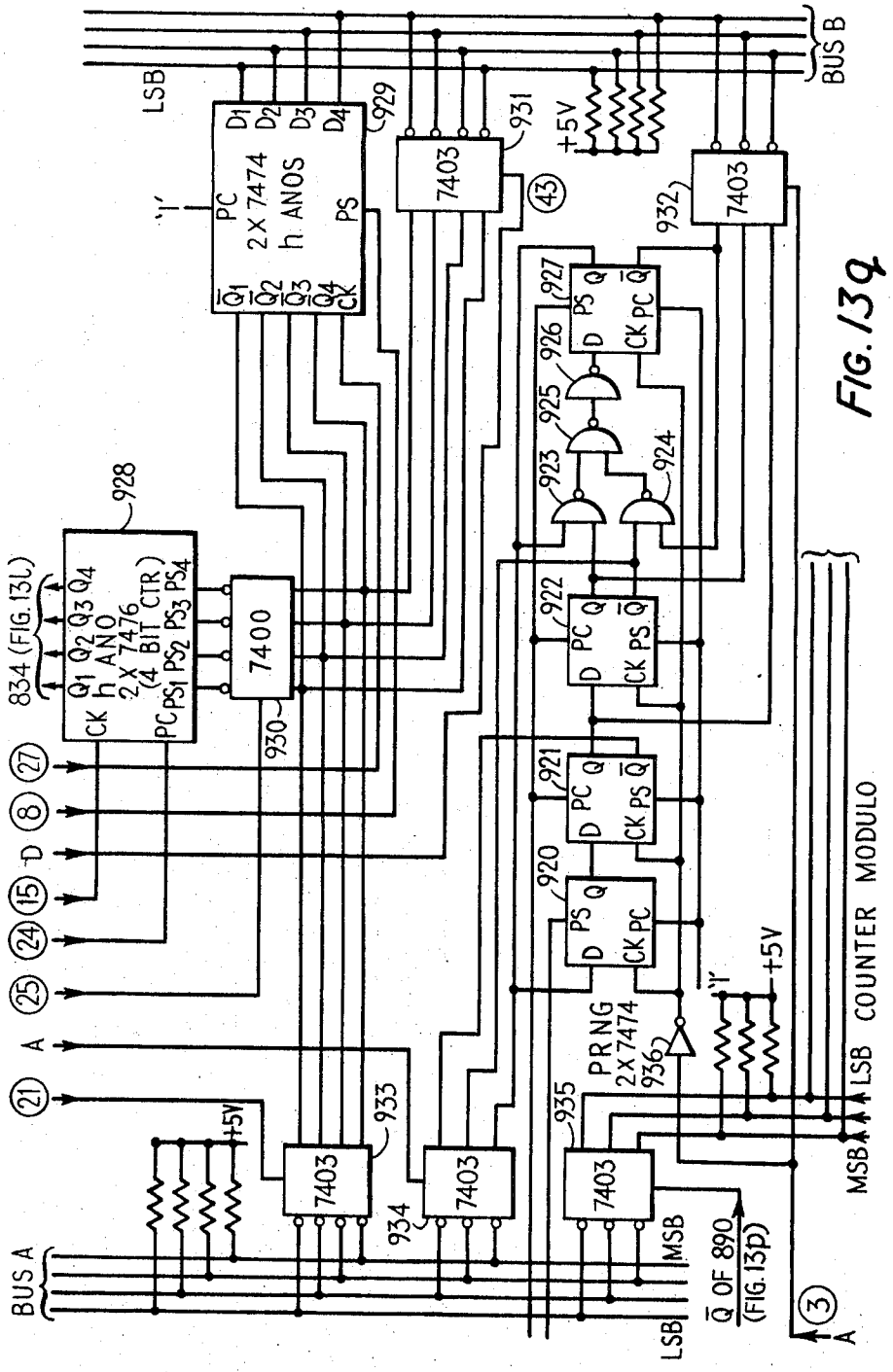

LSB
BUS B
+5V
7403
929
931
932
927
926
925
923
924
922
921
920
928
834 (FIG. 13J)
7400
930
27
8
15
24
25
A
21
BUS A
933
934
935
PRNG
2X7474
936
MSB
LSB
Q OF 890
(FIG. 13P)
3
A
LSB COUNTER MODULO

FIG. 13Q

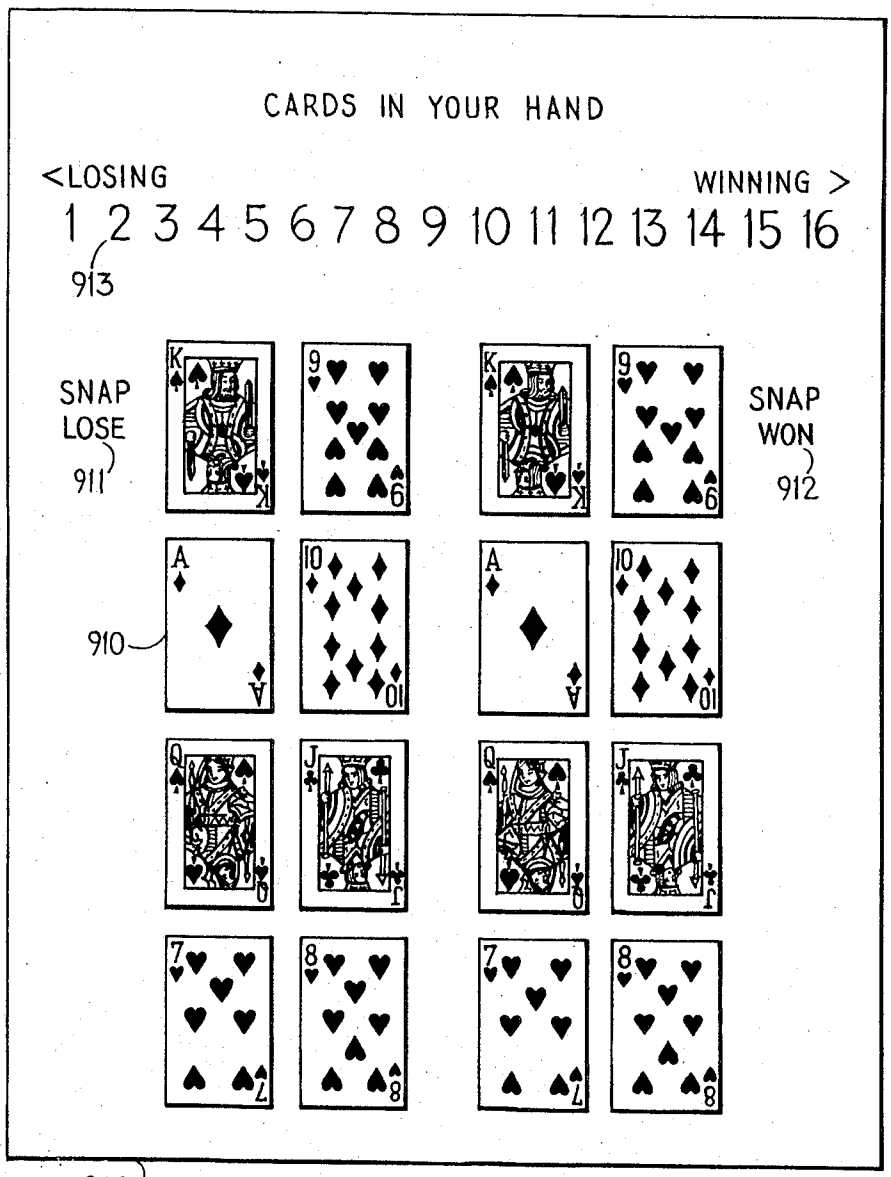

CARDS IN YOUR HAND
<LOSING
WINNING >
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
913
SNAP LOSE
911
SNAP WON
912
910
902

FIG. 15

GAMING MACHINES GAMES OF SKILL

This invention relates to amusement machines in which an individual plays against a machine or uses the machine so as to play against another player. By using his skill he may obtain a reward. Such a machine may be a part of another machine which is used for vending goods so that a customer may pay for goods and in addition he may play a game which, if won, shall cause a prize in the form of goods or money to be given to him.

In particular this invention consists of an electronic simulation of the game of "Snap." This is a game in which two players compete. Initially, they hold one pack of cards each and the object of the game is for one player to win all the other's cards. This is achieved by each player placing cards on a stack facing upwards one at a time. The players are synchronised as much as possible so that the top card of each player's stack is visible to both players at the same time. When two identical cards appear, both players may say "snap" and the first player to do so takes the stack of his opponent and places it in his hand such that it will appear after the cards he has already. The game then proceeds as before until one player has all the cards of his opponent. He is then deemed to have won the game.

When a player has placed all his cards on his stack and they have not been taken, he restores them to his hand and continues placing them in the same order as before.

If either player calls "snap" by mistake when the top cards are not identical, his opponent takes his stack and places it in his own hand so that it appears after the cards he holds already.

In one form of electronic simulation to be described herein, one player is an electronic or electromechanical machine. This machine recognizes rapidly the matching of two top cards of the stacks and starts a delaying device. A decision circuit determines whether the man player has signalled "snap" before or after the delaying device has signalled the machine player's snap. Advantageously, the machine player's snap is signalled to the man player by an audible "bleep," a gong, a prerecorded voice saying "snap" or a flashing lamp.

In order to enable the game to be played in this way, the cards are represented by codes held in cells of an electronic or mechanical memory in the game machine. Means are provided in the machine to display the top cards of the machine's and the man player's stacks. The cards displayed may be pictures, diagrams or characters which may or may not be used for advertising purposes in addition to their use in the game. For the purposes of the game, two identical sets of codes representing packs of the cards are held in the machine and are pseudorandomly dealt to the players before the game begins. Advantageously, one more card is dealt to the man player than the machine. This has the effect of reducing the possibility of games becoming interminable (as in "stalemate" in "Chess").

Also it is advantageous to include a second device which will prevent the "stalemate condition" completely. In one form, this device counts the number of cards placed since the last snap occurred and after a predetermined number (say twice the size of a pack) it causes the machine player to make a deliberately mistaken snap on the next occasion that there is only one card on its stack. This card is taken automatically by the player.

Another advantageous device controls the period of the delaying device in the machine player. This device consists of a register which accumulates a preset number of positive points for a man player's game win and subtracts a present number of points for the machine player's win. The accumulated score of points in the register is used to control the period of the delay such that a large number will cause a short period (making the game more difficult) and a small number will cause a long delay (making the game easier for the man). The effect of this device is to control the rate of winning games against the machine to a predetermined rate averaged over a number of games won or lost. The overall effect of the device is to make the game machine provide a competition between the present man player and those who played the machine before him.

It is convenient for the snap signal to be communicated to the machine by the man player by a push button switch. Alternatively a voice operated switch could be used. In addition an audible bleep or gong can be produced at the time the switch is operated. This sound should be distinguishable from the machine player's snap.

The game can be started by a coin operated switch or a push button. Conveniently, the controlling part of the machine can provide signals for operating a mechanism for dispensing goods or money soon after a coin is inserted and/or when the game has been won. Alternatively, or in addition, lamps can indicate the winning player.

Advantageously, a device can be provided which indicates the size of the man player's hand plus the size of his stack. This device makes the game more interesting and exciting to play. The device can indicate size by controlling the relative brightness of two adjacent lights, one brightening with increased size while the other dims. Alternatively, the size can be indicated by an illuminated picture of a stack of cards whose height can be made to vary accordingly, by switching on lamps which light adjacent sections of the picture, representing cards or groups of cards. Alternatively the size can be represented by a numerical display.

Throughout, the number of cards used in the game has not been stated because it is arbitrary. Advantageously, the size of each players hand can be nine for the man player and eight for the machine. When the rate of placing cards is one per second, the games average about 1 minute. Advantageously, different sets of cards can be displayed from game to game in order to preserve novelty, by increasing the number of different cards that the player may see, but maintaining the number of cards in any one game small enough to limit the length of a game session to a reasonably short time.

In an alternative form of the game machine, the machine player is replaced by a second button and modified decision device so that two men players can compete. Alternatively, the decision device can be extended to enable more than two players to compete.

According to the invention there is provided an amusement machine for simulating the playing of a game of snap, comprising means for simultaneously displaying at least one symbol selected from one series of symbols and at least one symbol selected from a second series of symbols;

means operable by a player to indicate an observed concurrence or relationship between the symbols selected from said respective series of symbols;

means in the machine for indicating when a concurrence has not been indicated before the occurrence of another event. In the form of game in which a human player plays against the machine, said another event is the ending of a predetermined time interval after the commencement of display of said symbols. In the form of game in which two human players play against each other, said another event is the operation by the second player of means to indicate said observed concurrence or relationship.

In order that the invention may be clearly understood and readily carried into effect, an embodiment thereof will now be described by way of example with reference to the accompanying drawings in which:

FIG. 1 is a block diagram indicating some of the stores included in the machine,

FIGS. 2 and 3 show a flow diagram indicating the successive steps in the operation of the machine,

FIG. 4 is a block diagram showing the circuitry which controls the sequence of operation in the machine,

FIG. 5 is a block diagram showing the stores in the machine and their interconnections,

FIG. 6 is a block diagram showing the parts of the machine concerned with snap decision and control of the machine player's delay,

FIG. 7 is a block diagram showing the means for controlling the machine's snap delay,

FIG. 8 is a block diagram showing the means for producing audible signals,

FIG. 9 is a block diagram showing the decoder for the display,

FIG. 10 is a block diagram showing the pseudo-random number generator,

FIG. 11 is a block diagram showing the dispenser control,

FIG. 12 is a block diagram showing the LSI chip used in the machine,

FIG. 13 is a detail circuit diagram of the LSI chip of FIG. 12,

FIG. 14 shows the machine, and

FIG. 15 shows the front panel of the machine.

Referring to FIG. 1 there are indicated some of the stores which are included in the machine of the present embodiment. The prefixes *h* and *y* refer to the man player and the machine player respectively. The *y*-store is a register which stores codes representing the cards which have been "dealt" to the machine player. At the commencement of a game 8 places in the store will be occupied. The *h*-store is a register which stores codes representing the cards which have been dealt to the human player. At the commencement of a game 9 places in the store will be occupied. The respective ANI registers store the address of the next input cell, the respective ANO registers store the address of the next output cell and the respective ANOS registers store the address of the next output if the stack is taken or picked up. Two sets of conductors, Bus A and Bus B are provided for transferring digital data between points in the machine.

In the flow diagram of FIGS. 2 and 3 the successive steps in the operation of the machine are shown. The encircled number inside the blocks indicate the signal instructions occurring at the relevant stage in accordance with the following Table:

TABLE

1. Step pseudo-random number generator (PRNG) to deal next pair of cards.
2. Set registers to an initialized state when machine is switched on.
3. Connect PRNG to data busses A and B.
4. Enable *y* store to input card code numbers from bus B to address contained in *y*ANI.
5. Enable *y* store to output card code numbers from address *y*ANO.
6. Enable *h* store to input card code numbers from bus A to address contained in *h*ANI.
7. Enable *h* store to output card code numbers from address *h*ANO.
8. Clear *h*ANOS and *y*ANOS, setting both card addresses to zero for start of game.
9. Turn off temporary store on bus B so that data is not retained.
10. Step *y*ANI to address next empty cell for card taken or dealt.
11. Step *h*ANI.
12. Set *h*ANI and *y*ANI to initial number of cards in players hands.
13. Turn on card displays and update display of size of player's hand.
14. Step *y*ANO to address next card to be displayed from *y* store.
15. Step *h*ANO to address next card to be displayed from *h* store.
16. Connect *y*ANI to data bus A.
17. Connect *y*ANO to data bus B.
18. Connect *h*ANI to data bus A.
19. Connect *H*ANO to data bus B.
20. Connect *y*ANOS to data bus A.
21. Connect *h*ANOS to data bus A.
22. Clear *y*ANO.
23. Copy contents of *y*ANOS to *y*ANO.
24. Clear *h*ANO.
25. Copy contents of *h*ANOS to *h*ANO
26. Copy data on bus B to *y*ANOS.
27. Copy data on bus B to *h*ANOS.
28. Connect output of *y* store to data bus A.
29. "Data on bus A = data on bus B".
30. Connect output of *h* store to data bus B.
31. Start game: from coin switch or start button.
32. Man player's snap: from push button or voice operated switch.
33. Compare card codes from *y* store and *h* store. Set up machine's snap delay time.
34. Turn on dispenser motor. Inhibit audible circuit.
35. Hold sequence in current state while dispensing.
36. Increment game score, and clear dispenser counter.
37. Enable latch on temporary store connected to bus B so that data is retained.
38. Increment lose counter.
39. Copy next stage number to current stage register in sequence generator. Period nominally 10 ms.
40. Enable signals generated in current stage. Period of this signal is nominally 10 ms, 1_s, 2_s or 250 ms.
41. Choose set of cards to be dealt: derived from least significant bits of *y*ANO (used as random number source).
42. Update "total cards" register.
43. Connect *h*ANOS to bus B.
44. Update "Hand Size" Register.

45. Hold sequence while snappable flip-flop set, that is until machine snap delay ends.

Referring to FIG. **2**, at the stage indicated by block **100** the game is switched on and the machine is switched on and the scores indicated by the machine are initialized, signal instruction **2** being used for this purpose. The next stage, **101**, simulates the dealing of a card to each hand from a pseudo-random number generator and it generally sets up the machine for operation, signal instructions at this stage being **1, 3, 4, 6,** 10, 11 and **41.** In stage **102** there is determined whether the start switch is on. If it is not on then the operation circulates back to the beginning of stage **101**, but if the switch is on then the operation proceeds to stage **103** in which both registers ANO and both registers ANOs are cleared, instruction signals being **22, 24** and **8.** The operation then proceeds to stage **104** when the addresses stored in *y*ANI and *h*ANI are set to the initial number of cards intended to be in the players' hands, namely **8** and **9** respectively, and the snap score indicator is set to **8** and the size indicator to **9.** The signal instructions in this stage are **12, 18, 42** and **44.**

The operation proceeds to stage **105** in which the next top cards in the two simulated hands of cards are selected and corresponding card lamps are tested. If the selected cards match a bistable is set to indicate a "snappable" condition and start a timing circuit which determines the time which the machine allows itself for snapping. The signal instructions are **28, 30** and **33.** If it has been determined at stage **105** that the card lamps are functioning then stage **106** follows in which the top cards are displayed for approximately one second and the size of the player's hand plus the stack, that is *h*ANI minus *h*ANOS, is calculated. The total size indicator is updated and a decision is made and stored as to who snapped first or made a mistake, that is the player or the machine. The signal instructions involved are **13,** 18, 42 and **43.** The next operation at stage **107** is to step on both output addresses, *y*ANO and *h*ANO, which indicate the address of the top card to the next position so that they indicate the next top cards. The signal instructions are **14** and **15.** At stage **105** if one of the card lamps had failed, the next operation in the sequence is that at stage **107**, that is to say stage **106** is by-passed.

Now, referring to FIG. **3**, the machine establishes at stage **201** whether the situation represents a snap or a mistake or neither. If it is established that there is neither a snap nor a mistake situation then the next step in the operation is **202** in which it is determined whether the *y* hand is empty. This involves signal instructions **16** and **17.** If the *y* hand is empty, that is to say *y*ANO is equal to *y*ANI then in stage **203** the contents of register *y*ANOS are copied into register *y*ANO and a caption "new *y* stack" is displayed for a quarter second. The signal instructions are **22** and **23.** The next step in the proceedings is step **204** which is also the next step after step **202** if it had been established that the *y* hand was not empty, the difference between the registers *h*ANI and *h*ANO is calculated and the hand size is updated. The signal instructions are **18, 19** and **44.** In this stage it is determined whether the *h* hand is empty. If it is not then the operation proceeds to stage **105** (FIG. **2**) and the operation continues through steps **105, 106, 107**, etc, If it is established that the *h* hand is empty, that is *h*ANO = hANI then stage **205** occurs in which the contents of register *h*ANOS are copied into register *h*ANO and a caption "new *h* stack" is displayed for one quarter second. The signal instructions involved are **24** and **25** and the operation continues with stage **105, 106, 107** etc.

If at stage **201** it is established that there is a snap or mistake situation in which the player (*h*) takes the machine's (*y*) stack than the operation proceeds to stage **206** in which the contents of the *y*ANO and *y*ANOS registers are exchanged and the snap score is incremented. The signal instructions are **37, 17, 23** and **26.** Then in stage **207** the contents of the *y* store in the cell identified by the register *y*ANO are copied to the *h* store cell identified by the register *h*ANI. The signal instructions are **5, 6, 28** and **9.** At the next stage, **208,** both *y*ANO and *h*ANI registers are stepped on and the difference between the register *h*ANI and *h*ANO is calculated so that the size of the hand can be updated, involving instructions **14, 11, 18, 19** and **44.** There is then determined in stage **209** whether the *y* stack is empty, involving signal instructions **17** and **20.** If the *y* stack is not empty the operation returns to stage **207.** If the *y* stack is empty, that is *y*ANO is equal to *y*ANOS then a determination is made in stage **210** as to whether they *y* hand is empty, involving instructions **16** and **17.** If it is not empty the operation proceeds back to stage **105** (FIG. **2**). If the *y* hand is not empty then in stage **211** a caption indicating "game won" is displayed and the score is incremented. The register *h*ANO is cleared in preparation for its use as a counter of articles to be dispensed. The signal instructions involved are **36** and **24.** There now follows stage **212** in which the dispenser counter is incremented and a test made as to whether the contents of this counter are equal to the value of the binary number on lines labelled "LOSE COUNTER MODULO" which are preset to indicate ONE LESS than the number of articles to be dispensed. This involves signal instructions **34, 15** and **19.** If the counter in *h*ANO is not equal to the aforesaid present number, then stage **212** is repeated. When the count is equal then the operation returns to stage **101** (FIG. **2**).

If the determination made at stage **201** is that there is a snap or mistake situation such that the machine should take the stack of cards associated with the player than the operation proceeds to stage **213** in which the contents of registers *h*ANO and *h*ANOS are exchanged and the snap score is decremented, involving signal instructions **37, 19, 25** and **27.** The contents of *h* store cell corresponding to the address in the *h*ANO register are transferred to the *y* store cell corresponding to the address in the *y*ANI register in stage **214,** involving signal instructions **4, 7, 30** and **9.** In stage **215** both the *h*ANO and *y*ANi register are stepped on, involving instructions **15** and **10.** A determination is then made at stage **216** as to whether the *h*stack is empty, signal instructions **19** and **20.** If the stack is not empty then the operation returns to stage **214.** If the stack is empty then in stage **217** by the calculation of the difference between *h*ANI and *h*ANO a determination is made as to whether the *h* hand is empty, signal instructions **18** and **19.** If it is not empty then the operation returns to stage **105** (FIG. **2**). If it is empty, that is *h*ANI is equal to *h*ANO then at stage **218** a caption "game lost" is displayed and the lose counter is incremented, signal instructions **38.** The operation now returns to stage **101** (FIG. **2**).

There is shown in FIG. **4** a block diagram of the arrangement for controlling the sequence of operations

associated with the steps of operation described in connection with FIGS. 2 and 3. Referring to FIG. 4, the stepping from one stage of the operation to the next is controlled by a clock 300 which has a period adjustable in the range from quarter second to two seconds. The clock produces two output signals which are the signals 39 and 40 of the Table. A pause signal can be applied to the clock by means of an OR-gate 301, and when such a signal is applied the signal 39 at a logic 1 for ten ms and this is succeeded by the signal at 40 becoming logic 1 and remaining for 10 ms. The input to the OR-gate 301 are the signals 45, which is applied when a snappable situation has arisen, the signal 35, which is a hold signal generated to allow the machine to dispense articles and the signal 32, corresponding to the player calling snap. When the pause signal applied from gate 301 to the clock is logic 1 then the signal 40 is logic 1 and the clock period is reset. When said pause signal applied from gate 301 is logic 0 the signal 40 remains at 0 after the selected period. A number representing the stage in the operations which has been reached is stored in store 303 and this controls a control signal distributor 304 which applies the signals to a plurality of output lines. These signals are the control signals 1, 3 to 28, 30 to 33, and 44 of the above Table. Signals from the distributor 304 are also applied to the clock 300 to control its period. Signals from the distributor 304 are also applied to a selector 305 which selects the number of the next stage in the operation. The next stage number is applied to a store 306 which stores the next stage number. The number of the next stage selected is modified if signals 29, representing the situation when the data on bus A is equal to the data on bus B and also by the signal 31 which is the signal to start the game, both these modifying signals being applied to selector 305. Under the control of clock 300 and signals 39 the number in store 306 is transferred to store 303 by means of a switch means 307 controlled by said signals 39. The numbers stored in stores 303 and 306 are also controlled by signals applied thereto by an OR-gate 308 which receives as its input signals 2, representing the initializing signals produced when the machine is switched on, and the start signals 31. This operates to set the stores 303 and 306 to the initial state.

In FIG. 5 there is shown the stores which are included in the machine and the interconnections thereof. The conductors BUS A and BUS B shown as horizontal lines towards the top of the Figure and towards the bottom of the Figure respectively, although shown as single conductors, are to be understood as referring to a plurality of conductors capable of carrying words expressed in binary digital form in parallel manner therealong. This applies to the other conductors shown in the Figure. The pseudo-random number generator 320 is connected to BUS A and BUS B through switches 321 and 322 respectively. These switches, like all the other switches shown in this Figure, are of the type which are closed by the application of control signals thereto. The control signals for switches 321 and 322 are the signals 3 as shown in the Table. The control signals are obtained from the distributor 304 (FIG. 4). The pseudo-random number generator 320 is stepped to deal the next pair of cards by the signal instruction 1 and is set to an initialized state at switch on by the instruction signal 2. The *h*ANOS store 323 obtains its input through a switch 324, controlled by signal instruction 27, from BUS B. The output of the *h*ANOS store 323 is connected to BUS A through a switch 325 controlled by instruction signal 21. The output is also applied to BUS B through a switch 326 controlled by signal instruction 43. The store 323 is cleared by the application of instruction signal 8 thereto. The *h*ANO store 327 is connected to the output of the *h*ANOS store 323 through a switch 328 controlled by instruction signal 25. The output of the *h*ANO store 327 is connected to BUS B through a switch 329, controlled by instruction signal 19, and also through a switch 330, controlled by instruction signal 7, to the address input of *h* store 331. The *h*ANO store 327 is stepped by the application of instruction signals 15 and cleared by the application of instruction signal 24. The *h*ANI store 332 is connected to BUS A through switch 333, controlled by instruction signal 18, and also through switch 334, controlled by instruction signal 6, to the address input of *h* store 331. The *h*ANI store 332 is set to equal 9 by application of instruction signal 12 and is stepped by the application of instruction signal 11. BUS A is connected to the input of *h* store 331 through a switch 335, controlled by instruction signal 6. The output of *h* store 331 is connected to BUS B through a switch 336, controlled by instruction signal 30. The output of *h* store 331 is also connected through a switch 337, controlled by instruction signal 13, to the means which displays the card which has been laid down by the player, 338.

BUS B is connected through a switch 339, controlled by instruction signal 26, to the input of the *y*ANOS store 340. The output of the store 340 is connected through a switch 341, controlled by instruction signal 20, to BUS A, and also through a switch 342, controlled by instruction signal 23, to the input of the *y*ANO store 343. The *y*ANOS store 340 is cleared by the application of instruction signals 8. The output of the *y*ANO store 343 is connected through a switch 344, controlled by instruction signal 17, to BUS B, and also through a switch 345, controlled by instruction signal 5, to the address input of the *y* store 346 the *y*ANO store 343 is stepped by the instruction signal 14 and cleared by the instruction signal 22. The *y*ANI store 347 is connected through a switch 348, controlled by instruction signal 16, 6, to BUS A, and also through a switch 349, controlled by instruction signal 4, to the address input of *y* store 346. The *y*ANI store 347 is set to equal 8 by instruction signal 12 and is stepped by instruction signal 10. BUS B is connected to the input of the *y* store 346 through a switch 350, controlled by instruction signal 4. The output of *y* store 346 is connected through a switch 351, controlled by instruction signal 28, to BUS A, and also through a switch 352 controlled by instruction signal 13, to a display means 353 which displays the card which has been turned up by the machine. The display means 338 and 353 are controlled by signal instructions 41.

A means for calculating the difference between the numbers appearing on BUS A and BUS B, 354 is connected to BUSSES A and B, and the output is applied to a zero detector 355 which provides an output signal instruction 29 when the result of the calculation is 0, that is A = B. The output of claculator 354 is also applied through a switch 356, controlled by instruction signal 42, to a means 357 which displays the total number of cards, and also through a switch 358, controlled by instruction signal 44, to a means 359 which displays the size of the hand. BUS B is connected to a temporary

store **360** which is controlled by a means **361** which controls the temporary store **360** to store the number on BUS B when required. The latch **361** is controlled by instruction signals **37** and **9**.

Referring to FIG. **6** which shows the portion of the machine concerned with snap decision and control of the machine player's delay, a bi-stable which is set when the situation is snappable, **400**, is set by signals from an AND-gate **401**. Gate **401** is energized by signal instructions **33** and **29** so that the bi-stable **400** is set when the cards displayed have been compared and similar cards have been displayed from the two packs. The Q output from bi-stable **400** is applied as one input of an AND-gate **403** and as one input of an AND-gate **402**. Gate **403** receives as its other input signal instruction **13** and its output is the hold instruction **45**. A second input of the gate **402** is the signal instruction **32** which is energized when a player presses the snap button. The Q output of bi-stable **400** is also applied as one input of an AND-gate **404**, the other input being the signal instruction **13**. The output of gate **404** is applied as the start signal to a delay circuit **405**. An output of delay circuit **405** is applied to an OR-gate **406**, the other input of which is the signal instruction **1**. The output of gate **406** is applied as a clear signal to a bi-stable **400**. The output of gate **402** is applied as one input of an OR-gate **407** the output of which is applied to a bi-stable **408** which is set to indicate a player's win, that is the situation when *h* is to take the *y* stack. The Q output of bi-stable **408** is a signal which indicates that *h* takes the *y* stack.

The $\overline{Q}$ output of bi-stable **400** is applied as one input of an AND-gate **409**, another input being the signal instruction **32**, and a third input being the $\overline{Q}$ output of bi-stable **408**. The $\overline{Q}$ output of bi-stable **400** is used as a signal to indicate that neither the machine nor the player has won.

The output of gate **409** is applied as one input of an OR-gate **410**, the other input of which is the output of the delay circuit **405**. The output of OR-gate **410** is applied as a set signal to a bi-stable **411** which is set to indicate the situation when the machine has won. The Q output of bi-stable **411** is used to provide a signal which indicates that *y* takes the *h* stack. The Q output of bi-stable **411** is used as the third input of gate **402**. Bi-stable **411** is cleared by signals obtained from an OR-gate **412**, the input of which are the Q signal from bi-stable **408** and the signal instruction **33**.

A register **413** which stores the game score is stepped up by instruction signal **36** which indicates that the player has won and is stepped down by signal instruction **38** which indicates that the player has lost. The signal instruction **38** is applied to register **413** through a divide circuit **414** which is capable of dividing by numbers between 1 and 8. The actual divide ratio is set by signals applied to the counter from an external source. These signals are preset and identified as the lose counter modulo. The register can be set to an initial value of 8 by the signal instruction **2**. The output of the register **413** is applied to the delay circuit **405** to control the delay provided by said circuit. A register **415** for storing the snap score is stepped up by signal instruction **26** indicating a snap win by the player and down by signal instruction **27** indicating a snap lost by the player. It is set to an initial value of 8 by signal instruction **12**. The output is also applied to the delay circuit **405**. The effect of this is to control the delay provided by circuit **405** so that if the player is winning too many times the delay is reduced to ease a machine win.

A circuit to prevent the situation of stalemate is provided comprising two JK flip-flops **416** and **417**. Signal instruction **22** is applied to clock the first flip-flop **416**, signal instruction **25** being applied to both the J and the K inputs. The Q output of flip-flop **416** is applied as the clock input of the second flip-flop **417** and the Q output thereof is applied as the second input of OR-gate **407**. The flip-flops **416** and **417** are cleared by the signal instruction **37**. An indicator for win/lose is provided comprising three AND-gates **418, 419** and **420** together with an OR-gate **421**. The signal *h* takes from the Q output of bi-stable **408** is applied as one input of each of the gates **418** and **419** and the *y* takes signals from the Q output of bi-stable **411** is applied as one input of gate **420**. Signals ϕ_R and ϕ_L are used as the other inputs of gates **418** and **420** respectively. The signals ϕ_R and ϕ_L are multiplex switching signals of approximately 1 kHz frequency which are applied in antiphase to the gates **418** and **420**. It will be evident that the two switching signals ϕ_R and ϕ_L must never be simultaneously at the 1 level. They are generated continuously throughout a game. Gate **419** has as its other input a signal indicating NOT game on. The outputs of the three gates **418, 419** and **420** are applied as the inputs of the OR-gate **421**, the output signal thereof being a signal indicating win/lose.

It will be appreciated that the delay time, that is the time which the machine allows itself for declaring snap is adjusted in accordance with the game score and the snap score. Typical delays are as follows:

Game Score	Snap Score	Delay Time (ms)
0	8	896
8	8	448
15	8	192
0	0	1252
8	0	512
15	0	224
0	15	672
8	15	392
15	15	164

FIG. **7** shows in greter detail the arrangement of the delay circuit **405** (FIG. **6**). There is provided an oscillator **430** which oscillates at a frequency of 4 kHz and the oscillations generated are supplied to a chain of binary dividers **431**. Signals obtained from the seventh binary divider in the chain, having a period of 32 ms are applied as one input of NAND-gate **432**. These signals are also applied as one input of an AND-gate **433**. The other input of the gate **433** is a start signal. The output of gate **433** is applied to a divide-by-4 circuit **434** the output of which is connected to the clock input of a flip-flop **435**. The J input of flip-flop **435** is maintained at a logic 1 level. The divider **434** and flip-flop **435** are cleared by signal instruction **33**. The output of flip-flop **435** is applied as the other input of NAND-gate **432**. The output of gate **432** is applied to a circuit **436** which is capable of dividing by **16**, but which can be controlled to divide in other ratios. The ratio is controlled by signals from the game score register **437**. The signals are applied in the form of the respective bits of the score through AND-gates **438** to **441** to respective stages of the divider **436**. The second inputs of the AND-gates **438** to **441** are the instruction signal **33**. The output of the divider circuit **436** is applied to a flip-

flop **438** which is connected in exactly the same manner as the flip-flop **435**, the output being taken to a NAND-gate **439** the other input of which is the output of an OR-gate **440**. The four inputs of the gate **440** are signals obtained from respective AND-gates **441** to **444**. The inputs of gate **441** are a signal representing the inverted most significant bit of the number registered in register **437**, the inverted bit representing the second most significant bit in said register **437** and a signal of period **32** ms obtained from divider **431**, namely the output of the seventh binary divider. The inputs of gate **442** are an inverted bit representing the most significant digit in register **437**, a bit representing the second most significant bit in register **437**, and a signal of period 16 ms obtained from the sixth binary stage of divider **431**. The inputs of gate **443** are a signal representing the most significant bit of the number stored in register **437** and a signal representing the inverted second most significant bit in said register, and a signal of period 8 ms obtained from the fifth stage of divider **431**. The inputs to gate **444** are signals representing the most significant bit and the second most significant bit in register **437** and a signal of period 4 ms obtained from the fourth stage of divider **431**. The output from gate **439** is applied to a divider **445** which is similar to divider **436** and is controlled through gates **446** to **449**, which are similar to the gates **438** to **441** from the number stored in the snap score register **450**. The output of divider **445** is applied to the clock input of flip-flop **451**, the J input of which is maintained at logic 1, and the output is used to control the machine snap.

Referring to FIG. **8** there is shown the portion of the portion of the circuitry of the machine which produces the bleep sounds indicating snap. An AND-gate **460** has as its inputs signal instructions **32**, produced by the player pressing the snap button, the same signals delayed by a delay means **461** by 200 ms, a 500 Hz signal and the instruction signal **34** applied through an inverter circuit **462**. An AND-gate **463** receives as its inputs signals indicating machine snap (from flip-flop **451** of FIG. **7**), the same signal delayed for 200 ms by delay means **464**, the signals from inverter **462**, signal instructions **13** and a **2** kHz signal. The outputs from gates **460** and **463** are applied as the inputs to an exclusive OR-gate **465** the output of which is amplified by amplifier **466** and applied to a loudspeaker **467**.

The decoder for energizing the display means is shown in FIG. **9**. The bits representing the number stored in the *y* store are applied to the respective AND-gates **470**, **471** and **472**, and the bits representing the number stored in the *h* store are applied to AND-gates **473**, **474** and **475**. The sets of gates **470** to **472** and **473** to **475** are alternately energized by the multiplex control signals ϕ_R and ϕ_L. The outputs from the three pairs of gates are applied as the respective inputs of OR-gates **476**, **477** and **478**. The resulting parallel 3 bit signal from gates **476**, **477** and **478** is applied to a decoder **479** which converts the 3 bit input to an 8 way output. The signal from gate **476** is applied directly, but the signals from gates **477** and **478** are applied to decoder **479** through exclusive OR-gates **480** and **481** respectively. The other inputs of gates **480** and **481** are signals obtained from latches **482** and **483** respectively. These latches are random bit latches and are energized through gates **484** and **485** respectively. Gate **485** has as its inputs the second to least significant bit of the number stored in the *y*ANO register applied to terminal **486** and the signal instruction **41**, and gate **484** has as its inputs the least significant bit of the number stored in the *y*ANO register applied to terminal **487** and the signal instruction **41**. Decoder **479** is enabled by signals obtained from an OR-gate **488** which receives as its inputs a signal instruction **13** indicating that the display is to be on and and a signal instruction **33**. The eight parallel output signals are applied to a lamp driver circuit **489** which is effectively a commutator which directs the eight input signals alternately to one set of eight output conductors to energize the right hand card lamps and to a second set of eight conductors which energize the left hand card lamps. The multiplexing of these output signals is controlled by the signals ϕ_R and ϕ_L. a signal obtained from a filament current detector in circuit **489** is applied as one input of a NAND-gate **490**, the other signal being the enable signal from gate **488**. The output of gate **490** appears at terminal **491** and is used as an instruction to skip the operation step **106** (FIG. **2**).

Most of the circuitry of the machine is conveniently prepared in the form of an LSI chip and the portion of FIG. **9** to the left of the dashed line CC is on said chip.

The pseudo-random number generator is shown in FIG. **10** and comprises four D-type flip-flops **500**, **501**, 502 and **503**. Flip-flops **501**, **502** and **503** are cleared by signal instructions **2**, and flip-flop **500** is cleared by signal instruction **8**. The flip-flops are stepped by signal instruction **1**. The Q output of flip-flop **500** is applied as the input to flip-flop **501**, and the Q output of flip-flop **501** is applied as the input to flip-flop **502**. The Q output of flip-flop **502** is applied as one input of an exclusive OR-gate **504**, and the output of gate **504** is applied as the input of flip-flop **503**. The Q output of flip-flop **503** is connected as the other input of gate **504**. The Q outputs of flip-flops **501**, **502** and **503** are applied to gates which can connect them to the Bus B and the $\overline{Q}$ outputs of said flip-flops **501**, **502** and **503** are connected to gates which can connect them to Bus A. The respective outputs represent pseudo-random numbers. The codes which can be generated by the generator are as follows:

	To Bus A	To Bus A
1.	000	111
2.	000	111
3.	100	011
4.	110	001
5.	111	000
6.	110	001
7.	011	100
8.	100	011
9.	010	101
10.	101	010
11.	111	000
12.	010	101
13.	001	110
14.	101	010
15.	011	100

The arrangement for controlling the dispenser is shown in FIG. **11**. A counter **510** is initially cleared under the control of signal instruction **36** at the commencement of operation stage **211** (FIG. **3**). A flip-flop **514** for holding the sequence has its $\overline{Q}$ output connected to a terminal **515** to provide the signal instruction **35**. Flip-flop **514** is cleared by the dispenser on instruction signal **34** which is also applied to the set input of flip-flop **516** which provides as its $\overline{Q}$ output a signal

to terminal 517 which maintains the dispenser in operation. The count on counter 510 is applied to inputs A and the "LOSE COUNTER MODULO" is applied through invertors 511 to 513 to inputs B of a 3 bit adder 520 whose outputs are connected to NOR gate 518 and carry input is connected to signal instruction 34. The NOR gate 518 accordingly provides an output which is transferred to flip-flop 514 when instruction signal 34 goes high and when the output of NOR gate 518 becomes 'I' it controls the operation sequence to 101 (FIG. 2) from 212 (FIG. 3). The flip-flop 514 receives clear signals from parallel switches 522 and 523 to the O V line. Switch 522 is the snap button and the other switch, 523, is the coin switch on the dispenser. The portion of the circuit below and to the right of the dashed line CCC is contained in the LSI chip.

In operation, at the beginning of step 211 (FIG. 3) the instruction signal 36 is at 1 and this sets counter 510 to 0. After 20 ms stage delay signal 36 returns to 0, and step 212 is reached. Instruction signal 34 is at 1 and this sets flip-flop 514 to provide at its $\overline{Q}$ output the instruction signal 35 which is now at 1; it also sets flip-flop 516 to operate the dispenser motor. When the coin switch 523 on the dispenser closes, instruction signal 32 becomes low and clears the hold sequence set by flip-flop 514, but holds sequence in turn by the signal through invertor 302 and OR gate 301 (FIG. 4). This sets instruction signal 35 to high. Thus sequence is held so long as instruction signal 32 is low. When the coin switch 523 opens, instruction signal 32 becomes high and the hold sequence is removed. After a 20 ms delay instruction signal 34 becomes 0. If the dispenser count in counter 510 has become equal to LOSE COUNTER MODULO, flip-flop 516 is cleared and the sequence changes to step 101 (FIG. 2), but if they are not equal the sequence returns to step 212 and the operation just described is repeated.

As already stated, the major portion of the electronic circuitry of the machine is contained on a LSI chip, and the arrangement of the chip is shown in FIG. 12. The boundaries of the chip are shown by the dashed line CCCC. The successive steps in the operation of the machine are controlled by the sequence control unit of FIG. 4, 530. The unit 530 receives clock and timing signals from a unit 531 (300 of FIG. 4), start game signals from an external source and also receives signals from the filament detector (from 489 to 490, FIG. 9). The control unit 530 provides control signals to a unit keeping the score and providing the machine snap delay 532 (see FIGS. 6 and 7), to the snap decision unit 533 (see FIG. 6), to the pseudo-random number generator (see FIG. 10), the registers and stores 535 (see FIGS. 5 and 6), the display decoder for the cards 536 (see FIG. 9), and to the clock unit 531. It also provides signals to the dispenser (terminal 517 of FIG. 11) and to the new stack, both external of the chip. The clock provides timing signals to the display decoder 536 (479 of FIG. 9) and also the multiplex control signals ϕ_R and ϕ_L. The circuit 532 receives a 3-bit parallel input from preset means, which by setting the levels on the three inputs determine the lose counter modulo and the number of articles to be dispensed minus 1. The snap decision unit 533 (see FIG. 6) receives an input from the snap button representing the player's SNAP, and also a signal from unit 532 representing the machine's SNAP. Unit 533 supplies an output to a WIN/LOSE indicator, a feedback signal to the control unit 530, a signal to the registers and stores unit 535, and a signal to an audible circuit 537 (see FIG. 8). The output of audible unit 537 is connected externally to a loudspeaker. (467 of FIG. 8). The pseudo-random number generator 534 provides its output to the register unit 535. A random number unit 538 (470 to 480, 482 to 487 of FIG. 9) is connected in a path from the register unit 535 to the display decoder 536 to which the register unit 535 is also directly connected. The display decoder provides an output to the lamp drivers, external of the chip, as shown at 489 (FIG. 9). The register unit 535 also provides an output to a player's cards hand size unit 539 (357, 359 of FIG. 5), which provides signals to an indicator external of the chip. Power is supplied to the chip at terminal 540.

FIG. 13*a* to 13*r* show the complete circuit in detail of the LSI chip shown in FIG. 12. It is shown in the form of a circuit comprising discreet components which will simulate the operation of the chip. Alphabetical references refer to lines carrying signals generated by the sequence control unit and encircled numerals correspond with those listed in the foregoing Table.

FIG. 13*a* shows a part of the sequence control of the unit (530 of FIG. 12) and comprises two four-line to sixteen-decoders with strobe inputs, type 74154, which are used to convert four bit binary words received at the terminals A, B, C and D to a plurality of instruction signals designated by the alphabetical symbols for use elsewhere in the circuit. The decoders are controlled by the AND-gates 602 and 603 receiving inverted inputs as indicated on the drawing from other parts of the circuit.

FIG. 13*b* shows part of the clock and timing unit (531 of FIG. 12). It comprises a chain of binary divider stages 610 to 618 which receives 4 kHz signals generated by a circuit comprising a 4-input Schmitt triggered positive NAND-gate (half of type 7413) having a resistive feedback associated with a timing capacitor 620 which is external of the chip. From the dividing chain are obtained pulses having durations point 5, 2, 4, 8, 16, 32 and 128 ms period.

FIG. 13*c* shows the circuits which provide the bleep sounds in response to a machine win or player SNAP, 537 of FIG. 12, comprises JK flip-flops 630, 631, 639 and 640 (type 7473) and gates 632 to 638 and 641 to 645 as shown. The output is connected externally of the chip to amplifier 466 and loudspeaker 467 of FIG. 8.

FIG. 13*d* shows another part of the sequence control unit (530 of FIG. 12). It comprises a chain of JK flip-flops, type 7473, 650 to 654 controlled by NAND-gates 655 to 664 which receive signals from the position of the circuit on FIG. 13*a* or 13*o* or elsewhere as indicated. The circuit also includes inverters 656, 657 and NAND-gates 655 and 668.

FIG. 13e shows part of the registers and stores unit (535 or FIG. 12, and also FIG. 5). The *y*ANOS store 670 comprises D-type flip-flops, type 7474; the *y*ANO store 671 comprises JK flip-flops, type 7476; the *y* store is a 64-bit read/write memory, that is sixteen words of four bits each, type 7489, although the last significant bit of the word is not used. The transfer of signals is controlled by NAND-gates, type 7403, 672, 673, 677, 678 and 679. Reference is directed to FIG. 13*r* in which the symbolism used in the present specification is described. That is to say the plurality of gates comprised in the type 7403 have been drawn as a single

block with a common enable connection. A D-type flip-flop is shown at **676** and NAND-gates at **690** to **692** and **681** to **688.** The binary to decimal decoder **689,** type 7442, is used to provide the signal instruction to illuminate the appropriate card in the display and corresponds with **479** on FIG. **9.**

FIG. **13***f* contains the snap decision unit **533** of FIG. **12** and the snap delay part **532** of FIG. **12.** A chain of JK flip-flops is shown at **700** to **706** associated with NAND-gates **707** to **713.** D-type flip-flop **714** is type **7474** as is flip-flop **716** and **733.** Flip-flop **724** is a JK flip-flop, type **7476** and flip-flop **728** is JK type (**7473**). JK flip-flops **731** and **732** are also type **7473.** NAND-gates **718** to **723, 725** to **727** and **715** are included in the circuit together with AND-gates **717, 730** and **733.** An inverter **729** is also used.

FIG. **13***g* shows the lose counter (**532** of FIG. **12**) and comprises a chain of JK flip-flops, type **7476** controlled by NAND-gates **744** to **747.** NAND-gate **748** together with inverters **749** to **751** are also included.

FIG. **13***h* shows NAND-gates **755** to **759** and inverters **760** and **761.**

FIG. **13***i* includes the score unit (**532** of FIG. **12**) and comprises a latch consisting of NAND-gates **770** and **771,** type 7410, an OR-gate **772** type 7425, a flip-flop **773** controlled by 2 kHz signals from the divider of FIG. **13***b*, a pair of D-type or bit bi-stable latches **774** and **775,** type 7475, the outputs of which are applied to NAND-gates **777** and **778,** type **7403,** a latch of a pair of NAND-gates **779** and **780,** a pair of AND-gates **781** and **782,** an inverter **783,** and three NAND-gates **784** to **786.**

The circuit of FIG. **13***j* comprises a chain of flip-flops **790** to **792,** NAND-gates **793, 795** and **797,** and inverters **794** and **796.**

FIG. **13**k which contains the registers for keeping the score comprises two synchronous up/down 4 bit binary counters, type **74193, 809** and **824** connected to NAND-gates **805** to **808** and **819** to **822,** and inverters **810, 811, 823** and **825.** AND-gates **812** and **826** are also included. There is also provided a chain of JK flip-flops **800** to **804** and **814** to **818** and a NAND-gate **813.**

FIG. **13***l* includes the *h* store, **830,** similar to the *y* store **680** of FIG. **13***e*, with connections to the BUS A and the BUS B, controlled by the NAND-gates **831** to **839.** The circuit also includes the *h*ANI store comprising JK flip-flops **835** to **838,** type **7473.**

FIG. **13***m* includes the *y*ANI store which comprises a chain of JK flip-flops **840** to **843,** and the circuit shows NAND-gates **840** to **847,** type 7403.

FIG. **13**n shows a series of NAND-gates, NOR-gates, amplifiers and inverters **850** to **862** which receive the alphabetically identified signals to produce the signals identified by encircled numerals.

FIG. **13***o* comprises a series of NOR-gates **870** to **878** each coupled to an inverter **880** to **888,** an inverter **879** being associated with gate **870.** The gates receive alphabetically identified signals from the sequence control circuit of FIG. **13***a* to provide signals which are applied to FIG. **13***d.*

FIG. **13***p* includes the control circuit for the dispenser together with a series of gates **891** to **899** which act in a similar manner to the gates of FIG. **13***o.* The dispenser unit is controlled by a D-type flip-flop **890** to provide an output signal to control the dispenser motor. A delay circuit **900** is utilized to provide a delayed signal when the machine is first switched on to constitute the initial reset signal, instruction signal 2 of the Table.

FIG. **13***q* includes the PRNG generator, **534** of FIG. **12** and also the *h*ANO and *h*ANOS stores. The PRNG includes a chain of four D-type flip-flops, type 7474, **920** to **922** and **927, 922** being connected to **927** by NAND-gates **923** to **926.** Clock pulses are applied to the flip-flops through an inverter **936.** The *h*ANO store **928** comprises four JK flip-flops, type **7476,** and the *h*ANOS store **929** comprises four D type flip-flops, type 7474. NAND-gates **933** to **935** and **930** to **932** are also provided.

FIG. **13***r* as already indicated shows the circuit symbol which has been adopted in the preceeding Figures for a set of four NAND-gates.

FIG. **14** shows the machine. A case **900** contains all the electronic circuitry and at the top of the machine is provided a slot **901** for the insertion of coins to initiate the operation of the machine. On a surface of the machine facing the player is a panel **902** shown in greater detail in FIG. **15.** Referring to FIG. **15,** the panel **902** includes a display of **8** playing cards such as **910** arranged to the left of the centre line of the machine in two columns of four. A similar display is arranged to the right of the centre line. As shown the cards displayed to the right are identical to those on the left. It will be evident that whilst the same cards must be available on the right hand side as on the left hand side they do not necessarily have to be arranged in the same order. In play, the player does not see any of these card representations until one on each side is illuminated by the operation of the circuitry, by the means **489** on FIG. **9.** There are provided captions "snap lose" and "snap won," **911** and **912** which again are not visible until one or the other is illuminated by the circuitry to indicate the state of the game. A series of numbers 1 to 16, **913** is arranged on the panel and one of these is illuminated at any one time to indicate the number of cards considered to be in the hand of the player. On the front of the machine is a switch button **903** which is pressed by the player to simulate his shout of snap. An aperture **904** is placed in the front of the machine for the ejection of goods or tokens as dispensed by the dispenser. Switch button **905** is optionally placed on the front of the machine when it is intended that the machine is to be used for one human player playing a second human player. It is similar to the switch button **903** and in operation in this fashion the machine delay timer is omitted or disconnected, and replaced by the second snap button **905.**

It will be evident that the machine can be modified in many ways still in accordance with the invention. For example the dispensing apparatus may be omitted and the machine may offer a free game to a winning player or it may be operated purely for amusement without the paying out of articles or tokens. In addition the coin mechanism may be omitted if it is desired to operate the machine without any payment being made, for example as a toy. It will be evident that it is not necessary to use conventional playing card representations on panel **902** and any convenient symbols may be utilized. The machine may be used not only for conventional snap games as described above but for other games based on the same concept, for example the game of slap-jack.

What is claimed is:

1. An amusement machine for simulating the playing of a game of snap, comprising means for simultaneously displaying at least one symbol selected from one series of symbols and at least one symbol selected from a second series of symbols;

means operable by a player to indicate an observed concurrence or relationship between the symbols selected from said respective series of symbols;

means in the machine for indicating when a concurrence has not been indicated before the occurrence of another event.

2. An amusement machine in accordance with claim 1, for a game in which a human player plays against the machine, wherein said another event is the ending of a predetermined time interval after the commencement of display of said symbols.

3. An amusement machine in accordance with claim 2, wherein said machine includes means for registering the number of games won or lost by said player.

4. An amusement machine in accordance with claim 3, wherein said machine includes means for adjusting said time interval in accordance with the number of games won or lost by said player or players.

5. An amusement machine in accordance with claim 1, for a game in which two human players play against each other, wherein said another event is the operation by the second player of means to indicate said observed concurrence or relationship.

6. An amusement machine in accordance with claim 1, wherein the operation of said machine is initiated by the insertion of a coin or token therein.

7. An amusement machine in accordance with claim 6, including means for dispensing articles, coins or tokens.

8. An amusement machine in accordance with claim 7, wherein the number of articles, coins or tokens dispensed depends on the number of games won or lost by a player.

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