United States Patent

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[54] **ELECTRON BEAM FOCUS CONTROL SYSTEM**
9 Claims, 9 Drawing Figs.

[52] **U.S. Cl.** **219/121EB,** 340/173
[51] **Int. Cl.** **B23k 15/00**
[50] **Field of Search** ..... 250/83.3 (H), 49.5; 315/11; 340/173 (R); 73/257, 258, 259; 219/121 (EB), 125 (PL), 121, 121 (L)

[56] **References Cited**

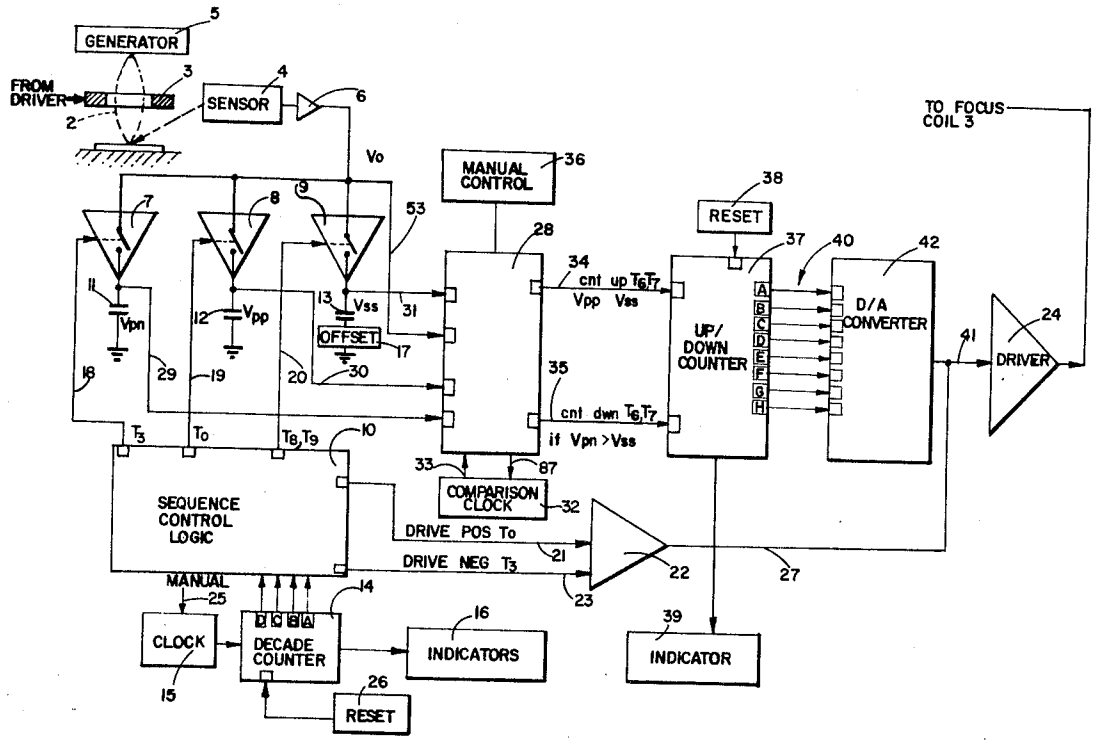
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ABSTRACT: The temperature of an electron beam at the face of a workpiece is sequentially sampled and a voltage representing the temperature is stored for comparison with prior voltage samples. The focus coil current is increased or decreased as a function of the relative difference between the compared samples. When the samples are equal, the comparison is discontinued.

The sampling sequence of the system is controlled by a counter operating at one rate and the comparison is controlled by logic gated at a relatively higher rate so that the change in the focus coil current can be completed before the next sample is taken.



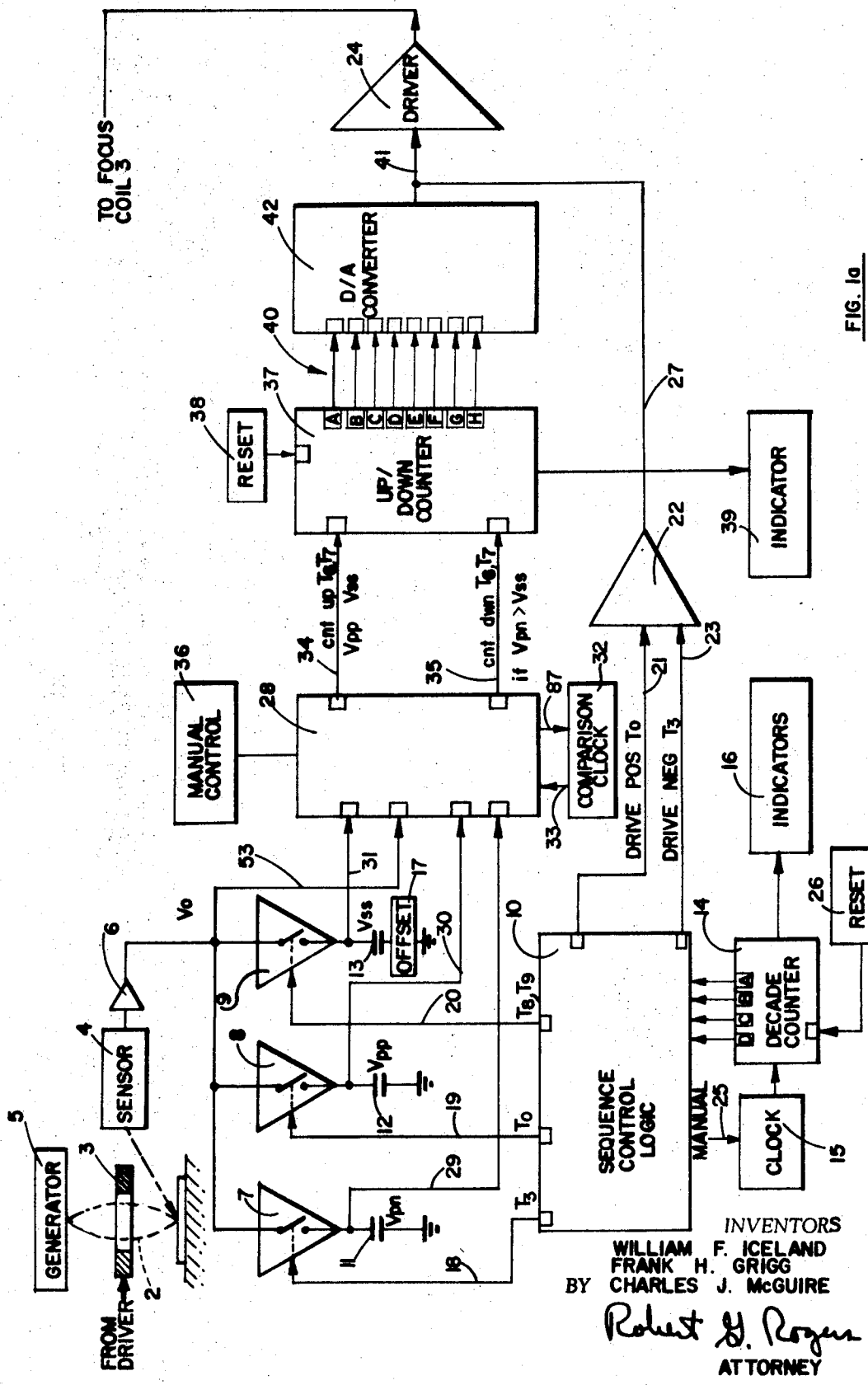


FIG. 1a

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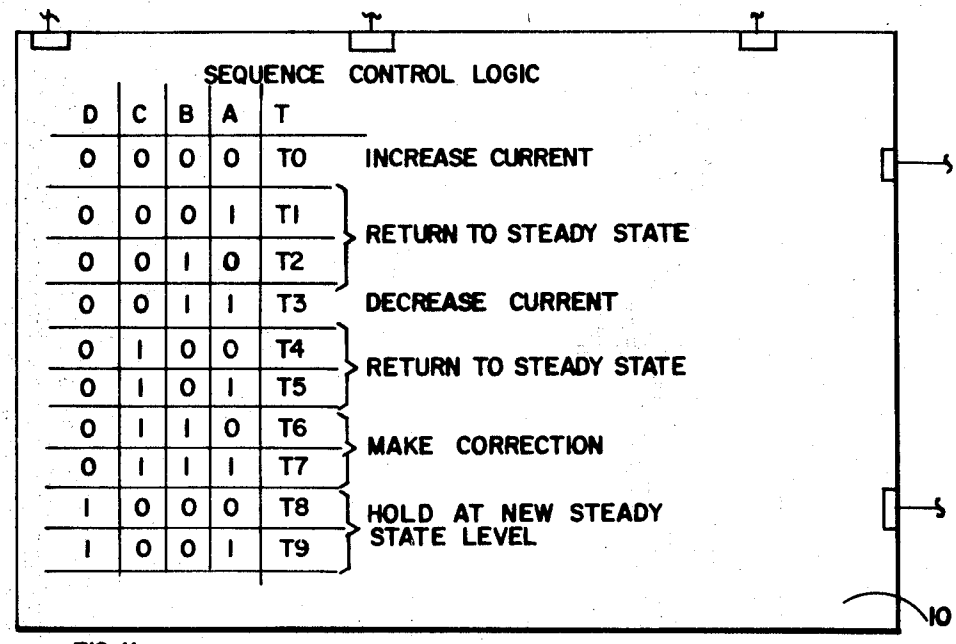


FIG. 1b

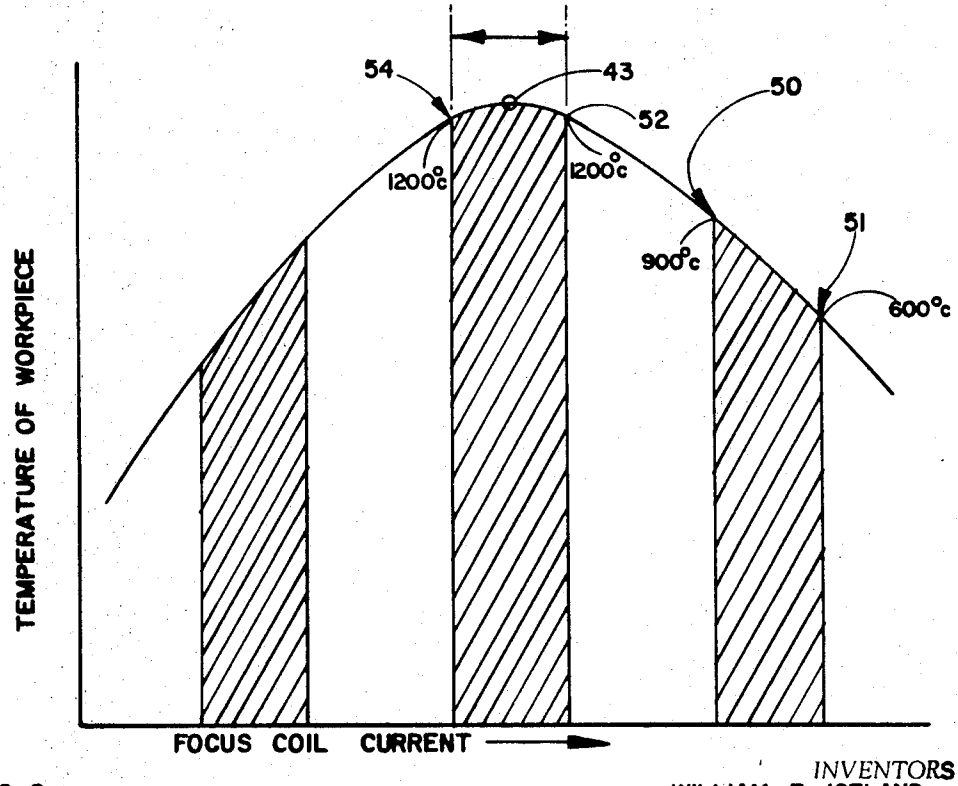


FIG. 2

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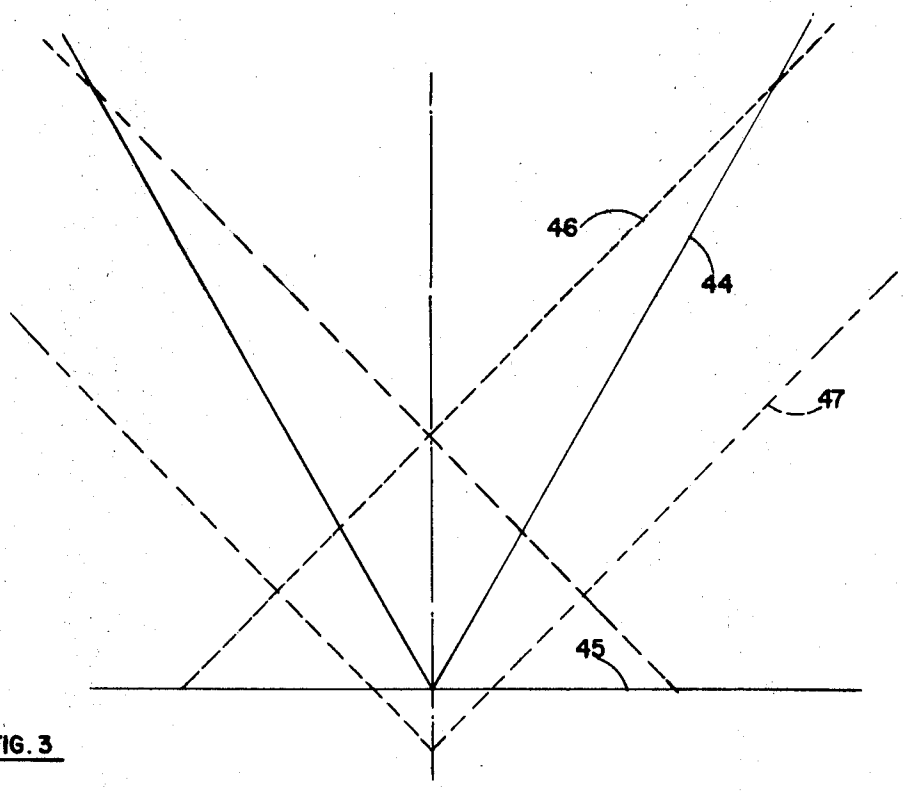


FIG. 3

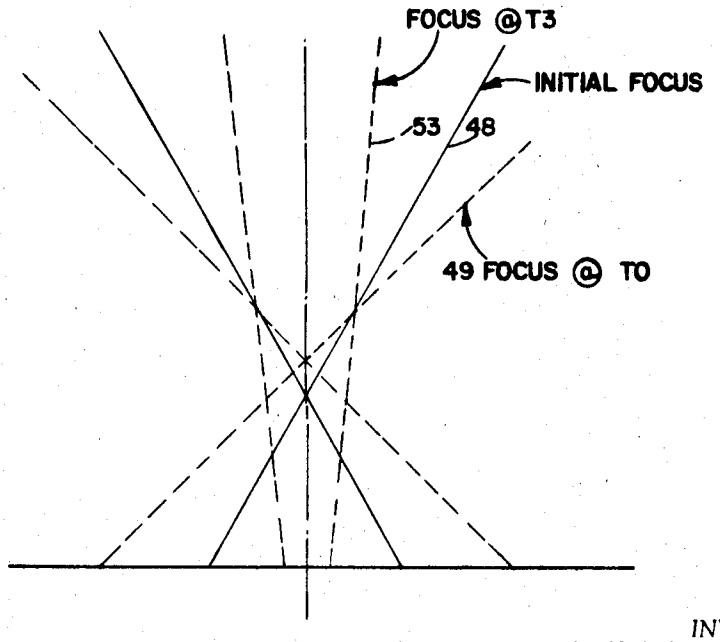


FIG. 4

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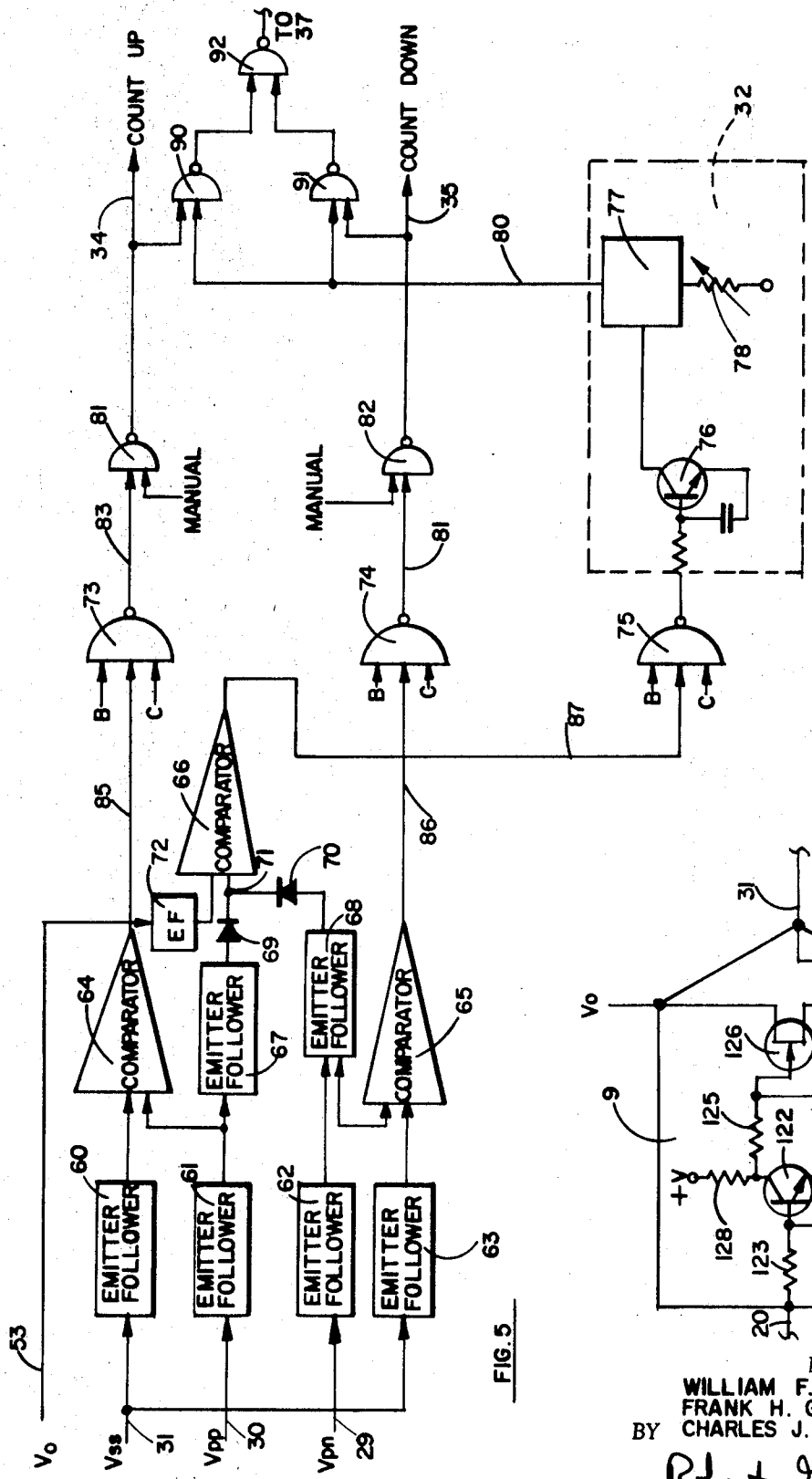


FIG. 5

FIG. 7

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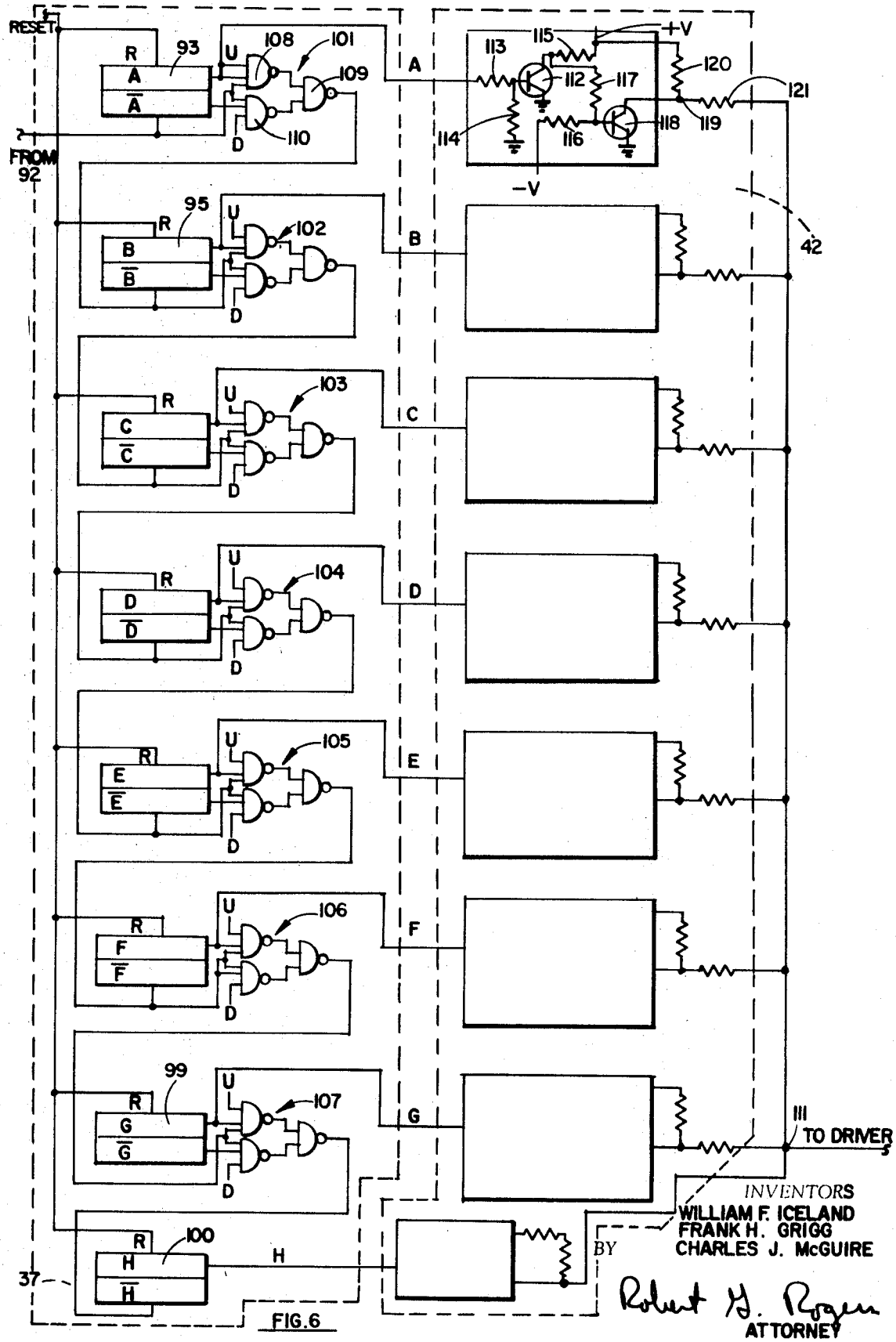


FIG.6

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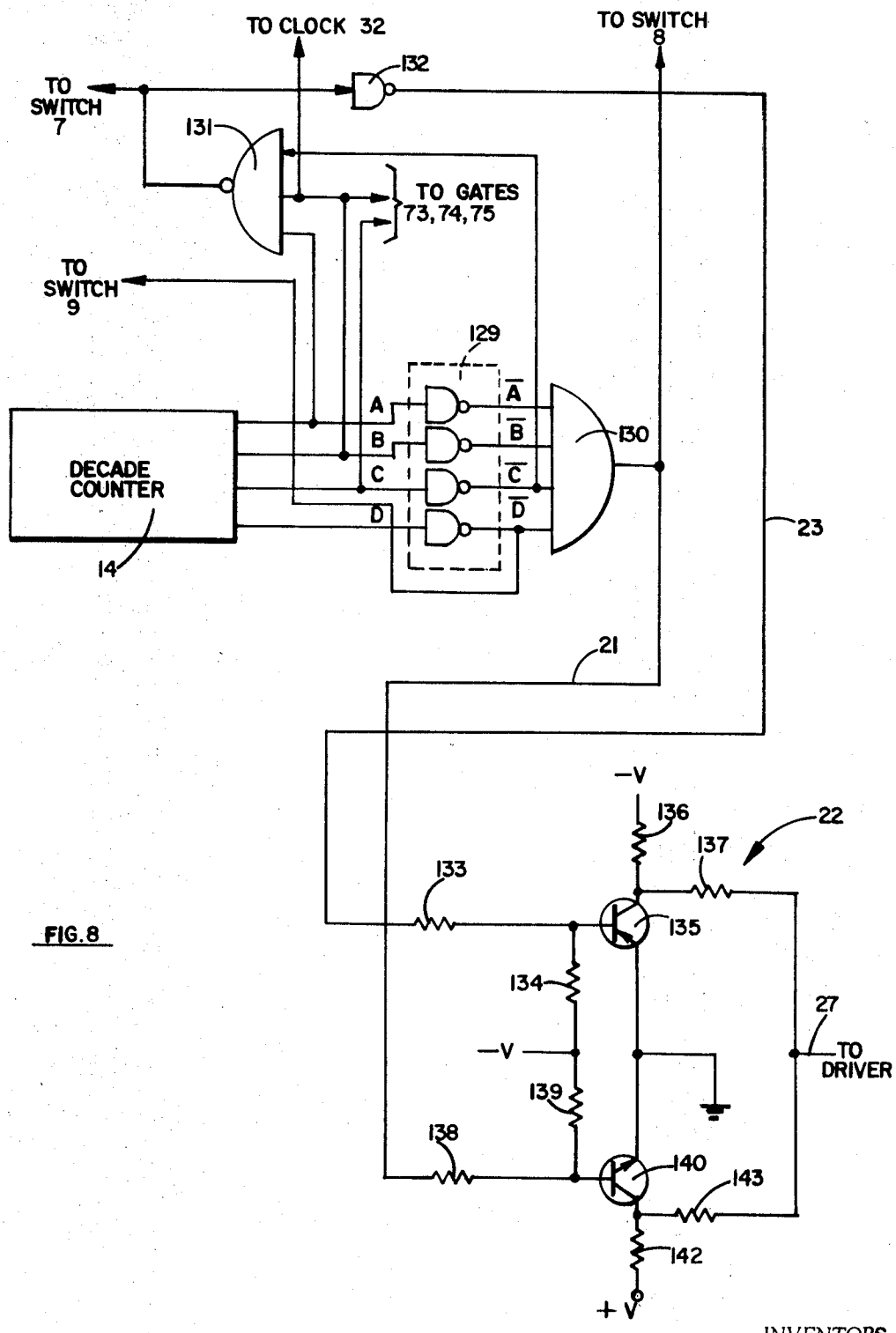


FIG. 8

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ELECTRON BEAM FOCUS CONTROL SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to an electron beam focus control system and more particularly to such a system in which the focus coil current is sequentially changed until a peak temperature at the face of a workpiece is indicated.

2. Description of Prior Art

A system is needed to eliminate the necessity for an operator to visually determine the optimum electron beam configuration, or focus, on the surface of a workpiece being welded. Certain systems use a manually controlled potentiometer for obtaining the maximum beam intensity. However, manually controlled, systems must be adjusted periodically for each weld, due to the inherent deterioration of the tungsten filament, and any variance necessary in beam voltage or current requirements.

A preferred system should be able to automatically adjust the focus to achieve the maximum beam intensity or any other beam intensity at the face of a workpiece as required for a particular operation. The present system provides such a capability.

SUMMARY OF THE INVENTION

Briefly, the invention comprises a system for sampling the temperature of a workpiece being heated by an electron beam. The temperature varies as a function of the beam intensity. The sampled temperature is converted to a voltage and compared with prior samples. The focus coil current is changed as a function of the difference between the voltages until a predetermined beam intensity at the workpiece is achieved.

In the preferred system, the beam focus is changed first in one direction and then in another. The temperature is sampled as each focus is changed. A voltage representing each sample is stored and sequentially compared with other samples. A drive signal is generated to change the relative focus as a function of the sense of the temperature changes which occurred during the initial focusing sequence. The drive signal is changed during each operating cycle until the samples are equal. The operating sequence is controlled by a counter operated at one rate. The comparison logic is gated at a relatively higher rate so that the change in beam focus is completed before the next sampling interval within an operating cycle.

In another embodiment, an analog system is used in controlling the beam focus. An analog signal representing the temperature generated by the beam at the workpiece is compared with a reference voltage. If the signals are not equal, an output voltage is generated to change the focus coil current.

For certain applications, it is desired to focus the beam at a point above or below the surface of the workpiece. In that case, the measured temperature at the face of the workpiece is less than the maximum temperature possible. Therefore, the system must be biased, or offset, to indicate maximum beam intensity at the surface even though the beam is focused for maximum intensity at a position displaced from the surface.

Therefore, it is an object of this invention to provide an improved electron beam welding control system for automatically controlling the focus of an electron beam relative to the surface of the workpiece.

It is another object of this invention to provide an improved digital electron beam welding control system having a constant focus control for an electron beam relative to the surface of the workpiece.

A still further object of this invention is to provide an improved system for controlling the focus of an electron beam on a workpiece using an offset circuit to obtain maximum beam intensity at a point displaced from the surface of the workpiece.

It is another object of this invention to provide an improved system for controlling the focus of an electron beam in which adjacent temperature samples are stored and compared for indicating the sense and amplitude of temperature changes at the surface of the workpiece due to changes in the focus of an electron beam.

A still further object of this invention is to provide an improved electron beam focus control system which is adaptable to a repetitive preset beam configuration.

A further object of this invention is to provide an improved electron beam focus system which is not as dependent on visual observations of an operator in determining the maximum intensity of the beam.

A further object of this invention is to provide an improved beam focus control system for minimizing the problems due to the inherent deterioration of the resistance of the filament and any variance in beam voltage or current setting for different welding operations.

These and other objects of the invention will become more apparent when taken in connection with the drawings, a brief description of which follows:

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1*a* is a block diagram of a digital system for automatically controlling the focus of an electron beam at the surface of a workpiece being welded.

FIG. 1*b* is a table showing the operating sequence of the FIG. 1*a* system.

FIG. 2 is a plot of the temperature change at the surface of a workpiece as a function of the focus coil current.

FIG. 3 is a representation of the beam focus for different focus coil current values. FIG. 4 is a different representation of the beam focus for different focus coil current values.

FIG. 5 is a schematic diagram of the compare logic shown generally in FIG. 1.

FIG. 6 is a schematic diagram of the counter and digital-to-analog converter shown generally in FIG. 1.

FIG. 7 is a schematic diagram of one embodiment of a switch circuit usable in the FIG. 1 embodiment.

FIG. 8 is a schematic diagram of one embodiment of the sequence control logic illustrated generally in FIG. 1.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1*a* is a block diagram of a digital system for controlling the focus of an electron beam **2** by controlling the sense and amplitude of current in focus coil **3**. The electron beam is produced from generator **5** which may comprise a filament actuated by a power source.

The beam configuration is sensed by sensor **4** which may be a standard infrared detector measuring temperature change. The temperature of a workpiece varies as a function of an electron beam focus, or configuration. The sensor **4** detects the change in the beam focus and generates a voltage representing that change. The sensor may include a motor driven shutter and lens for permitting the temperature of the workpiece to be selectively chopped. In other words, with the chopper in one position, the heat from the workpiece is permitted to be sensed whereas in another position the heat is blocked from the sensor.

The voltage is amplified by amplifier **6** and provided as input V_0 to one of three switches **7**, **8** and **9**. The switches are sequentially turned on by control signals generated by sequence control logic **10**. The switches may be implemented by semiconductor devices such as field effect transistors. If field effect transistors are used, the control signals are applied to the gate electrodes of the devices.

Capacitors **11**, **12** and **13** are connected at the outputs of the switches **7**, **8** and **9**, respectively, for storing the output voltage from the switches, approximately V_0. The other sides of the capacitors are connected to electrical ground except for capacitor **13**. In one embodiment, offset control circuit **17** is connected between the capacitor and ground. The offset circuit is discussed subsequently.

Sequence control logic **10**, which may be implemented by AND gates or equivalent circuitry, receives the DCBA outputs from decade counter **14**. The outputs are encoded by the sequence control logic, as shown in block **10**, to provide sequence control signals T_0 through T_9. The control function of each signal is shown in the table illustrated as FIG. 1*b*.

Decade counter **14** may be implemented by series connected flip-flops including interconnecting logic gates. For that embodiment, the D flip-flop receives control pulses from clock **15**. The counter recycles at each count of nine.

The clock **15** may be implemented by unijunction oscillator or by other circuitry well known to persons skilled in the art. In some embodiments, it may be preferred to provide an intermediate switch so that manual inputs can be provided to counter **14**. In that way, the system can be held in any desired step in the control sequence. Similarly, manual inputs can also be provided to set decade counter **14** to a desired count. Manual control inputs **25** and **26** are shown for the clock **15** and decade counter **14**, respectively.

FIG. 1*a* also illustrates indicator **16** which receives signals from decade counter **14**. The count in the counter (representing the timing sequence) is therefore visible to an operator at all times during the operation of the system. Indicators, such as Nixie tubes, are commercially available.

In addition to providing sequence control signals on lines **18**, **19** and **20** to switches **7**, **8** and **9**, respectively, sequence control logic **10** also provides a drive positive signal at T_0 on line **21** to pulse amplifier **22** and a drive negative signal at T_3 on line **23**. The pulse amplifier provides a negative pulse to focus coil driver **24** for decreasing the focus current and a positive pulse for increasing the current.

In one embodiment, two opposite conductivity transistors may be connected in a push-pull arrangement between positive and negative voltages for providing the positive and negative pulses at the output of amplifier **22**. For that embodiment, lines **21** and **23** are connected to the base electrodes of the transistors. Line **27** at the output of amplifier **22** conducts the pulses to the focus coil driver **24**.

The voltage stored on capacitors **11**, **12** and **13** are provided as inputs to comparison logic **28** on lines **29**, **30** and **31**, respectively. The voltage on line **29** is used for comparison purposes when the focus coil current is required to be decreased. The voltage on line **30** is used for comparison purposes when the current in the focus coil must be increased. The voltage on line **31** indicates the steady state condition of the focus coil.

It is pointed out that in a separate embodiment, the offset control circuit **17** may be interposed between capacitor **13** and electrical ground for biasing the steady state voltage to a value other than the normal steady state voltage. For example, if it is desired to focus the electron beam for producing less than the maximum temperature at the workpiece surface, the offset circuit, such as a voltage source with a potentiometer control, could be used to increase or decrease the steady state voltage to obtain any desired temperature at the workpiece surface.

Although the system would function as though the maximum temperature and being achieved at the workpiece surface, the offset voltage provided by offset circuit **17** would shift the maximum temperature to another temperature as a function of the voltage provided by circuit **17**. However, for purposes of describing the preferred embodiment, it is assumed that the offset voltage is zero.

Clock **32** provides control pulses to comparison logic **28** on line **33** in response to an output from the comparison logic at certain times during the operating sequence. The control pulses enable the compared voltages on the lines **29**, **30** and **31** to be gated into the up-down counter **37**. The clock is enabled and disabled by a signal on line **87** as shown in more detail in FIG. **5**.

A count-up signal is generated on line **34** at the output of comparison logic **28** and a countdown signal is generated on line **35** of the comparison logic. The count-up signal is generated at times T_6 and T_7 if the V_{pp} on capacitor **12** is greater than the V_{ss} voltage on capacitor **13**. Similarly, the countdown signal is generated at T_6 and T_7 if the V_{pn} signal on capacitor **11** is greater than the V_{ss} on capacitor **13** at those times.

A manual input to comparison logic **28** from line **36** may be used to manually control the comparison as may be required for test purposes. In the instances when the manual input is being used for controlling the comparison logic, manual controls are also provided to clock **15** and counter **14**.

The outputs from the comparison logic **28** are provided as counting pulses to the up-down counter **37**. For purposes of the Figure 1 embodiment, the up-down counter **37** is an 8-bit counter having bit positions A, representing the least significant digit, through H, representing the most significant digit of the count.

Counter **37** also has a manual input from reset **38** which may be used during certain tests for resetting the counter to a particular count. The counter also provides inputs to indicators **39** for producing a visual indication of the count in the counter. The indicators **39** may be comprised of three Nixie tubes and decoding circuitry or by other visual indicators well-known to persons skilled in the art.

The outputs from the counter **37**, A through H, are provided as inputs to the digital-to-analog converter **42** on lines designated generally by numeral **40**. Each of the lines **40** provides either a relatively high or relatively low voltage to the digital-to-analog converter. For example, if the least significant digit A is a zero, a relatively low voltage is provided, whereas if the least significant digit had been a one, a relatively high voltage would have been provided. The digital inputs are converted to a drive current signal at the output of converter **42** on line **41**. The current is amplified by focus coil driver **24** for providing drive current to the focus coil **3**. An amplifier and emitter follower may be provided between the focus coil driver **24** and coil **3** if required. The amplifier and emitter follower may be included within the coil driver **24** symbol.

A brief description of the operation of system **1** can best be understood by referring to FIG. **2**. FIG. **2** shows a plot of the focus coil current versus temperature. As indicated by the plot, the temperature increases to a maximum value at point **43** as the focus coil current increases. However, if the current is increased past that point, the temperature decreases.

An example of the focus of the beam at point **43** is shown in FIG. **3**. The maximum temperature is represented by the focus of the beam **44** on workpiece **45**. As the focus coil current is increased, as shown in FIG. **2**, the beam focus changes so that it appears as shown by the dotted beam **46**. A decrease of the focus coil current on the opposite side of the maximum point **43** may result in a beam configuration as shown by dotted outline **47**.

In the usual case, the maximum temperature that may be generated by a focus beam is determined as a function of the materials being welded. Once the maximum temperature has been determined, the beam current and accelerating voltage are determined. For example, for welding aluminum, a welding temperature of approximately 1200° F. may be required. Based on that temperature, the welding parameters for generating the electron beam are determined. It is known that by maintaining the beam in a sharp focus on the surface of the workpiece, the temperature of 1200° F. may be maintained.

In operation, clock **15** is turned on to force counter **14** to pass through its counting cycle. At T_0, the **0000** count in the decade counter **14** is decoded by sequence control logic **10** for providing a drive positive signal on line **21** into amplifier **22**. For the duration of that count, a pulse is provided on line **27** into focus coil driver **24**. The output from the driver **24** causes the current in focus coil **3** to increase. At the same time, switch **8** is closed so that capacitor **12** charges to a voltage value representing the temperature of the beam on the workpiece during the T_0 time interval. For purposes of illustration, assume that the beam was initially focused as shown by the beam configuration **48** in FIG. **4**. At T_0, assume that the focus

changed as shown by beam configuration **49** in FIG. **4**. As a result, the temperature at the workpiece would have decreased for the assumed conditions.

An illustration of the example can be seen by referring to FIG. **2**. For example, assume that the initial focus caused a temperature of 900° C. as shown at point **50** in FIG. **2**. The increase in focus coil current would cause the temperature to drop to approximately 600° C. at point **51**.

The drive positive pulse is terminated at the end of T_0 and the system is permitted to return to its steady state condition, i.e. beam configuration **48**, during the time intervals T_1 and T_2. At time T_3, the **0011** count in decade counter **14** is decoded by sequence control logic **10** for providing a drive negative signal on line **23** into pulse amplifier **22**. For the T_3 time interval, a pulse is provided on line **27** into focus coil driver **24** for decreasing the focus current in coil **3**. For the assumed circumstances, the beam focus may change from configuration **48** as shown in FIG. **4** to beam configuration **52** in FIG. **4**. It should be obvious from an examination of FIG. **4**, therefore, that the temperature at the workpiece would have increased.

Refer to FIG. **2** for an example of the change in temperature relative to the decrease in focus coil current. The temperature would increase from 900° C. at point **50** to approximately 1200° C. at point **51**. Switch **7** is closed at T_3 so that capacitor **11** stores a voltage representing the increase in temperature during T_3. During T_4 and T_5, the drive negative pulse is discontinued so that the system can return to its steady state value as represented by point **50** in FIG. **2** and by beam configuration **48** in FIG. **4**.

During T_6 and T_7, the voltages stored on the capacitors **11** through **13** are compared in comparison logic **28**. For the example assumed, the steady state voltage would be greater than the V_{pp} voltage on capacitor **12** and the V_{pn} voltage on capacitor **11** would be greater than the steady state voltage, V_{ss}, on capacitor **13**. At T_6 and T_7 time, clock **32** is enabled if either V_{pn} or V_{pp} is greater than V_{ss}. In other words, if the voltages are equal, the clock is not enabled at T_6 and T_7 time. However, for the example assumed, clock **32** is enabled and the comparison logic gates a signal from comparison logic **28** to up-down counter **37** on line **35**. The countdown signal forces the counter to decrease its count by one. As a result, the output on lines **40** into digital-to-analog converter **42** causes a decrease in the voltage on line **41** to focus coil driver **24**. The current in coil **3** is instantaneously decreased. A voltage representing the temperature of the beam at the workpiece is provided into comparison logic **28** on line **53** so that if either V_{pn} or V_{pp} become equal to the temperature, during T_6 and T_7, the clock **32** is disabled for preventing further changes in the focus coil current.

At T_8 and T_9, the counts **1000** and **1001** of the decade counter **14** are decoded for closing switch **9**. Capacitor **13** is then enabled to charge to a voltage representing the temperature of the workpiece at the end of T_7 time. Since it was determined that the counter **37** was initially too high, and therefore had to be counted down by a signal on line **35**, the beam focus may appear as shown by configuration **53** in FIG. **4** at the end of T_7 time. The temperature for that example may appear as the temperature at point **52** in FIG. **2**.

The cycle is repeated at T_0 until the increase in coil current at T_0 and the decrease in coil current at T_3 cause the temperature at the workpiece to shift from point **54** as shown in FIG. **2**. In that case, V_{pp} and V_{pn} would not be greater than V_{ss} so that the count in counter **0** and, therefore, the output from D–A converter **42** would remain the same. The temperature at the workpiece would be approximately the maximum temperature of 1350° C. as represented by point **43** in FIG. **2**. The beam focus would appear as shown by configuration **44** in FIG. **3**.

FIG. **5** is a schematic diagram of one embodiment of the comparison logic **28** shown generally in FIG. **1**. The comparison logic includes emitter followers **60**, **61**, **62** and **63** between switches **7**. **8** and **9** voltage comparators **64** and **65**. The emitter followers are provided for isolation. The outputs from emitter followers **67** and **68**. Diodes **69** and **70** are also provided at input **71** to gate into capacitor **66** the highest voltage from the emitter followers **68** and **67**. The other input to voltage comparator **66** is taken from the output of amplifier **6** through emitter follower **72**.

The output from voltage comparator **64** is true when V_{pp} is greater than V_{ss}. Similarly, the output from voltage comparator **65** is true when V_{pn} is greater than V_{ss}. The output from voltage comparator **66** is true when either V_{pp} or V_{pn} is greater than V_0.

NAND gates **73**, **74** and **75** receive inputs from voltage comparators **64**, **65** and **66**, respectively. The other inputs B and C to the NAND gates are taken from the decade counter **14**. NAND gate **75** provides a drive signal for the clock **32** at T_6 and T_7 if V_{pp} or V_{pn} are less than V_0.

Switch **76** of the clock is interposed between the oscillator **77** of the clock and the output from NAND gate **75**. The oscillator may be implemented by a unijunction semiconductor device which has its control electrode connected to the collector of the transistor of switch **76**. When the transistor is off, a capacitor at the control electrode is permitted to charge. When the switch **76** is on, the capacitor is discharged so that the oscillator is turned off. Potentiometer **78** varies the resistance of an RC time constant for varying the frequency of the oscillator. The oscillator output may appear as shown by pulse group **79** on line **80**.

NAND gates **73** and **74** provide inputs to NAND gates **81** and **82** which also receive manual inputs. For automatic operation, the manual inputs are connected to a high voltage so that the signal on lines **83** and **84** control the output from NAND gates **81** and **82**, respectively. It is also pointed out that since the B and C inputs to NAND gates **73**, **74** and **75** taken from decade counter **14** are high during T_6 and T_7, the signals on lines **85**, **86** and **87** control the outputs from the NAND gates **73**—**75**. For example, if the signal on line **85** is true during T_6 and T_7, the output from NAND gate **73** is false, whereas if the input on line **85** is false during T_6 and T_7, the output from NAND gate **73** is true.

The outputs from NAND gates **81** and **82** provide the count up (U) and countdown (D) signals on lines **34** and **35**, respectively. The count-up and countdown signals on lines **34** and **35** are provided as inputs to the up-down counter **37**, as shown in FIG. **6**. In addition, the up-down counting signals are provided as inputs to NAND gates **90** and **91** which also receive a clock signal from clock **32** on line **80**.

The count-up signal is true at T_6 and T_7 if V_{pp} is greater than V_{ss}, whereas the countdown signal is true at T_6 and T_7 if V_{pn} is greater than V_{ss}. Both signals are not true or false at the same time. It is pointed out that the count-up and countdown signals are only gated through gates **90** and **91** if V_{pp} or V_{pn} are greater than V_0. The outputs from gates **90** and **91** provide inputs to NAND gate **92** which is used as a clock signal for the first bit position of counter **37**. The counter is described in more detail in connection with FIG. **6**.

If the count-up signal is true at T_6 and T_7, the countdown signal is false. Therefore, when the clock is false, the output from gate **90** will be true. The output from gate **91** will also be true so that the output from gate **92** will be false. However, when the clock signal is true the output from gate **90** will be false, the output from gate **91** will remain true, and the output from gate **92** will become true so that it can be used as a clock signal.

FIG. **6** is a schematic diagram of the up-down counter **37** comprising flip-flops **93** through **100**. Flip-flop **93** is gated by the output from NAND gate **92**. Each succeeding flip-flop is gated by the output from the preceding flip-flop by logic **101** through **107**. For example, the output from logic **101** provides a clock input to flip-flop **94**. The output from flip-flop **94** is provided as a clock input to flip-flop **95** through logic **102**. The output from the logic gates **101** through **107** is either high or low as a function of the up and down inputs taken from lines **88** and **99** as shown in FIG. **5**. If the up input is high, the true output from the flip-flops is gated through to the next in-

put. For example, if the up input is high for the first bit position of the counter, the A output is gated through NAND gates **108** and **109** to the clock input of flip-flop **94**. If the down input had been true, the $\overline{A}$ input would have been gated through NAND gate **110** and NAND gate **109** to the clock input to flip-flop **94**. A similar explanation is true for the remaining bit positions of the counter **37**.

In addition, the true, i.e. A, B, C, D, E, F, G, and H outputs from the flip-flop are provided as inputs to the A to D converter **42**. For convenience, only one bit position, the least significant digit, of the A to D converter is shown. The other bit positions are shown as blocks for convenience. The output from all the bit positions are summed at point **111** with the pulsed output from pulse amplifier **22** to provide an input signal to the focus coil driver **24**.

The circuitry for generating the voltage representing the least significant digit comprises transistor **112** which is turned on by the A signal from flip-flop **93**. The signal is divided across resistors **113** and **114** at the base of the transistor. Resistor **115** is provided as a load resistor between the collector of the transistor and a voltage source +V. The output from transistor **112** is taken from its collector. The voltage at the collector and the voltage, −V at one side of resistor **116**, provide a control voltage at the base electrode of transistor **118**. Resistor **117** is provided between the collector of transistor **112** and the base electrode of transistor **118**.

When transistor **112** is on, transistor **118** is off. When transistor **112** is off, transistor **118** is on. When transistor **118** is on, point **119** is connected to ground and 0 volts are provided at the least significant digit. When transistor **118** is off, the +V volts are divided across resistors **120** and **121** to provide a voltage at point **111** representing the least significant digit.

For purposes of illustrating one example, the +V and −V voltages may be 5 volts and the **120** and **121** resistors may be 2k and 510k, respectively. The resistors of the corresponding stages between corresponding points **119** and **111** are consecutively reduced by a factor of approximately two so the resistor at the most significant digit would be approximately 1.3k for the example given.

FIG. **7** is a circuit diagram of switch **9** shown generally in FIG. **1**. The other switches **7** and **8** may be implemented by similar circuitry. The switch comprises transistor **122** which receives an input signal from the sequence control logic on its base electrode. The signal from the sequence control logic **10** is divided across resistors **123** and **124**. The collector of the transistor **122** is tied to a voltage source V through resistor **128**. The output is provided from the collector across resistor **125** to the gate electrode of field effect transistor **126**. The gate electrode of transistor **126** is biased by voltage −V across resistors **127** and **125**. The voltage at the gate electrode of transistor **126** changes as a function of the off or on condition of transistor **122**.

When transistor **126** is on, capacitor **13** is charged with voltage V_0 appearing on the other electrode of the field effect transistor **126**. The transistor is turned on at T_8 and T_9 when the signal at the gate of transistor **122** is low. At that time, the transistor **122** is turned off so that the voltages V and −V are divided between resistors **127**, **128** and **125** to turn transistor **126** on.

FIG. **8** is an illustration of the sequence control logic **10** shown generally in FIG. **1**. The sequence control logic may be implemented by four NAND gates **129** each receiving ABCD output signals from decade counter **14**. The NAND gates **129** invert the ABCD signals and provide input signals to NAND gate **130**. In addition, the $\overline{C}$ and $\overline{D}$ output signals are provided as input signals to NAND gate **131** and switch **9** respectively. The $\overline{D}$ signal is false only during T_8 and T_9. However, since it is low, transistor **122** is turned off for enabling the conduction of transistor **126** of switch **9**.

$\overline{C}$ is high during T_3 time. However, since the other inputs A and B to NAND gate **131** are also high during T_3 time, the output from NAND gate **131** is low and switch **7** is turned on to permit the storing of V_0 on capacitors **11**.

At T_0, the outputs from NAND gates **129** are all true so that the output from NAND gate **130** is low. The low output from NAND gate **130** turns switch **8** on so that capacitor **12** can store the V_0 voltage.

NAND gate **130** provides an input into pulse amplifier **22** on line **21**. NAND gate **131** provides an input into **132** which inverts the output from **131** to provide an input to pulse amplifier **22** on line **23**. At T_3, the A and B inputs to NAND gate **131** are high and the $\overline{C}$ input is high. As a result, the output is low, inverted through NAND gate **132** to provide a high input on line **23** to pulse amplifier **22**. As a result of the high input to pulse amplifier **22**, a negative output pulse is provided on line **27** to the summing point at the output of D to A converter **42**.

FIG. **8** also illustrates one embodiment of the pulse amplifier **22**. The amplifier includes resistors **133** and **134** between the output on NAND gate **132** and voltage source −V. The resistors provide a voltage divider which enables transistor **135** to turn on as a function of the output from NAND gate **132**. When transistor **135** is on, voltage −V is dropped across resistor **136** to electrical ground. When transistor **135** is off, the −V voltage is dropped across resistors **136** and **137** to provide a negative pulse at the output of the driver on line **27**.

Resistors **138** and **139** provide a voltage divider between NAND gate **130** and voltage source −V for enabling transistor **140** to turn on as a function of the output from NAND gate **130**. When the transistor is off, voltage +V is dropped across resistors **142** and **143** to provide a plus voltage output from the driver on line **27**. Only one of the transistors **135** and **140** are turned off at a time. The transistors are consecutively turned off to provide a plus pulse for increasing the focus coil current and a negative pulse for decreasing the focus coil current as previously described.

We claim:

1. A system for controlling the focus of an electron beam on a workpiece, said system comprising,

means for sequentially changing the focus of the beam during certain time intervals,

means for sequentially sensing the temperature at the workpiece as the focus is changed including means for storing voltages representing the temperature during each sensing sequence and for representing the steady state temperature,

means for comparing said stored voltages for changing the current through the focused coil to a new steady state value as a function of the relative values of each sensed temperature.

2. The system recited in claim **1** wherein said focus is initially changed in one direction during one time interval and then in the opposite direction during a subsequent time interval,

said means for sensing including means for storing a voltage indicating the temperature at the workpiece during the time intervals whereby by comparing the stored voltages to the voltage representing the steady state temperature, the means for comparing generates a signal for increasing or decreasing the focus coil current for increasing or decreasing the temperature at the workpiece until a predetermined temperature has been sensed.

3. The system recited in claim **1** further including counter means responsive to the means for comparing for increasing or decreasing its count as a function of the voltages stored during the sensing sequences relative to the stored voltage representing the steady state temperature at the workpiece.

4. The system recited in claim **3** including means responsive to said counter means for maintaining the current in said coil a value represented by the count in said counter means, until changed during a subsequent sequence if said sensed voltages are not approximately equal.

5. The system recited in claim **3** further including clock means responsive to a difference in said voltages for actuating a counter during certain sequences of said system's operation and for interrupting said counter when the voltages are equal.

6. The system recited in claim **3** further including means for converting the count into a drive current, said drive current

being provided through a focus coil for focusing said electron beam.

7. The system recited in claim 1 further including means for generating a recycling sequence of pulses for controlling the operating sequence of said system,

said focus being changed during each cycle until a maximum temperature has been sensed at the workpiece.

8. The system recited in claim 1 including means for biasing said means for sequentially sensing for indicating a temperature, which is different from the temperature sensed at the workpiece whereby said beam can be focused for producing a temperature other than the maximum temperature at the workpiece.

9. The system recited in claim 1 wherein said means for sequentially sensing comprises a plurality of switches including a first switch for storing a voltage as the focus of the coil is increased, a second switch for storing a voltage as the focus of the coil is decreased, and a third switch for storing a voltage indicating the steady state temperature of the electron beam on the workpiece.