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(73) Octrooihouder(s):
**Stichting Energieonderzoek Centrum Nederland te Petten.**

(72) Uitvinder(s):
**Jochen Löffler te Petten.**
**Evert Eugène Bende te Petten.**
**Johannes Adrianus Maria van Roosmalen te Petten.**
**Ian John Bennett te PETTEN.**

(74) Gemachtigde:
**ir. C.M. Jansen c.s. te Den Haag.**

(54) **Assembly of photo-voltaic cells and method of manufacturing such an assembly.**

(57) An assembly of photovoltaic cells is assembled using cells in the form of strips cut from wafers, or wafers forming such cells. The cells are with edges facing each other. Base and emitter areas on a same planar surface of the cells extend towards the adjacent edges of successive cells. Electrical connections between base areas of a first cell and emitter areas of the second cell are created by depositing electrical conductor material, such as a conduct or paste or electrolyte on cells and running between the cells as they have been placed. Solid electrical connections are subsequently formed from the material on and between the first and second cells. An electrically insulating material may be provided in a space between the edges, the electrical conductor material between the cells being deposited on the electrically insulating material. The electrical conductor material between the cells may form a bend to connect base and emitter areas that are located at an offset from each other.

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Title: Assembly of photo-voltaic cells and method of manufacturing such an assembly

## Field of the invention

The invention relates to a method of manufacturing an assembly of photo-voltaic cells and to an assembly of photo-voltaic cells.

## Background

It is conventional to connect photo-voltaic cells in series so as to obtain an output voltage that is the sum of the voltages of the individual photo-voltaic cells.

A photo-voltaic cell, such as a solar cell, comprises a semi-conductor body wherein incoming light excites free charge carriers, which flow as electric current to the terminals of the cell. As used herein, a semi-conductor body may comprise both a semi-conductor substrate wherein the incoming light excites the free charge carriers, emitter and surface field layers and layers such as dielectric layers and/or conductive layers on the substrate, the surface field layer and/or the emitter layer. In the surface field layer the net doping has the same conductivity type as in the substrate and in the emitter layer the net doping has opposite conductivity type. Typically, the surface field layer has enhanced doping concentration than the substrate. In the following, the surface field layers and surface areas/regions with or without enhanced doping will be referred to as base layers and base areas/regions. It is known to realize the terminals by means of metal tracks on the cell, on electric contact with the base and emitter layers. The metal tracks may be formed by printing tracks of conductive paste or ink on the surface of the cell, followed by a sintering step for sintering metal grains in the paste or ink.

In an interdigitated back contact cell (IBC cell) an alternating pattern of parallel narrow linear base and emitter areas is provided on the back surface of the cell, with metal tracks on the base and emitter areas. A conventional IBC has bus bars perpendicular to the tracks to collect current from the tracks. At one end the metal tracks on the base areas are connected to a first bus bar and at the other end the metal tracks on the emitter areas are connected to a second bus bar. In an IBC

cell, the base areas are usually much narrower than the emitter areas, to reduce loss of minority charge carriers in the bulk.

Conventionally, a series connection of photovoltaic cells is realized by placing cells side by side and soldering an electrically conductive tab or wire to bus bars of a pair of cells. Thus, the manufacture of an assembly of photo-voltaic cells comprises two steps of applying conductors: one on individual cells to contact the semi-conductor material and one between cells to connect the cells in series. In the first step an interdigitated pattern of electrically conductive fingers is applied on the base and emitter areas and wider conductor areas called bus bars are provided perpendicularly to the fingers on either side of the interdigitated pattern, in contact with the base and emitter areas respectively. In the second step the cells are placed side by side and the bus bars of adjacent cells are connected by soldering tabs to the bus bars.

WO2010057674 has proposed to forego the need for bus bars using electrically conductive wires directly soldered on the fingers of adjacent cells as a series connection. Soldering the wires along the length of the fingers reduces the output resistance because the relatively high resistance of the long and thin fingers is connected in parallel with the lower resistance of the wires. More cell area can be used for current collection because the bus bars can be omitted. However, application of wires to the thin fingers complicates assembly.

GB 2459274 describes a photo-voltaic cell design with a semi-conductor on glass structure, wherein strips of bulk semi-conductor underneath successive pairs of parallel linear base and emitter areas are electrically separated from one another, for example by cutting trenches through the bulk and optionally depositing isolator material in the trenches. This makes it possible to make use of a series connection of adjacent strips, which is provided by adding an electrical connection of the linear base area of one strip to the linear emitter area of the next strip along the entire length of the strip. GB 2459274 proposes to use chemical vapor deposition of an Al layer for this purpose, followed by local etching of the Al layer between the linear base and emitter areas on the same strip, so as to prevent a short circuit.

This type of assembly of photovoltaic cells has the problem that the cell strips have a width in the order of the pitch of the base- and emitter areas, which means that the strips will be very narrow e.g. at most a few millimeters. The narrow

width increases the relative significance of perimeter effects like recombination losses, which in turn imposes increased demands on passivation. Furthermore, the manufacturing method of
GB 2459274 is mainly practicable when the strips are not handled separately: the narrow width makes separate handling difficult.

## Summary

Among others, it is an object to provide for an improved series connection of photo-voltaic cells in an assembly of photovoltaic cells.

A method of manufacturing an assembly of photovoltaic cells according to claim 1 is provided. The cells have first and second edges, with alternating elongated base and emitter areas manufactured on a same planar surface extending between the edges. The alternating emitter and base areas may alternate directly, but alternatively areas with other properties may be provided between the alternating emitter and base areas. Each cell may be an IBC wafer, or the cells may be strips cut from one or more of such IBC wafers. Preferably the elongated base and emitter areas extend up to the edges, but alternatively one or both of these areas need not reach up to the first and second edges. A first and second cell are placed adjacent to each other with the first edges of the cells facing each other.

Subsequently, electrical connections are formed between pairs of respective base and emitter areas of the first and second cell. The electrical connections are formed by depositing electrical conductor material on the first and second cell and between the cells, and forming electrical contact to the base and emitter areas and the insulating material along tracks. This makes it possible to connect interdigitated base and emitter areas of different cells directly in series. A bus bar is not needed, so that cells without bus bars may be used, such as strips cut from a larger wafer.

In an embodiment, the electrical conductor material between the cells is deposited on electrically insulating material provided in a space between the first and second cell. The space filled with electrically insulating material need not be the entire space between the cells. The space with electrically insulating material may extend all the way down to the level of the opposite surface of the cells and/or over

the entire length of the interface between the cells, but it need not do so. The space may be limited to a layer near the level of the surfaces of the cells on which the base and emitter areas are provided, and/or to parts of the length.

The electrical conductor material between the cells may consist entirely material substantially at a level of the surface of the cells on the electrically insulating material or even above, i.e. between the cells as seen from a direction perpendicular to the surface of the cells. But the electrical conductor material between the cells may also comprise material at other levels between the levels of the front and back surface of cells, in this case between the cells as seen in a direction parallel to the surface of the cells.

The cells may have layout with a succession of identical pairs of respective ones of the parallel base areas and the emitter areas, with half size base and emitter areas near the edges of the cells on opposite sides of the succession of pairs. Thus current mismatch between the last connected base and emitter areas near the edges can be avoided. Reduced mismatch is possible also with base and emitter areas of other sizes used, when at least one of the base and emitter areas is smaller than the corresponding base or emitter areas size in the pairs.

In a further embodiment an additional narrow unconnected base or emitter area may be present at one edge beyond the last connected emitter or base area so that the same type of area (base or emitter) is present at both edges. This avoids risks of short circuits and eases manufacturing.

The track shaped contact may be formed as part of the deposition, e.g. by printing the electrical conductor material in a pattern of tracks, or plating on a precursor that has been applied in such a pattern, or by first forming an electrically insulating layer with an opening in the form of the track and depositing a blanket layer of conductor material over this layer and into the opening. Alternatively, the tracks may be formed afterwards, for example by removing electrical conductor material that has been applied in a blanket layer first, e.g. by plating or physical vapor deposition. When the cells are obtained by cutting strips from wafers, part or all of the tracks on the cells may be formed prior to cutting, the part of the track on the insulating material being added afterwards. This gives more freedom in selecting the type of track on the cells. In this way a better contact with the semi-conductor may be ensured. In an embodiment, the part of the tracks on the cells that is formed prior to

cutting extends up to the first and/or second edge of the cell. In another embodiment the part of the tracks on the cells that is formed prior to cutting is separated from the edges by an area of the cell where no track is formed or left prior to cutting. This may reduce effects of cutting.

In an embodiment a series connection of more than two cells is used, wherein each pair of successive cells is connected in this way. Further conductor tracks may be applied that cross from the other strip to the next and so on to form contacts with the base and emitter surface areas on adjacent strips. The shape of the conductor tracks may be formed when the tracks are applied to the strips, or it may be defined previously on a substrate, the strips being arranged in a row by placing them on the substrate that already carries or contains the tracks.

In an embodiment the tracks have first and second parts extending in parallel to the elongated parallel base and emitter areas on the first and second cells respectively, at an offset in the first direction with respect to each other, and a third part on the electrically insulating material bridging at least part of said offset. In this way it is not necessary to align the parts of the track on different cells. For more effective passivation, it may be desirable to use tracks with widths that are smaller than those of the underlying emitter and/or base areas. For low resistance it is desirable to use tracks substantially in the middle of the emitter and/or base areas. Such constraints can make it impossible to align the tracks without using relative position shifts between successive cells. Such shifts may be awkward to realize. By using the insulator material between the cells to bridge lateral offsets between the parts of the track on different cells, more freedom in the position of the cells is possible without substantial deviations from the desirable position of the tracks on the cells themselves. In an embodiment, the tracks extend parallel to the edges of the base and emitter areas up to the edges of the cells. But alternatively, an insubstantial part of the track on the base and emitter areas near the side may deviate for example over a distance from the side of the cell that is no more than the distance between the cells.

In an embodiment the part of the track on the insulating material may comprise a curved bend, which provides for excess length of the track compared to a minimum length needed to bridge the offset. In this way it is made possible that the track deals with strain between the cells.

In another embodiment, tracks parts on the emitter and base areas may have respective different widths. In this way relatively more of the emitter area may be used for the track for example than if the track parts on the base and emitter areas have the same widths. In this way different trade-offs between maximum passivation and minimum resistances may be used on the emitter and base. In an extreme, the tracks may cover a majority of the width of the emitter and/or base areas. Use of the strips wherein the emitter and base regions have less length than in a complete semi-conductor wafer from which the strips have been cut reduces the series resistance of an assembly of photo-voltaic cells that are connected in series. Use of parallel conductor tracks that form both connections between different strips and contacts to the base and emitter areas of the strips reduces the complexity of the manufacturing process. Arrangement of the strips with the cuts facing each other makes it possible to reduce the effect of the resistance of the fired conductor tracks, which is higher or equal than that of added conductor wires. Herein the use of wide strips cut from larger semi-conductor bodies with pre-manufactured base and emitter areas, so that the strip width in the base emitter elongation direction is larger than the width of base/emitter area pairs in the direction transverse to that elongation direction (e.g. at least ten times larger), reduces recombination losses at the perimeter, compared with strips whose width contains only one base/emitter area pair.

Brief description of the drawing

These and other objects and advantages will become apparent from a description of exemplary embodiments, using the following figures

Figure 1 shows plane view of an assembly of rectangular photo-voltaic strips

Figure 2 shows a cross-section through the assembly of photo-voltaic strips

Figure 3 shows a flow chart of manufacturing the assembly

Figure 4 shows a substrate for mounting photo-voltaic strips

Figure 5a shows an edge strips

Figure 5b-d show rows of strips

Figure 5e shows a strip or use in a row of strips

Figure 6a,b show strips with wide emitter surface areas

## Detailed description of exemplary embodiments

Figure 1 shows a plane view of an assembly of rectangular photo-voltaic strips 11, the rectangular shape having a first and second size along an x and y direction (horizontal and vertical in the plane of the drawing respectively). The first size is smaller than the second size or equal. Each strip 11 has alternating base surface areas 10 and emitter surface areas 12 (indicated by references on only one of strips 11). The base and emitter surface areas are parts of the surface below which the strips 11 contain a base and emitter respectively. As used herein, base and emitter surface areas refer both to areas wherein the base and emitter are directly adjacent the surface and areas wherein one or more layers like an oxide layer lie between the surface and the base and emitter. The base and emitter are provided at a surface of a semiconductor wafer, that is, by diffusion into the surface or by providing a base and/or emitter layer on the surface. For reference the base areas have been shaded. The emitter and base regions may be directly adjacent to each other or there may be a small area in between them of other properties, e.g. of lower doping or a passivated area. Although base surface areas 10 and emitter surface areas 12 are shown to extend up to the edges, it should be realized that alternatively one or both of these areas may be separated from one or both edges, e.g. by a surface area of lower conductivity (doping), a passivated area or a trench. This may reduce edge effects due to cutting.

Strips 11 are arranged successively along a row in the x direction (with exaggerated distances between the strips). In the illustrated embodiment, emitter surface areas 12 are aligned with base surface areas 10 of adjacent strips 11 and vice versa. Although five strips 11 with four base surface areas 10 and four emitter surface areas 12 are shown by way of examples, it will be understood that a different number of strips and /or a different number of surface areas may be used. Although a row of strips is shown, it should be appreciated that alternatively a row of columns may be used, wherein each column may contain one or more strips 11 successively along the y-direction, each with base and emitter surface areas 10, 12 alternatingly along the y-direction.

Conductor tracks 14, 16 (only two indicated by references) are each provided on the surface areas of a pair of adjacent strips. Each conductor tracks 14, 16

is provided on the base surface area of a first strip of the pair and on the emitter surface area 12 of the second strip of the pair, continuing from the first to the second one of the strips of the pair. Conductor tracks 14, 16 form electrical connections between the base and emitter surface areas. For each of the strips 11, except the rightmost strip in the row, first conductor tracks 14 connect base surface areas 10 of the strip 11 to emitter surface areas 12 of the next neighboring strip 11 on the right. For each of the strips 11, except the leftmost strip in the row, second conductor tracks 14 connect emitter surface areas 12 of the strip 11 to base surface areas 10 of the next neighboring strip 11 on the left. The base surface areas 10 on the rightmost strip 11 and the emitter surface areas 12 on the leftmost strip 11 at the ends of the row may be connected to electrical terminals by further conductor tracks (not shown).

As will be appreciated, the illustrated connections apply to embodiments wherein an even number of strips 11 is used. When an odd number is used base surface areas 10 on the rightmost and leftmost strip 11 may be connected to the external terminals, emitter surface areas 12 on the rightmost and leftmost strip 11 being connected to base surface areas on the strips to the left and right of the rightmost and leftmost strip 11 respectively. Alternatively, the emitter surface areas 12 on the rightmost and leftmost strip 11 may be connected to the external terminals. Furthermore, it should be noted that the connection pattern shown in the figure is only one simple example of possible connections. More complicated connections are possible and additional components such as diodes may be included in connections. In one embodiment, a meandering pattern of connections may be used.

Figure 2 shows a cross-section through the assembly of rectangular photovoltaic strips 11 and conductor tracks 14, mounted on an optically transparent substrate 20, which may be a glass substrate for example. In another embodiment the conductor tracks 14 may be provided between the surface of strips 11 and substrate 20. In this case a non-transparent substrate may be used. A reflective substrate may be used for example.

In operation, when strips 11 are exposed to light, electrical potential differences arise between the base and emitter surface areas 10, 12 of each strip 11, as is known per se. Conductor tracks 14, 16 electrically connect the strips in series so that the potential differences are summed, giving rise to a sum potential difference between the emitter surface areas 12 of the leftmost strip 11 and the base surface

areas 10 of the rightmost strip 11. When an electrical load is connected to the external terminals of the assembly, net current flows from a first external terminal through a surface area on the first strip in the row, to another surface area on that first strip and from there via one of the conductor tracks to a surface area on the next strip and so on through successive strips, until the second external terminal is reached.

Figure 3 shows a flow chart of manufacture of the assembly. In a first step 31 a photovoltaic wafer with alternate base and emitter layers, but as yet without conductor tracks to contact these areas, is prepared using any known method. This may include diffusion steps, wherein doping material of mutually opposite conductivity types is made to diffuse into the surface of a semi-conductor wafer. In layers in areas that form base and emitter areas, doping of mutually different conductivity type may form the majority. A base layer is formed with enhanced doping of the same conductivity type as the semi-conductor wafer. An emitter layer with the opposite conductivity type as the semi-conductor wafer. In an exemplary process, one of a base or emitter layer is formed first on the entire back surface and subsequently the other of the base or emitter layer is formed locally in regions. In alternative implementations of the first step 31, an applied layer or layers of semiconductor material on the semi-conductor wafer may be used to form the base and emitter surface areas in a hetero-junction structure or combinations thereof. A TCO (transparent conductive oxide) region, metal layer region or other conductor may be provided on the material on the substrate that forms the hetero-junction, to serve as a conductor track, or as a seed for forming a conductor track. First step 31 may comprise other known sub-steps, such as texturing, applying one or more dielectric layers, applying one or more conductive oxide layers etc. The resulting wafer comprises base and emitter surface areas of rectangular shape, with a longest side in a first direction (the x direction). The base and emitter surface areas may be 100 millimeters or more long for example. 156 millimeter is currently a standard size. The base and emitter surface areas alternate in the second direction (the y-direction). The width of a combination of a base and emitter area in the y-direction may be between 0.5 to 50 millimeters for example, with a fraction of 0.3 to 0.99 taken up by the emitter area.

In a second step 32 the photovoltaic wafer is cut into strips along cuts that extent in the y-direction, i.e. cuts that are perpendicular to the longest direction of the

rectangular shape of the areas on the wafer. Cutting may be performed by dicing, laser cutting, laser grooving followed by breaking, wet chemical etching, or cleaving e.g. by thermal laser separation or stealth dicing for example. Use of a cut surface has the effect that strips are obtained that do not have parasitic diffusion at the cut edges, which may arise if diffusion is applied to a strip. Similarly, a dielectric layer that is grown prior to cutting will not show edge growth effects. The strips may have a width of 10 to 50 millimeters from cut to cut for example. The strips may have a length in the y direction of more than 100 millimeters millimeter for example, the size of a wafer or parts thereof, e.g. length and width are similar or equal. As a result of the cuts, the length of the base and emitter surface areas in the x-direction on the strips is a fraction of their length on the wafer.

In a third step 33 the strips are placed side by side in a row on an optically transparent substrate. Strips cut from the same wafer may be placed side by side, but alternatively strips from different wafers may be placed side by side, or a mix of strips from the same wafer and from different wafers may be placed side by side. 2 to 100 strips may be placed in the row for example. Successive strips in the row succeed each other in the x-direction. The strips are aligned with each other so that base surface areas of each strip are aligned with the emitter areas of the next strip and vice versa. When the strips contain the same number of base surface areas as the number of emitter surface areas, this may be realized by rotating each second strip in the row a hundred and eighty degrees relative to its neighbors. In another embodiment, two types of wafers may be used, a first one with base surface areas on both ends of the strips and a second one with emitter surface areas on both ends of the strips.

In a fourth step 34, electrically insulating filler material is provided in clefts between the strips in the row. A polymer, glass frit, sol-gel may be used for example. This filler material may function as support for the conductor material between the strips. Filler material is provided in clefts between the strips in the row. Although the filler material may fill the entire clefts, alternatively it may fill only part. Alternatively, electrically insulating material may be provided by or on the optically transparent substrate.

In a fifth step 35 conductor material is applied to the row of strips and the filler material, in a pattern of tracks that each extend only over adjacent base and emitter surface areas from a pair of adjacent strips and filler material in between.

Each track may be from 0.01 to 50 millimeters wide for example, but of course not wider than the underlying base or emitter surface area and have length up to approximately the width of two strips from leaving no more than half the width of the strips uncovered to the edge of the strip on the side of the strip over which the track does not extend to the next strip in the row. In an embodiment strips covered with a conductive oxide layer in electrical contact with underlying semi-conductor material may be used, the tracks being applied on the conductive oxide or other conductor. When a conductive oxide layer is used, the conductive oxide layer is preferably patterned in mutually isolated areas over the base and emitter surface areas respectively. Techniques for providing such pattern oxide layers are known per se, e.g. by growing the layer after applying a sacrificial mask that prevents growth on the edge between base and emitter areas, or by selective removal of the oxide on the edge. In an embodiment the conductive oxide may be provided prior to cutting.

The conductor material may be a conventional paste comprising grains of conductive substance, such as Ag or Cu paste that only requires low temperature processing. Alternatively, digital printing like inkjet printing may be used with inks that contain Ag or Cu particles, or the conductor material may be applied by dispensing, physical vapor deposition (PVD) of metals like Ag, Al, Cu, or seeding with one of the above techniques combined with plating.

The conductor material may be applied in a pattern of the tracks by screen printing for example, but other techniques like dot printing, lithographic printing, application of a layer of conductive material followed by selective removal; may be used. In an embodiment different types of conductor materials may be used to print parts of the conductor tracks on the base and emitter surface areas respectively, for example in different printing steps, and optionally using the same or different baking steps for each type. In another embodiment the same material may be used.

Furthermore, conductor material may be applied in tracks that each extends only over a base or emitter surface area on strips at the end of the row, for connection to the external terminal. Each such track may be from 0.01 to 50 millimeters wide for example and leave no more than half the width of the strip uncovered to the edge of the strip on the side adjacent the next strip.

Although a process has been described wherein electrical conductor material is applied to the row of strips in a pattern of tracks in fifth step 35, after

placing the strips side by side, it should be appreciated that alternatively part or all of the conductor material pattern of tracks on the strips may be applied before placing the strips side by side in third step 33, preferably before a second step 32.

A further step comprising a firing through process may be used before cutting, for example, to provide conductor tracks on the strips. As is known per se, firing through process may comprise applying conductor material in tracks, on an electrically insulating layer on the substrate, followed by a heating to make the conductor material penetrate through the electrically insulating layer to the semi-conductor material. In an embodiment a fire through paste with silver grains, glass frit and a binder may be used.

Optionally, a further part of the electrical conductor material may be applied on the strips after cutting, in contact with the electrical conductor material that has been applied on the strips before cutting. This may be done for example together with application of electrical conductor material on the filler material. Plating could be used to grow electrical conductor material on the electrical conductor material that has been applied on the strips before cutting.

In fifth step 35 the row of strips with the applied conductive material may be processed to fix conductor tracks in electrical contact with the base and emitter surface areas. This may comprise heating or drying for example.

In a sixth step 36 the assembly is finished using steps that are known per se. This may comprise connecting conductor wires from external terminals to the tracks that extend only over a base or emitter surface area on strips at the end of the row. Furthermore, this may comprise adding a protective layer etc.

It should be appreciated that the described process is only one embodiment of a process for manufacturing of the assembly of strips. In an embodiment a passivating layer may be provided on the base and emitter surface areas, with openings, the applied conductor tracks running at least partly over the openings.

Furthermore, although an embodiment of the manufacturing process has been described wherein a firing step was used to fire a paste of conductor material, it should be appreciated that other types of conductor material may be applied to form the tracks that do not require firing. Low temperature contact methods are known per se for solar cells.

In another embodiment the tracks of conductor material may be applied on the substrate before placing the strips on the substrate, with the base and emitter surface areas facing the substrate. Alternatively, the strips may be placed in a row and the substrate with the tracks may be placed on the row of strips.

Figure 4 shows a substrate 40 with a pattern of tracks 42, 44 of conductor material that may be used in this embodiment. In addition to tracks 42, 44 bus bars 46a,b are provided, including a first bus bar 46a connected to all the tracks that connect to a single strip at the beginning of the row and a second bus bar 46b connected to all the tracks that connect to a single strip at the end of the row. Bus bars 46a,b may form the external terminals of the assembly. The positions where the strips will be placed on the substrate are indicated by dashed lines 48 (exaggerated distances between the strips). In an embodiment substrate 40 may be a flexible foil.

A similar layout with external terminal in the form of bus bars may be realized when the conductor material is applied directly on the strips. Auxiliary strips, which may have the same thickness as the strips, but which need not be of semi-conductor material may be placed to the left and right of the row of strips. Tracks of conductor material may be applied to the contact strips, extending from the contact strips to each emitter surface area on the adjacent strip of semi-conductor material, or to each emitter surface area on the adjacent strip of semi-conductor material, whichever is not connected to the next strip. The auxiliary strips may be of electrically conductive material, in which case no bus bars need to be applied. Alternatively, the auxiliary strips may be isolators or semiconductors, conductor material being printed on an auxiliary strip to form a busbar and the tracks that extend to the adjacent strip. When the auxiliary strip is of semiconductor material the same material may be used as in the other strips. This prevents different thermal expansion. When the auxiliary strip is of semiconductor material a pattern of base and emitter surface areas is not needed on the auxiliary strip. Figure 5a shows an edge strip 50 and adjacent strip 52 of an assembly, wherein the pattern of base surface areas 54a and emitter surface areas 56a on the edge strip 50 differs corresponds to the pattern of base surface areas 54b and emitter surface areas 56b of the busbar 58 and fingers. The adjacent strip 52 merely has alternating base and emitter surface areas 54b, 56b, with conductor tracks 59 extending from the base surface areas 54b of the adjacent strip 52 to the emitter surface areas 56b on the edge

strip 50. Edge strip 50 and adjacent strip 52 may be part of an array of strips with a further strip next to adjacent strip 52 on the side opposite edge strip 50 and so on, with conductor tracks (not shown) from the emitter surface areas 56b of the adjacent strip to base surface areas on the next strip and so on. As may be noted, the pattern is very similar to that of an interdigitated back contact (IBC) solar cell, with base and emitter fingers, except that strips are cut and each second strip is rotated by a hundred and eighty degrees relative to the next strip and no bus bars are used along the long side of the strips.

Although embodiments have been shown wherein the base and emitter surface areas have equal width in the y-direction, it is preferred to have emitter surface areas that are wider than the base surface areas. This provides for higher efficiency. In conventional interdigitated back surface cells the base areas have a much smaller width than the emitter areas for efficiency reasons (e.g. twenty percent or less of this width). It is preferred that at least one of the following measures are applied: (1) the width of the base and emitter areas is the same, or (2) strips with different layout, or at least differently oriented strips, are used next to each other, or (3) successive are used at an offset along the y-direction, i.e. the direction along the interface between the strips, or (4) connections between base and emitter areas of successive strips extend at least partly in the y-direction.

Figure 5b shows an embodiment wherein strips 500, 502 with base and emitter regions of unequal width are alternately used with a hundred and eighty degrees rotation between successive strips 500, 502. Conductor lines 504, 506 are used to connect base regions 10 and emitter regions 12 of successive strips 500, 502.

Figure 5c shows an embodiment wherein strips 500, 502 with base and emitter regions of unequal width are alternately used at an offset along the y-direction, i.e. the direction of the interface between successive strips 500, 502. Conductor lines 504, 506 are used to connect base regions 10 and emitter regions 12 of successive strips 500, 502.

Figure 5d shows an embodiment wherein strips 500, 502 with base and emitter regions of unequal width are used. Conductor lines 504, 506 between base and emitter areas 10, 12 (labels only indicated for one strip) in successive strips 500, 502 extend at least partly in the y-direction along the interface between the strips 500, 502. As shown conductor lines 504, 506 extend at least partly in the y-direction in the

sense that they run obliquely, in along a direction vector that has components in the x and y direction (the component in the y direction preferably being the largest). But other patterns may be used, such as conductor lines 504, 506 with bends, corners etc. As long as the conductor lines 504, 506 bridge a distance in the y-direction, which will usually be larger than the distance bridged in the x-direction.

It should be noted that the assembly of cells achieve maximum efficiency when the current generating capacities of connected emitter and base regions are substantially equal, i.e. if they receive charge carriers generated by incoming light in same-sized collection areas of the strip. If the collection areas are not equal, the smallest collection area may become determinative of the efficiency.

Special care is needed to reduce the difference between the collection areas of connected regions adjacent the strip edges along the x-direction. A design may be used wherein each strip comprises a number of bands, each band extending in the x-direction between the interfaces to the adjacent strips, each band comprising an emitter region and a base region.

In an embodiment an integer number of equal bands is used, flanked on opposite sides of the strip by a base region of half the size of the base regions in the bands and an emitter region of half the size of the emitter regions in the bands. Use of half the size results in optimum efficiency, but use of less than full size emitter regions at the edges already leads to an improvement. In this type of embodiment successive strips may be mounted rotated by a hundred and eighty degrees relative to one another, so that the half size base region of one strip is adjacent the half size emitter region of the next strip and vice versa. In this case no offset is needed. Figure 5e shows the layout of a strip made according to this design.

It may be noted that figure 5d shows base and emitter regions edges along the x-direction at opposite extreme y coordinates of the strips. This may be difficult to realize because it requires patterned processing (e.g. printing) up to the edge for at least one of these types of region. For example, if an emitter region is first created as a blanket that covers the entire back surface, followed by the addition of local back surface field regions with doping that locally suppress the emitter Therefore, the type of region that is produced by patterned processing is preferably separated from the edge by a (small) region of the other type, as shown in figure 5e. Alternatively, cutting (e.g. laser cutting) may be used to realize a region of a first type (base or emitter) up

to the edge from wafer with a region of the other type between the edge of the wafer and the region of the first type. For efficiency reasons it is desirable to provide the conductors lines on the strips 500, 502 in the middle of the emitter and base regions.

Figure 6a shows an embodiment with strips 11 wherein the emitter surface areas that are wider than the base surface areas. The same elements have been indicated with the same elements as in Figure 1. As may be noted, in this embodiment conductor tracks 14, 16 may be used that have a wider extension in the emitter surface areas 12 than in the base surface areas 10. This provides for lower resistance.

Although embodiments have been shown wherein identical strips are used and wherein, in each strip, the number of base surface areas equals the number of emitter surface areas, it should be appreciated that instead different strips may be used, with unequal numbers of base and emitter surface areas. Figure 6b shows an embodiment with first strips 11a of a first type and second strips 11b of a second type part alternating with one another. The first and second type of strips may be obtained by cutting different types of wafer into strips or by processing two different types of strips on a wafer, the different types of wafer having mutually different patterns of base and emitter surface areas, with patterns in the y-direction that correspond to the strips. The first type of strip has one more emitter surface area than base surface areas. The second type of strip has one less emitter surface area than base surface areas.

Although an embodiment has been described wherein wafers are cut into the strips with cuts perpendicular to the longest side of rectangular shaped base and emitter surface areas, it should be appreciated that alternatively cuts at a different non-zero angle may be used, e.g. at an angle between sixty and a hundred and twenty degrees to the longest direction. In this case, the row of strips may be replaced by a row of columns strips, one or more columns containing more than one strip, which may have different length. Thus less of the wafers may be lost.

Although an embodiment has been shown wherein no conductor tracks were applied on the wafer before cutting, it should be appreciated that additional conductor tracks may be applied on the wafer before cutting. In this embodiment, the conductor tracks that connect different strips may be added after cutting, when the strips have been arranged in a row, or when the strips are placed on a substrate with

conductor tracks. This makes it possible to use a baking, curing or firing step to provide contact to the base and emitter surface areas before cutting.

Although an embodiment has been described wherein both base and emitter surface areas are created before cutting, it should be appreciated that alternatively one could be applied after cutting. For example a phosphor (n-type) diffusion may be applied before cutting and a boron diffusion (p-type) may be applied after cutting. Semiconductor material wherein phosphor has been diffused locally before cutting, in areas where a boron diffusion is needed, or phosphor may be applied to selected areas only. Thus, perimeter effects of at least on of the diffusions may be avoided by applying the diffusion before cutting. Its is also possible to create both base and emitter surface areas on the strips after cutting. This reduces the need to prevent damage to the base and emitter surface areas during cutting, but it increases perimeter effects.

Instead of using diffusion into the semiconductor wafer of the strips to create base and/or emitter surface areas, a layer or layers of doped semi-conductor material may be added on the surface of the semi-conductor material of the strips to form base and/or emitter surface areas, for example to form a heterojunction.

As mentioned, a patterned conductive oxide layer or other conductor, e.g. a metal, e.g. Ag or Al, may be provided on the surface of the wafer before cutting, and the conductor tracks being applied on the conductive oxide.

Although an embodiment has been shown wherein only one row of strips is used in the assembly, it should be appreciated that the assembly may contain a plurality of rows of strips in parallel or series with each other. In this way the desired output voltage can be realized. All conductor tracks on all strips in a row may be applied together in the same step, all conductor tracks on parallel rows of strips may be applied together in the same step.

Although embodiments have been described wherein the electrical conductors are provided between the strips substantially at a level of the back surface of the strips, it should be appreciated that alternatively the electrical conductors between the strips may be partly or wholly provided in the cleft between the strips. For example, when a paste of electrical conductor material is pushed onto the assembly, it may be pushed into the cleft. The electrical conductor material between

the strips may also be provided partly or entirely above the level of the surface of the strips, i.e. not in the cleft between the strips.

Although embodiments have been shown wherein the part of the electrical conductors between the strips is provided on electrical insulating material that is provided in a space between the cells, either at the level of the back surface, above or below, it should be appreciated that alternatively, this electrical insulating material may be omitted, which may simplify the process. For example, the electrical conductor material may reach to the substrate at the bottom of the cleft between the strips. As another example, if the distance between the strips is small, cohesion in a paste of electrical conductor material may be sufficient to allow for electrical conductor material in or over the cleft, with a space between the electrical conductor material and the substrate.

When the electrical conductor material is provided at levels between those of the front and back surface of the strips, the surface of the electrical conductor material may dip below the level of the back surface of the cells. Also, the electrical conductor material may be in contact with the side walls of the strips at the cleft. With strips that have been cut from wafers this need not be a problem, because the resulting side wall will have low doping levels. However, in an embodiment an insulating layer may be provided on the sidewalls, e.g. as a layer that is also used for passivation, before applying the conductor material, to prevent risk of short circuit.

## Conclusies

1. Een werkwijze voor het vervaardigen van een samenstel van foto-voltaische cellen, met gebruik van tenminste een eerste en tweede cel, waarbij elke cel een eerste en tweede rand heeft en langwerpige paralelle basis- en emittergebieden op éénzelfde planair oppervlak van de cel zich uitstrekkend van de eerste naar de tweede rand, waarbij de basis en emittergebieden met elkaar afwisselen in een eerste richting langs de eerste en tweede randen, welke werkwijze omvat

- rangschikken van de eerste en tweede cellen naast elkaar met de eerste rand van de eerste cel gekeerd naar de eerste rand van de tweede cel;
- vormen van elektrische verbindingen tussen respectievelijke van de basisgebieden van de eerste cel en respectievelijke van de emittergebieden van de tweede cel door het deponeren van elektrisch geleidermateriaal aan op de eerste en tweede cel en doorlopend tussen de eerste en tweede cel; en
- vormen van de elektrische verbindingen uit dat materiaal op en tussen de eerste en tweede cellen.

2. Een werkwijze volgens conclusie 1, omvattende het voorzien van elektrisch isolerend materiaal in een ruimte tussen de eerste en tweede cel, deponeren van het elektrische geleidermateriaal tussen de eerste en tweede cel op het elektrisch isolerende materiaal.

3. Een werkwijze volgens één der voorafgaande conclusies, omvattende het snijden van de eerste en tweede cel uit eenzelfde wafel, of uit wafels met identieke lay-out, en het vervolgens uitvoeren van het genoemde rangschikken van de eerste en tweede cel naast elkaar op een substraat.

4. Een werkwijze volgens conclusie 3, waarin het elektrische geleidermateriaal op de eerste en tweede cel tenminste gedeeltelijk

gedeponeerd wordt op de wafel voorafgaand aan snijden en het elektrische geleidermateriaal gedeponeerd wordt tussen de eerste en tweede cel na het rangschikken van de eerste en tweede cellen naast elkaar en het optioneel voorzien van elektrisch isolerend materiaal.

5. Een werkwijze volgens conclusie 3 of 4, waarin de eerste cel en de tweede cel derde en vierde randen hebben die lopen tussen de eindpunten van de derde en vierde randen op tegenoverliggende kanten van de cellen waarbij de eerste cel en de tweede cel identieke lay-out hebben, omvattende een opeenvolging van paren van respectievelijke van de basisgebieden en de emittergebieden, waarbij de emittergebieden van elk paar eenzelfde eerste grootte hebben, waarbij de basisgebieden van elk paar eenzelfde tweede grootte hebben, waarbij een verdere van de emittergebieden een derde grootte heeft die kleiner is dan de eerste grootte en zich bevindt tussen de opeenvolging van paren en de derde rand van de eerste en tweede cel, waarbij een verdere van de basisgebieden een vierde grootte heeft hoogstens gelijk aan de tweede grootte, en zich bevindt tussen de opeenvolging van paren en de vierde rand van de cel, waarbij de eerste cel en de tweede cel gerangschikt worden met eindpunten van de derde rand van de eerste cel en de vierde rand van de tweede cel naast elkaar en vice versa.

6. Een werkwijze volgens een der voorafgaande conclusies, waarin het contact langs de sporen wordt gevormd door het deponeren van het elektrische materiaal op de basis en emittergebieden en tussen de eerste en tweede cellen selectief in sporen waarin het elektrische geleidermateriaal wordt gevormd tot elektrisch contact met de basis- en emittergebieden na het rangschikken van de eerste en tweede cellen naast elkaar.

7. Een werkwijze volgens een der voorafgaande conclusies, waarin tenminste één spoor gevormd wordt waarin het elektrisch geleidermateriaal in elektrisch contact is met de basis- en emittergebieden, waarbij het spoor het eerste en tweede spoorgedeelte heeft die zich respectievelijk uitstrekken

parallel aan de langwerpige paralelle basis- en emittergebieden op de eerste en tweede cellen met een offset ten opzichte van elkaar in de eerste richting en een derde spoorgedeelte tussen de eerste en tweede cel dat tenminste een gedeelte van genoemde offset overbrugt.

8. Een werkwijze volgens conclusie 7 waarin de eerste en tweede spoorgedeelten zich respectievelijk uitstrekken tot aan genoemde eerste en tweede randen van de eerste en tweede cellen.

9. Een werkwijze volgens een der voorafgaande conclusies, waarin de eerste en tweede spoorgedeelte respectievelijk in hoofdzaak halverwege tussen grenzen van de basis- en emittergebieden met aangrenzende emitter- en basisgebieden op dezelfde cel gevormd worden.

10. Een werkwijze volgens een der voorafgaande conclusies, waarin de basisgebieden een smallere breedte hebben in de eerste richting dan de emittergebieden, waarbij tenminste één van de sporen een eerste spoorgedeelte heeft op het basisgebied dat smaller is in de eerste richting dan een tweede spoorgedeelte van het tenminste ene spoor op het emittergebied.

11. Een werkwijze volgens één der voorafgaande conclusies, omvattende het snijden van de cellen uit een wafel of wafels, omvattende de basis- en emittergebieden, waarbij de cellen gesneden worden met gebruik van een snede of snedes dwars op genoemde lengterichting.

12. Een samenstel van foto-voltaische cellen omvattende

- een eerste en tweede cel geplaatst naast elkaar waarbij elke cel een eerste en tweede rand heeft en langwerpige paralelle basis- en emittergebieden op eenzelfde planair oppervlak van de cel, zich uitstrekkend van de eerste naar de tweede rand, waarbij de basis- en emittergebieden elkaar afwisselen in een eerste richting langs de eerste en tweede randen, waarbij de eerste rand van de eerste cel en de eerste rand van de tweede cel naar elkaar toegekeerd zijn;

- elektrisch geleidermateriaal gevormd in elektrisch contact met de basis- en emittergebieden en tussen de eerste en tweede cellen, waarbij elk spoor zich uitstrekt over een respectievelijk paar van één van de basisgebieden van de eerste cel en één van de emittergebieden van de tweede cel en tussen de eerste en tweede cel.

13. Een samenstel volgens conclusie 12, omvattende elektrisch isolerend materiaal in een ruimte tussen de eerste en tweede cel, waarbij het elektrisch geleidende materiaal tussen de eerste en tweede cel gedeponeerd is op het elektrisch isolerende materiaal.

14. Een samenstel volgens conclusie 12 of 13 waarin de eerste cel en de tweede cel elk derde en vierde randen hebben die lopen tussen eindpunten van de eerste en tweede randen, waarbij de eerste cel en de tweede cel een identieke lay-out hebben, waarbij de lay-out een opeenvolging van paren van respectievelijke van de basis- en de emittergebieden bevat waarbij de emittergebieden van elk paar eenzelfde eerste grootte hebben, waarbij de basisgebieden van elk paar eenzelfde tweede grootte hebben, een verdere van de emittergebieden die een derde grootte heeft die kleiner is dan de eerste grootte zich bevindt tussen de opeenvolging van paren en de derde rand van de eerste en tweede cel, een verdere van de basisgebieden die een vierde grootte heeft die ten hoogste gelijk is aan de tweede grootte zich bevindt tussen de opeenvolging van paren en vierde rand van de cel, waarbij de eerste cel en de tweede cel geplaatst zijn met eindpunten van de derde rand van de eerste cel en de vierde rand van de tweede cel naast elkaar en vice versa.

15. Samenstel volgens conclusie 12 tot 14, waarin de lay-out een aanvullend emittergebied of een aanvullen basisgebied bevat respectievelijk tussen de verdere van de basisgebieden en de derde rand of tussen de verdere van de emittergebieden en de vierde rand, waarbij het aanvullende

emittergebied of het aanvullende basisgebied geen eigen externe aansluiting heeft.

16. Een samenstel volgens een der conclusies 12 tot 15, waarin de verdere van de emittergebieden in hoofdzaak half de grootte heeft van de emittergebieden in genoemde paren.

17. Een samenstel volgens foto-voltaische cellen volgens een der conclusies 12 tot 16, waarin tenminste één van de sporen een eerste en een tweede spoorgedeelte bevat die zich respectievelijk parallel aan de langwerpige parallelle basis- en emittergebieden op de eerste en tweede cellen uitstrekken, met een offset in de eerste richting ten opzichte van elkaar, en een derde spoorgedeelte op het elektrisch isolerende materiaal dat tenminste een gedeelte van genoemde offset overbrugt.

18. Een samenstel van foto-voltaische cellen volgens conclusie 17, waarin de eerste en tweede spoorgedeelte zich tot aan de eerste en tweede rand van respectievelijk de eerste en tweede cellen uitstrekken.

19. Een samenstel van foto-voltaische cellen volgens conclusie 17 of 18, waarin het derde spoorgedeelte is gevormd met een gekromde bocht in het derde spoorgedeelte, waarbij de bocht voorziet in overmaat aan lengte van het derde spoorgedeelte vergeleken met een minimum lengte die nodig is om de offset te overbruggen.

20. Een samenstel van foto-voltaische cellen volgens een der conclusies 12 tot 19, waarin de eerste en tweede gedeelte van de sporen in hoofdzaak halverwege liggen tussen grenzen van de basis- en emittergebieden aan elkaar.

21. Een samenstel van foto-voltaische cellen volgens een der conclusies 12-20, waarin de basisgebieden smallere breedte hebben in de eerste richting dan de emittergebieden, waarbij tenminste een van de sporen een eerste gedeelte op het basisgebied hebben dat smaller is in de eerste richting dan een tweede gedeelte van het tenminste ene spoor op het emittergebied.

22. Een samenstel van foto-voltaische cellen volgens een der conclusies 12 tot 21, omvattende het snijden van cellen uit een wafel of wafels, die de basis- en emittergebieden omvatten waarbij de cellen gesneden worden met een snede of snedes dwars op genoemde langwerpige richting.

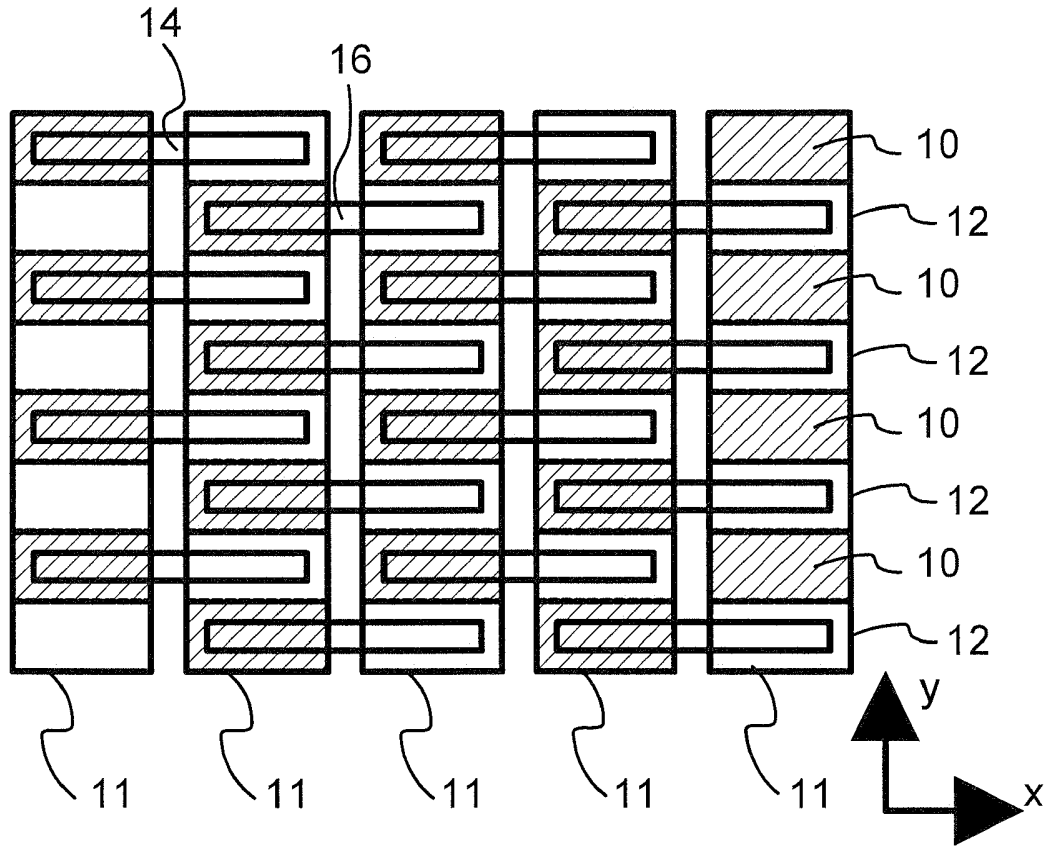



Fig.1

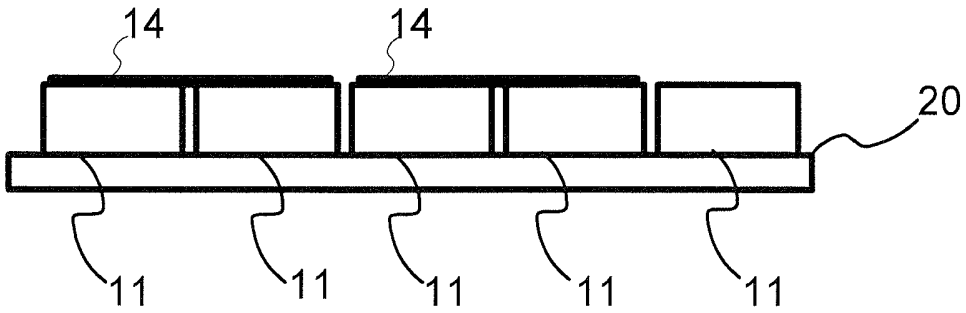



Fig.2

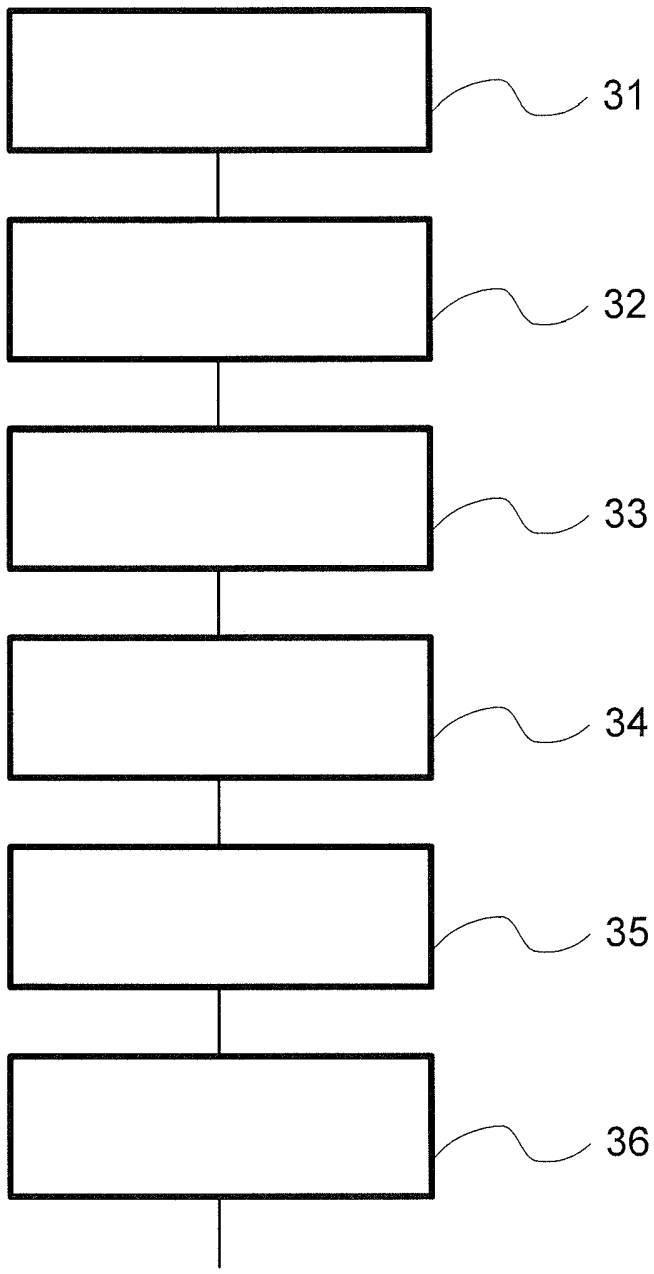



Fig.3

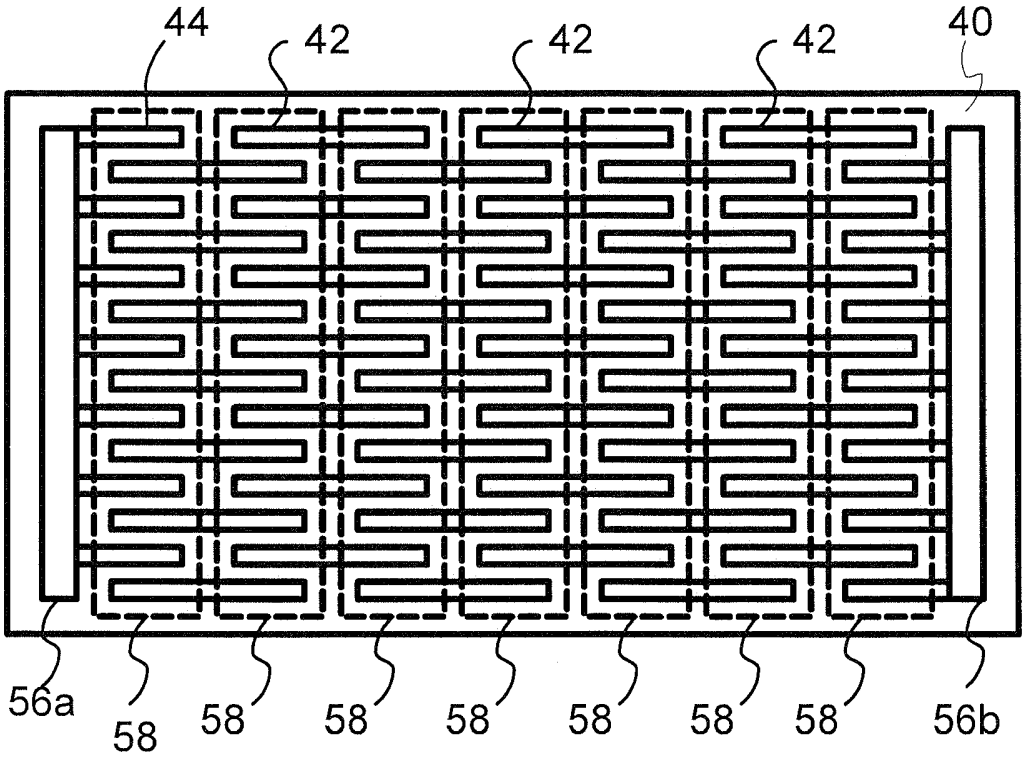

44
42
42
42
40
56a
58
58
58
58
58
58
58
56b

Fig.4

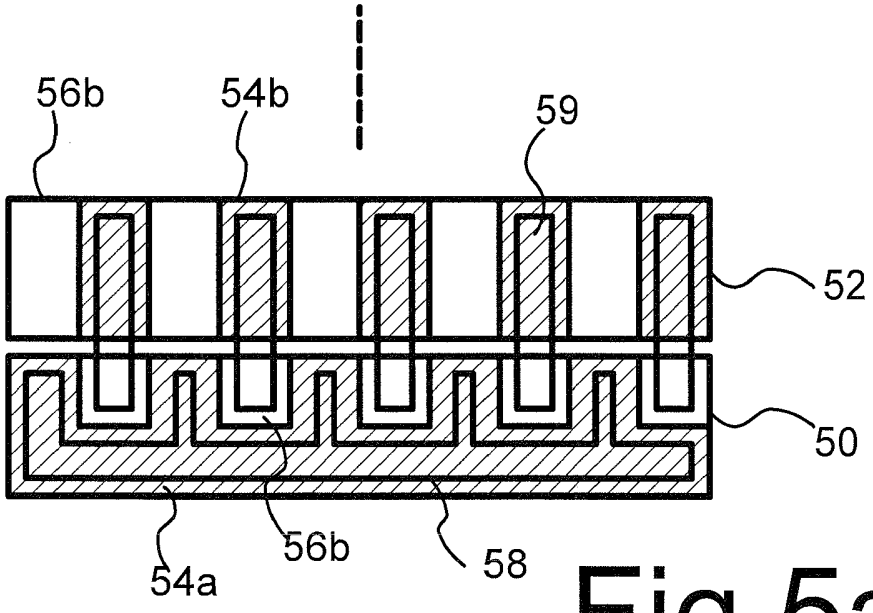
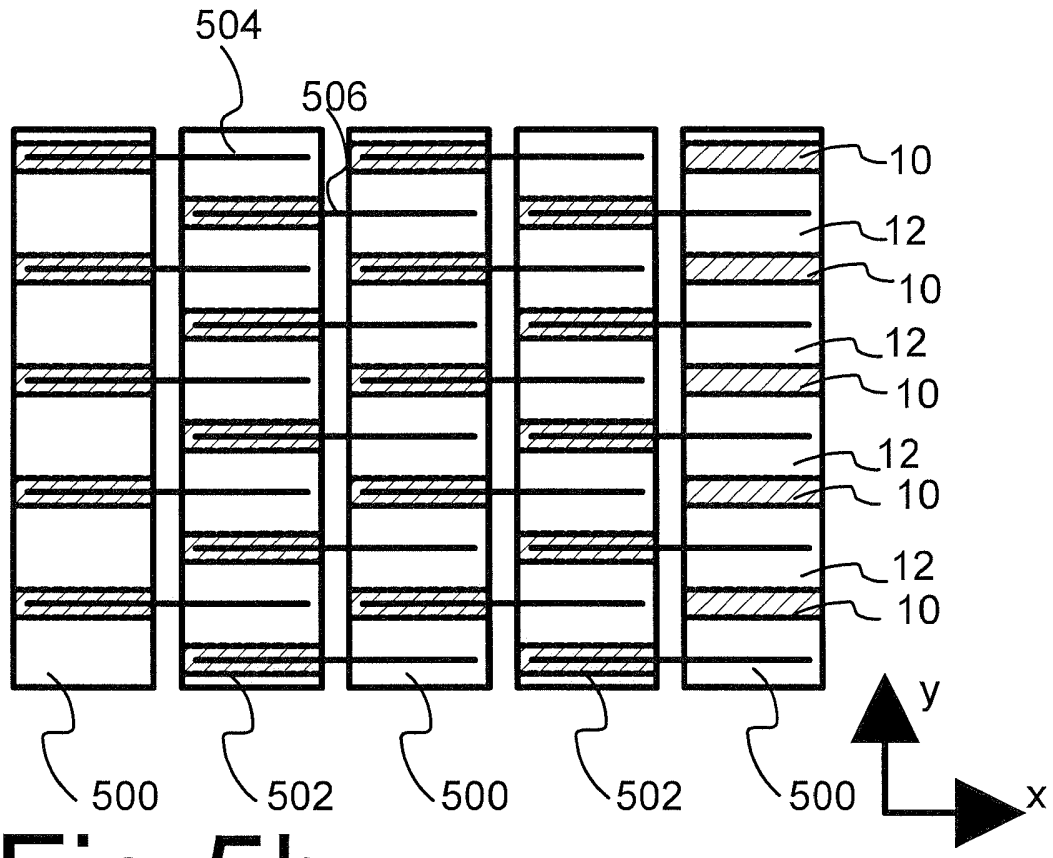

56b
54b
59
52
50
54a
56b
58

Fig.5a


504
506
10
12
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y
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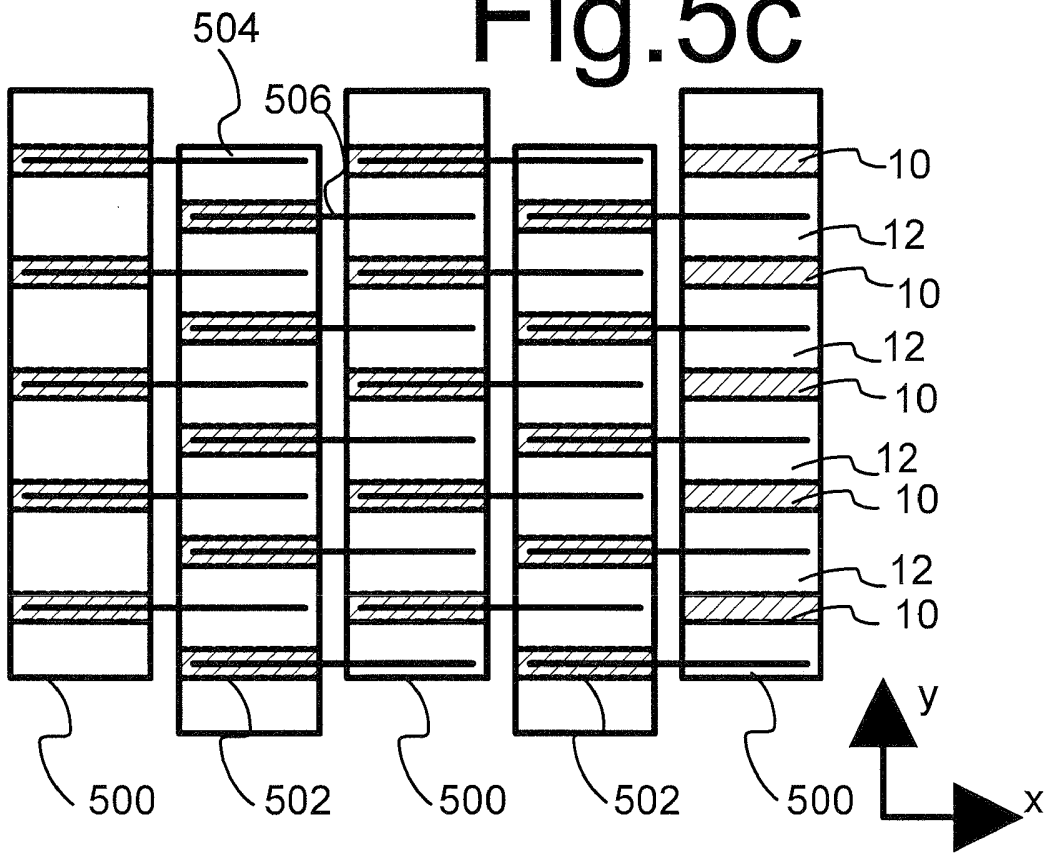
Fig.5b

Fig.5c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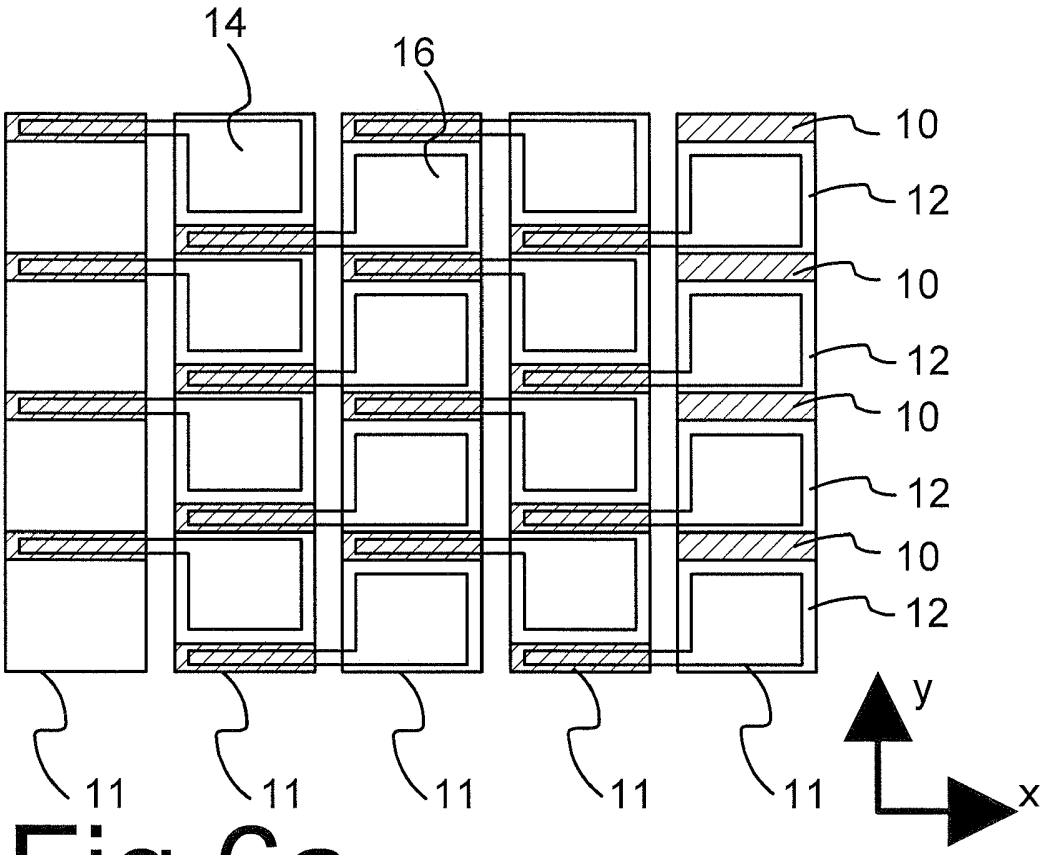
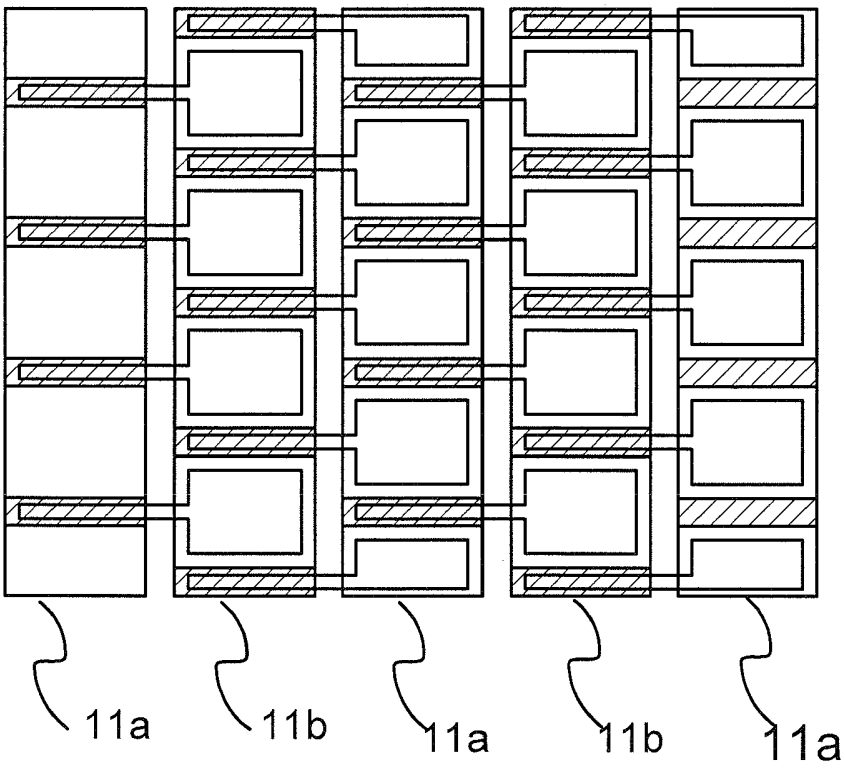



Fig.6a

Fig.6b



# SAMENWERKINGSVERDRAG (PCT)

## RAPPORT BETREFFENDE NIEUWHEIDSONDERZOEK VAN INTERNATIONAAL TYPE

| IDENTIFICATIE VAN DE NATIONALE AANVRAGE | KENMERK VAN DE AANVRAGER OF VAN DE GEMACHTIGDE |
|---|---|
| | **P96866NL00** |
| Nederlands aanvraag nr.<br>**2010558** | Indieningsdatum<br>**03-04-2013** |
| | Ingeroepen voorrangsdatum |
| Aanvrager (Naam)<br>**Stichting Energieonderzoek Centrum Nederland** | |
| Datum van het verzoek voor een onderzoek van internationaal type<br>**15-06-2013** | Door de Instantie voor Internationaal Onderzoek aan het verzoek voor een onderzoek van internationaal type toegekend nr.<br>**SN60246** |

**I. CLASSIFICATIE VAN HET ONDERWERP** (bij toepassing van verschillende classificaties, alle classificatiesymbolen opgeven)

Volgens de internationale classificatie (IPC)

**H01L31/05;H01L31/068**

**II. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK**

Onderzochte minimumdocumentatie

| Classificatiesysteem | Classificatiesymbolen |
|---|---|
| **IPC** | **H01L** |

Onderzochte andere documentatie dan de minimum documentatie, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

| | | | |
|---|---|---|---|
| III. | ☐ | **GEEN ONDERZOEK MOGELIJK VOOR BEPAALDE CONCLUSIES** | (opmerkingen op aanvullingsblad) |
| IV. | ☐ | **GEBREK AAN EENHEID VAN UITVINDING** | (opmerkingen op aanvullingsblad) |

# ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2010558

A. CLASSIFICATIE VAN HET ONDERWERP
INV. H01L31/05 H01L31/068
ADD.

Volgens de Internationale Classificatie van octrooien (IPC) of zowel volgens de nationale classificatie als volgens de IPC.

B. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK

Onderzochte miminum documentatie (classificatie gevolgd door classificatiesymbolen)
H01L

Onderzochte andere documentatie dan de mimimum documentatie, voor dergelijke documenten, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

Tijdens het onderzoek geraadpleegde elektronische gegevensbestanden (naam van de gegevensbestanden en, waar uitvoerbaar, gebruikte trefwoorden)
EPO-Internal, WPI Data

C. VAN BELANG GEACHTE DOCUMENTEN

| Categorie ° | Geciteerde documenten, eventueel met aanduiding van speciaal van belang zijnde passages | Van belang voor conclusie nr. |
|---|---|---|
| X | DE 10 2011 001061 A1 (SOLARWORLD INNOVATIONS GMBH [DE])<br>6 september 2012 (2012-09-06)<br>* alineas [0064], [0066], [0067]; figuur 1 *<br>* alinea [0073] - alinea [0075]; figuur 2 *<br>* alinea [0076] - alinea [0083]; figuur 3 *<br>* alinea [0085] - alinea [0089]; figuur 4 *<br>* alinea [0103] - alinea [0107]; figuur 7 *<br>* alinea [0109] - alinea [0113]; figuren 8-10 *<br>* alinea [0114] - alinea [0119]; figuren 11,12 *<br>-----<br>-/-- | 1-3,6-9, 12,13, 17,18,20 |

[X] Verdere documenten worden vermeld in het vervolg van vak C.

[X] Leden van dezelfde octrooifamilie zijn vermeld in een bijlage

° Speciale categorieën van aangehaalde documenten

"A" niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft

"D" in de octrooiaanvrage vermeld

"E" eerdere octrooi(aanvrage), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven

"L" om andere redenen vermelde literatuur

"O" niet-schriftelijke stand van de techniek

"P" tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur

"T" na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvrage, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding

"X" de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur

"Y" de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht

"&" lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

| Datum waarop het onderzoek naar de stand van de techniek van internationaal type werd voltooid | Verzenddatum van het rapport van het onderzoek naar de stand van de techniek van internationaal type |
|---|---|
| 19 november 2013 | |

| Naam en adres van de instantie | De bevoegde ambtenaar |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Hofmann, Kerrin |

1

**ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE**

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2010558

C.(Vervolg). VAN BELANG GEACHTE DOCUMENTEN

| Categorie ° | Geciteerde documenten, eventueel met aanduiding van speciaal van belang zijnde passages | Van belang voor conclusie nr. |
|---|---|---|
| X | GORDON I ET AL: "Development of interdigitated solar cell and module processes for polycrystalline-silicon thin films", THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, deel 511-512, 26 juli 2006 (2006-07-26), bladzijden 608-612, XP025007255, ISSN: 0040-6090, DOI: 10.1016/J.TSF.2005.12.124 [gevonden op 2006-07-26] * samenvatting * * bladzijde 608, linker kolom, alinea 1 - bladzijde 610, rechter kolom, alinea 4; figuren 1,2 * | 1,2,6-8, 10-13, 21,22 |
| X | WO 2006/123938 A1 (REC ASA [NO]; SAUAR ERIK [NO]; ANDERSSON PER [NO]; AAMODT HELGE CATO []) 23 november 2006 (2006-11-23) * bladzijde 3, alinea 4 - bladzijde 4, alinea 1 * * bladzijde 4, alinea 8 - bladzijde 5, alinea 2; figuur 1a * | 1,6,12 |
| A | JOHN VAN ROOSMALEN ET AL: "Crystalline silicon interconnected strips (XIS): Introduction to a new, integrated device and module concept", PHOTOVOLTAIC SPECIALISTS CONFERENCE (PVSC), 2012 38TH IEEE, IEEE, 3 juni 2012 (2012-06-03), bladzijden 1129-1134, XP032258019, DOI: 10.1109/PVSC.2012.6317801 ISBN: 978-1-4673-0064-3 * het gehele document * | 1-22 |

1

**ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE**

Informatie over leden van dezelfde octrooifamilie

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2010558

| In het rapport genoemd octrooigeschrift | Datum van publicatie | Overeenkomend(e) geschrift(en) | Datum van publicatie |
|---|---|---|---|
| DE 102011001061 A1 | 06-09-2012 | CN 102694037 A | 26-09-2012 |
| | | DE 102011001061 A1 | 06-09-2012 |
| | | US 2012279546 A1 | 08-11-2012 |
| WO 2006123938 A1 | 23-11-2006 | GEEN | |

**OCTROOICENTRUM NEDERLAND**

# WRITTEN OPINION

| File No. | Filing date *(day/month/year)* | Priority date *(day/month/year)* | Application No. |
|---|---|---|---|
| SN60246 | 03.04.2013 | | NL2010558 |

International Patent Classification (IPC)
INV. H01L31/05 H01L31/068

Applicant
Stichting Energieonderzoek Centrum Nederland

This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the application
- ☒ Box No. VIII Certain observations on the application

| | Examiner |
|---|---|
| | Hofmann, Kerrin |

Application number

# WRITTEN OPINION

NL2010558

## Box No. I Basis of this opinion

1. This opinion has been established on the basis of the latest set of claims filed before the start of the search.

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ on paper

   ☐ in electronic form

   c. time of filing/furnishing:

   ☐ contained in the application as filed.

   ☐ filed together with the application in electronic form.

   ☐ furnished subsequently for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

## Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

| | | | |
|---|---|---|---|
| Novelty | Yes: | Claims | 4, 5, 10, 14-16, 19, 21 |
| | No: | Claims | 1-3, 6-9, 11-13, 17, 18, 20, 22 |
| Inventive step | Yes: | Claims | 4, 5, 14-16, 19 |
| | No: | Claims | 1-3, 6-13, 17, 18, 20-22 |
| Industrial applicability | Yes: | Claims | 1-22 |
| | No: | Claims | |

2. Citations and explanations

**see separate sheet**

# WRITTEN OPINION

## Box No. VIII Certain observations on the application

see separate sheet

**Re Item V**

**Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1 Reference is made to the following documents:

D1 DE 10 2011 001061 A1 (SOLARWORLD INNOVATIONS GMBH [DE]) 6 september 2012 (2012-09-06)

D2 GORDON I ET AL: "Development of interdigitated solar cell and module processes for polycrystalline-silicon thin films", THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, deel 511-512, 26 juli 2006 (2006-07-26), bladzijden 608-612, XP025007255, ISSN: 0040-6090, DOI: 10.1016/J.TSF.2005.12.124 [gevonden op 2006-07-26]

D3 WO 2006/123938 A1 (REC ASA [NO]; SAUAR ERIK [NO]; ANDERSSON PER [NO]; AAMODT HELGE CATO [] 23 november 2006 (2006-11-23)

2 INDEPENDENT CLAIM 1

2.1 The present application does not meet the criteria of patentability, because the subject-matter of claim 1 is not new.

2.2 D1 discloses (references in parenthesis applying to this document):

*Een werkwijze voor het vervaardigen van een samenstel van foto- voltaische cellen* (par. 1), *met gebruik van tenminste een eerste en tweede cel* (100, fig. 1, 7), *waarbij elke cel een eerste en tweede rand heeft* (see fig. 1) *en langwerpige paralelle basis- en emittergebieden op éénzelfde planair oppervlak van de cel zich uitstrekkend van de eerste naar de tweede rand* (base contacts 102, emitter contacts 104 show implicitly layout of base and emitter areas on cell surface; par. 66, 67), *waarbij de basis en emittergebieden met elkaar afwisselen in een eerste richting langs de eerste en tweede randen* (see fig. 1), *welke werkwijze omvat*

*- rangschikken van de eerste en tweede cellen naast elkaar met de eerste rand van de eerste cel gekeerd naar de eerste rand van de tweede cel* (see fig. 7; par. 105);

*- vormen van elektrische verbindingen tussen respectievelijke van de basisgebieden van de eerste cel en respectievelijke van de emittergebieden van de tweede cel* (par. 104) *door het deponeren van elektrisch geleidermateriaal* (electrode material 300, 400; par. 106, 110) aan op de eerste en tweede cel en doorlopend tussen de eerste en tweede cel (par. 110, fig. 8, 9, 10)*; en*

*- vormen van de elektrische verbindingen* (302) *uit dat materiaal op en tussen de eerste en tweede cellen* (par. 110).

2.3 The subject-matter of claim 1 is also disclosed in documents D2 (fig. 1, 2b) and D3 (fig. 1a).

3 INDEPENDENT CLAIM 12

3.1 The present application does not meet the criteria of patentability, because the subject-matter of claim 12 is not new.

3.2 D1 discloses (references in parenthesis applying to this document):

*Een samenstel van foto-voltaische cellen* (fig. 9) *omvattende*

*- een eerste en tweede cel* (100) *geplaatst naast elkaar waarbij elke cel een eerste en tweede rand heeft en langwerpige paralelle basis- en emittergebieden* (see fig. 1 and par. base contacts 102, emitter contacts 104; par. 66, 67) *op eenzelfde planair oppervlak van de cel* (see fig. 1, 2), *zich uitstrekkend van de eerste naar de tweede rand, waarbij de basis- en emittergebieden elkaar afwisselen in een eerste richting langs de eerste en tweede randen* (see fig. 1, 2), *waarbij de eerste rand van de eerste cel en de eerste rand van de tweede cel naar elkaar toegekeerd zijn* (par. 105);

*- elektrisch geleidermateriaal* (302, par. 79) *gevormd in elektrisch contact met de basis- en emittergebieden en tussen de eerste en tweede cellen* (par. 104, 110), *waarbij elk spoor* (302) *zich uitstrekt over een respectievelijk paar van één van de basisgebieden van de eerste cel en één van de emittergebieden van de tweede cel en tussen de eerste en tweede cel* (see fig. 3, 9).

3.3 The subject-matter of claim 12 is also disclosed in documents D2 (fig. 1, 2b) and D3 (fig. 1a).

4 DEPENDENT CLAIMS

4.1 Dependent claims 2, 3, 6-9, 11, 13, 17, 18, 20, 22 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of novelty for the following reasons:

4.1.1 D1 discloses:

**Claims 2, 13:** ... insulating material (304) between cells

**Claim 3:** ... same layout, arrangement (par. 105, fig. 7)

**Claims 6-9, 17, 18, 20:** ... conductive track (interconnector) layout (fig. 3, 9)

4.1.2 D2 discloses:

**Claims 11, 22:** ... wafer cutting in long side cell direction (fig. 1, grooves for cell separation)

4.2 Dependent **claims 10, 21** do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of inventive step for the following reason:

4.2.1 D2 teaches base contacts (p-contacts) which are broader than emitter contacts (n-contacts, fig. 1, 2b)

4.3 The combination of the features of dependent claims 4, 5, 14-16, 19 is neither known from, nor rendered obvious by, the available prior art.

## Re Item VIII

### Certain observations on the application

1 Claims 1, 12, 22 are not clear.

1.1 The terms *"erste en tweede rand"* and *"eerste rand van de eerste cel gekeerd naar de eerste rand van de tweede cel"* used in claims 1 and 12 are vague and unclear and leave the reader in doubt as to the meaning of the technical feature to which it refers, thereby rendering the definition of the subject-matter of said claim unclear. Any edge of the cell can be defined as first or second edge and the arrangement of the cells with respect to their edges is not unambiguously clear.

1.2 Some of the features in the apparatus claim 22 relate to a method of manufacturing the apparatus rather than clearly defining the apparatus in terms of its technical features. The intended limitations are therefore not clear from this claim.