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(54) IMPROVEMENTS IN OR RELATING TO MOS SEMI-CONDUCTOR STORAGE MODULES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to MOS semi-conductor storage modules of the type in which MOS transistor storage cells are disposed between word and bit lines, and at least one sense amplifier is disposed symmetrically with respect to two respective bit lines for evaluating the read signals appearing on the bit lines, said or each sense amplifier being arranged in a column, and in which the storage cells connected to the bit lines leading to the sense amplifiers form at least one storage cell field.

It is known for MOS stores to be designed such that a respective MOS transistor storage cell is disposed at each intersection point between a word line and bit line. Such a transistor storage cell can be a known single transistor storage cell for example. To be able to more positively evaluate the read signals appearing on the bit lines during the reading operation, which signals are very small, a respective sense amplifier may be disposed symmetrically between each two associated bit lines. Such a sense amplifier can be constituted by a symmetrical flip-flop, for instance. Then such an MOS store is built up on a storage module from a column of sense amplifiers and two storage cell fields of which a first is disposed on one side of the column of sense amplifiers, and a second is disposed on the other side of the column of sense amplifiers. Such an MOS store is described for example, in Electronics, Sept. 13, 1973, pages 117 to 121.

Since the read signals are very small, it is normally ensured that the storage cell fields formed on each side of the sense amplifiers are as symmetrical as possible. Thus, when selecting a storage cell during a reading operation, any distorting signals occurring in the process should be equal on both sides of the sense amplifier, which means that identical increases in capacitance take place on both sides and the bit lines are charged to the same bias level before the reading operation. These requirements can be satisfied using the following measures: the bit lines need to be charged up by identical charging transistors that are actuated by an identical charging timing signal; the distorting signals that arise through the selection of a cell column on one side of the sense amplifier are equalised by an identical distortion signal by selecting a so-called compensation or dummy cell on the other side. The capacitive equilibrium on both sides of the sense amplifier can also be achieved with the aid of compensation cells which balance the increase in capacitance on the bit lines through the addressed cells. In addition, any capacitive imbalance which arises as a result of selecting a selector switch disposed between a bit line and a data line is corrected by a special equalisation element on the other bit line associated with the same sense amplifier.

However, in the known storage modules the requirements indicated above are only partially satisfied, because the two cell fields separated by a column of sense amplifiers are relatively far apart, and consequently manufacturing tolerances have a considerable effect on the properties of individual components such as transistors, capacitors etc.

One object of the present invention is the provision of an MOS storage module in which any adverse influence of manufacturing tolerances is substantially eliminate during weighting of read signals.

The invention consists in an MOS semiconductor module of the type having MOS transistor storage cells disposed between word and bit lines, in which a respective

sense amplifier is disposed symmetrically between each two bit lines to facilitate the evaluation of the read signals appearing on the bit lines, said sense amplifiers being disposed in a column, and in which the storage cells connected to the bit lines leading to first inputs of the sense amplifiers form a first storage cell field and the storage cells connected to the bit lines leading to second inputs of the sense amplifiers form a second storage cell field, said column of sense amplifiers being disposed on the storage module on one side of all said storage cell fields and data lines for conveying read-out signals from the sense amplifiers being disposed on said same one side of the storage cell fields.

It is expedient to arrange the sense amplifiers symmetrically between the two bit lines. Then even with a small bit line grid spacing, the sense amplifiers do not have to be disposed in an echelon formation.

At the points of intersection between a word line and the two bit lines associated with any one sense amplifier, a storage cell is provided at one point of intersection only, although an additional capacitor can be provided at the other intersection point. In this way the increase in capacitance when selecting a storage cell on one bit line can be offset with the aid of the additional capacitor. Distortion signals occurring when the storage cell is selected appear in the same way on the other bit line as well. Since the storage cell and the capacitor are very close together, variations in tolerance affect both equally.

The bit lines associated with a sense amplifier are preferably connected at their ends remote from the storage cells through respective selector switches to data lines. The signals read from a storage cell are carried away from the storage cell field on these data lines, or new information to be recorded in the storage cell field is fed into the storage cell field on these data lines. Two such data lines are provided, one data line in each case being connected to one bit line associated with the associated sense amplifier through a first selector switch, and the other data line to the other bit line associated with that sense amplifier through a second selector switch. The selector switches associated with any one sense amplifier are actuated by one common timing signal. In this design the selector switches can be immediately adjacent to one another on the storage module. Since they may also be identical in design, they provide equal additional capacitance, and consequently it is not necessary to provide additional compensation elements.

It is also expedient if a read amplifier is disposed between the two data lines. Since complementary signals appear on the two data lines during the reading operation, this enables the read amplifier to function faster and more reliably.

Before a reading operation can start, advantageously the bit lines have to be charged up by means of charging transistors. Preferably, these charging transistors are closely grouped on the module. This means that any distorting signals appearing on the bit lines through actuation of charging transistors are the same for both the bit lines associated with any one sense amplifier.

A large storage cell field can be split up into a plurality of storage cell fields, each storage cell field exhibiting its own column of sense amplifiers. The individual storage fields with their columns of sense amplifiers can be connected one behind another. In this way the bit lines become shorter with a consequent reduction in the bit line capacitance and any magnification of read signals.

A further advantage of a preferred embodiment of MOS storage module constructed in accordance with the invention lies in the fact that during the recording operation information can pass directly to the sense amplifier and the two bit lines along the two data lines and associated selector switches in complementary form, which leads to a reduction in recording time.

The invention will now be described with reference to the drawings, in which:—

Figure 1 schematically illustrates one known MOS store;

Figure 2 schematically illustrates the basic principle of a store constructed in accordance with the invention;

Figure 3 shows circuit details of one exemplary embodiment of a store constructed in accordance with the invention;

Figure 4 is a set of explanatory waveform diagrams relating to the embodiment shown in Figure 3;

Figure 5 shows one exemplary embodiment of a store without compensation cells;

Figure 6 is a set of explanatory waveform diagrams for operating the store embodiment shown in Figure 5;

Figure 7 schematically illustrates an alternative exemplary embodiment in which a plurality of storage cell fields are connected one behind another; and

Figure 8 is a set of explanatory waveform diagrams for operating the store embodiment shown in Figure 7.

The known store shown in Figure 1 utilises single transistor storage cells SZ. The single transistor storage cells SZ each consist of a selection transistor MS and a storage cpacitor CS. The gate of each selection transistor is connected to a respective word line, X1 to XN, and by a controlled electrode to a respective bit line BL or BR. The bit lines are connected to a respective sense amplifier BW. Here two bit lines, namely BL and BR, are provided per sense amplifier BW. One bit

line BL is connected to one input of the sense amplifier BW, and the other bit line BR is connected to the other input of the sense amplifier BW. In the example shown in Figure 1, only one storage cell is provided on each side of the sense amplifier BW, but obviously a larger number of such storage cells can be connected to the bit lines BL and BR on each side, to form respective storage cell fields ZFL and ZFR.

Of the known construction illustrated in Figure 1, only one sense amplifier BW is shown, with its two associated bit lines BL and BR. In reality a greater number of such sense amplifiers BW are disposed in a column one above another, as is indicated by a broken line in Figure 1.

In addition to the storage cell fields ZFL and ZFR, provision is made for a column LS for respective charging transistors ML. With the aid of the charging transistors ML, the bit lines BL and BR are charged up before the reading operation.

Moreover, on both sides of the sense amplifiers BW, there is a column of compensation cells DZ each consisting of a transistor MD and a capacitor CD. These compensation or dummy cells are designed to ensure that when a storage cell is selected the resultant increase in capacitance on one bit line and any distortion signal transmitted to the bit line through this are equalised by actuating the compensation cell on the other side of the sense amplifier BW. The compensation cells are connected to a common generator GE, through which the capacitors CD are charged up to a moderate voltage in known manner.

Finally, one bit line, namely the bit line BR, is shown connected through a selection transistor MA to a data line DA. When a timing signal Y is applied to the gate of the selection transistor MA, the bit line BR is connected with the data line DA and information can be exchanged between the data line DA and the bit line BR. The capacitive charging from the selection transistor MA to the bit line BR is balanced on the other bit line BL by a compensating capacitor CX.

Other elements shown in Figure 1 are charging timing signal lines SV which charging transistors ML are actuated, charging voltage lines UV via which potential is fed through the charging transistors ML to the associated bit line, and actuating lines XDL and XDR for the respective compensation cells DZ and the word lines X1 to XN.

One disadvantage of this known store arrangement consists in the fact that, as is clearly shown in Figure 1, the two storage cell fields ZFL and ZFR are separated from one another by a column of sense amplifiers BW and must therefore lie fairly far apart. This makes it easily possible for the properties of the transistors and capacitors in the two storage cell fields to differ, and thus different conditions may apply at the two inputs of a sense amplifier BW.

Figure 2 shows schematically how this disadvantage in the design of the store is overcome in an embodiment of the present invention. Here only a basic storage cell field ZFD is shown, but the essential thing is that this storage cell field ZFD, in which the two storage cell fields ZFL and ZFR of Figure 1 are combined, is disposed entirely on one side of a column of sense amplifiers BW1 to BW3, by way of example. The storage cells lying at the points of intersection between word lines and bit lines are shown by small circles in Figure 2, the circles that are filled in indicating the points at which storage cells of storage cell field ZFL were disposed in the known arrangement, whilst circles that are not filled in denote points at which storage cells of the other storage cell field ZFR were located in the known arrangement. This illustration is merely intended to allow comparison of the novel store shown in Figure 2 with the known arrangement shown in Figure 1.

In the embodiment illustrated in Figure 2, three pairs of bit lines BL1 and BL3 are provided, these being connected to associated sense amplifier BW1 to BW3. Here, any one sense amplifier BW is located between its two associated bit lines, thus for example, the sense amplifier BW1 is connected between bit lines BL1 and BR1. The sense amplifiers BW lie in a column one above another. Word lines X1, X2, X3, XN—2, XN—1 and XN are shown. Obviously, a practical embodiment could have a large number of each of these elements.

A more precise illustration is given in Figure 3, to show details of the circuit for one sense amplifier BW with its associated bit lines BL and BR, and the associated units connected to these bit lines.

The storage cell field ZF has two word lines X1 and X2, and two storage cells SZ. One storage cell lies between the word line X1 and the bit line BL, whilst the other storage cell lies between the word line X2 and the bit line BR. In each case they are single transistor storage cells consisting of a selection transistor MS and a storage capacitor CS designed in known manner. Near the cell field ZF there is a column LS of respective charging transistors ML. The charging transistors ML are actuated by a charging timing signal SV to apply a charging potential UV to the bit lines BL and BR. Near the column LS with the charging transistors ML there is a column DZ of compensation cells. These each consist of a known arrangement of a transistor MD and a capacitor CD, directly comparable to the storage cells. A common generator GE is provided to charge the capacitors CD up to a

moderate level in the pauses provided for their operation.

The sense amplifier BW is disposed as near as possible to the cell field ZF, the column LS with its charging transistors and the column DZ with its compensation cells. The broken line above and below the sense amplifier BW is intended to indicate that the store consists of a whole column of such sense amplifiers BW with associated elements. Here the sense amplifier BW lies between its two associated bit lines BL and BR. The ends of these lines remote from the storage cell field are each connected to a respective data line DA1, DA2 through respective selector switches MA1 and MA2, which are actuated simultaneously by a common selection signal Y. Disposed between the data lines DA1 and DA2 there is a read amplification circuit LV, at the output of which an amplified read signal DO is emitted. The data lines DA1 and DA2 are common to all the bit lines of a storage cell field.

When a given storage cell, e.g. the one adjoining the word line X1, is actuated, the associated selection transistor MS is made to conduct and an exchange of charge can then take place between the storage capacitor CS and the associated bit line BL. But when the word line X1 is actuated, capacitive coupling produces a distortion signal on the bit line BL and in addition, the capacitance of the bit line BL is increased. At the point of intersection between the word line X1 and the other bit line BR there is provided a distortion coupling capacitor CST through which the bit line BR is influenced in the same way as the bit line BL is affected by the storage cell. Through this distortion coupling capacitor therefore distorting signals are also passed over to the bit line BR, and an increase in capacitance is produced on the bit line BR. Thus some of the distortion signals on the bit line BL are equalised by the distortion coupling capacitor and the rest is eliminated by the compensation cell. In addition the moderate level needed for reliable reading is ensured on the bit line BR through the compensation cell DZ. This prevents the distortion signals having any effect when a read signal is being evaluated.

The operation of the store shown in Figure 3 will now be explained with reference to the explanatory set of waveform diagrams given in Figure 4, where voltages are plotted against time t. First the charging timing signal SV is applied and the charging transistors ML made to conduct. This allows the bit lines BL and BR to charge up as is shown in the third and fourth lines of Figure 4. The data lines DA1 and DA2 are also charged up. The charging timing signal SV is then turned off and a signal is applied, e.g. to word line X1, to select the storage cell lying between the bit line BL and the word line X1. A corresponding voltage change then takes place on the bit line, depending upon whether the storage capacitor CS was charged or not, i.e. depending upon whether a binary "1" or a binary "0" was stored in the storage capacitor CS. If a binary "1" was stored, the voltage at bit line BL rises (solid curve, line 3); but if, in contrast, the information in the storage capacitor CS was a binary "0" then the voltage on the bit line BL falls (broken line curve in line 3). Thus the voltage change on the bit line BL when a storage cell is selected is initially attributable to the information read out. At the same time however, the bit line BL is affected by a distortion signal the cause of which has already been described above. This distortion signal occurs simultaneously on the other bit line BR, through the compensation cell and the distortion coupling capacitor CST as shown in the fourth line of Figure 4. The compensation cell and the capacitor CST are so designed that distortion signals on the bit line BR match the distortion arising on the bit line BL when the storage cell is selected.

At the points in time indicated by an arrow in lines 3 and 4 the sense amplifier BW begins to evaluate the read signal. The sense amplifier BW is preferably a symmetrical flip-flop, so that it is set into one stable state by the read signal that is present. This produces a voltage corresponding to that one stable state of the flip-flop circuit on one bit line BL, while a voltage is produced on the other bit line BR corresponding to the other stable state of the flip-flop. The corresponding conditions prevailing on the bit lines BL and BR are shown by solid and broken curves in lines 3 and 4 of Figure 4, where solid curves belong together and broken lines belong together.

After the sense amplifier BW has evaluated the read signal, the selection transistors MA can be actuated by the signal Y. This transfers the voltage conditions on the bit lines BL and BR to the data lines DA1 and DA2, as is shown in the last two lines in Figure 4.

From there the signal passes to the read amplifier LV which amplifies this read signal and emits it at its output DO.

Here the precise function of the compensation cells has not been examined in detail, as the function of these compensation cells is known in the art.

Another exemplary embodiment is shown in Figure 5. This embodiment differs from that shown in Figure 3 in that no compensation cells DZ are provided. It is possible to omit the compensation cells if the increase in capacitance arising on any one bit line through selection of a storage cell can be offset with the aid of a distortion coupling capacitor CST designed for this purpose. The

bit lines BL and BR can be charged up to the moderate level required for reliable reading with the aid of a reference voltage UR applied to the respective charging transistors ML. Otherwise the store shown in Figure 5 is identical to the store shown in Figure 3.

Figure 6 shows a set of explanatory waveform diagrams for the operation of the store shown in Figure 5, with voltages plotted against time *t*. The conditions are almost completely the same as those shown for Figure 4. The only difference lies in the fact that a distortion signal on any bit line not connected with the selected storage cell is now produced solely by the respective distortion coupling capacitor CST. With appropriate choice of capacitor CST the increase in capacitance on both bit lines and the capacitive coupling between a word and bit line can be made roughly the same for both bit lines.

Figure 7 illustrates details of an exemplary embodiment where one large storage cell field is split up into smaller storage cell fields, namely two in the embodiment illustrated to necessitate relatively shorter bit lines in a storage cell field. Each storage cell field has its own associated column of sense amplifiers. In the example shown, a storage cell field ZF1 has a column BWS1 of sense amplifiers BW and storage cell field ZF2 has a column BWS2 of similar sense amplifiers BW. One sense amplifier is shown for each column of sense amplifiers. Here again, the store cell fields associated with one column of sense amplifiers lie on one side of the column of the sense amplifiers. Here the individual cell fields ZF1 and ZF2 are connected one behind another with the aid of connecting switches. This means that the bit lines are connected to the bit lines of the neighbouring storage cell field through connecting switches. The bit lines BL1 and BR1 of the storage cell field ZF1 are thus connected through connecting switches MD to the associated bit lines BL2 and BR2 of the storage cell field ZF2. The free ends of these bit lines are linked to associated data lines DA1 and DA2 through respective selector switches MA. Connecting switches MD are actuated with the aid of a common timing signal D, while a signal Y is applied to selection switches MA.

The operation of the circuit arrangement shown in Figure 7 will now be described with the aid of the set of explanatory waveform diagrams shown in Figure 8. For example, word line X1 is selected in storage cell field ZF1. The resultant read signal is fed to the associated sense amplifier BW in column BWS1. This sense amplifier is activated and amplifies the read signal. Then the connecting transistors MD are actuated and made to conduct by a signal D. The amplified read signal is thus passed on via bit lines BL2 and BR2 to the sense amplifier BW in the column BWS2 of similar sense amplifiers. The sense amplifier BW in the column BWS2 of Figure 7 switches into the same state as the sense amplifier BW in the column BWS1. Once the sense amplifier BW in the column BWS2 has also reached a stable state the signal Y can be applied to the selection transistors MA and the amplified read signal can be fed to the data lines DA1 and DA2.

The procedure is reversed during a recording operation. The information to be recorded is initially fed to the bit lines BL2 and BR2, via the switch elements MA, from the data lines DA1 and DA2. The sense amplifier BW in column BWS2 is set accordingly. Then the connection transistors MD are rendered conductive and the information is passed on to the sense amplifier in the column BWS1. This sense amplifier is thus also switched into the corresponding state. The operation of recording in a storage cell then takes place through selection of a word line inside the storage field.

During a re-generation operation the storage cell fields and their associated sense amplifiers always remain separated. This means the connecting transistors MD and the selection transistors MA are blocked. One column is selected in each storage cell field, amplifying the read signals in the associated sense amplifier and feeding them back to the storage cells. This reduces the required number of regeneration cycles by splitting the large cell field into a plurality of parts.

A store constructed in accordance with the invention can be produced by any known MOS technique, and no particular technological problems are introduced due to the positioning of the storage cell field to one side of the sense amplifier.

A prime advantage of the store lies in the very fact that all the storage cells of the storage cell field are disposed to one side of the sense amplifiers, as this makes it possible to locate the sense amplifiers between the associated bit lines, and to connect each bit line directly through a selection switch to a data line, whilst the selection switches can be located next to one another, and the charging transistors can also be next to one another, and complementary signals passed to the data lines during the reading operation to both inputs of a read amplifier. Since the components working together during a reading or recording operation lie directly next to one another on the storage module, the characteristic properties of these individual components will show less variation due to manufacturing variations so that any distorting signals influence the sense amplifiers in the same way and are normally eliminated by the sense amplifier.

WHAT WE CLAIM IS:—

1. An MOS semi-conductor module of

the type having MOS transistor storage cells disposed between word and bit lines, in which a respective sense amplifier is disposed symmetrically between each two bit lines to facilitate the evaluation of the read signals appearing on the bit lines, said sense amplifiers being disposed in a column, and in which the storage cells connected to the bit lines leading to first inputs of the sense amplifiers form a first storage cell field and the storage cells connected to the bit lines leading to second inputs of the sense amplifiers form a second storage cell field, said column of sense amplifiers being disposed on the storage module on one side of all said storage cell fields and data lines for conveying read-out signals from the sense amplifiers being disposed on said same one side of the storage cell fields.

2. A semi-conductor module as claimed in claim 1, in which the bit lines are arranged on the storage module such that the two associated bit lines leading to a sense amplifier are disposed next to one another, and the associated sense amplifier lies between said two bit lines.

3. A semi-conductor storage module as claimed in claim 1, or claim 2, in which a storage cell is disposed at a point of intersection between a word line and bit line only at one of the two points of intersection between the word line and the two bit lines associated with each said sense amplifier.

4. A semi-conductor storage module as claimed in Claim 3, in which the second point of intersection of said word line with the two bit lines associated with said sense amplifier has an additional capacitor through which the capacitive distortion signals arising on one bit line through selection of the storage cell lying at the first point of intersection are equalised by a distortion signal on the other bit line.

5. A semi-conductor storage module as claimed in any preceding Claim, in which there are provided two selection switches actuated together by a selection signal and respectively disposed between the two bit lines leading to the associated sense amplifier and data lines common to the storage fields for extracting data from and feeding it into said storage fields.

6. A semi-conductor storage module as claimed in Claim 5, in which said selection switches are disposed on the opposite side of the sense amplifiers to the cell fields, and the two selection switches associated with any one sense amplifier lie directly next to one another on the storage module.

7. A semi-conductor storage module as claimed in any preceding Claim, in which charging transistors for the bit lines associated with any given sense amplifier to provide for charging up the bit lines are located close together on the storage module.

8. A semi-conductor storage module as in any preceding Claim, in which a plurality of respective cell fields for one column of sense amplifiers are disposed next to one another on a storage module.

9. A semi-conductor storage module as claimed in Claim 8, in which said respective cell fields disposed next to one another are each connected one behind the other.

10. A semi-conductor storage module as claimed in Claim 9, in which selector switches are provided for breaking the link with the neighbouring cell field, said switches being disposed between two neighbouring storage fields, in the bit lines.

11. An MOS semi-conductor module substantially as described with reference to Figure 2, 3, 5 or 7.

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1593866 COMPLETE SPECIFICATION
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Sheet 1

Fig.1

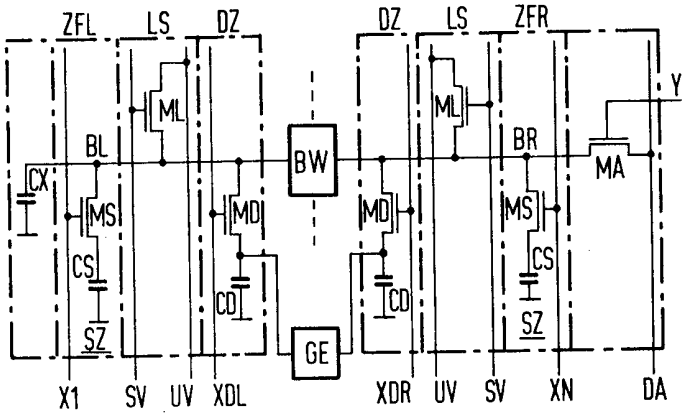

Fig.2

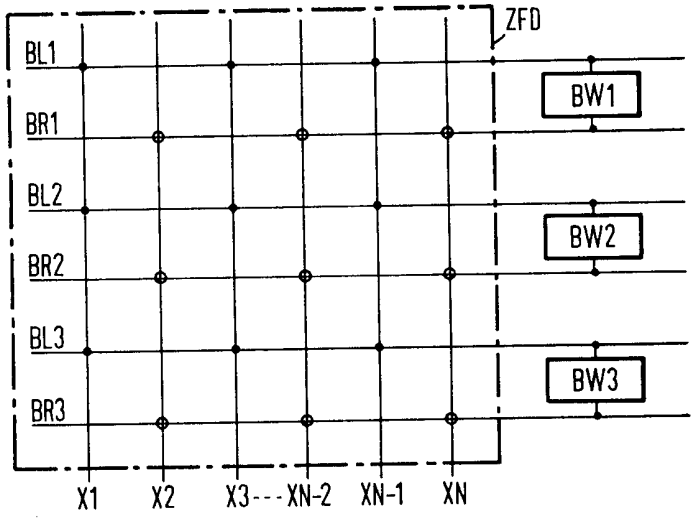

Fig. 3

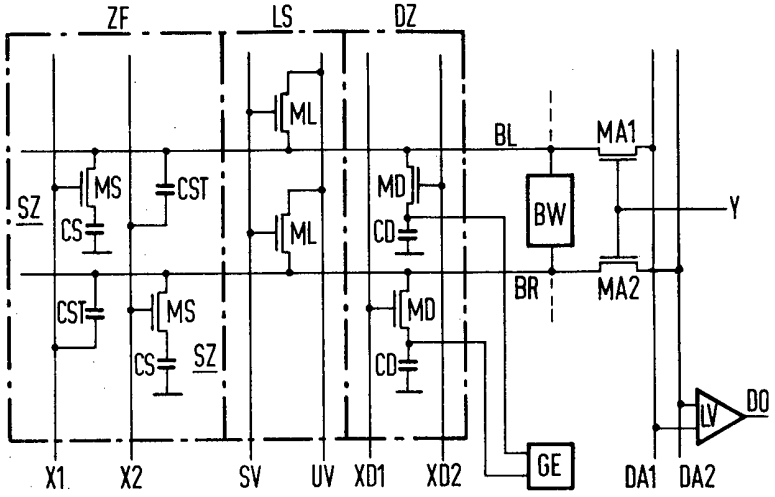
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Fig. 4

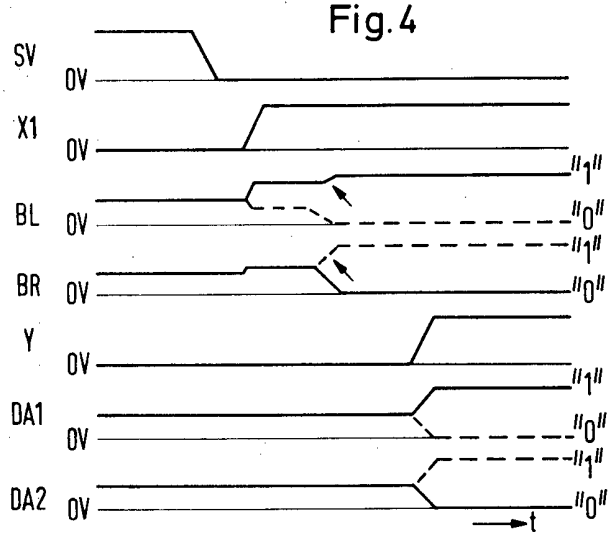
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Fig. 5

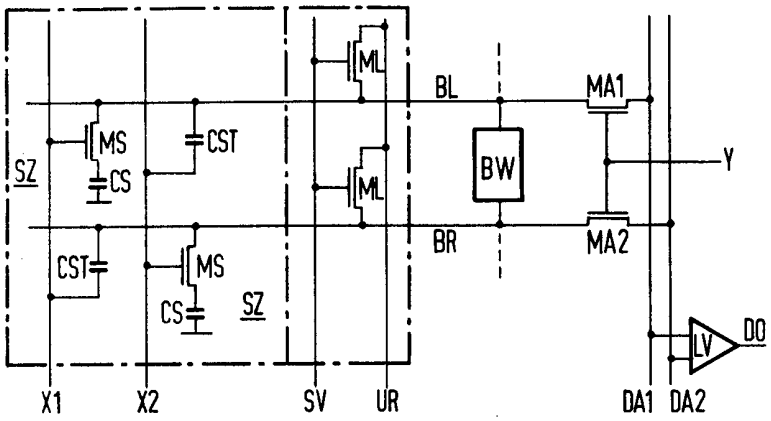
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Fig. 6

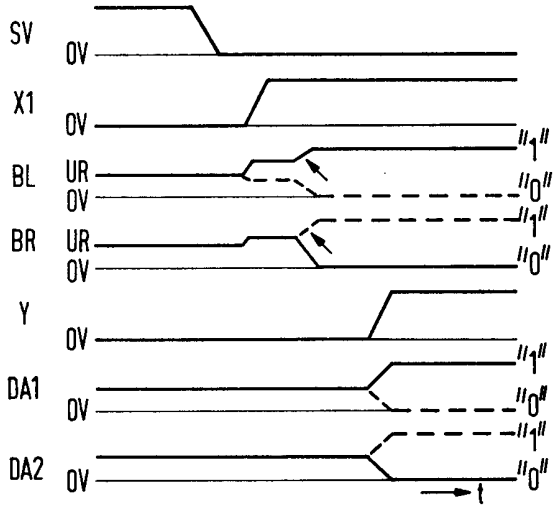
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Fig.7

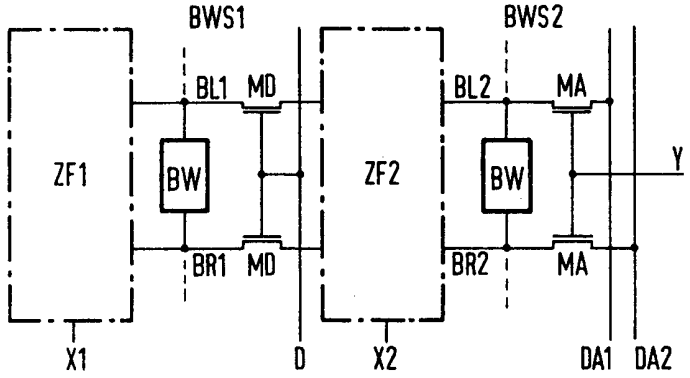
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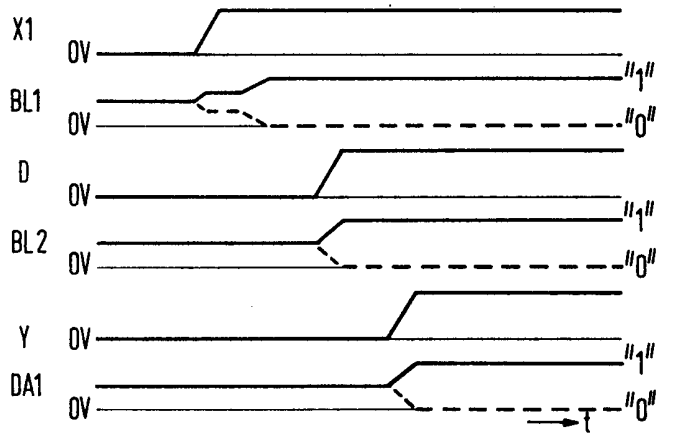
Fig.8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