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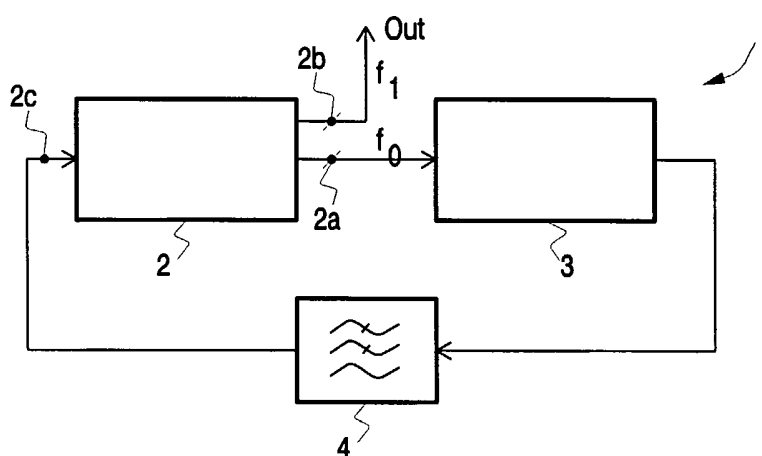
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(54) Title: OSCILLATOR WITH HARMONIC OUTPUT



(57) Abstract: An oscillator circuit (1) comprises an oscillator (2) and a synthesizer (3) connected in a feedback loop. The oscillator produces two signals: a first signal which is fed to the synthesizer and a second signal which constitutes the output signal of the circuit. The second signal is a harmonic of the first signal, thus allowing the synthesizer to operate at a much lower frequency than the actual output signal of the circuit. As a result, the power consumption of the circuit is reduced. The oscillator circuit is advantageously used in receivers for consumer devices.



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Oscillator with harmonic output

The present invention relates to an oscillator with harmonic output. More in particular, the present invention relates to an oscillator device comprising an oscillator circuit and a synthesizer circuit connected in a feed-back loop.

Various types of oscillators are known. A particularly effective type of
5 oscillator device involves a feed-back loop with a phase detector, a so-called Phase Locked Loop (PLL). This type of oscillator device is capable of generating high-frequency signals having a very accurately defined frequency over a wide frequency range. The feed-back loop feeds a control signal, typically a control voltage, to the control input of the oscillator circuit. This allows the oscillator frequency to be tuned, hence the term Voltage Controlled Oscillator
10 (VCO). The feed-back loop further involves one or more frequency dividers which, together with the phase detector, constitute a frequency synthesizer.

Although such an oscillator involving a PLL provides very satisfactory results, in some applications the power consumption of the synthesizer poses a problem. As the power consumption of the divider circuits increases with frequency, the power consumed
15 may become a problem in applications involving high frequencies, in particular RF (Radio Frequency) applications. In addition, the dividers become more expensive as their typical operating frequency increases. These problems severely limit the use of high frequency and in particular RF applications of said type of oscillators in consumer electronics and in other applications where cost is crucial.

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United States Patent US 5,712,596 discloses a tunable crystal oscillator with harmonic output. This known oscillator allows relatively higher frequencies to be produced. However, it is not suggested to use this known oscillator in combination with a synthesizer in
25 a feed-back loop. In addition, this type of oscillator cannot work in the UHF (Ultra High Frequency) range and cannot be tuned over a wide frequency range.

Accordingly, it is an object of the present invention to overcome these and other problems of the Prior Art and to provide an oscillator device which contains an economical controlled oscillator circuit capable of generating high frequencies.

It is another object of the present invention to provide an oscillator device
5 which is compact and has a low power consumption.

It is a further object of the present invention to provide an economical receiver capable of receiving RF digital signals.

Accordingly, the present invention provides an oscillator device comprising an oscillator circuit and a synthesizer circuit, wherein the synthesizer circuit has an output
10 terminal connected to an input terminal of the oscillator circuit for providing a control signal, wherein the oscillator circuit has a first output terminal connected to an input terminal of the synthesizer circuit for providing a first signal having a first frequency to the synthesizer, wherein the oscillator circuit has a second output terminal for providing a second signal having a second frequency, and wherein the second frequency is a harmonic of the first
15 frequency.

By feeding the base frequency to the synthesizer while using a harmonic of the base frequency as the output frequency, the synthesizer operates on a frequency which is only a fraction of the output frequency. This results in a less critical design and a reduced power consumption of the synthesizer. In addition, any components used in the synthesizer or
20 oscillator may have larger component values (capacitance, resistance), resulting in a greater accuracy.

It is noted that United States Patent US 6,441,692 discloses an oscillator arrangement comprising a voltage controlled oscillator, a phase comparator, a loop filter and a feed-back loop. A harmonic of the oscillator frequency is used in the feed-back loop. The
25 single output signal of the oscillator arrangement is filtered by a band-pass filter so as to only produce the fundamental oscillator frequency.

In the present invention, the second frequency preferably is the first harmonic of the first frequency. However, the present invention is not so limited and embodiments can be envisaged in which the second, third, fourth or higher harmonic is used, instead of or in
30 addition to the first harmonic.

Advantageously, a low-pass filter is preferably arranged between the output terminal of the synthesizer and the input terminal of the oscillator circuit. Such a filter serves to convert the output signal of the synthesizer into a suitable input signal (control or tuning

signal) for the oscillator circuit. The low-pass filter may advantageously be integrated into either the oscillator circuit 2 or the synthesizer 3.

The present invention also provides an oscillator circuit for use in the oscillator device defined above, the oscillator circuit comprising an amplifier, a resonance network, a filter stage, an input terminal for receiving a tuning signal, a first output terminal for outputting a first signal having a first frequency and a second output terminal for outputting a second signal having a second frequency, wherein the filter stage is connected to the second output terminal and is designed for suppressing the first frequency and passing the second frequency, the second frequency being a harmonic of the first frequency.

Preferably, the filter stage is designed such that it constitutes a virtual short circuit to ground for the first frequency while constituting a parallel tuned circuit for the harmonic frequency.

The present invention further provides a receiver device, comprising an input filter for filtering an antenna signal, an amplifier for amplifying the filtered antenna signal, a mixer for mixing the amplified antenna signal with an oscillator signal produced by an oscillator section, a filter for filtering the mixed signal, a demodulator for demodulating the filtered mixed signal, and a slicer for slicing the demodulated signal so as to produce a binary output signal, wherein the oscillator section comprises an oscillator device as defined above and/or an oscillator circuit as defined above. An advantage of the receiver device according to the present invention is its reduced interference sensitivity as the oscillator section operates at a different frequency from the remainder of the receiver device.

Additionally, the present invention provides a consumer device, in particular a wireless digital headphone, comprising a receiver device as defined above.

The present invention will further be explained below with reference to exemplary embodiments illustrated in the accompanying drawings, in which:

Fig. 1 schematically shows a oscillator device according to the present invention.

Fig. 2 schematically shows an embodiment of an oscillator circuit according to the present invention.

Fig. 3 schematically shows an embodiment of an oscillator circuit according to Fig. 2 in more detail.

Fig. 4 schematically shows a filter characteristic utilized in the embodiment of Fig. 2.

Fig. 5 schematically shows an embodiment of a receiver device according to the present invention.

5 Fig. 6 schematically shows an embodiment of a wireless digital headphone according to the present invention.

The oscillator device 1 shown merely by way of non-limiting example in Fig. 10 1 comprises oscillator 2, a synthesizer 3 and a filter 4 arranged in a loop. The oscillator 2 is a controlled oscillator, preferably a voltage controlled oscillator (VCO) whose output frequency may be tuned by a suitable control signal. The oscillator 2 constitutes the oscillator proper of the oscillator device 1 and may comprise a tuning circuit and an amplifier (not shown), the output terminal of the tuning circuit being connected to the input terminal of the amplifier and an output of the amplifier being connected to a first input terminal of the tuning circuit so as to provide a feed-back signal. A second input terminal of the tuning circuit constitutes the input terminal of the oscillator 2 and is connected to the output terminal of the filter 4. Such an oscillator arrangement will later be explained in more detail with reference to Fig. 2.

20 The synthesizer 3 shown schematically in Fig. 1 may comprise one or more dividers and a phase detector (not shown). Suitable synthesizers are commercially available as a single component, for example synthesizer LV2105V manufactured by Sanyo Electric Co. Ltd. of Tokyo, Japan. The filter 4 is a suitable low-pass filter which serves to convert the output signal of the synthesizer into a control signal for the oscillator 2. Typically, the filter 4 averages the output signal of the synthesizer. Although the filter 4 is shown as a separate component in Fig. 1, it may be incorporated in either the oscillator 2 or the synthesizer 3.

The oscillator 2 has not one but two output terminals. A first output terminal 2a is connected to the input terminal of the synthesizer 3, as mentioned above, while a second output terminal 2b constitutes the output terminal of the oscillator device 1. In accordance with the present invention, the output signal at the first terminal 2a has a base frequency f_0 , while the output signal at the second terminal 2b has a higher frequency f_1 which is a harmonic of the base frequency. In other words, the higher frequency f_1 is a multiple of the base frequency f_0 . In a preferred embodiment, the higher frequency f_1 is the first harmonic of the base frequency ($f_1 = 2 \times f_0$), but in other embodiments the higher frequency may be the

second, third or even fourth harmonic of the base frequency. In still other embodiments, more than one higher frequency may be output, for example $f_1 (= 2 \times f_0)$, $f_2 (= 3 \times f_0)$ and $f_3 (= 4 \times f_0)$.

5 A great advantage of the present invention is that the loop constituted by the oscillator 2, the synthesizer 3 and the filter 4 operates at a much lower frequency (f_0) than the output frequency ($f_1, f_2, \dots$). In particular, this reduces the power consumption of the synthesizer as the operating frequency of the dividers is reduced. It will be understood that a reduced power consumption reduces the cost of the device as less input power is required and less power is dissipated. In addition, the lower frequency requires larger component values
10 (resistance, capacitance) which are more accurate, thus improving the overall accuracy of the device.

An exemplary embodiment of the oscillator 2 of Fig. 1 is schematically shown in Fig. 2. The oscillator 2 is shown to comprise a tuning circuit TC, an amplifier AM and a base frequency filter BF. The amplifier AM has two output terminals, one of which is
15 directly connected to the first oscillator output terminal 2a while the other is connected to the second oscillator output terminal 2b via the base frequency filter BF. The input terminals of the tuning circuit TC are connected to one output terminal of the amplifier AM and the oscillator input terminal 2c respectively. The output terminal of the tuning circuit TC is connected to the input terminal of the amplifier AM. As can be seen, the tuning circuit TC
20 and the amplifier AM are connected in a feed-back loop for producing the oscillator frequency, which can be tuned by the signal input at oscillator terminal 2c. The base frequency filter BF removes the base frequency from the output signal of the amplifier AM so that only harmonic frequencies ($f_1, f_2, \dots$) are present at the second oscillator output 2b, while the base frequency (f_0) is output at the first oscillator output terminal 2a. The filter BF
25 may be designed such that only a single harmonic frequency (e.g. f_1) is passed and that all other harmonic frequencies are suppressed.

The oscillator 2 of Fig. 2 will be further explained below with reference to an exemplary embodiment shown in Fig. 3.

The oscillator circuit of Fig. 3 comprises a transistor T_1 which, in combination
30 with bias resistors R_1 and R_4 and output transistor R_3 , provides amplification (amplifier AM of Fig. 2). An LC resonance network (tuning circuit TC) is constituted by capacitors $C_5, C_6, C_8, C_9, C_{10}$, inductance L_1 and varicap (= variable capacitor) D_1 . Capacitor C_{11} and resistor R_5 (loop filter LF) constitute part of filter 4 of Fig. 1. An input (control) signal received at input terminal 2c is fed, via said loop filter LF (R_5 and C_{11}) to the varicap D_1 . This allows the

tuning of the resonance network and hence of the basic oscillator frequency f_0 , and makes the oscillator 2 a voltage controlled oscillator (VCO).

A supply voltage denoted VC is fed to transistor T_1 via a resistor R_6 and a further resistor R_2 . Capacitor C_{12} serves to suppress any voltage supply noise.

5 In accordance with the present invention, a filter stage is connected to the collector of transistor T_1 . This filter stage (base frequency filter BF) consists of capacitors C_1 , C_2 and inductance L_2 . The component values of C_1 , C_2 and L_2 are chosen such that the filter arrangement is a virtual short circuit (C_1 , L_2) to ground for the oscillator frequency (f_0) while being a parallel tuned circuit (C_2 , L_2) for the first harmonic frequency (f_1). The resulting filter
10 characteristic is schematically shown in Fig. 4, where an exemplary base frequency (f_0) of 426.4 MHz is assumed, resulting in a first harmonic (f_1) of 852.8 MHz. As can be seen, the base frequency is suppressed while the first harmonic is passed with substantially no damping (amplitude reduction). In the example shown higher harmonics are gradually suppressed but further suppression of higher harmonics is possible using a modified filter
15 arrangement. Alternatively, the first harmonic may be suppressed in addition to the base frequency, and higher harmonics may be passed with substantially no damping. Instead of the (single) notch filter shown, a multi-notch filter could be used. It will be understood that the particular frequencies mentioned above are given by way of example only and that other frequencies may equally well be used.

20 Returning to Fig. 3, resistor R_2 determines the output impedance of the oscillator 2 at the second output terminal 2b where the higher frequency (f_1) is output. As can be seen, the base frequency (f_0) is output at the first output terminal 2a which is connected to the emitter of transistor T_1 . Coupling capacitors C_3 and C_4 remove any DC component of the output signals. As will be understood by those skilled in the art, the oscillator arrangement of
25 Fig. 3 may be regarded as a modified grounded collector configuration.

The oscillator device 2 of the present invention can advantageously be utilized in an RF (radio frequency) receiver. An exemplary embodiment of a receiver is shown in Fig. 5. The receiver 10 shown comprises an RF (Radio Frequency) filter 11, an amplifier 12, a mixer 13, an IF (Intermediate Frequency) filter 14, an FM detector 15, a base-band filter 16, a
30 slicer 17, an audio processing unit 18 and a speaker 19. In addition, the receiver 10 comprises an oscillator device 1 which in turn comprises an oscillator 2, a synthesizer 3, a loop filter 4, a crystal 5 and a microcontroller 6.

The receiver 10 of Fig. 5 receives an RF input signal from an antenna 21. The first filter 11, which preferably is an SAW (surface acoustic wave) filter, blocks out-of-band

signals and reduces leakage of signals from the receiver to the antenna. The pass band of the first filter 11 is, in the embodiment shown, centered around 864 MHz, thus making the receiver suitable for the 863-865 MHz frequency band reserved for the European cordless audio standard EN 301 357. The filtered signal is passed to a mixer where it is mixed with an
5 853.3 MHz signal generated by the oscillator device 1. This results in a down conversion of the 864 MHz signal to 10.7 MHz. The down converted signal is then filtered by the second filter 14 and may be amplified by a further amplifier (not shown). The resulting signal is fed to a detector for FM detection and reaches, via the third filter 16, the binary slicer 17 which recovers the digital signal. The digital data stream (in the example shown 220-300 kbit/s)
10 output by the slicer 17 may be passed to further devices, for example a digital signal processor or, as in the example shown, an audio processing unit 18 which may contain a digital/analog (D/A) converter and an output amplifier. The loudspeaker 19 may be accommodated in a headphone as shown in Fig. 6.

The oscillator device 1 schematically shown in Fig. 5 largely corresponds with
15 the oscillator device 1 of Fig. 1. However, two additional components are shown in Fig. 5: the crystal 5 and the microcontroller 6. The crystal 5 provides a reference frequency for the synthesizer 3, while the microcontroller 6 controls the dividers of the synthesizer 3 so as to produce the desired frequency. As in Fig. 1, the signal output to the mixer 13 is a harmonic of the signal used in the loop constituted by the oscillator 2, synthesizer 3 and loop filter 4.

20 An important advantage of the receiver 10 according to the present invention is its ability to tune in to the frequency of the RF channel. To this end, several resistors having distinct resistance values may be selectively connected to one or more inputs of the microcontroller. The resistors may be selected by means of a switch or other selection device. Each resistor connected to an input of the microcontroller defines a setting of the dividers in
25 the synthesizer 3, each setting corresponding with a specific frequency. In this way, one of several distinct frequencies (channels) may be selected.

It is noted that the components of the receiver 10 may be known *per se*, with the exception of the oscillator device 1. It will further be understood that various modifications, additions and deletions can be made to the receiver 10 of Fig. 5. For example,
30 the microcontroller 6 may be omitted, and further filters and intermediate amplifiers may be added. The pass frequency of the first filter 11 need not be 864 MHz (EN 301 357 frequency band in Europe) but may for example be approximately 914 MHz (ISM band in the USA) or any other frequency suitable for a particular application, for example a frequency in the MHz or GHz range.

The present invention is particularly suitable for use in consumer electronics devices but is not so limited and may also be applied in professional devices which involve wireless connections, in particular wireless digital RF connections. An example of a consumer product in which the present invention may advantageously be used is a wireless digital headphone for use with audio ("stereo") equipment. Accordingly, the present invention further provides a wireless digital headphone comprising an oscillator device as described above. Such a headphone is shown in Fig. 6. As can be seen, the headphone 20 has an antenna 21 for receiving a signal. A receiver 10 (not shown in Fig. 6) connected to the antenna 21 is accommodated in the headphone 20. Instead of the conventional type of headphone shown which comprises two speaker units connected by a headpiece, a headphone consisting of two separate ear plugs may be used.

Other applications in which the invention may be utilized are, for example, wireless loudspeaker (e.g. wireless surround speakers, wireless second room speakers, full wireless speakers), PC audio streaming to audio sets for MP3 and WMA (Microsoft's Windows Media Audio), wireless internet radio, wireless audio transfer from a PC or audio set to a PDA (Personal Digital Assistant), portable audio equipment (wireless transfer from e.g. CD player to headset), and other applications in which a "wireless link" can be used. Instead of, or in addition to audio, video could be transmitted, for example still images.

The present invention is based upon the insight that using a harmonic oscillator output signal allows the oscillator to operate at a significantly reduced oscillation frequency. This in turn reduces the power consumption of the oscillator and allows less expensive components to be used. The present invention benefits from the further insight that an oscillator producing a harmonic output signal can advantageously be utilized in a high-frequency receiver.

It is noted that any terms used in this document should not be construed so as to limit the scope of the present invention. In particular, the words "comprise(s)" and "comprising" are not meant to exclude any elements not specifically stated. Single (circuit) elements may be substituted with multiple (circuit) elements or with their equivalents.

It will be understood by those skilled in the art that the present invention is not limited to the embodiments illustrated above and that many modifications and additions may be made without departing from the scope of the invention as defined in the appending claims.

CLAIMS:

1. An oscillator device (1) comprising an oscillator circuit (2) and a synthesizer circuit (3), wherein the synthesizer circuit has an output terminal connected to an input terminal of the oscillator circuit for providing a control signal, wherein the oscillator circuit has a first output terminal (2a) connected to an input terminal of the synthesizer circuit for
5 providing a first signal having a first frequency (f_0) to the synthesizer, wherein the oscillator circuit has a second output terminal (2b) for providing a second signal having a second frequency (f_1), and wherein the second frequency (f_1) is a harmonic of the first frequency (f_0).
2. The oscillator device according to claim 1, wherein the second frequency (f_1)
10 is the first harmonic of the first frequency (f_0).
3. The oscillator device according to claim 1, wherein the second frequency (f_1) is the second or third harmonic of the first frequency (f_0).
- 15 4. The oscillator device according to any of the preceding claims, wherein a low-pass filter (4) is arranged between the output terminal of the synthesizer (3) and the input terminal of the oscillator circuit (2).
5. An oscillator circuit (2) for use in the oscillator device (1) according any of
20 claims 1-4, the oscillator circuit comprising an amplifier (T_1 , R_1 , R_4), a resonance network (C_5 , C_6 , C_8 , C_9 , C_{10} , L_1 , D_1), a filter stage (C_1 , C_2 , L_2), an input terminal (2c) for receiving a tuning signal, a first output terminal (2a) for outputting a first signal having a first frequency (f_0) and a second output terminal (2b) for outputting a second signal having a second frequency (f_1), wherein the filter stage is connected to the second output terminal and is
25 designed for suppressing the first frequency (f_0) and passing the second frequency (f_1), the second frequency being a harmonic of the first frequency.

6. The oscillator circuit according to claim 5, wherein the filter stage (C_1 , C_2 , L_2) is designed such that it constitutes a virtual short circuit to ground for the first frequency (f_0) while constituting a parallel tuned circuit for the harmonic frequency (f_1).
- 5 7. A receiver device (10), comprising an input filter (11) for filtering an antenna signal, an amplifier (12) for amplifying the filtered antenna signal, a mixer (13) for mixing the amplified antenna signal with an oscillator signal produced by an oscillator section (1), a filter (14) for filtering the mixed signal, a demodulator (15) for demodulating the filtered mixed signal, and a slicer (17) for slicing the demodulated signal so as to produce a binary
10 output signal, wherein the oscillator section (1) comprises an oscillator device according to any of claims 1-4 and/or an oscillator circuit (2) according to claim 5 or 6.
8. A consumer device (20), comprising a receiver device (10) according to claim 7.
- 15 9. The consumer device according to claim 8 which comprises a headphone.

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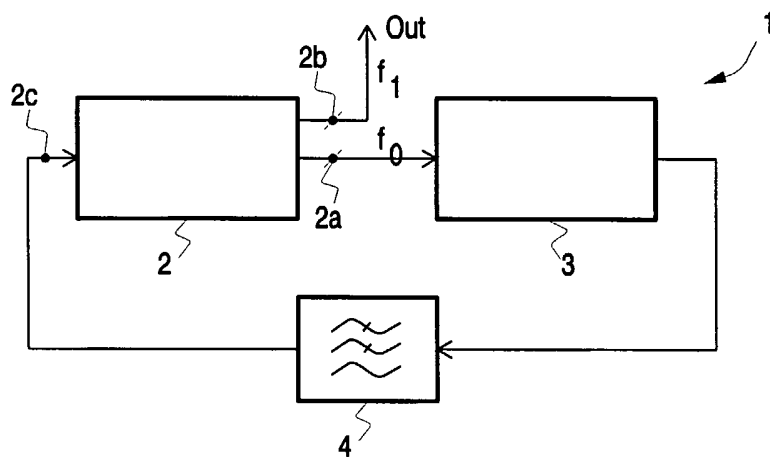


FIG. 1

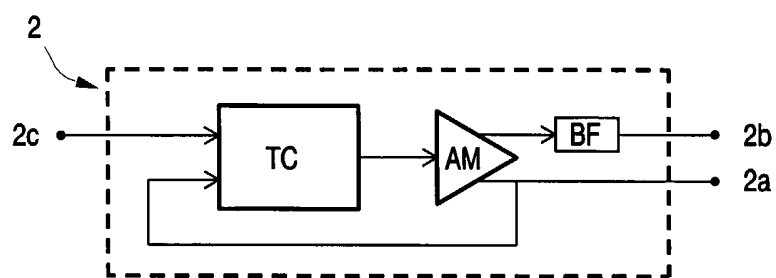


FIG. 2

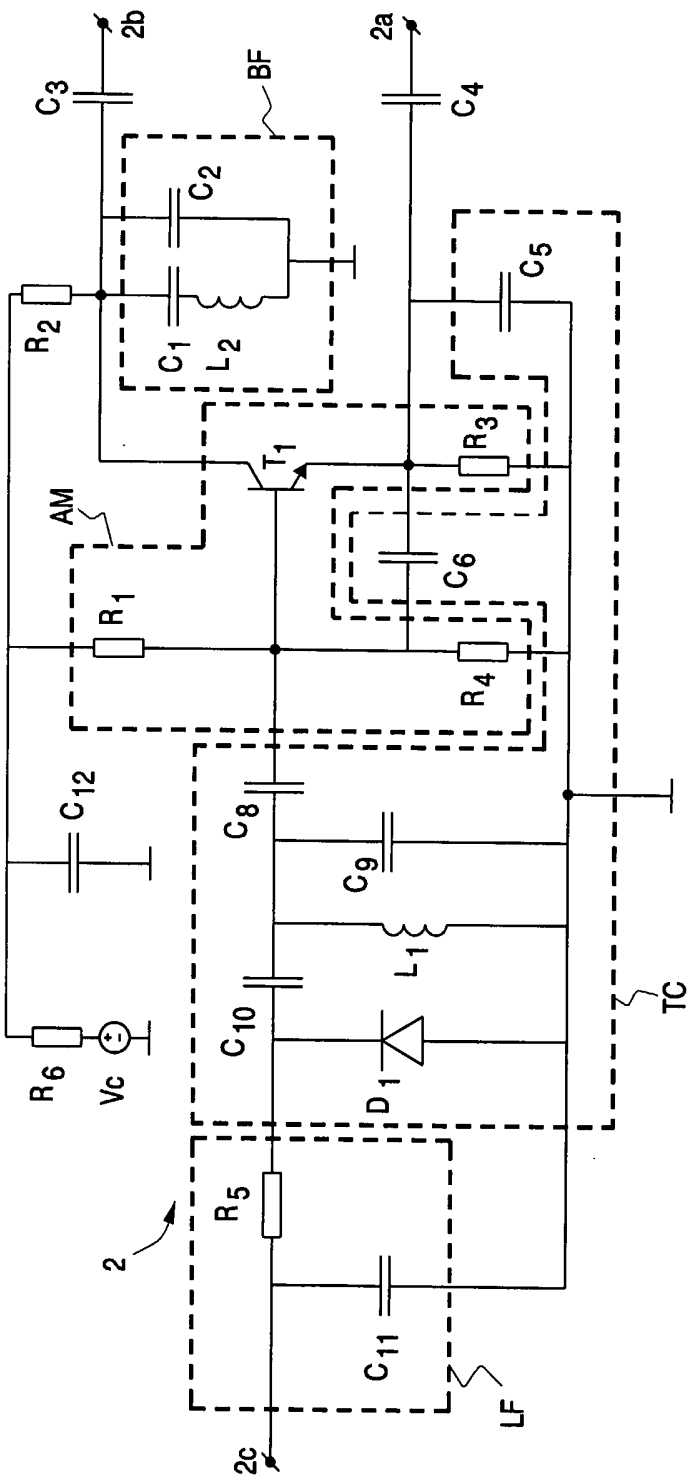


FIG. 3

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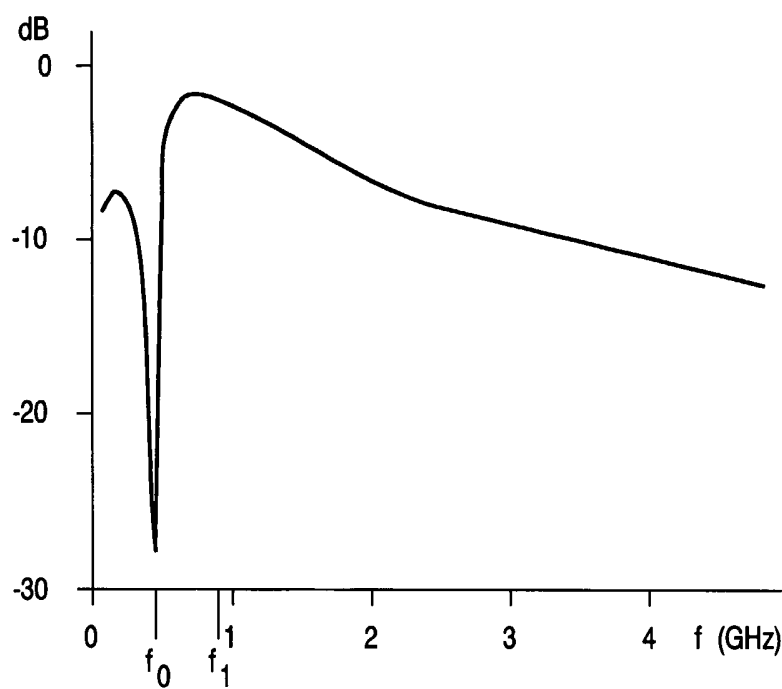


FIG. 4

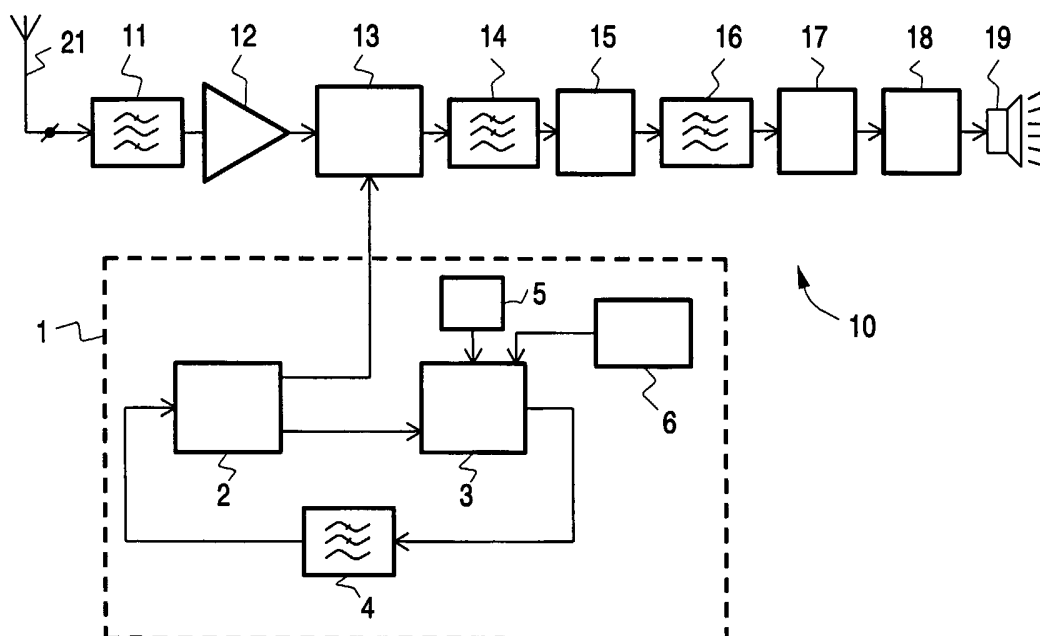


FIG. 5

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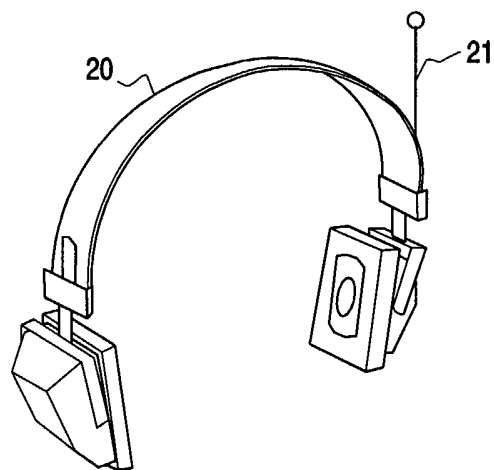


FIG. 6