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(54) **Systems for controlling pixels**

Systeme zur Pixelansteuerung

Systèmes de contrôle des pixels

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Description

BACKGROUND

[0001] The present application relates in general to display devices and relates in particular to a system for controlling a light emitting pixel of a display device.

[0002] Electroluminescence (EL) display devices include organic light emitting diode (OLED) displays and polymeric light emitting diode (PLED) displays. In accordance with associated driving methods, an OLED can be an active matrix type or a passive matrix type. An active matrix OLED (AM-OLED) display typically is thin and exhibits lightweight characteristics, spontaneous luminescence with high luminance efficiency and low driving voltage. Additionally, an AM-OLED display provides the perceived advantages of increased viewing angle, high contrast, high-response speed, full color and flexibility.

[0003] An AM-OLED display is driven by electric current. Specifically, each of the matrix-array pixel areas of an AM-OLED display includes at least one thin film transistor (TFT), serving as a driving TFT, to modulate the driving current. Driving current is modulated based on the variation of capacitor storage potential to control the brightness and gray level of the pixel areas.

[0004] The gray level is selected by using a voltage divider comprising resistors. Fig. 1a is a schematic diagram of a conventional voltage divider. The voltage divider 10 comprises resistors serially connected between a high voltage source (Vcc) and a low voltage source (Gnd). Each point between two resistors has a corresponding voltage indicating a particular gray level.

[0005] A point 110 of voltage divider 10 can provide a maximum gray level indicating a maximum brightness of the AM-OLED. Since a voltage divider only provides one maximum gray level, if a user desires to adjust the maximum brightness of the AM-OLED higher, the AM-OLED requires several voltage dividers.

[0006] Fig. 1b is a schematic diagram of another conventional voltage divider. A voltage between two resistors can be adjusted according to the resistance of two resistors. In this case, a first maximum gray level provided by voltage divider 10 is 100nits, a second maximum gray level provided by voltage divider 12 is 150nits, and a third maximum gray level provided by voltage divider 14 is 200nits. Therefore, the brightness of the AM-OLED can be adjusted by providing different maximum gray levels; however, the cost and volume of the AM-OLED are increased.

[0007] EP 1 600 924 A1, which is prior art according to Art. 54(3) of the European Patent Convention, discloses an organic light emitting display, wherein a first pixel and a second pixel share a data line, a select scan line, and a driving element, and wherein a field is divided into first and second subfields. An organic light emitting element of the first pixel is driven by a first emission control signal transmitted to a first emit scan line, and an organic light emitting element of the first pixel is driven by a second emission control signal transmitted to a second emit scan line. The first emission control signal has a low-level pulse in the first subfield, the second emission control signal has a low-level pulse in the second subfield, and a select signal transmitted to the select scan line has a low-level pulse in each of the first and second subfields. In addition, a scan driver for driving the select signal line, the first emit scan line, and the second emit scan line is provided. This document does not disclose in particular a combinatorial logic unit in the sense of claim 1.

[0008] WO 2005/036515 A1 discloses an active matrix electroluminescent display which has means for interrupting the drive of current through the display element. Row driver circuitry for the display has a shift register and logic arrangement for generating the drive voltage for the interrupting means, and which includes a pulse having a duration which can be varied up to substantially the full field period less the address period. The signal or signals propagated through the shift register arrangement control the pulse duration. Control for a row of the display is achieved by row addressing of the pixels with control of the overall light emission period of each row. The control enables a scrolling addressing scheme to be implemented. The logic arrangement receives, however, only two shifted signals to control a light emitting pixel.

SUMMARY

[0009] It is an object of the present invention to provide an improved system for controlling a first light emitting pixel of a display, which can be operated in a more flexible manner.

[0010] This problem is solved by a system for controlling a first light emitting pixel of a display according to claim 1. Further advantageous embodiments are the subject-matter of the dependent claims.

[0011] Systems for controlling pixels are provided. An exemplary embodiment of such a system comprises a scan driver comprising: a first shift-register unit operative to output a first shift signal according to a first start signal; a second shift-register unit operative to output a second shift signal according to the first shift signal for lighting the first pixel; a third shift-register unit operative to output a third shift signal according to the second shift signal; and a first processor operative to control the first pixel to receive the first data signal according to the first, the second, and the third shift signals. A duty cycle of the first start signal determines a light-emitting duration of the first pixel.

[0012] Another embodiment of a system for controlling a pixel comprises: a data signal line operative to provide data to the pixel; and a scan driver operative to control illumination of the pixel during sequential time periods such that, if data provided by the data signal line is different between a first time period and a second time period, brightness of the pixel differs during a third time period and a sequential fourth time period. The pixel is illuminated during the third time period and the fourth

time period.

[0013] Another embodiment of a system for controlling a pixel comprises a display device. The display device comprises a display panel comprising a first pixel; an EL driver operative to output a start signal; a data driver operative to output a first data signal to the first pixel; and a scan driver operative to output a first scan signal and a second scan signal to the first pixel. The first pixel is operative to receive the first data signal according to the first scan signal and the first pixel is illuminated according to the second scan signal. The scan driver comprises: a first shift-register unit operative to output a first shift signal according to the first start signal; a second shift-register unit operative to output a second shift signal according to the first shift signal for lighting the first pixel; a third shift-register unit operative to output a third shift signal according to the second shift signal; and a first processor operative to control the first pixel to receive the first data signal according to the first, the second, and the third shift signals. A duty cycle of the first start signal establishes a light-emitting duration of the first pixel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The invention can be more fully understood by reading the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

- Fig. 1a is a schematic diagram of a conventional voltage divider;
- Fig. 1b is a schematic diagram of another conventional voltage divider;
- Fig. 2a is a schematic diagram of an embodiment of a system for controlling pixels;
- Fig. 2b is a schematic diagram of an embodiment of a display device used in the system of Fig. 2a;
- Fig. 3 is a schematic diagram of an embodiment of a scan driver;
- Fig. 4 is a timing diagram of the scan driver of Fig. 3;
- Fig. 5 is a schematic diagram of another embodiment of a scan driver;
- Fig. 6 is a schematic diagram of another embodiment of a scan driver.

DETAILED DESCRIPTION

[0015] Systems for controlling pixels are provided. As will be described with reference to several exemplary embodiments, brightness of the pixels of a display can be adjusted, such as by increasing the light-emitting duration of the pixels. In this regard, Fig. 2a is a schematic diagram of an embodiment of a system for controlling pixels that is implemented as an electronic device. Note that such an electronic device can be provided in various configurations, such as a PDA, a display monitor, a notebook computer, a tablet computer, or a cellular phone. Electronic device 2 comprises a display device 20 and a digital-to-analog converter (DAC) 25. DAC 25 supplies power to display device 20.

[0016] Fig. 2b is a schematic diagram of an embodiment of display device 20. As shown in Fig. 2b, display device 20 comprises a display panel 21 comprising pixels P_{11}~P_{mn}, a data driver 22, a scan driver 23, and an electroluminescence (EL) driver 24, which can be implemented by an integrated circuit (IC).

[0017] Data driver 22 provides data signals D_1~D_m to pixels P_{11}~$P_{mn.}$ Scan driver 23 receives a start signal (STV) output from EL driver 24 and controls pixels P_{11}~P_{mn} by scan signals S_1~S_n and XS_1~XS_n. Pixels P_{11}~P_{mn} receive data signals D_1~D_m according to scan signals S_1~S_n and pixels P_{11}~P_{mn} are illuminated according to scan signals XS_1~XS_n.

[0018] Fig. 3 is a schematic diagram of an embodiment of a scan driver. For clarity, only two pixels of the display are shown. The structures of the pixels shown in Fig. 3 are given as an example; however, in other embodiments, other configurations can be used.

[0019] Scan driver 23 comprises a shift register circuit 33 and processors 34~37. Shift register circuit 33 comprises shift register units VSR_1~VSR_4. Each shift register unit outputs a shift signal according to a duty cycle of start signal STV.

[0020] Processor 34 comprises logic units 341 and 342. A first input terminal of logic unit 341 is floating and a second input terminal of logic unit 341 receives shift signal SS_1. A first input terminal of logic unit 342 is coupled to an output terminal of logic unit 341 and a second input terminal of logic unit 342 receives shift signal SS_2. Since the first input terminal of logic unit 341 is floating, an output terminal of logic unit 342 does not control a pixel. Processor 35 comprises logic units 351 and 352. Logic unit 351 receives shift signals SS_1 and SS_2. Logic unit 352 receives an output signal of logic unit 351 and shift signal SS_3 to generate scan signal SD_1. Pixel 31 receives data signal DS according to scan signal SD_1. Shift signal SS_2 also corresponds to scan signals XSD_1. Pixel 31 is illuminated according to scan signal XSD_1.

[0021] Processor 36 comprises logic units 361 and 362. Logic unit 361 receives shift signals SS_2 and SS_3. Logic unit 362 receives an output signal of logic unit 361 and shift signal SS_4 to generate scan signal SD_2. Pixel 32 receives data signal DS according to scan signal SD_2. Shift signal SS_3 corresponds to scan signals XSD_2. Pixel 32 is illuminated according to scan signal XSD_2.

[0022] Processor 37 comprises logic units 371 and 372. Logic unit 371 receives shift signals SS_3 and SS_4. A first input terminal of logic unit 372 receives an output signal of logic unit 371 and a second input terminal of logic unit 372 is floating. Since the second input terminal of logic unit 372 is floating, an output terminal of logic unit 372 does not control a pixel.

[0023] In this embodiment, logic units 341, 351, 361, and 371 are XOR gates and logic units 342, 352, 362, and 372 are AND gates.

[0024] Fig. 4 is a timing diagram of the embodiment of

the scan driver depicted in Fig. 3. In Fig. 3, shift register units VSR_1~VSR_4, respectively, output shift signals SS_1~SS_4 responsive to shift register unit VSR_1 receiving start signal STV.

[0025] Pixel 31 receives data signal DS according to shift signals SS_1~SS_3 received by processor 35. As shown in Fig. 4, a logic level of shift signal SS_1 is low and those of shift signals SS_2 and SS_3 are high such that a logic level of scan signal SD_1 is high in period P_1.

[0026] Therefore, transistor 311 can be turned on. A data signal is transmitted to capacitor 312 through transistor 311 to charge capacitor 312. Transistor 313 is turned on for outputting driving current I_1 as a voltage of capacitor 312 reaches a first preset value. Since a logic level of scan signal XSD_1 is high, transistor 314 is turned on in period P_1. Light-emitting element 315 is illuminated as driving current I_1 is transmitted to light-emitting element 315 by transistor 314.

[0027] In period P_2, the logic level of scan signal XSD_1 is low such that light-emitting element 315 is extinguished. Since the logic level of scan signal SD_2 is high, capacitor 322 is charged such that driving current I_2 is provided by transistor 323. Light-emitting element 325 receives driving current I_2 and is illuminated as the logic level of scan signal SD_2 is high.

[0028] In period P_3, the logic level of scan signal XSD_2 is low such that light-emitting element 325 is extinguished. In period P_4, the logic level of scan signal XSD_1 is high such that transistor 314 is turned on. Since the voltage of capacitor 312 maintains the first preset value, transistor 313 generates driving current I_1, which is provided to light-emitting element 315 for illuminating that element.

[0029] In period P_5, since the logic level of scan signal SD_1 is high, capacitor 312 is again charged according to data signal DS such that the voltage of capacitor 312 reaches a second preset value. Transistor 313 generates new driving current I_1 according to the new voltage of capacitor 312. Since the logic level of scan signal XSD_1 is also high, light-emitting element 315 is illuminated.

[0030] In period P_4, the voltage of capacitor 312 depends on the data signal DS received by transistor 311 in period P_1. In period P_5, the voltage of capacitor 312 depends on the data signal DS received by transistor 311 in period P_5. Although light-emitting element 315 is illuminated in periods P_4 and P_5, if data signal DS in period P_1 is different than the data signal DS in period P_5, the brightness of light-emitting element 315 in period P_4 differs from the brightness of light-emitting element 315 in period P_5.

[0031] In period P_6, the logic level of scan signal XSD_2 is high such that transistor 324 is turned on. Since the voltage of capacitor 322 can turn on transistor 323, light-emitting element 325 receives driving current I_2 and is illuminated.

[0032] In period P_7, since the logic level of scan signal SD_2 is high, capacitor 322 is again charged according to data signal DS. Transistor 323 outputs new driving current I_2 according to the voltage of capacitor 322. Since the logic level of scan signal XSD_2 is also high, light-emitting element 325 is illuminated.

[0033] The voltage of capacitor 322 in period P_6 depends on the data signal DS received by transistor 321 in period P_2. The voltage of capacitor 322 in period P_7 depends on the data signal DS received by transistor 321 in period P_7. Although light-emitting element 325 is illuminated in periods P_6 and P_7, if data signal DS in period P_2 is different than the data signal DS in period P_7, the brightness of light-emitting element 325 in period P_6 is different from the brightness of light-emitting element 325 in period P_7.

[0034] Taking pixel 31 as an example, since start signal STV only has a cycle in period P_8, the light-emitting state of light-emitting element 315 is luminous-dark-luminous in periods P_1~P_4. If transistor 314 is replaced by a PMOS transistor or the start signal cycle is inverted, the light-emitting state of light-emitting element 315 is changed to dark-luminous-dark in periods P_1~P_4. The light-emitting state of light-emitting element 315 is luminous-dark-luminous-dark-luminous as start signal STV has two cycles in period P_8.

[0035] Duration of each light-emitting state depends on the duty cycle of start signal STV. Assume a display panel requires 16.63ms to display an image and the light-emitting states of all light-emitting elements in the display panel are luminous-dark-luminous. Then, if the duration of the luminous state is 16.63ms, the brightness of the display panel is 100%, if the duration of the luminous state is 13.304ms, the brightness of the display panel is 80%. If the duration of the luminous state is 8.315ms, the brightness of the display panel is 50%.

[0036] For example, assume light-emitting element 315 is illuminated during periods P_1, P_4, and P_5 according to scan signal XSD_1. If the light-emitting duration (the duration of periods P_1, P_4, and P_5) of light-emitting element 315 is 13.304ms, the brightness of the display panel is 80%. Therefore, the duty cycle of start signal STV controls the light-emitting duration of light-emitting element and thus controls the brightness of the display panel. Because of this, a user can adjust the brightness of the display panel according to actual requirements for reducing power consumption.

[0037] Fig. 5 is a schematic diagram of another embodiment of a scan driver. Each of the logic units 342, 352, 362, and 372 further receives a vertical output enable signal ENBV. Each of the buffers 371~374 has an amplification function. Buffer 371 amplifies scan signal SD_1 for turning on transistor 311. Buffer 372 amplifies scan signal XSD_1 for turning on transistor 314. Buffer 373 amplifies scan signal SD_2 for turning on transistor 321. Buffer 374 amplifies scan signal XSD_2 for turning on transistor 324.

[0038] Fig. 6 is a schematic diagram of another embodiment of a scan driver. Each pixel comprises three sub-pixels for displaying red, green and blue, respectively. For clarity, Fig. 6 only shows a pixel comprising sub-

pixels 61~63 respectively displaying red, green and blue.

[0039] Each shift register unit VSR_{1B}~VSR_{3B} provides a shift signal as shift register unit VSR_{1B} receives start signal STV_B. Processor 64 receives shift signals provided by shift register units VSR_{1B}~VSR_{3B} for generating scan signal SD_1. Sub-pixels 61~63 respectively receive data signals DS_R, DS_G and DS_B according to scan signal SD_1. A shift signal provided by shift register ister unit VSR_{2B} is scan signal XSD_{1B}. Sub-pixel 63 is illuminated according to scan signal XSD_{1B}.

[0040] When shift register unit VSR_{1R} receives start signal STV_R, a shift signal provided by shift register unit VSR_{2R} is used as scan signal XSD_{1R}. Sub-pixel 61 is illuminated according to scan signal XSD_{1R}.

[0041] When shift register unit VSR_{1G} receives start signal STY_G, a shift signal provided by shift register unit VSR_{2G} is used as scan signal XSD_{1G}. Sub-pixels 62 is illuminated according to scan signal XSD_{1G}.

[0042] The light-emitting duration of sub-pixels 61 ~ 63 are respectively controlled by duty cycles of start signals STV_R, STV_G and STV_G.

[0043] In summary, the light-emitting duration of the pixels of a display can be controlled by the duty cycle of start signal STV. The brightness of the display panel is brighter as the light-emitting duration of the pixels is longer, and vice versa. Therefore, a user can adjust the brightness of the display panel according to actual requirements.

Claims

1. A system (2) for controlling a first light emitting pixel (31, 63) which is adapted to receive a first data signal (DS, DS_B) when a first scan signal (SD1) is active and to emit light when a first light emission control signal (XSD1, XSD_{1B}) is active, said system comprising:

a display device (20) comprising:

a scan driver (23) comprising:

a first shift-register stage (VSR1, VSR_{1B}) adapted to input a first start signal (STV, STV_B) and to output a first shifted signal (SS1);
a second shift-register stage (VSR2, VSR_{2B}) adapted to input the first shifted signal (SS1) and to output a second shifted signal (SS2);
a third shift-register stage (VSR3, VSR_{3B}) adapted to input the second shifted signal (SS2) and to output a third shifted signal (SS3); and
a first combinatorial logic unit (35, 64) adapted for generating the first scan signal (SD1) in accordance with the first (SS1), the second (SS2), and the third (SS3) shifted signals;
wherein said first shift-register stage (VSR1, VSR_{1B}), said second shift-register stage (VSR2, VSR_{2B}) and said third shift-register stage (VSR3, VSR_{3B}) form a shift register circuit (33);
a display panel (21) disposing the first light emitting pixel (31, 63);
an electroluminescence driver (24) adapted to output the first start signal (STV, STV_B); and
a data driver (22) adapted to output the first data signal (DS, DS_B) to the first light emitting pixel (31, 63);

wherein the second shifted signal (SS2) serves as the first light emission control signal (XSD1, XSD_{1B}); and
wherein the first combinatorial logic unit (35, 64) comprises:

a first logic unit (351) comprising a first input terminal adapted to receive the first shifted signal (SS1), a second input terminal adapted to receive the second shifted signal (SS2) and a first output terminal,
wherein the first logic unit (351) is adapted such that the first output terminal outputs a first logic level when a logic level of the first shifted signal (SS1) equals that of the second shifted signal (SS2) and such that the first output terminal outputs a second logic level when the logic level of the first shifted signal (SS1) differs from that of the second shifted signal (SS2); and
a second logic unit (352) comprising a third input terminal connected to the first output terminal, a fourth input terminal adapted to receive the third shifted signal (SS3), and a second output terminal connected to the first light emitting pixel (31, 63) to provide the first scan signal (SD1),

wherein the second logic unit (352) is adapted such that the second output terminal outputs the first logic level when one or both of the logic levels of the first output terminal and the third shifted signal (SS3) equal the first logic level and such that the second output terminal outputs the second logic level when the logic level of the first output terminal and that of the third shifted signal (SS3) equal the second logic level.

2. The system as claimed in claim 1, wherein the first light emitting pixel (31) comprises a first transistor (311), a second transistor (313), a third transistor (314), a light-emitting element (315) and a capacitor (312), wherein the first transistor (311) is adapted to transmit the first data signal (DS) to the gate of the second transistor (313) in accordance with the first scan signal (SD1), wherein the second transistor (313), the third transistor (314) and the light-emitting element (315) are serially connected between a first voltage level (Vcc) and a second level (Vss), the third transistor (314) is controlled by the second shifted signal (SS2) and the capacitor (312) is connected between the gate and the source of the second transistor (313).

3. The system as claimed in claim 1 or 2, wherein the second logic unit (352) further comprises a fifth input terminal adapted to receive a control signal (ENBV), wherein the second logic unit (352) is further adapted such that the second output terminal outputs the first logic level when at least one of the logic levels of the control signal (ENBV), the first output terminal or third shifted signal (SS3) equals the first logic level, and such that the second output terminal outputs the second logic level when the logic levels of the control signal (ENBV), of the first output terminal and of the third shifted signal (SS3) equal the second logic level.

4. The system as claimed in claims 1 or 3, wherein the display panel (21) further comprises a second light emitting pixel (61) and a third light emitting pixel (62) disposed on said display panel (21) and wherein the scan driver (23) further comprises:

a fourth shift register stage (VSR_{1R}) adapted to input a second start signal (STV_R) and to output a fourth shifted signal;
a fifth shift register stage (VSR_{2R}) adapted to input the fourth shifted signal and to output a fifth shifted signal as second light emission control signal (XSD_{1R});
a sixth shift register stage (VSR_{1G}) adapted to input a third start signal (STV_G) and to output a sixth shifted signal;
a seventh shift register unit (VSR_{2G}) adapted to input the sixth shifted signal and to output a seventh shifted signal as third light emission control signal (XSD_{1G}); wherein the scan driver is adapted to provide the first scan signal (SD1) to the first light emitting pixel (63), the second light emitting pixel (69), and the third light emitting pixel (62) to control the first light emitting pixel (63), the second light emitting pixel (S1), and the third light emitting pixel (62), respectively, to receive the first data signal (DS_B), a second data signal (DS_R), and a third data signal (DS_G), respectively, and is adapted to control the light-emitting duration of the first light emitting pixel (63), the second light emitting pixel (61), and the third light emitting pixel (62), respectively, using the first light emission control signal (XSD_{1B}), second light emission control signal (XSD_{1R}) and third light emission control signal (XSD_{1G}), respectively, in accordance with a duty cycle of the first start signal (STV_B), the second start signal (STV_R), and the third start signal (STV_G), respectively.

5. The system as claimed in claim 4, wherein the first light emitting pixel (63) is adapted to display a blue color, the second light emitting pixel (61) is adapted to display a red color, and the third light emitting pixel (62) is adapted to display a green color.

6. The system as claimed in any of the preceding claims, wherein the first logic unit (351) is an XOR gate and the second logic unit (352) is an AND gate.

7. The system as claimed in claim 4 or 5, wherein the data driver (22) is further adapted to output the second data signal (DS_R) to the second light emitting pixel (61) and the third data signal (DS_G) to the third light emitting pixel (62).

8. The system as claimed in any of the preceding claims, further comprising:

a digital-to-analog converter (DAC) adapted to supply power to the display device (20).

9. The system as claimed in any of the preceding claims, further comprising:

means for supplying power to the display device (20).

Patentansprüche

1. System (2) zum Steuern eines ersten Lichtemissionspixels (31, 63), welches ausgelegt ist, um ein erstes Datensignal (DS, DS_B) zu empfangen, wenn ein erst Scan-Signal (SD1) aktiv ist, und um Licht zu emittieren, wenn ein erstes Lichtemissions-Steuersignal (Xsd1, Xsd_{1B}) aktiv ist, wobei das System umfasst:

eine Anzeigeeinrichtung (20), umfassend:

einen Steuerungstreiber (23), der umfasst:

eine erste Schieberegisterstufe (VSR1, VSR_{1B}) die zum Eingeben eines ersten Startsignals (STV, STV_B) und zur Aus-

gabe eines ersten verschobenen Signals (SS1) ausgelegt ist;
eine zweite Schieberegisterstufe (VSR2, VSR_{2B}), die zum Eingeben des ersten verschobenen Signal (SS1) und zur Ausgabe eines zweites verschobenen Signals (SS2) ausgelegt ist;
eine dritte Schieberegisterstufe (VSR3, VSR_{3B}), die zum Eingeben des zweiten verschobenen Signals (SS2) und zur Ausgabe eines dritten verschobene Signals (SS3) ausgelegt ist; und
eine erste kombinatorische Logikeinheit (35, 64), die zum Erzeugen des ersten Scan-Signals (SD1) in Übereinstimmung mit dem ersten (SS1), mit dem zweiten (SS2) und mit dem dritten (SS3) verschobenen Signal ausgelegt ist;
wobei die ersten Schieberegisterstufe(VSR1, VSR_{1B}), die zweite Schieberegisterstufe (VSR2, VSR_{2B}) und die dritte Schieberegisterstufe (VSR3, VSR_{3B}) eine Schieberegisterschaltung (33) ausbilden,
eine Anzeigetafel (21) Anordnen des ersten Lichtemissionspixels (31, 63);
einen Elektrolumineszenz-Treiber (24), der ausgelegt ist, um das erste Startsignal (STV, STV_B) auszugeben; und
einen Datentreiber (22), der ausgelegt ist, um das erste Datensignal (DS, DS_B) an das erste Lichtemissionspixel (31, 63) auszugeben;
wobei das zweite verschobene Signal (SS2) als das erste Lichtemissions-Steuersignal (Xsd1, Xsd_{1B}) dient; und
wobei die erste kombinatorische Logikeinheit (35, 64) umfasst:

eine erste Logikeinheit (351) mit einem ersten Eingangsanschluss, der ausgelegt ist, um das erste verschobene Signal (SS1) zu empfangen, mit einem zweiten Eingangsanschluss, der ausgelegt ist, um das zweite verschobene Signal (SS2) zu empfangen, und mit einem ersten Ausgangsanschluss,
wobei die erste Logikeinheit (351) ausgelegt ist, so dass der erste Ausgangsanschluss einen ersten Logikpegel ausgibt, wenn ein Logikpegel des ersten verschobenen Signals (SS1) gleich dem des zweiten verschobenen Signals (SS2) ist, und so dass der erste Ausgangsanschluss einen zweiten Logikpegel ausgibt, wenn der Logikpegel des ersten verschobenen Signals (SS1) von dem des zweiten verschobenen Signals (SS2) verschieden ist; und
eine zweite logische Einheit (352) mit einem dritten Eingangsanschluss, der mit dem ersten Ausgangsanschluss verbunden ist, mit einem vierten Eingangsanschluss, der ausgelegt ist, um das dritte verschobene Signal (SS3) zu empfangen, und mit einem zweiten Ausgangsanschluss, der mit dem ersten Lichtemissionspixel (31, 63) verbunden ist, um das erste Scan-Signal (SD1) bereitzustellen,
wobei die zweite Logikeinheit (352) ausgelegt ist, so dass der zweite Ausgangsanschluss den ersten Logikpegel ausgibt, wenn einer oder beide der Logikpegel des ersten Ausgangsanschlusses und das dritte verschobene Signal (SS3) gleich dem ersten Logikpegel sind, und so dass der zweite Ausgangsanschluss den zweiten Logikpegel ausgibt, wenn der Logikpegel des ersten Ausgangsanschlusses und der des dritten verschobenen Signals (SS3) gleich dem zweiten Logikpegel sind.

2. System nach Anspruch 1, wobei das erste Lichtemissionspixel (31) einen ersten Transistor (311), einen zweiten Transistor (313), einen dritten Transistor (314), ein Lichtemissionselement (315) und einen Kondensator (312) umfasst, wobei der erste Transistor (311) ausgelegt ist, um das erste Datensignal (DS) an das Gate des zweiten Transistors (313) in Übereinstimmung mit dem ersten Scan-Signal (SD1) zu übertragen, wobei der zweite Transistor (313), der dritte Transistor (314) und das Lichtemissionselement (315) in Reihe zwischen einem ersten Spannungspegel (Vcc) und einen zweiten Pegel (Vss) geschaltet sind, der dritte Transistors (314) von dem zweiten Signal verschoben Signal (SS2) gesteuert wird und der Kondensator (312) zwischen Gate und Source des zweiten Transistors (313) geschaltet ist.

3. System nach Anspruch 1 oder 2, wobei die zweite Logikeinheit (352) weiterhin einen fünften Eingangsanschluss aufweist, der ausgelegt ist, um ein Steuersignal (ENBV) zu empfangen, wobei die zweite Logikeinheit (352) weiterhin so ausgelegt ist, dass der zweite Ausgangsanschluss den ersten Logikpegel

ausgibt, wenn wenigstens der Logikpegel des Steuersignals (ENBV), des ersten Ausgangsanschlusses oder des dritten verschobenen Signals (SS3) gleich dem ersten Logikpegel ist, und so dass der zweite Ausgangsanschluss den zweiten Logikpegel ausgibt, wenn die Logikpegel des Steuersignals (ENBV), des ersten Ausgangsanschlusses und des dritten verschobenen Signals (SS3) gleich dem zweiten Logikpegel sind.

4. System nach einem der Ansprüche 1 oder 3, wobei die Anzeigetafel (21) weiterhin ein Lichtemissionspixel (61) und ein drittes Lichtemissionspixel (62) aufweist, die auf dem Anzeigefeld (21) angeordnet sind, und wobei der Scantreiber (23) weiterhin umfasst:

eine vierte Schieberegisterstufe (VSR_{1R}), die zum Eingeben eines zweiten Startsignals (STV_R) und zum Ausgeben eines vierten verschobenen Signals ausgelegt ist;
eine fünfte Schieberegisterstufe (VSR_{2R}), die zum Eingeben des vierten verschobenen Signals und zur Ausgabe eines fünften verschobenen Signals als das zweite Lichtemissions-Steuersignal (XSD_{1R}) ausgelegt ist;
eine sechste Schieberegisterstufe (VSR_{1G}), die zum Eingeben eines dritten Startsignals (STV_G) und zum Ausgeben eines sechsten verschobenen Signals ausgelegt ist;
eine siebte Schieberegistereinheit (VSR_{2G}), die zum Eingeben des sechsten verschobenen Signals und zur Ausgabe eines siebten verschobenen Signals als das dritte Lichtemissions-Steuersignal (XSD_{1G}) ausgelegt ist; wobei
der Scantreiber dazu ausgelegt ist, um dem ersten Lichtemissionspixel (63) das erste Scan-Signal (SD1) bereit zu stellen, wobei das zweite Lichtemissionspixel (61) und das dritte Lichtemissionspixel (62) ausgelegt sind, um das erste Lichtemissionspixel (63) zu steuern, wobei das zweite Lichtemissionspixel (61) und das dritte Lichtemissionspixel (62) jeweils ausgelegt sind, um das erste Datensignal (DS_B), ein zweites Datensignal (DS_R) und ein drittes Datensignal (DS_G) zu empfangen, und dazu ausgelegt ist, um jeweils die Dauer der Lichtemission des ersten Lichtemissionspixels (63), des zweiten Lichtemissionspixel (61) und des dritten Lichtemissionspixels (62) zu steuern, und zwar unter Verwendung des ersten Lichtemissions-Steuersignals (XSD_{1B}), des zweiten Lichtemissions-Steuersignals (XSD_{1R}) und des dritten Lichtemissions-Steuersignals (XSD_{1G}) und jeweils in Übereinstimmung mit einem Tastverhältnis des ersten Startsignals (STV_B), des zweiten Startsignals (STV_R) und des dritten Startsignals (STV_G).

5. System nach Anspruch 4, wobei das erste Lichtemissionspixel (63) ausgelegt ist, um eine blaue Farbe anzuzeigen, wobei das zweite Lichtemissionspixel (61) ausgelegt ist, um eine rote Farbe anzuzeigen, und das dritte Lichtemissionspixel (62) ausgelegt ist, um eine grüne Farbe anzuzeigen.

6. System nach einem der vorhergehenden Ansprüche, wobei die erste Logikeinheit (351) ein XOR-Gatter und die zweite Logikeinheit (352) ein UND-Gatter ist.

7. System nach Anspruch 4 oder 5, wobei der Datentreiber (22) weiterhin zur Ausgabe des zweiten Datensignals (DS_R) an das zweite Lichtemissionspixel (61) und des dritten Datensignals (DS_G) an das dritte Lichtemissionspixel (62) ausgelegt ist.

8. System nach einem der vorhergehenden Ansprüche, weiterhin umfassend:

einen Digital-zu-Analog-Wandler (DAC), der ausgelegt ist, um die Anzeigeeinrichtung (20) mit Strom zu versorgen.

9. System nach einem der vorhergehenden Ansprüche, weiterhin umfassend Mittel zur Stramversorgung der Anzeigeeinrichtung (20).

Revendications

1. Un système (2) de commande d'un premier pixel émetteur de lumière (31, 63), qui est adapté pour recevoir un premier signal de donnée (DS, DS_B) dès lors qu'un premier signal de balayage (SD1) est actif et peut émettre de la lumière lorsqu'un premier signal de commande d'émission de lumière (XSD1, XSD_{1B}) est actif, ledit système comprenant :

un dispositif d'affichage (20) comprenant :

un pilote de balayage (23) comprenant :

un premier étage de registre à décalage (VSR1, VSR_{1B}) adapté pour recevoir un premier signal de démarrage (XTV, STV_B) et pour générer un premier signal décalé (SS1) ;
un second étage de registre à décalage (VSR2, VSR_{2B}) adapté pour recevoir le premier signal décalé (SS1) et pour générer un second signal décalé (SS2) ;
un troisième étage de registre à décalage (VSR3, VSR_{3B}) adapté pour recevoir le second signal décalé (SS2) et pour générer un troisième signal décalé (SS3) ;

une première unité logique combinatoire (35, 64) adaptée pour la génération du premier signal de balayage (SD1) en fonction des premier (SS1), second (SS2) et troisième (SS3) signaux décalés ;
dans lequel ledit premier étage de registre à décalage (VSR1, VSR_{1B}), ledit second étage de registre à décalage (VSR2, VSR_{2B}) et ledit troisième étage de registre à décalage (VSR3, VSR_{3B}) forment un circuit de registre à décalage (33) ;
un plateau d'affichage (21) comportant le premier pixel générateur de lumière (3, 63) ;
un pilote d'électroluminescence (24) adapté à la génération du premier signal de démarrage (STV, STV_B); et
un pilote de données (22) adapté à la génération du premier signal de données (DS, DS_B), pour le premier pixel émetteur de lumière (31, 63);

dans lequel le second signal décalé (SS2) sert de premier signal de commande d'émission de lumière (XSD, XSD_{1B}) ; et
dans lequel la première unité logique combinatoire (35, 64) comporte :

une première unité logique (351) comprenant une première électrode d'entrée adaptée pour recevoir le premier signal décalé (SS1), une seconde électrode d'entrée adaptée pour recevoir le second signal décalé (SS2) et une première électrode de sortie ;
dans laquelle la première unité logique (351) est adaptée pour que la première électrode de sortie génère un premier niveau logique lorsque le niveau logique du premier signal décalé (SS1) est égal à celui du second signal décalé (SS2) et de telle manière que la première électrode de sortie génère un second niveau logique lorsque le niveau logique du premier signal décalé (SS1) diffère de celui du second signal décalé (SS2) ; et
une seconde unité logique (352) comprenant une troisième électrode d'entrée connecté à la première électrode de sortie, une quatrième électrode d'entrée étant adapté à la réception du troisième signal décalé (SS3), et une seconde électrode de sortie connectée au premier pixel émetteur de lumière (31, 63) pour la génération du premier signal de balayage (SD1) ;

dans lequel la seconde unité logique (352) est adaptée de manière à ce que la seconde électrode de sortie génère le premier niveau logique lorsqu'une ou les deux niveaux logique de la première électrode de sortie et le troisième signal décalé (SS3) est égal au premier niveau logique et de telle façon que la seconde électrode de sortie génère le second niveau logique lorsque le niveau logique de la première électrode de sortie et celui du troisième signal décalé (SS3) est égal au second niveau logique.

2. Le système tel que revendiqué dans la revendication 1, dans lequel le premier pixel émetteur de lumière (31), comporte un premier transistor (311), un second transistor (313, un troisième transistor (314), un élément générateur de lumière (315) et une capacité (312), dans lequel le premier transistor (311) est adapté à la transmission du premier signal de données (DS) à la grille du second transistor (313) en fonction du premier signal de balaye (SD1), dans lequel le second transistor (313), le troisième transistor (314) et l'élément générateur de lumière (315) sont connectés en série entre un premier niveau de tension (Vcc) et un second niveau (Vss), le troisième transistor (314) est commandé par le second signal décalé (SS2) et la capacité (312) est connectée entre la grille et la source du second transistor (313).

3. Le système tel que revendiqué dans la revendication 1 ou 2 dans lequel la seconde unité logique (352) comporte en outre une cinquième électrode d'entrée adapté à la réception d'un signal de commande (ENBV), dans lequel la seconde unité logique (352) est adaptée en outre à ce que la seconde électrode de sortie génère le premier niveau logique lorsqu'au moins un des niveaux logiques du signal de commande (ENBV), la première électrode de sortie ou le troisième signal décalé (SS3) sont égaux au premier niveau logique, et de telle manière que la seconde électrode de sortie génère le second niveau logique lorsque les niveaux logiques du signal de commande (ENBV), de la première électrode de sortie et du troisième signal décalé (SS3) sont égaux au second niveau logique.

4. Le système tel que revendiqué dans les revendications 1 ou 3, dans lequel le plateau d'affichage (21) comporte en outre un second pixel générateur de lumière (61) et un troisième pixel générateur de lumière (62) disposés sur ledit panneau d'affichage (21) et dans lequel le pilote de balayage (23) comporte en outre :

un quatrième étage de registre à décalage

(VSR_{1K}) adapté pour entrer un second signal de démarrage (STV_R) et pour générer un quatrième signal décalé ;
un cinquième étage de registre à décalage (VSR_{2R}) adapté pour entrer le quatrième signal de démarrage et pour générer un cinquième signal décalé en tant que second signal de commande d'émission de lumière (XSD_{1R}) ;
un sixième étage de registre à décalage (VSR_{1G}) adapté pour entrer le troisième signal de démarrage STV_G) et pour générer un sixième signal décalé ;
un septième étage de registre à décalage (VSR_{2G}) adapté pour entrer le sixième signal de démarrage STV_G) et pour générer un septième signal décalé pour être un troisième signal de commande d'émission de lumière (CSD_{1G}) ;
dans lequel le pilote de balayage est adapté à fournir le premier signal de balayage (SD1) au premier pixel générateur de lumière (63), le second pixel émetteur de lumière (61), et le troisième pixel émetteur de lumière (32) pour la commande du premier pixel émetteur de lumière (63), le second pixel émetteur de lumière (61) et le troisième pixel émetteur de lumière (62), respectivement, pour recevoir le premier signal de donnée (DSB), un second signal de données (DSR), et un troisième signal de données (DSG, respectivement et
est adapté à la commande de la durée d'émission de lumière du premier pixel émetteur de lumière (63), du second pixel émetteur de lumière, et du troisième pixel (62) émetteur de lumière, respectivement, en se servant du premier signal de commande d'émission de lumière (XSD_{1B}), du second signal de commande d'émission de lumière (XSD_{1R}) et du troisième signal de commande d'émission de lumière (XSD_{1G}), respectivement, en fonction du rapport cyclique du premier signal de démarrage (STV_B), du second signal de démarrage (STV_R), et du troisième signal de démarrage (STV_G), respectivement.

5. le système tel que revendiqué dans la revendication 4, dans lequel le premier pixel émetteur de lumière (63) est adapté à l'affichage d'une couleur bleue, le second pixel émetteur de lumière (61) est adapté à l'affichage d'une couleur rouge, et le troisième pixel émetteur de lumière (62) est adapté à l'affichage d'une couleur verte.

6. Le système tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel la première unité logique (351) est une porte XOR et la seconde unité logique (352) est une porte ET.

7. Le système tel que revendiqué dans la revendication 4 ou 5, dans lequel le pilote de données (22) est en outre adapté à générer le second signal de données (DS_R) vers le second pixel émetteur de lumière (61) et le troisième signal de données (DS_G) vers le troisième pixel émetteur de lumière (62).

8. Le système tel que revendiqué dans l'une quelconque des revendications précédentes, comprenant en outre :

un convertisseur numérique-analogique (DAC) adapté à l'alimentation électrique du dispositif d'affichage (20).

9. Le système tel que revendiqué dans l'une quelconque des revendications précédentes, comprenant en outre :

des moyens pour l'alimentation électrique du dispositif d'affichage (20).

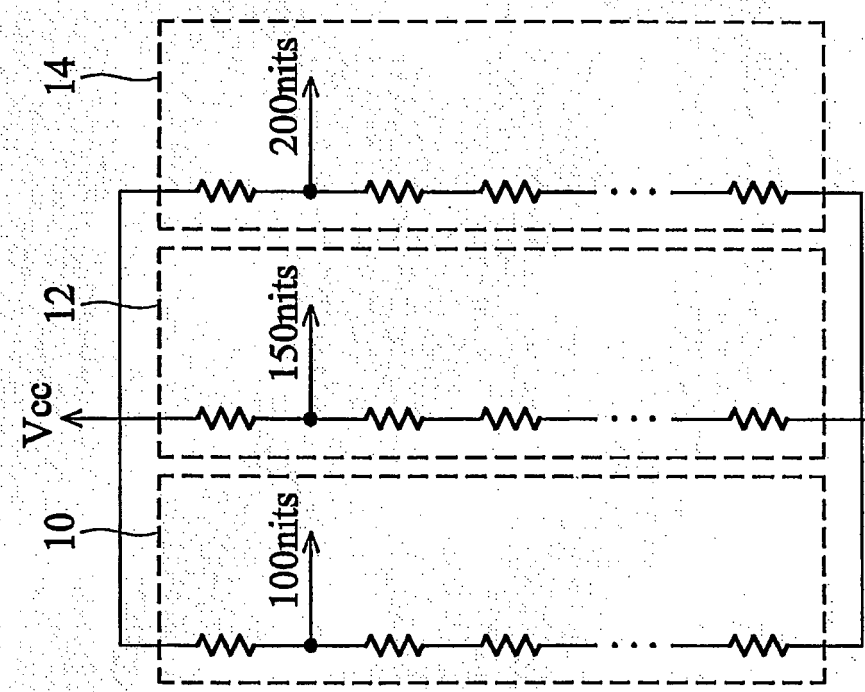


FIG. 1b (Related Art)

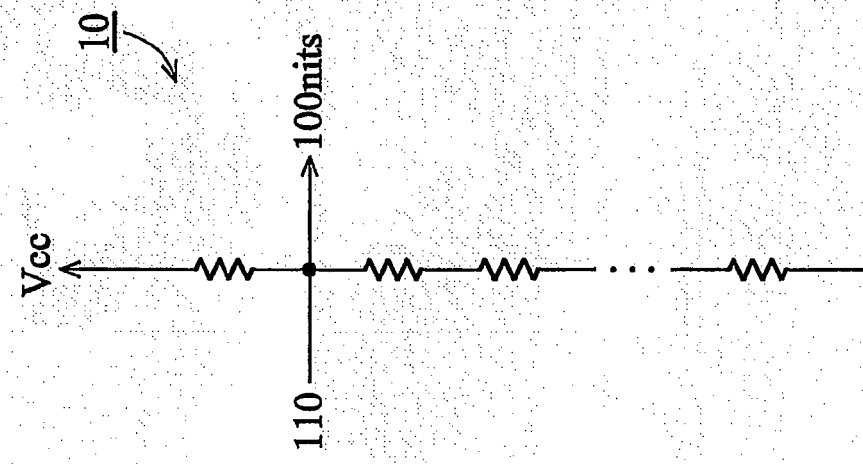


FIG. 1a (Related Art)

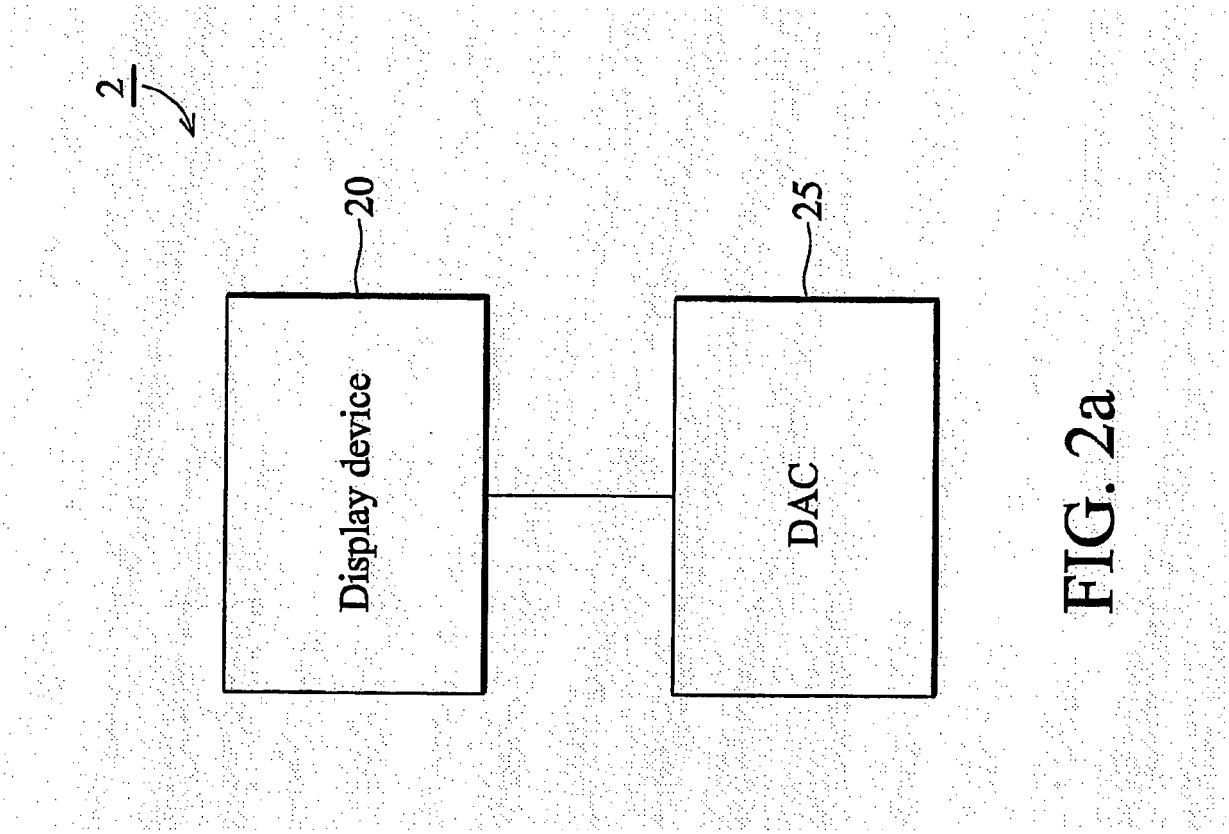


FIG. 2a

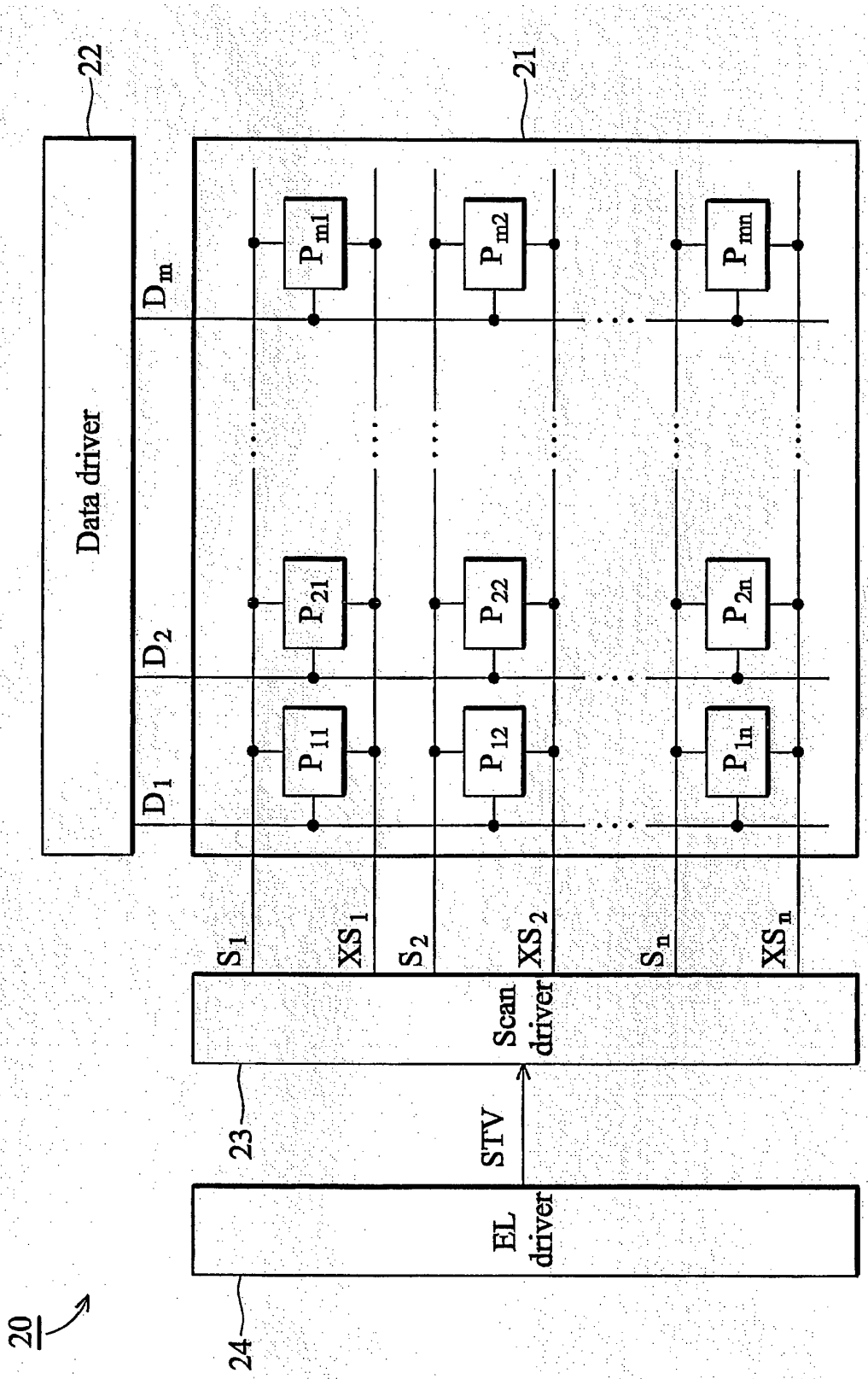
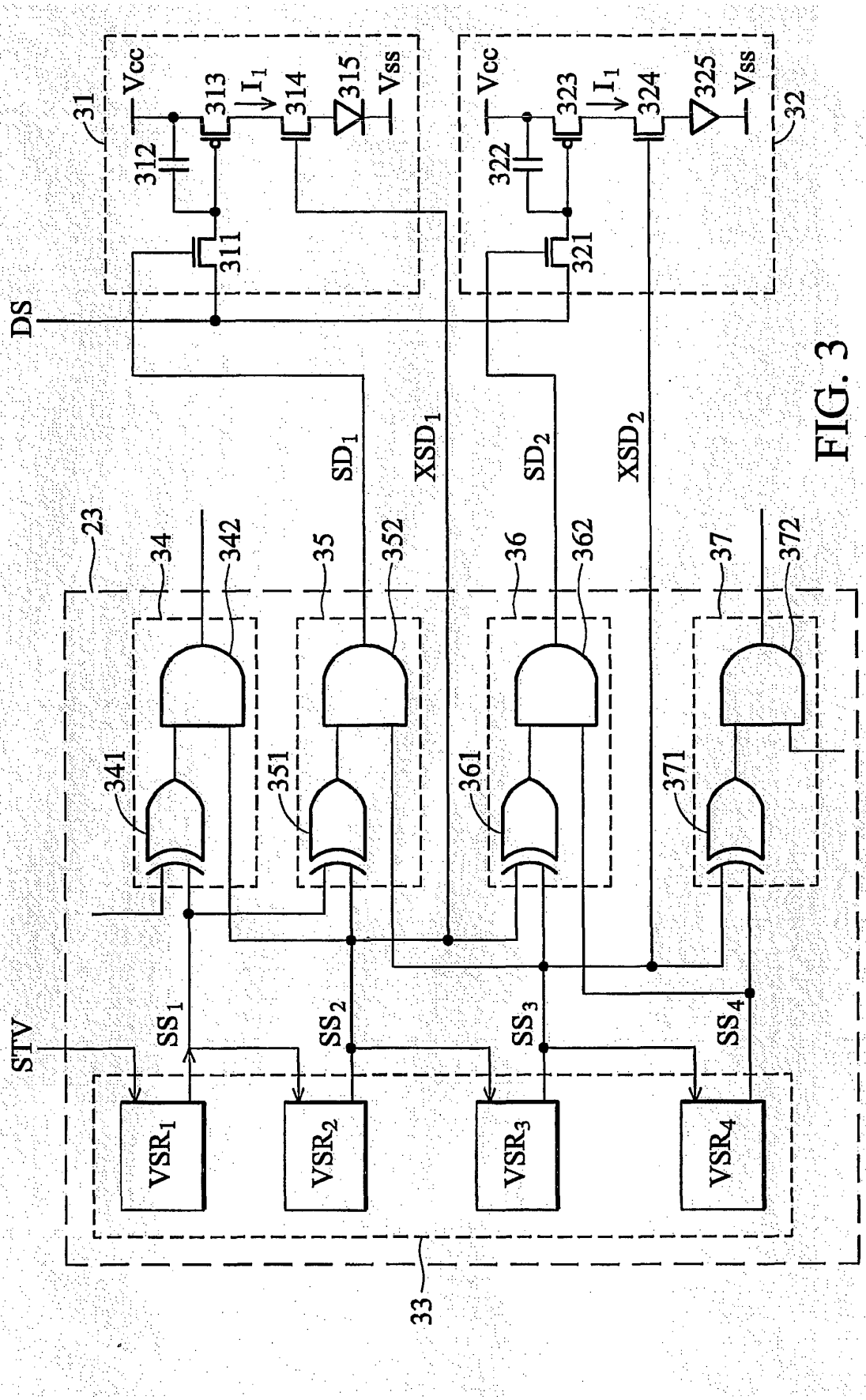

20
22
21
Data driver
D_m
D_2
D_1
P_{m1}
P_{m2}
P_{mn}
P_{21}
P_{22}
P_{2n}
P_{11}
P_{12}
P_{1n}
S_1
XS_1
S_2
XS_2
S_n
XS_n
Scan driver
23
STV
EL driver
24

FIG. 2b


Vcc
Vss
DS
STV
SD1
XSD1
SD2
XSD2
SS1
SS2
SS3
SS4
VSR1
VSR2
VSR3
VSR4
23
31
32
33
34
35
36
37
311
312
313
314
315
321
322
323
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341
342
351
352
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362
371
372

FIG. 3

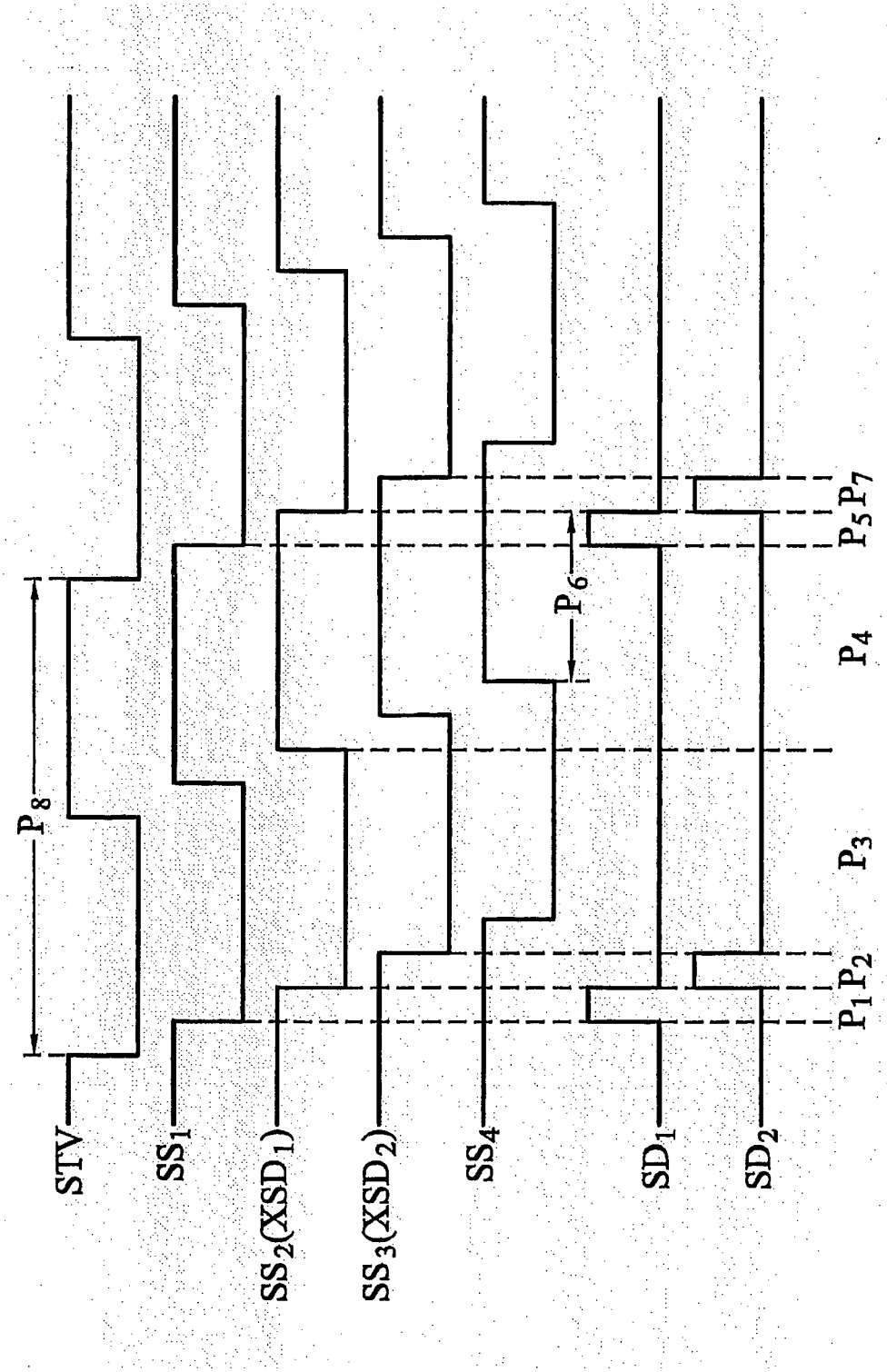

FIG. 4

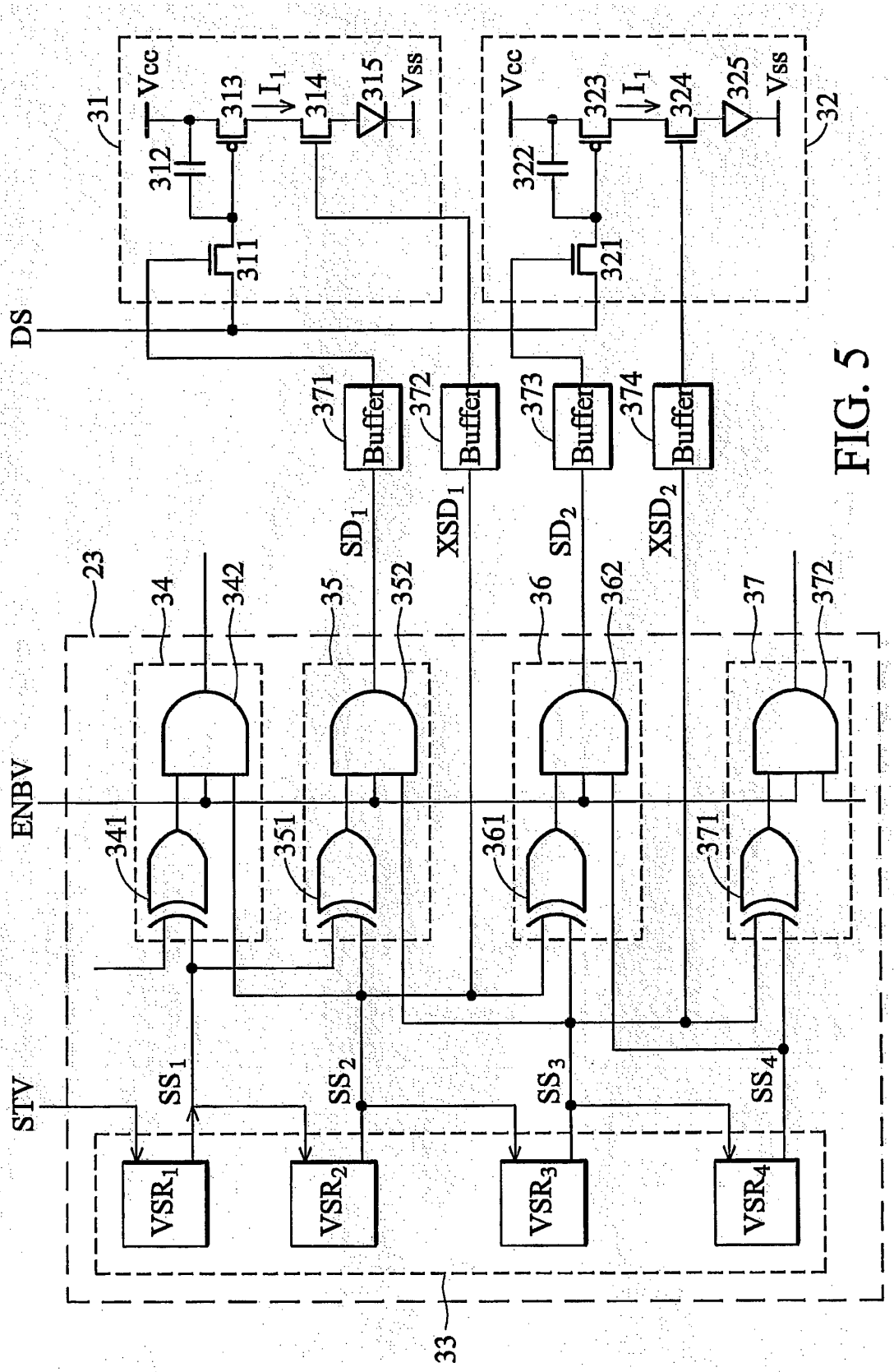
31
Vcc
313
I1
314
315
Vss
312
311
DS
32
323
324
325
322
321
371
372
373
374
Buffer
SD1
XSD1
SD2
XSD2
23
34
342
35
352
36
362
37
372
ENBV
341
351
361
371
STV
SS1
SS2
SS3
SS4
VSR1
VSR2
VSR3
VSR4
33

FIG. 5

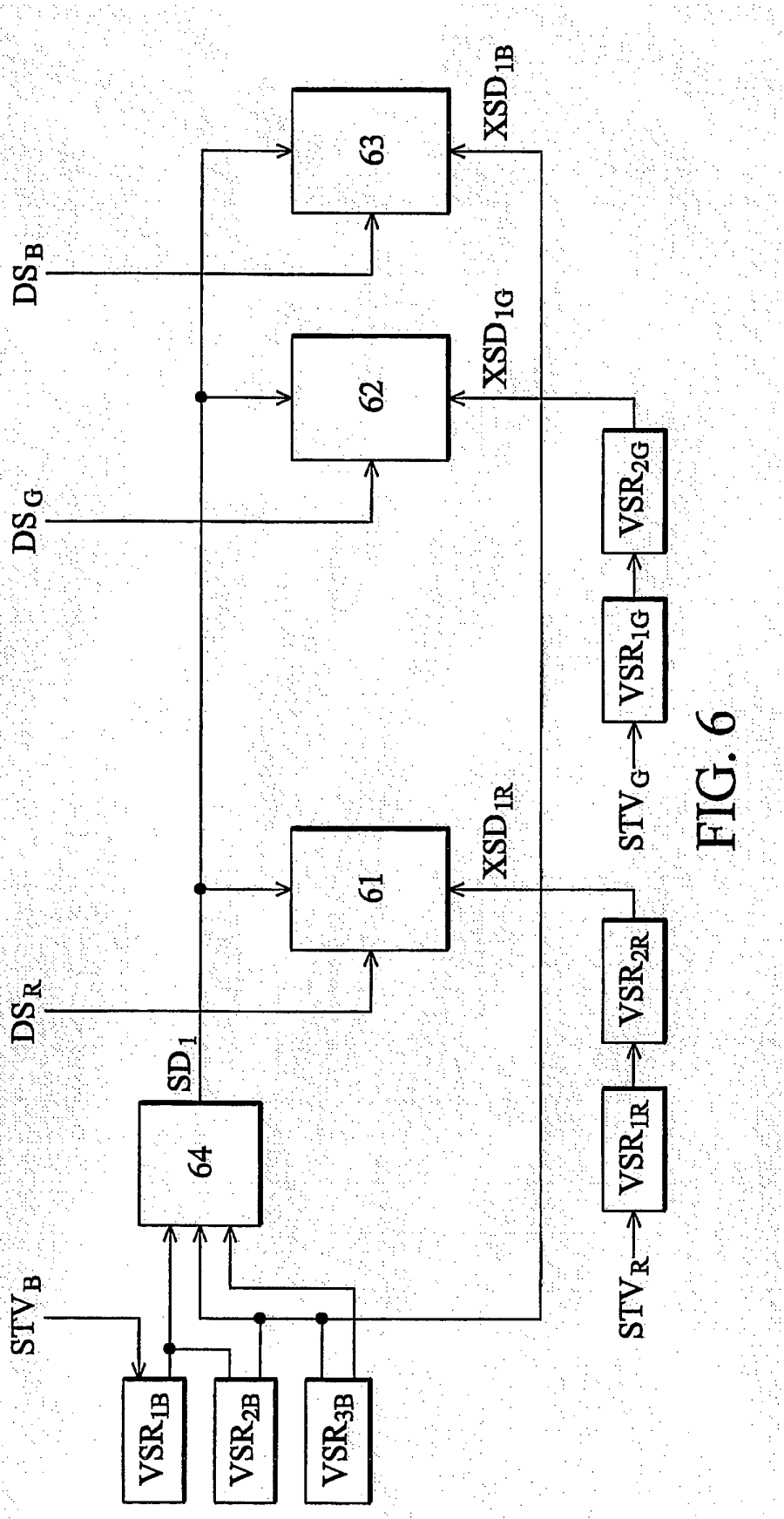
63
62
61
64
DS_B
DS_G
DS_R
SD_1
XSD_1B
XSD_1G
XSD_1R
STV_B
STV_G
STV_R
VSR_1B
VSR_2B
VSR_3B
VSR_1R
VSR_2R
VSR_1G
VSR_2G

FIG. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- WO 2005036515 A1 **[0008]**