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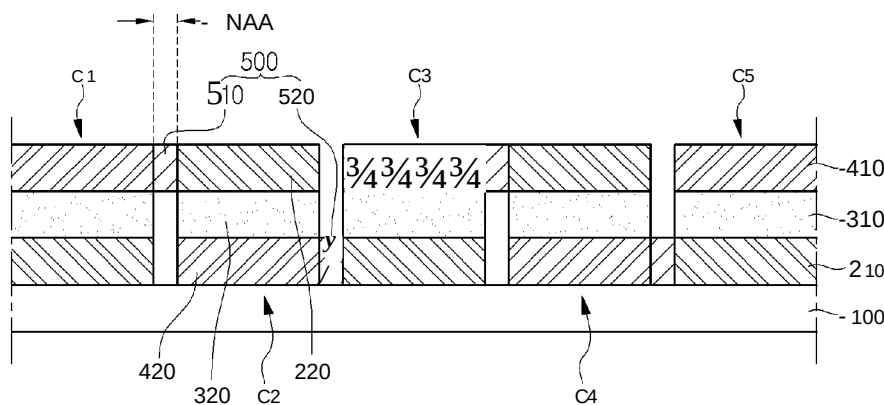
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(54) Title: SOLAR CELL MODULE AND METHOD OF FABRICATING THE SAME



(57) Abstract: Disclosed are a solar cell module and a method of fabricating the same. The solar cell module according to the embodiment includes first solar cells including a first P-type semiconductor layer, a first buffer layer, and a first N-type semiconductor layer sequentially disposed on a support substrate; second solar cells including a second N-type semiconductor layer, a second buffer layer, and a second N-type semiconductor layer sequentially disposed on the support substrate; and a connecting electrode connecting the first solar cells to the second solar cells.



WO 2013/085372 A1

Description

Title of Invention: SOLAR CELL MODULE AND METHOD OF FABRICATING THE SAME

Technical Field

- [1] The embodiment relates to a solar cell module and a method of fabricating the same.

Background Art

- [2] Solar cells may be defined as devices to convert light energy into electrical energy by using photovoltaic effect of generating electrons when light is incident onto a P-N junction diode. The solar cell may be classified into a silicon solar cell, a compound semiconductor solar cell mainly including a group I-III-VI compound or a group III-V compound, a dye-sensitized solar cell, and an organic solar cell according to materials constituting the junction diode.
- [3] A solar cell made from CIGS (CuInGaSe), which is one of group I-III-VI Chalcopyrite-based compound semiconductors, represents superior light absorption, higher photoelectric conversion efficiency with a thin thickness, and superior electro-optic stability, so the CIGS solar cell is spotlighted as a substitute for a conventional silicon solar cell.
- [4] Referring to FIG. 1, a CIGS thin film solar cell is generally fabricated by sequentially forming a support substrate 10 including sodium, a back electrode layer 20, a light absorbing layer 30, a buffer layer 40, a high-resistance buffer layer 50, and a front electrode layer 60.
- [5] Different from a bulk solar cell, the CIGS thin film solar cell includes a plurality of unit cells, which are connected with each other in series or parallel through patterning processes (P1 to P3). Gaps G1 and G2 are formed while the P1 process and the P3 process are being performed, so that a non-active area (NAA), which is not contributed to the photoelectric output of the solar cell module, is generated. The non-active area (NAA) leads to a power loss in the range of about 5% to about 10% based on the whole output power of the solar cell module.

Disclosure of Invention

Technical Problem

- [6] The embodiment provides a solar cell module which includes a connecting structure to minimize a non-active area (NAA), and a method for fabricating the same.

Solution to Problem

- [7] According to the embodiment, there is provided a solar cell module including first solar cells including a first P-type semiconductor layer, a first buffer layer, and a first N-type semiconductor layer sequentially disposed on a support substrate; second solar

cells including a second N-type semiconductor layer, a second buffer layer, and a second N-type semiconductor layer sequentially disposed on the support substrate; and a connecting electrode connecting the first solar cells to the second solar cells.

- [8] A method of fabricating a solar cell module according to the embodiment includes: forming first solar cells spaced apart from each other by a predetermined distance on a first support substrate; forming second solar cells spaced apart from each other by a predetermined distance on a second support substrate; coating one side surfaces of the first solar cells and opposite side surfaces of the second solar cells with a connecting electrode forming material, respectively; interposing the second solar cells between the first solar cells spaced apart from each other by the predetermined distance; and baking the connecting electrode forming material to form a connecting electrode.

Advantageous Effects of Invention

- [9] The solar cell module according to the embodiment has a structure in which the solar cells are repeatedly disposed in the longitudinal direction. The structure may allow the non-active area to be minimized, so that the loss of the output power of the solar cell module may be reduced from the range of 5 % to 10 % to the range of 0.5 % to 2.0 %. Thus, the photoelectric output of the solar cell module according to the embodiment may be improved.
- [10] In addition, since the solar cell module has a structure in which an electron-transfer path may be minimized, the series resistance is reduced and the short current is increased, so that the photoelectric output is increased.

Brief Description of Drawings

- [11] FIG. 1 is a sectional view showing a solar cell module according to the related art;
- [12] FIG. 2 is a sectional view showing a solar cell module according to the embodiment;
- [13] FIG. 3 is a sectional view illustrating electron transfer of the solar cell module according to the embodiment; and
- [14] FIGS. 4 to 8 are sectional views illustrating a method of fabricating the solar cell module according to the embodiment.

Mode for the Invention

- [15] In the description of the embodiments, it will be understood that, when a substrate, a layer, a film, or an electrode is referred to as being "on" or "under" another substrate, another layer, another film, or another electrode, it can be "directly" or "indirectly" on the other substrate, the other layer, the other film, or the other electrode, or one or more intervening layers may also be present. Such a position of each component has been described with reference to the drawings. The thickness and size of each component shown in the drawings may be exaggerated, omitted or schematically drawn for the purpose of convenience or clarity. In addition, the size of elements does not utterly

reflect an actual size.

- [16] FIG. 2 is a sectional view showing the solar cell module according to the embodiment. Referring to FIG. 2, the solar cell module according to the embodiment includes first solar cells C1, C3 and C5, second solar cells C2 and C4, and a connecting electrode 500 which connects the first solar cells C1, C3 and C5 to the second solar cells C2 and C4.
- [17] The first solar cells C1, C3 and C5 are spaced apart from each other by a predetermined distance. Further, the second solar cells C2 and C4 are interposed between the first solar cells C1, C3 and C5 spaced apart from each other by the predetermined distance. If the second solar cells C2 and C4 may be interposed between the first solar cells C1, C3 and C5, the distance between the first solar cells C1, C3 and C5 is not limited numerically.
- [18] The first solar cells C1, C3 and C5 and the second solar cells C2 and C4 have a reverse phase structure. In more detail, the first solar cells C1, C3 and C5 include a first P-type semiconductor layer 210, a first buffer layer 310 and a first N-type semiconductor layer 410 which are sequentially disposed on a support layer 100. Further, the second solar cells C2 and C4 include a second N-type semiconductor layer 410, a second buffer layer 320 and a second P-type semiconductor layer 220 which are sequentially disposed on the support layer 100.
- [19] Further, the first solar cells C1, C3 and C5 and the second solar cells C2 and C4 are electrically connected through a connecting electrode 500. In detail, the connecting electrode 500 includes a first connecting electrode 510 and a second electrode 520. The first and second connecting electrodes 510 and 520 may face each other in the longitudinal direction. In detail, the first and second connecting electrodes 510 and 520 may diagonally face each other in the longitudinal direction. That is, the first connecting electrode 510 is directly disposed on a top surface of the support substrate 100, and the second connecting electrode 520 is disposed not to make contact with the support substrate 100.
- [20] The first connecting electrode 510 makes direct contact with one side surface of the first N-type semiconductor layer 410 of the cell C1 and an opposite side surface of the second P-type semiconductor layer 220 of the cell C2 adjacent to the cell C1. Thus, the first N-type semiconductor layer 410 of the cell C1 is electrically connected to the second P-type semiconductor layer 220 of the cell C2 adjacent to the cell C1 through the first connecting electrode 510.
- [21] Further, the second connecting electrode 520 makes direct contact with one side surface of the second N-type semiconductor layer 420 of the cell C2 and an opposite side of the first P-type semiconductor layer 210 of the C3 adjacent to the cell C2. Thus, the second N-type semiconductor layer 420 of the cell C2 is electrically connected to

the first P-type semiconductor layer 210 of the cell C3 adjacent to the cell C2 through the second connecting electrode 520.

[22] Referring to FIG. 2, the solar cell module include a non-active area (NAA) formed only in an area in which the connecting electrode 500. That is, the gaps G1 and G2, which are formed through the patterning process for fabricating a solar cell module according to the related art, are minimized, so that the loss of the photoelectric output of the solar cell module may be reduced from the previous range of about 5 % to about 10 % to the range of about 0.5 % to about 2.0 %. Thus, the photoelectric output of the solar cell module according to the embodiment may be improved. Further, referring to FIG. 3, Different from the solar cell module according to the related art, the solar cell module according to the embodiment may allow electron-transfer path to be minimized. Thus, the series resistance of the solar cell module according to the embodiment may be reduced and the short current is increased, so that the photoelectric output may be increased.

[23] The support substrate 100 has a plate shape and supports the first solar cells C1, C3 and C5 and the second solar cells C2 and C4. The support substrate 100 may include an insulator. The support substrate 100 may include a glass substrate, a plastic substrate, or a metallic substrate. In more detail, the support substrate 100 may include a soda lime glass substrate. The support substrate 100 may be transparent. The support substrate 100 may be rigid or flexible.

[24] The first and second P-type semiconductor layers 210 and 220 are light absorbing layers from which electron-hole pairs are generated by the solar light incident into the solar cell module. Each of the first and second P-type semiconductor layers 210 and 220 includes group I-III-VI-based compound. For example, each of the first and second P-type semiconductor layers 210 and 220 may have the CIGSS ($\text{Cu}(\text{In,Ga})(\text{Se,S})_2$) crystal structure, the CISS ($\text{Cu}(\text{In})(\text{Se,S})_2$) crystal structure or the CGSS ($\text{Cu}(\text{Ga})(\text{Se,S})_2$) crystal structure.

[25] Each of the first and second N-type semiconductor layers 410 and 420 may include zinc oxide, ITO (indium tin oxide) or IZO (indium zinc oxide). In more detail, each of the first and second N-type semiconductor layers 410 and 420 may be prepared with AZO (Al doped zinc oxide).

[26] The first and second N-type semiconductor layers 410 and 420 have the characteristics of an N-type semiconductor. That is, the first and second N-type semiconductor layers 410 and 420 may form N-type semiconductor layers and may form PN junctions with the first and second P-type semiconductors 210 and 220, respectively.

[27] The first buffer layer 310 is disposed between the first P-type semiconductor 210 and the first N-type semiconductor layer 410. In addition, the second buffer layer 320 is

disposed between the second P-type semiconductor layer 220 and the second N-type semiconductor layer 420. Since the P-type semiconductor layers 210 and 220 and the N-type semiconductor layers 410 and 420 represent the great difference in the lattice constant and the bandgap energy therebetween, a buffer layer having the intermediate bandgap between the bandgaps of the two materials is required to form the superior junction between the two materials.

[28] Each of the first and second buffer layers 310 and 320 may include CdS, ZnS, InXSY and InXSeYZn(O,OH), but the embodiment is not limited to them.

[29] Meanwhile, although not depicted in the drawings, the high-resistance buffer layer (not shown) may be additionally formed on the first and second buffer layers 310 and 320, but the embodiment is not limited thereto. The high-resistance buffer layer may include i-ZnO, which is zinc oxide not doped with impurities.

[30] The connecting electrode 500 is a conductive layer. The back electrode layer 200 may include at least one of molybdenum (Mo), gold (Au), aluminum (Al), chrome (Cr), tungsten (W), and copper (Cu).

[31] FIGS. 4 to 8 are sectional views illustrating the method of fabricating a solar cell module according to the embodiment. The description about the fabricating method may be essentially incorporated with the above description about the solar cell module.

[32] Referring to FIG. 4, the first solar cells C1, C3 and C5 are formed on the first support substrate 100. First, the first P-type semiconductor layer 210 is formed on the first support substrate 100. The first P-type semiconductor layer 210 may be formed through the sputtering process or the evaporation scheme. For example, the first P-type semiconductor layer 210 may be formed through various schemes such as a scheme of forming a Cu(In,Ga)Se₂ (CIGS) based the first P-type semiconductor layer 210 by simultaneously or separately evaporating Cu, In, Ga, and Se and a scheme of performing a selenization process after a metal precursor layer has been formed.

[33] Regarding the details of the selenization process after the formation of the metallic precursor layer, the metallic precursor layer is formed on the back electrode layer 200 through a sputtering process employing a Cu target, an In target, a Ga target or an alloy target. Thereafter, the metallic precursor layer is subject to the selenization process so that the first P-type semiconductor layer 210 based on Cu (In, Ga) Se₂ (CIGS) is formed.

[34] In addition, the sputtering process employing the Cu target, the In target, and the Ga target and the selenization process may be simultaneously performed.

[35] Further, the first P-type semiconductor layer 210 based on a CIS or CIG may be formed through the sputtering process employing only Cu and In targets or only Cu and Ga targets and the selenization process.

[36] Then, the first buffer layer 310 is deposited on the first P-type semiconductor layer

210. The first buffer layer 310 may be formed through ALD (atomic layer deposition), MOCVD (Metal-Organic Chemical Vapor Deposition) or CBD (chemical bath deposition). In more detail, the first buffer layer 310 may be formed through CBD.

[37] Last, the first N-type semiconductor layer 410 is formed on the first buffer layer 310. The first N-type semiconductor layer 410 may be prepared by laminating a transparent conductive material on the first buffer layer 310. In more detail, the first N-type semiconductor layer 410 may be prepared through the sputtering process or CVD (chemical vapor deposition). In addition, in order to form the first N-type semiconductor layer 410 through the sputtering process, an RF sputtering scheme employing a ZnO target or a reactive sputtering scheme employing a Zn target may be utilized.

[38] Thereafter, the plurality of first solar cells C1, C3 and C5 are separated from each other by patterning the first P-type semiconductor layer 210, the first buffer layer 310 and the first N-type semiconductor layer 410. The patterning process may be performed through a mechanical process or a laser process. For example, the patterning process may be performed by mechanically scribing the layers 210, 310 and 410 using a scribing tip or irradiating laser onto the layers 210, 310 and 410.

[39] Referring to FIG. 5, the second solar cells C2 and C4 are formed on the second support substrate 110. In more detail, the second solar cells C2 and C4 may be prepared by sequentially laminating the second P-type semiconductor layer 220, the second buffer layer 320, the second N-type semiconductor layer 420 on the second support substrate 110. The description about the preparation of the second solar cells C2 and C4 may include all details described above about the preparation of the first solar cells C1, C3 and C5, and will be omitted for convenience to avoid duplicated description thereof.

[40] Referring to FIGS. 6 and 7, a material for forming the connecting electrodes is coated on side surfaces of the first and second P-type semiconductor layers 210 and 220, respectively. Referring to FIG. 8, the second solar cells C2 and C4 are interposed among the first solar cells C1, C3 and C5. At this time, the second support substrate 110, on which the second solar cells C2 and C4 are formed, is turned over to allow the first solar cells C1, C3 and C5 to correspond to the second solar cells C2 and C4. Thus, the layers constituting the first solar cells C1, C3 and C5 and the layers constituting the second solar cells C2 and C4 are disposed in the reverse order.

[41] Thereafter, the process of fabricating the solar cell module may be completed by heat treating the connecting electrode forming material 500. The heat-treating process may include a typical sintering process for fabricating an electrode of a solar cell.

[42] Any reference in this specification to "one embodiment," "an embodiment," "example embodiment," etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of

the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to effect such feature, structure, or characteristic in connection with other ones of the embodiments.

[43] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

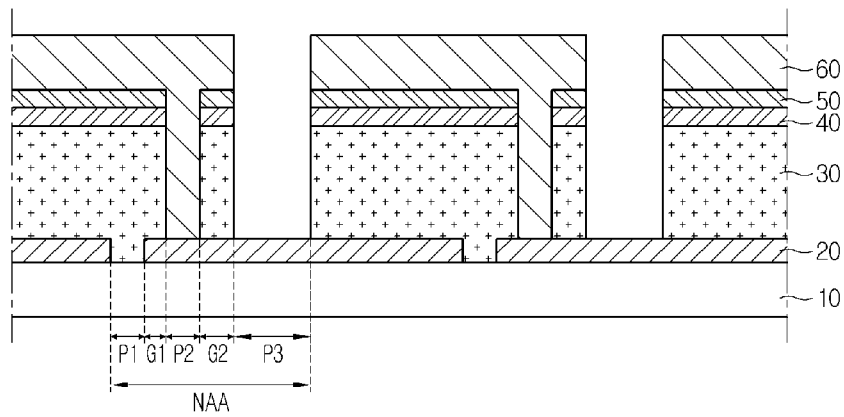
Claims

- [Claim 1] A solar cell module comprising:
first solar cells including a first P-type semiconductor layer, a first buffer layer, and a first N-type semiconductor layer sequentially disposed on a support substrate;
second solar cells including a second N-type semiconductor layer, a second buffer layer, and a second N-type semiconductor layer sequentially disposed on the support substrate; and
a connecting electrode connecting the first solar cells to the second solar cells.
- [Claim 2] The solar cell module of claim 1, wherein the first solar cells are spaced apart from each other by a predetermined distance and the second solar cells are disposed between the first solar cells spaced apart from each other by the predetermined distance.
- [Claim 3] The solar cell module of claim 1, wherein the connecting electrode includes a first connecting electrode and a second electrode facing the first connecting electrode.
- [Claim 4] The solar cell module of claim 3, wherein the first connecting electrode is disposed on a top surface of the support substrate.
- [Claim 5] The solar cell module of claim 3, wherein the first connecting electrode connects the first N-type semiconductor layer of the first solar cell to the second P-type semiconductor layer of the second solar cell.
- [Claim 6] The solar cell module of claim 3, wherein the first connecting electrode makes direct contact with one side surface of the first N-type semiconductor layer and an opposite side surface of the second P-type semiconductor layer.
- [Claim 7] The solar cell module of claim 3, wherein the second connecting electrode connects the first P-type semiconductor layer of the first solar cell to the second N-type semiconductor layer of the second solar cell.
- [Claim 8] The solar cell module of claim 3, wherein the second connecting electrode makes direct contact with one side surface of the first P-type semiconductor layer and an opposite side surface of the second N-type semiconductor layer.
- [Claim 9] The solar cell module of claim 1, wherein each of the first P-type semiconductor layer and the second P-type semiconductor layer includes a group I-III-VI compound.
- [Claim 10] The solar cell module of claim 9, wherein the group I-III-VI compound

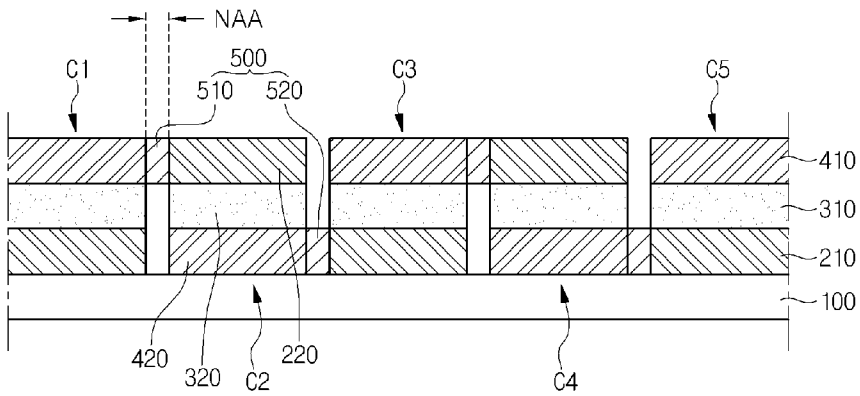
includes CISS ($\text{Cu}(\text{IN})(\text{Se},\text{S})_2$) compound or CIGSS ($\text{Cu}(\text{IN},\text{Ga})(\text{Se},\text{S})_2$) compound.

- [Claim 11] The solar cell module of claim 1, wherein each of the first and second buffer layers includes CdS.
- [Claim 12] The solar cell module of claim 1, wherein each of the first and second N-type semiconductor layers includes boron doped zinc oxide (ZnO:B , BZO), aluminum doped zinc oxide (AZO) or gallium doped zinc oxide (GZO).
- [Claim 13] A method of fabricating a solar cell module, the method comprising:
forming first solar cells spaced apart from each other by a predetermined distance on a first support substrate;
forming second solar cells spaced apart from each other by a predetermined distance on a second support substrate;
coating one side surfaces of the first solar cells and opposite side surfaces of the second solar cells with a connecting electrode forming material, respectively;
interposing the second solar cells between the first solar cells spaced apart from each other by the predetermined distance; and
baking the connecting electrode forming material to form a connecting electrode.
- [Claim 14] The method of claim 13, wherein the forming of the first solar cells includes:
sequentially forming a first P-type semiconductor layer, a first buffer layer, and a first N-type semiconductor layer on the first support substrate.
- [Claim 15] The method of claim 14, wherein the connecting electrode forming material is coated on one side of the first P-type semiconductor layer.
- [Claim 16] The method of claim 13, wherein the forming of the second solar cells includes:
sequentially forming a second P-type semiconductor layer, a second buffer layer, and a second N-type semiconductor layer on the second support substrate.
- [Claim 17] The method of claim 16, wherein the connecting electrode forming material is coated on one side of the second P-type semiconductor layer.

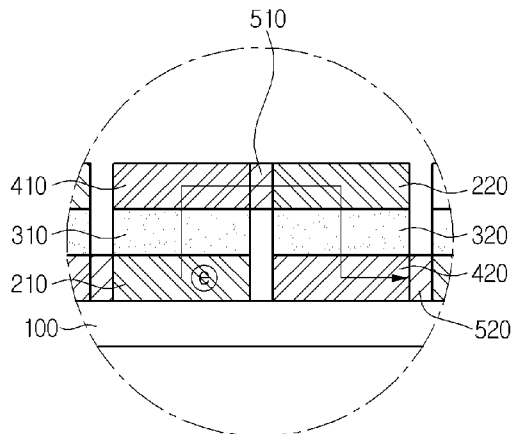
[Fig. 1]



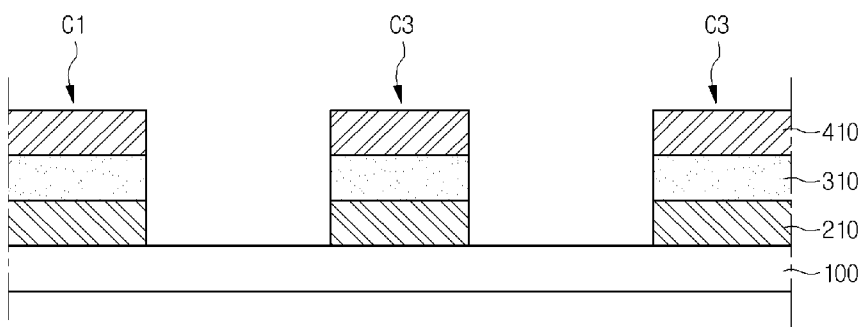
[Fig. 2]



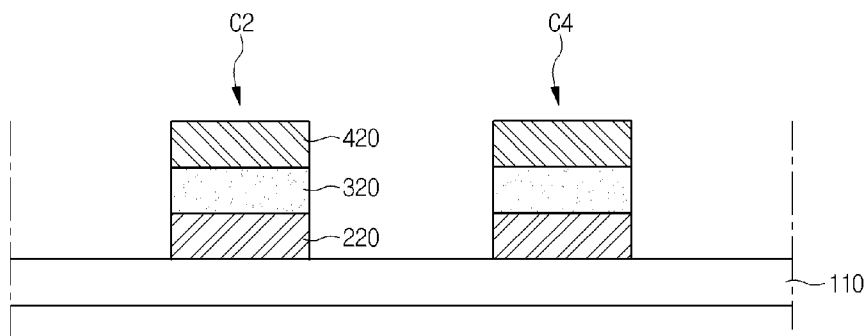
[Fig. 3]



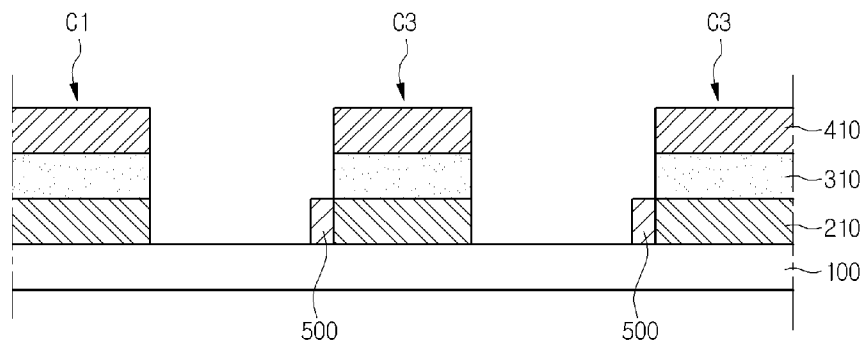
[Fig. 4]



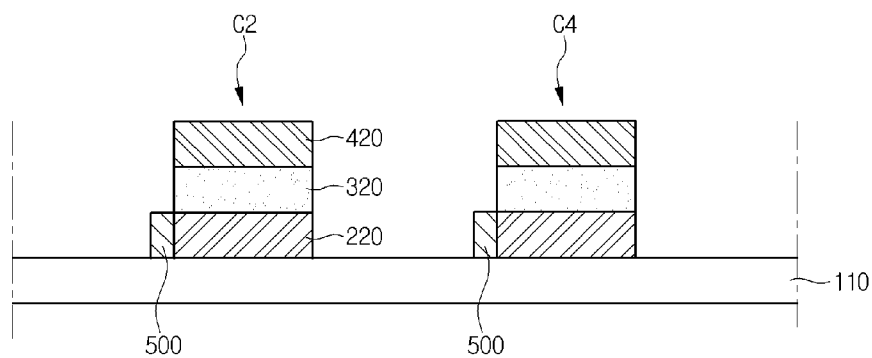
[Fig. 5]



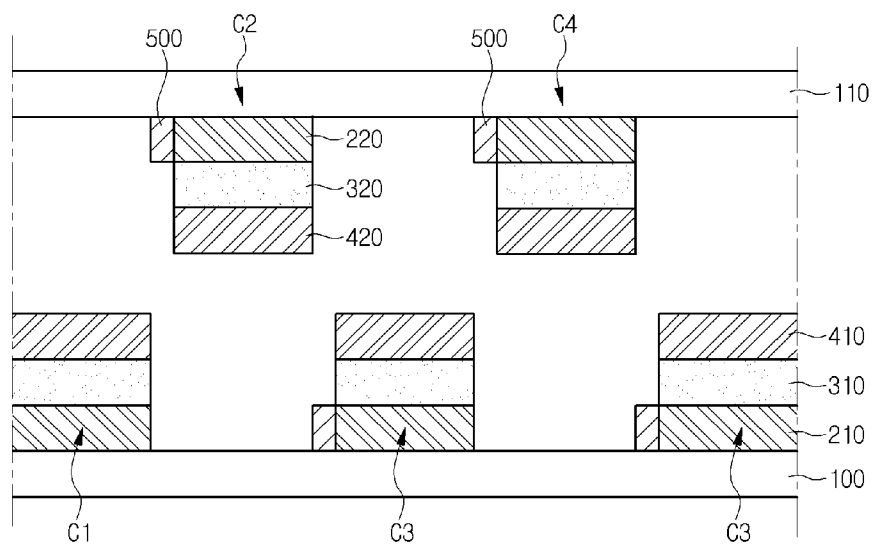
[Fig. 6]



[Fig. 7]



[Fig. 8]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR2012/010719

A. CLASSIFICATION OF SUBJECT MATTER**HOIL 31/06(2006.01)i, HOIL 31/042(2006.01)1, HOIL 31/18(2006.01)1**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 31/06; HOIL 31/042

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: 태양*,solar*,photo*,connect*,p-type,n-type,buffer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2011-0100725 A (Jusung Engineering co.,ltd.) 15 September 2011 See abstract , claims , paragraphs 64-72 , and figure 3b.	1-17
A	KR 10-2009-0093192 A (TG solar corporation) 02 September 2009 See abstract , claims , paragraphs 46-48 , and figure 1i.	1-17
A	KR 10-2011-0035510 A (TG solar corporation) 06 April 2011 See abstract , claims , paragraph 39,49, and figure 7.	1-17
A	KR 10-2009-0122728 A (Samsung Electronics co.,ltd.) 01 December 2009 See abstract , claims , paragraphs 16,17 and figure 2.	1-17

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

18 MARCH 2013 (18.03.2013)

Date of mailing of the international search report

19 MARCH 2013 (19.03.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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