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(54) **FREQUENCY JITTERING CONTROL CIRCUIT AND METHOD FOR A PFM POWER SUPPLY**

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(52) **U.S. Cl.**

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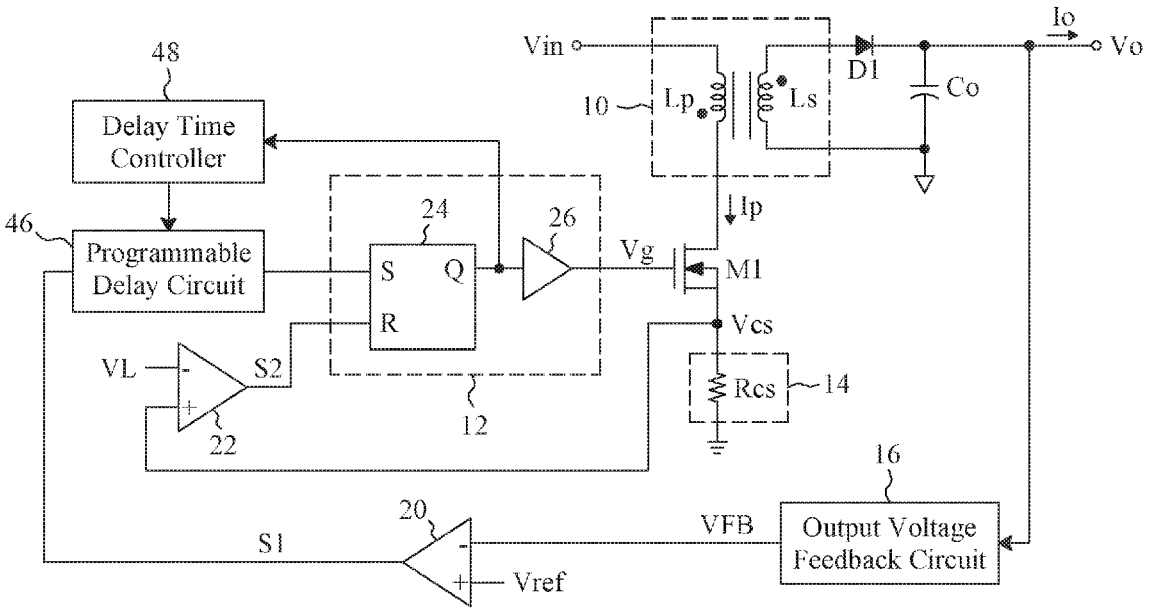
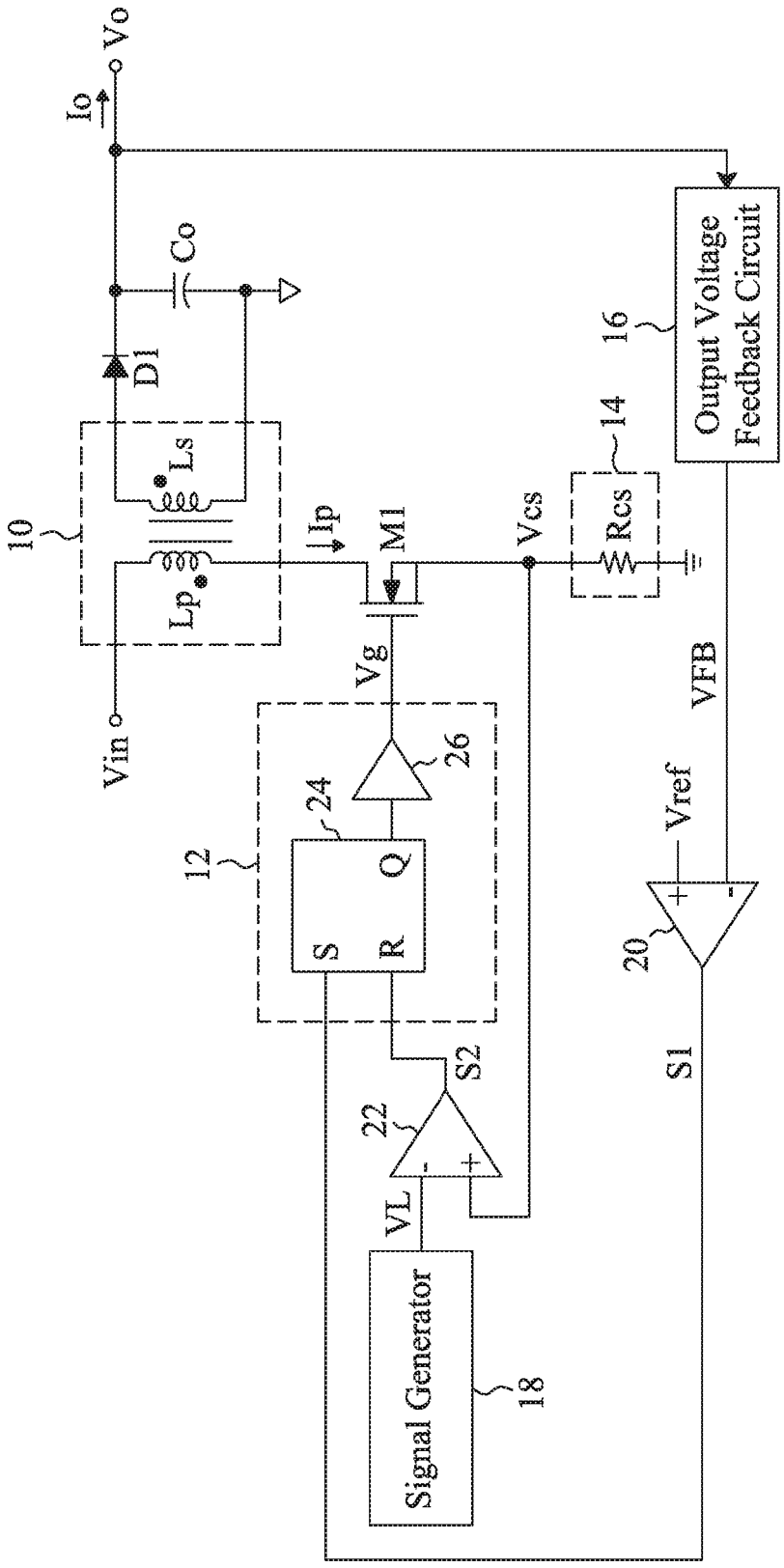
(57) **ABSTRACT**

A frequency jittering control circuit for a PFM power supply includes a pulse frequency modulator to generate a frequency jittering control signal to switch a power switch to generate an output voltage. The frequency jittering control circuit jitters an input signal or an on-time or off-time of the pulse frequency modulator to jitter the switching frequency of the power switch to thereby improve EMI issue.




Vo
Io
Co
D1
Ls
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10
Ip
M1
Vcs
Rcs
14
16
Output Voltage Feedback Circuit
Vin
Vg
26
24
12
S
R
Q
VFB
Vref
20
S1
S2
22
VL
Signal Generator
18

Fig. 1

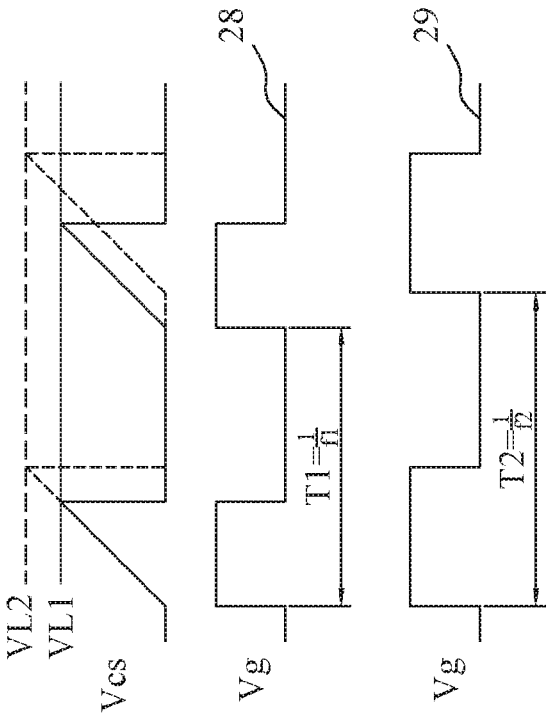


Fig. 2

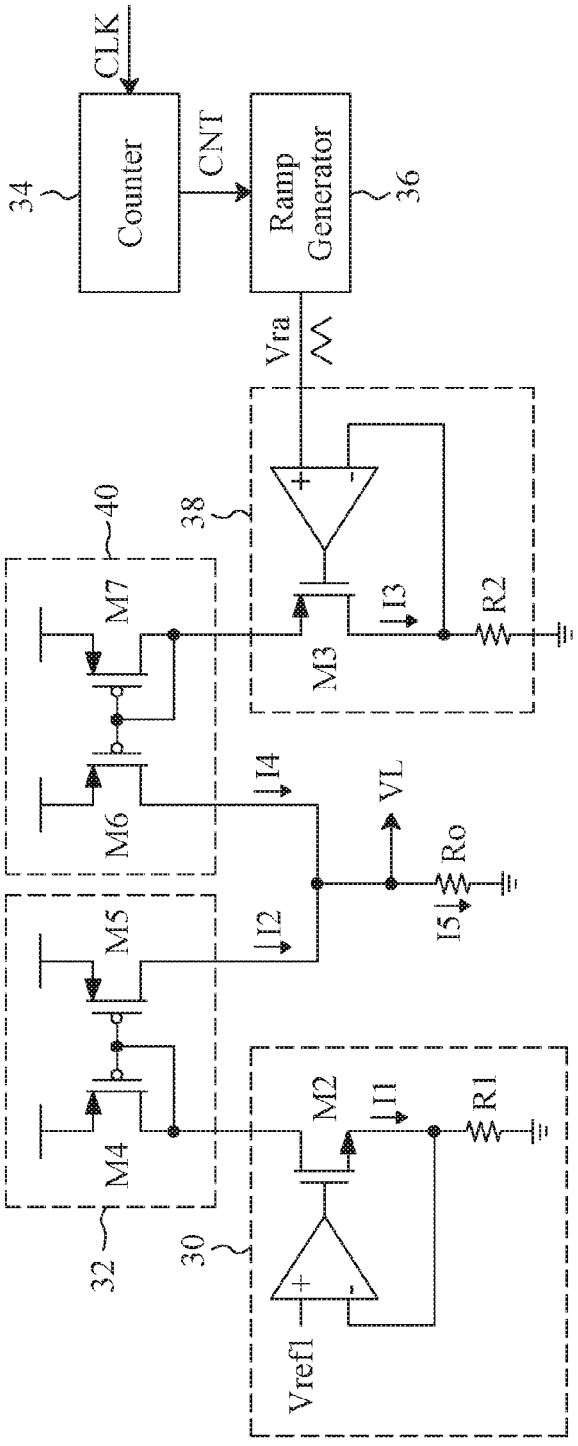

CLK
34
Counter
CNT
Ramp Generator
36
Vra
38
40
M7
M6
M5
M4
M3
M2
I1
I2
I3
I4
I5
R1
R2
Ro
VL
32
30
Vref1

Fig. 3

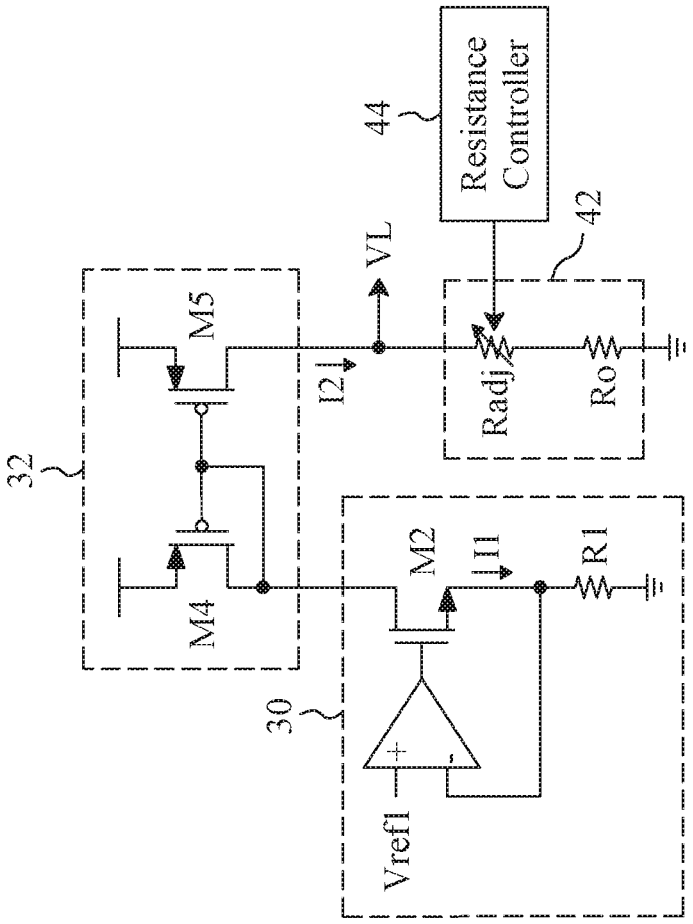
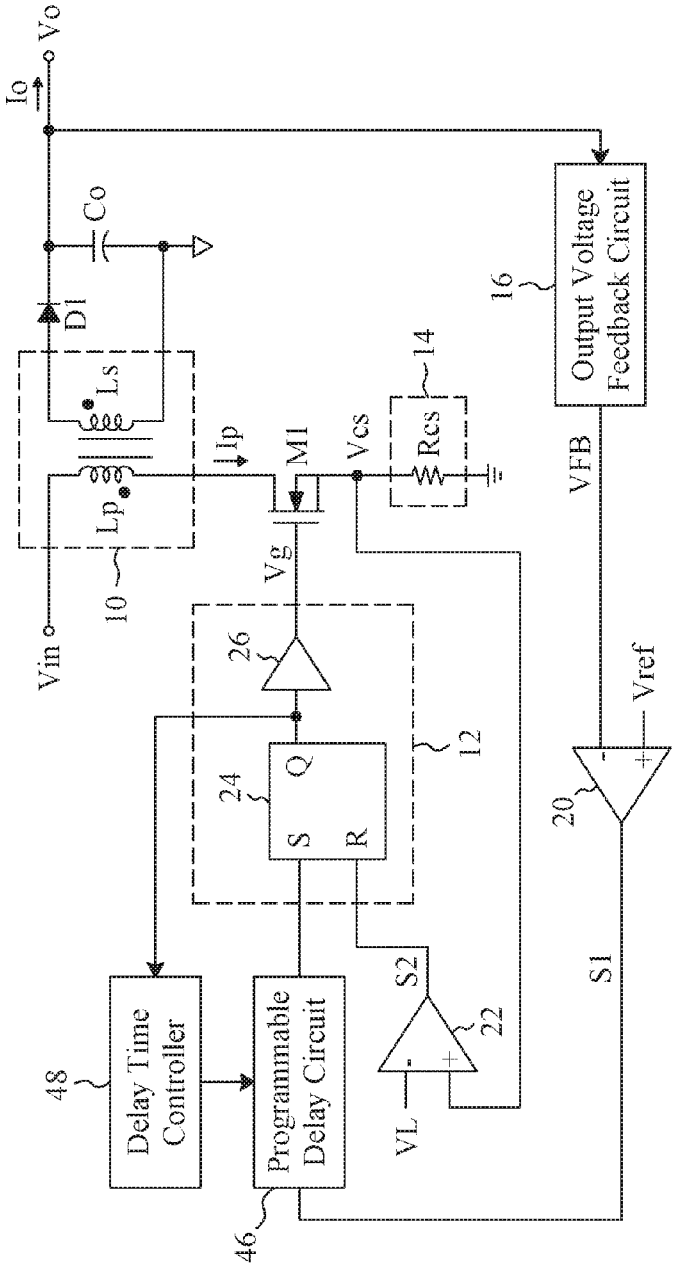

Resistance Controller
44
42
VL
M5
I2
Radj
Ro
32
M2
I1
R1
M4
30
Vref1

Fig. 4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Co
D1
Ls
Lp
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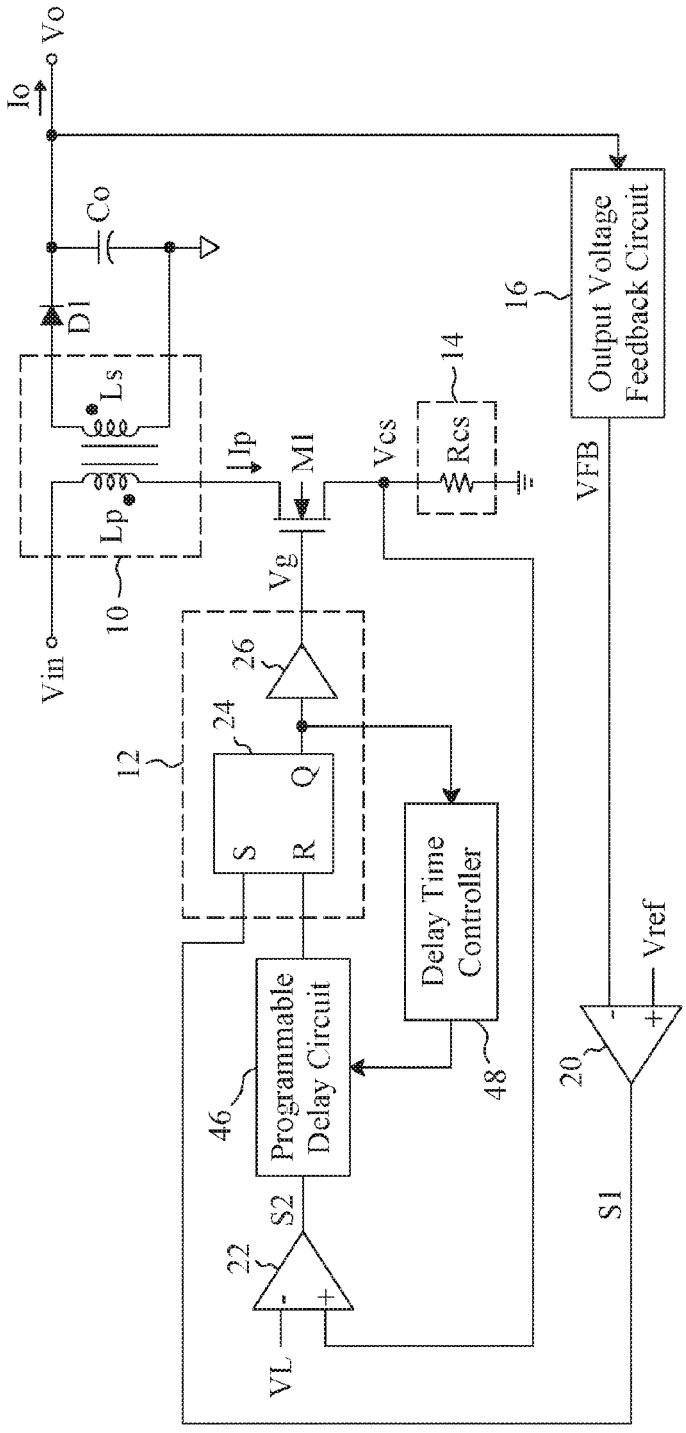
Vin
Ip
M1
Vcs
Rcs
14
16
Output Voltage Feedback Circuit
VFB
Vg
26
24
Q
S
R
12
20
Vref
S1
S2
22
VL
48
Delay Time Controller
Programmable Delay Circuit
46

Fig. 5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Output Voltage Feedback Circuit
VFB
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10
Vin
26
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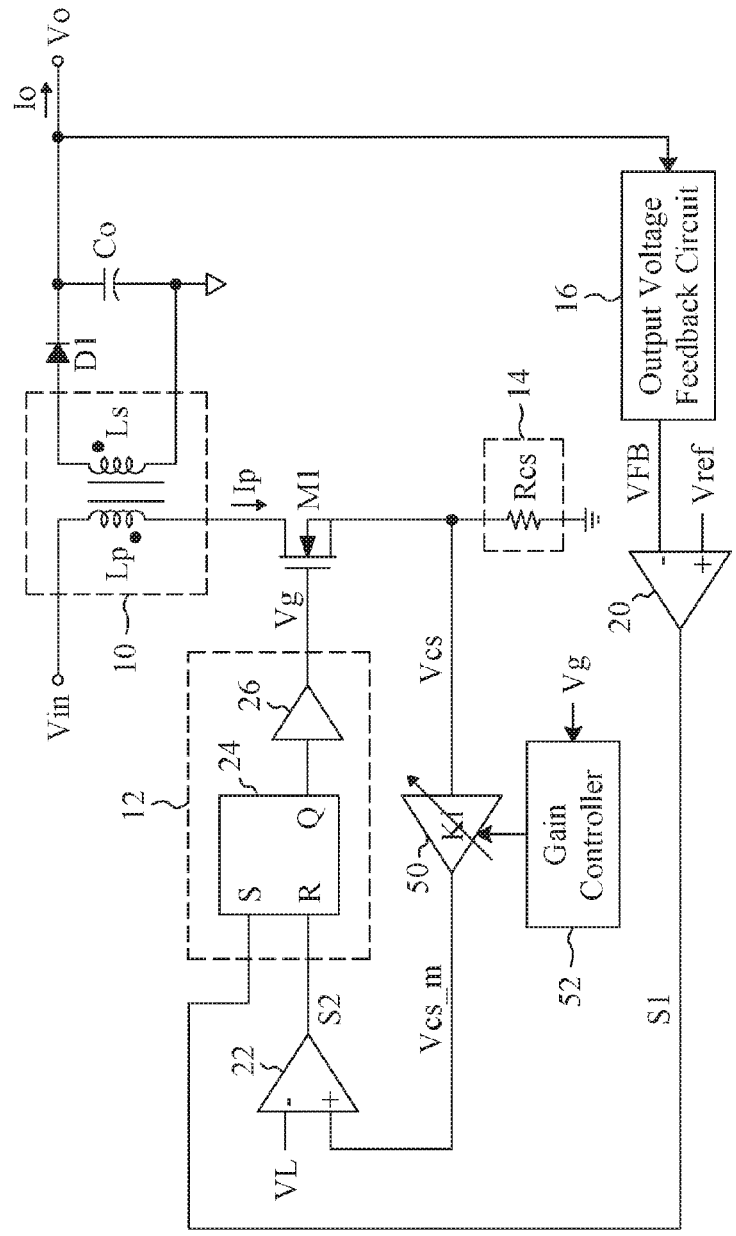
S
R
Q
Delay Time Controller
Programmable Delay Circuit
46
48
S2
22
VL
20
Vref
S1

Fig. 6


Io
Vo
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Rcs
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16
Output Voltage Feedback Circuit
VFB
Vref
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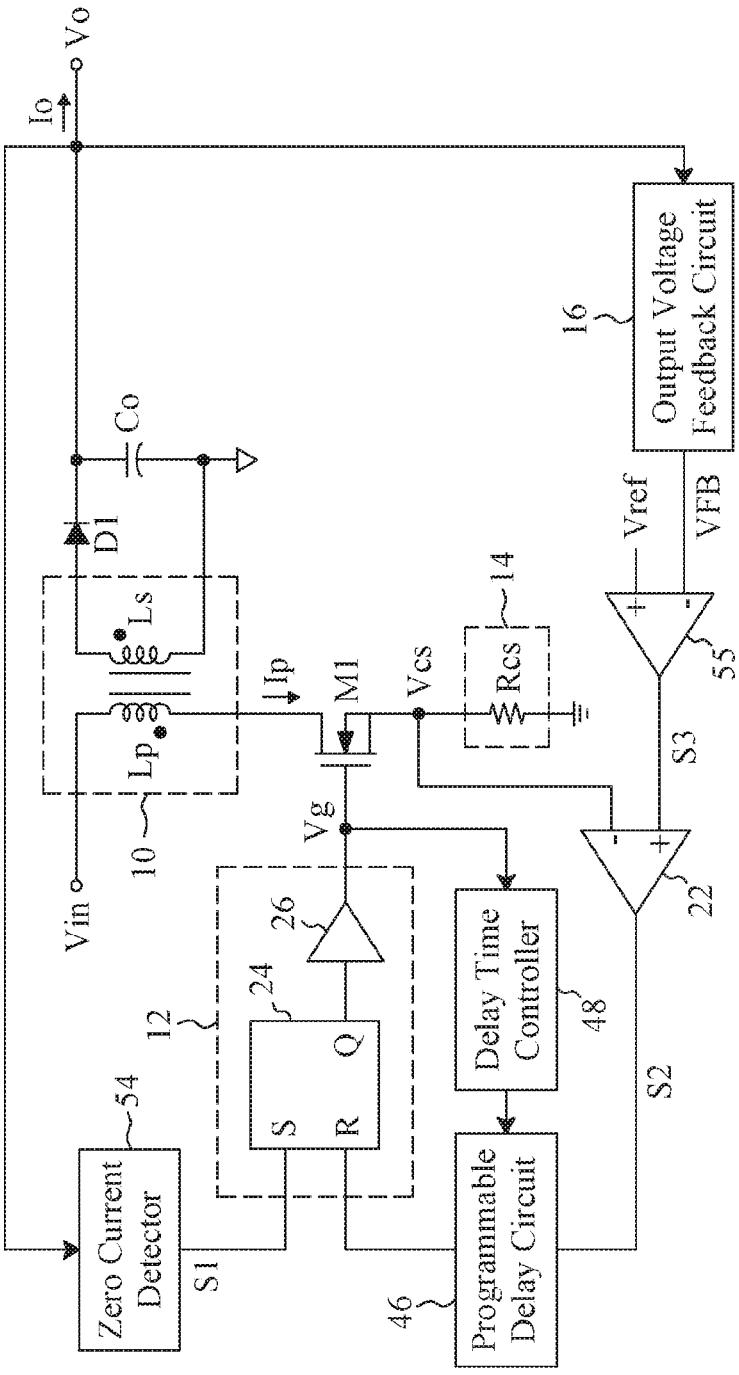
Vin
Vg
Vcs
26
24
12
S
R
Q
50
K1
Gain Controller
52
22
S2
Vcs_m
VL
S1

Fig. 7


Vo
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Vcs
Rcs
14
Vg
Vin
26
12
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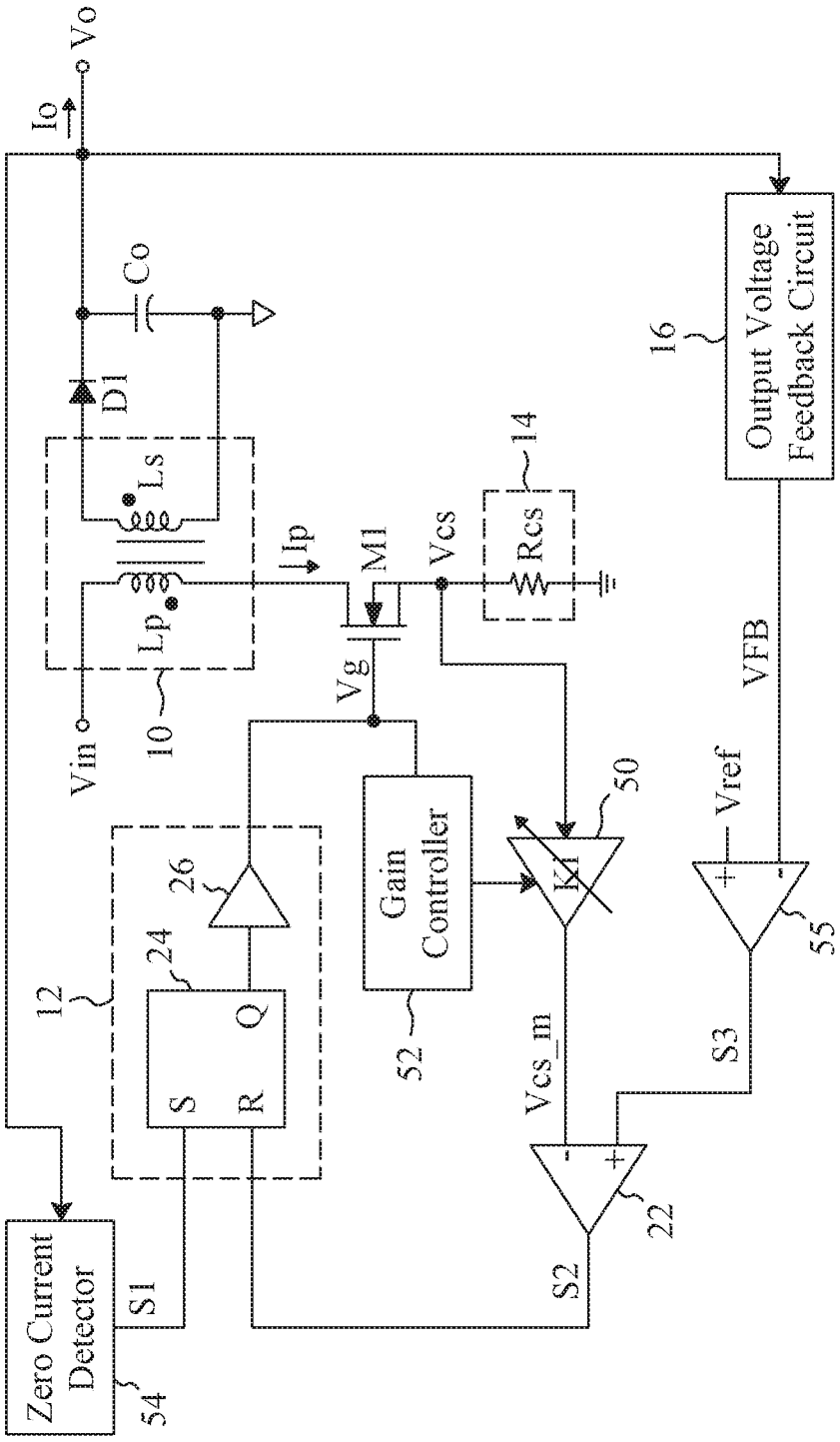
S
R
Q
54
Zero Current Detector
S1
Delay Time Controller
48
Programmable Delay Circuit
46
S2
22
S3
55
Vref
VFB
16
Output Voltage Feedback Circuit

Fig. 8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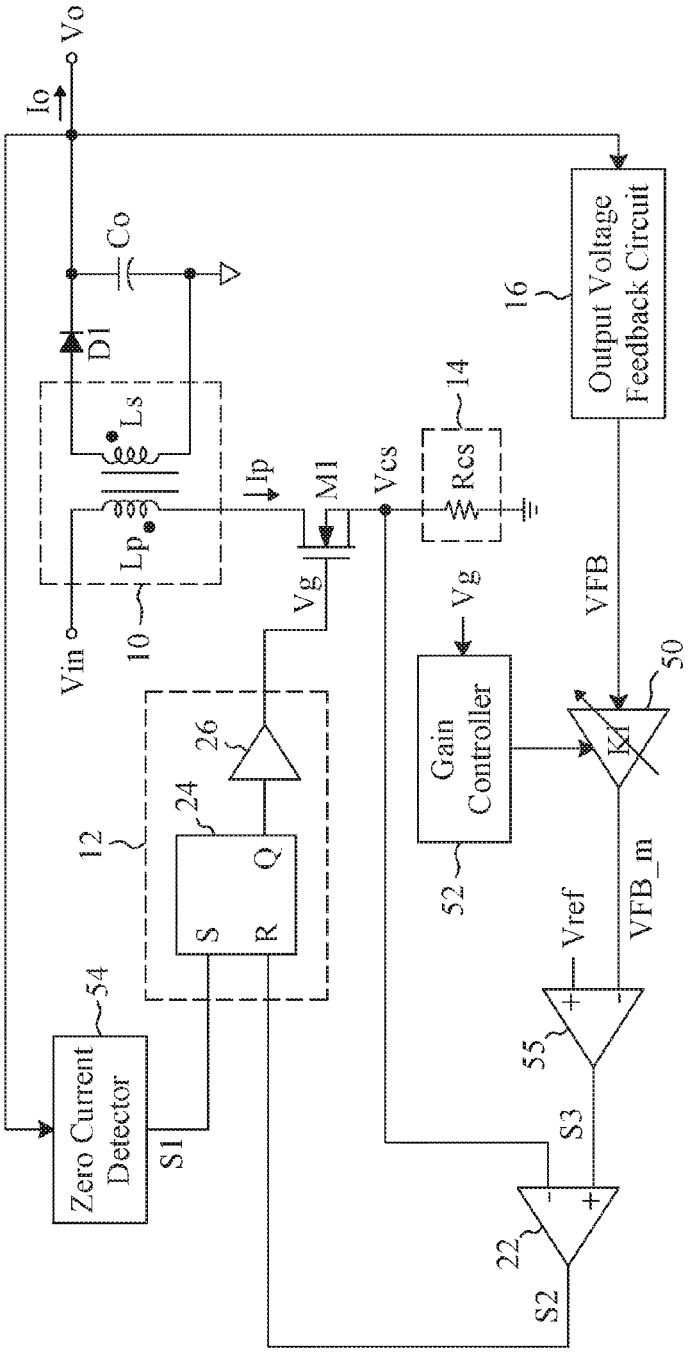
Output Voltage Feedback Circuit
VFB
Vg
Vin
10
Vref
50
Gain Controller
K1
26
24
12
Q
S
R
52
Vcs_m
S3
55
Zero Current Detector
S1
54
S2
22

Fig. 9


Vo
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Ls
Lp
10
Vin
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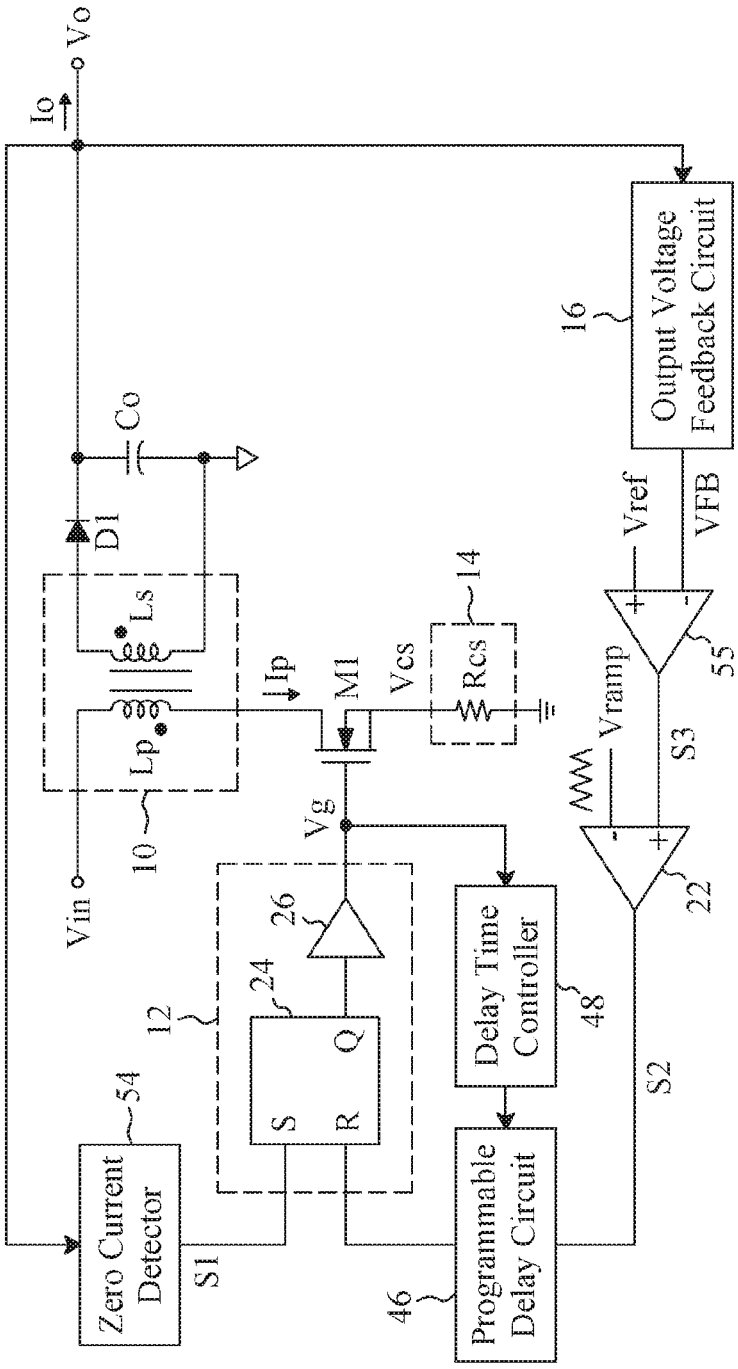
M1
Vcs
Rcs
14
16
Output Voltage Feedback Circuit
VFB
Vg
Vg
Gain Controller
52
50
K1
26
24
12
S
R
Q
Vref
VFB_m
55
54
Zero Current Detector
S1
S3
22
S2

Fig. 10


Vo
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Vin
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M1
Vcs
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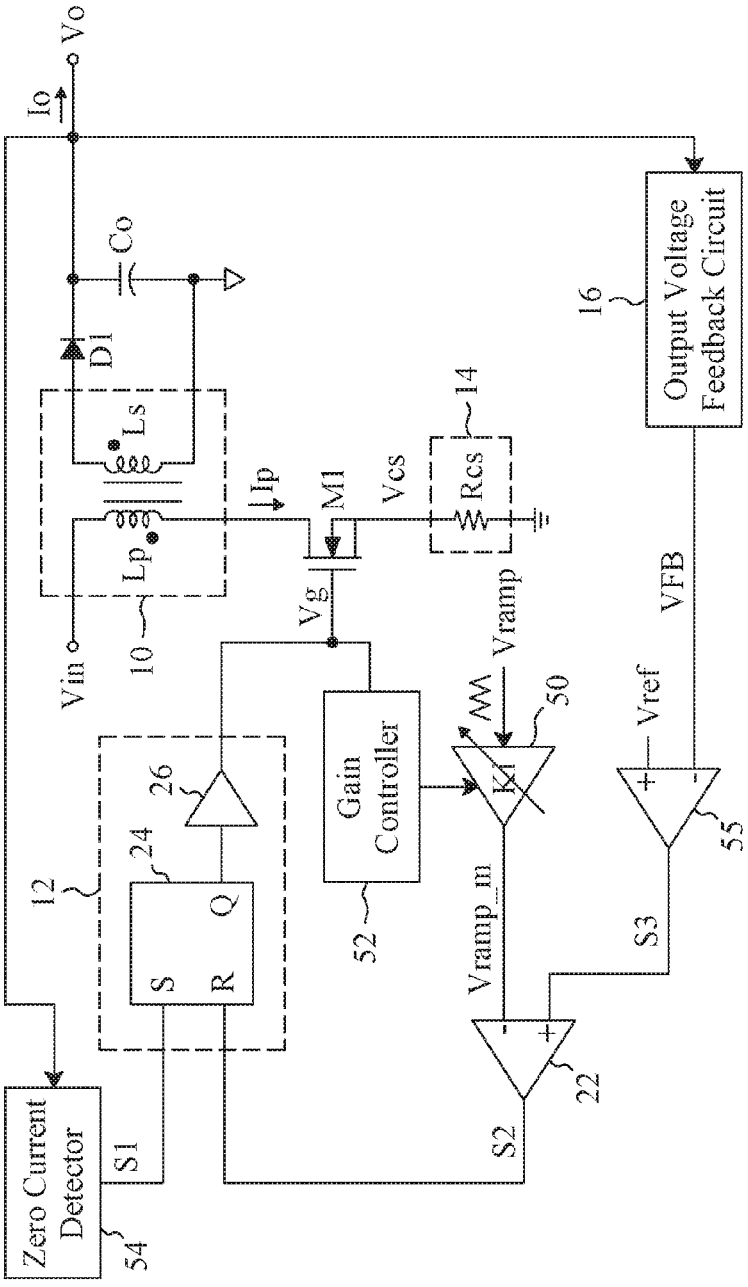
S
R
Q
54
Zero Current Detector
S1
46
Programmable Delay Circuit
Delay Time Controller
48
S2
16
Output Voltage Feedback Circuit
Vref
VFB
55
Vramp
S3
22

Fig. 11


Vo
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M1
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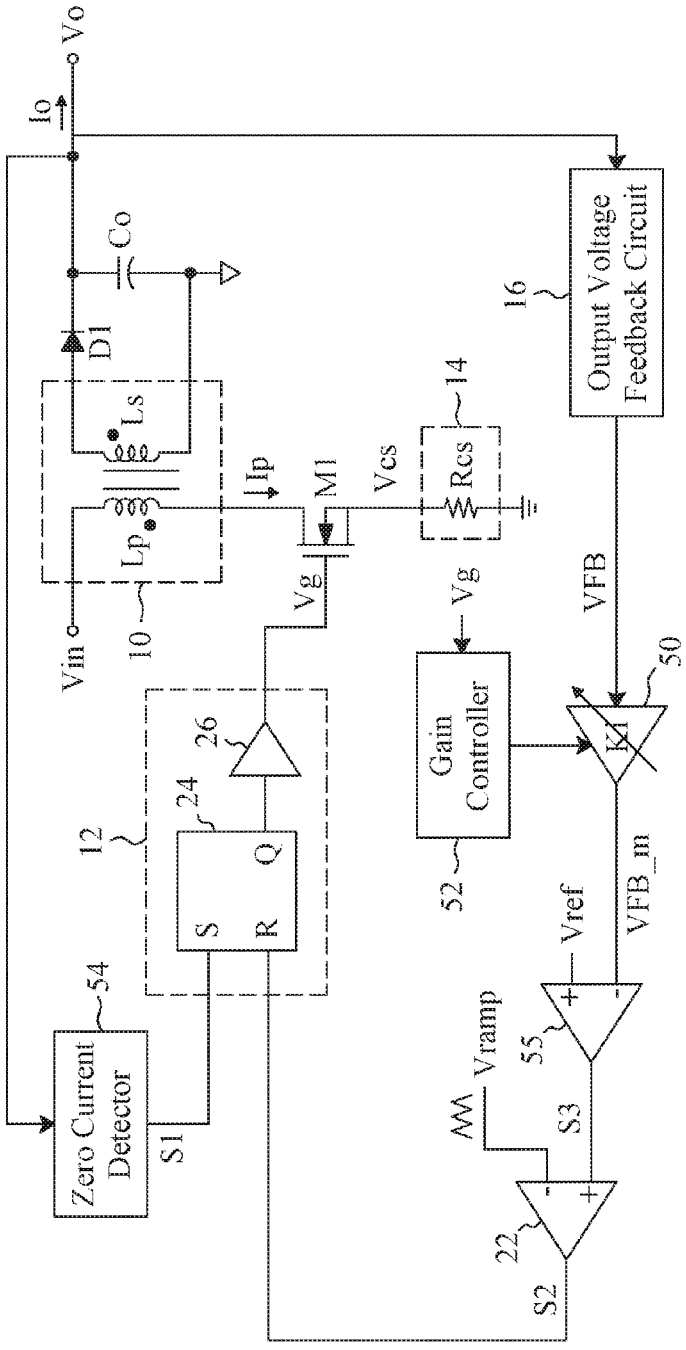
Vramp
16
Output Voltage Feedback Circuit
VFB
Vref
55
50
K1
Gain Controller
52
26
12
24
S
R
Q
Vramp_m
S3
22
S2
Zero Current Detector
S1
54

Fig. 12


Vo
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M1
Vcs
Rcs
14
16
Output Voltage Feedback Circuit
Vin
10
Vg
Vg
VFB
Gain Controller
50
Ki
26
24
12
S
R
Q
52
Vref
VFB_m
54
Zero Current Detector
S1
Vramp
55
S3
22
S2

Fig. 13

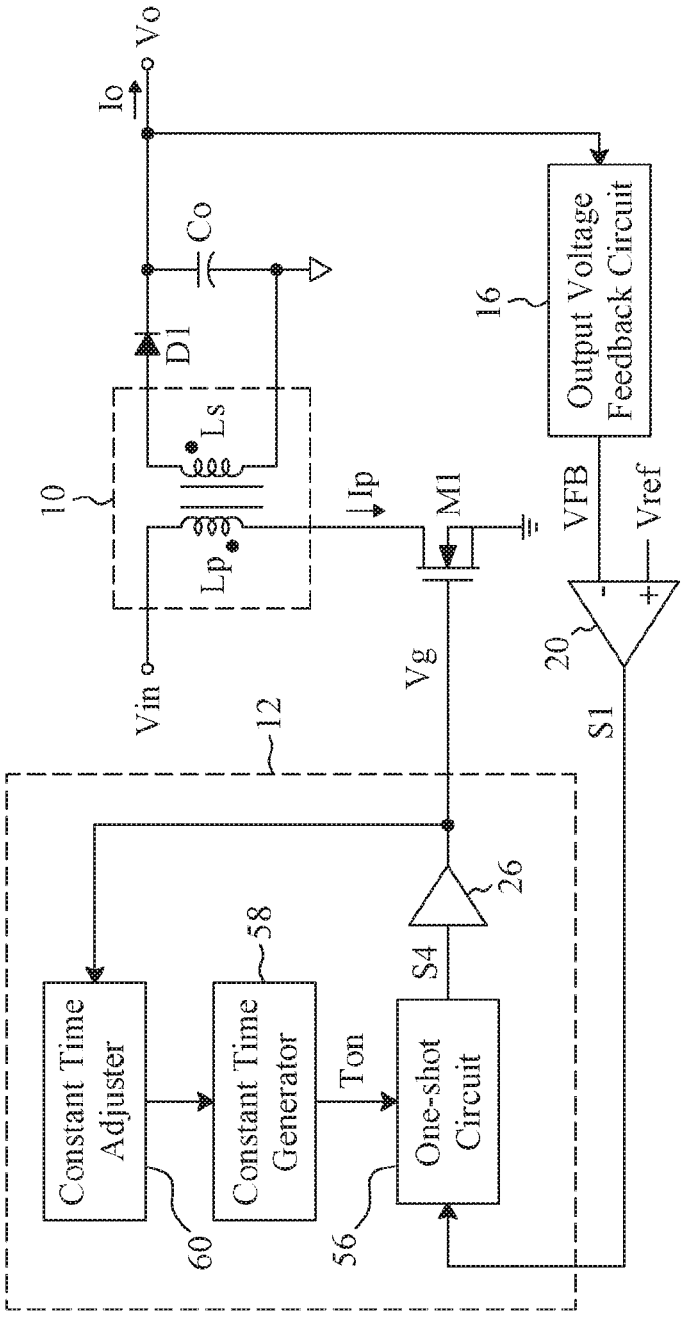
Vo
Io
Co
D1
Ls
Lp
10
Ip
M1
VFB
Vref
16
Output Voltage Feedback Circuit
20
Vin
12
Vg
S1
26
S4
58
Constant Time Adjuster
Constant Time Generator
Ton
One-shot Circuit
60
56

Fig. 14

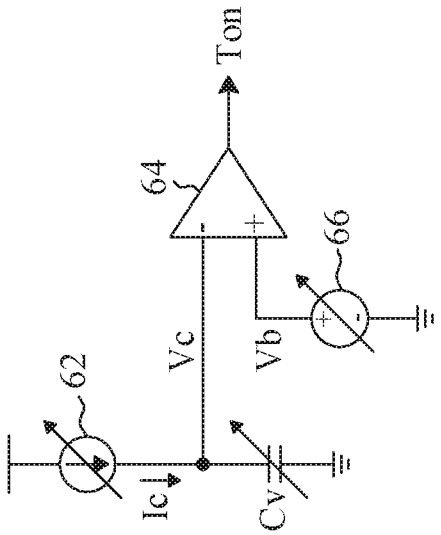

Fig. 15

FREQUENCY JITTERING CONTROL CIRCUIT AND METHOD FOR A PFM POWER SUPPLY

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a Continuation of U.S. patent application Ser. No. 13/567,272, filed 6 Aug. 2012, which claims priority to Taiwan Patent Application No. 100130691, filed 26 Aug. 2011, and all the benefits accruing therefrom under 35 U.S.C. §119, the contents of which in its entirety are herein incorporated by reference.

FIELD OF THE INVENTION

[0002] The present invention is related generally to a switching mode power supply (SMPS) and, more particularly, to pulse frequency modulation (PFM) power supply.

BACKGROUND OF THE INVENTION

[0003] Electro-magnetic interference (EMI) is known as a critical issue in designing a switching power supply, and is typically improved by spread-spectrum approaches that improve EMI by jittering the switching frequency of the power supply. Existing pulse width modulation (PWM) power supply devices, as those disclosed in U.S. Pat. Nos. 5,929,620, 6,249,876 and 7,289,582, mainly accomplish spectrum-spreading by jittering the frequency of the oscillator and in turn jittering the switching frequency of the power supply. A PFM power supply is a variable-frequency system whose switching frequency varies with its load, so is less subject to EMI. Such a PFM power supply, however, when having a consistent load, has its switching frequency held consistent, and thus still suffers from EMI. Nevertheless, it is infeasible in the PFM power supply to jitter the switching frequency by jittering the frequency of an oscillator that is absent.

SUMMARY OF THE INVENTION

[0004] An objective of the present invention is to provide a frequency jittering control circuit and method for a PFM power supply.

[0005] According to the present invention, a frequency jittering control circuit for a PFM power supply comprises a pulse frequency modulator for generating a frequency jittering control signal to switch a power switch and generate an output voltage. In a peak-current mode PFM power supply, the pulse frequency modulator turns on the power switch by triggering the control signal responsive to a first signal, and turns off the power switch by terminating the control signal responsive to a second signal. The frequency jittering control circuit jitters the first or second signal to generate the frequency jittering control signal. In a quasi resonant mode PFM power supply, the pulse frequency modulator jitters the on or off time in order to generate the frequency jittering control signal. In a constant-on-time mode or constant-off-time mode PFM power supply, the pulse frequency modulator jitters the constant on-time or constant off-time in order to generate the frequency jittering control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] These and other objectives, features and advantages of the present invention will become apparent to those skilled in the art upon consideration of the following description of the preferred embodiments according to the present invention taken in conjunction with the accompanying drawings, in which:

[0007] FIG. **1** is a circuit diagram of a first embodiment according to the present invention;

[0008] FIG. **2** is a waveform diagram of the control signal for switching the power switch shown in FIG. **1**;

[0009] FIG. **3** is a circuit diagram of a first embodiment for the signal generator shown in FIG. **1**;

[0010] FIG. **4** is a circuit diagram of a second embodiment for the signal generator shown in FIG. **1**;

[0011] FIG. **5** is a circuit diagram of a second embodiment according to the present invention;

[0012] FIG. **6** is a circuit diagram of a third embodiment according to the present invention;

[0013] FIG. **7** is a circuit diagram of a fourth embodiment according to the present invention;

[0014] FIG. **8** is a circuit diagram of a fifth embodiment according to the present invention;

[0015] FIG. **9** is a circuit diagram of a sixth embodiment according to the present invention;

[0016] FIG. **10** is a circuit diagram of a seventh embodiment according to the present invention;

[0017] FIG. **11** is a circuit diagram of an eighth embodiment according to the present invention;

[0018] FIG. **12** is a circuit diagram of a ninth embodiment according to the present invention;

[0019] FIG. **13** is a circuit diagram of a tenth embodiment according to the present invention;

[0020] FIG. **14** is a circuit diagram of an eleventh embodiment according to the present invention; and

[0021] FIG. **15** is a circuit diagram of an embodiment for the constant time generator shown in FIG. **14**.

DETAILED DESCRIPTION OF THE INVENTION

[0022] A first embodiment according to the present invention shown in FIG. **1** is a peak-current mode PFM power supply that comprises a transformer **10**, a power switch M**1** connected in series to a primary coil Lp of the transformer **10**, and a frequency jittering control circuit that generates a frequency jittering control signal Vg for switching the power switch M**1**, thereby converting an input voltage Vin into an output voltage Vo. In the frequency jittering control circuit, there are a pulse frequency modulator **12** for generating the control signal Vg according to a first signal S**1** and a second signal S**2**, a current detector **14** for detecting a current Ip of the power switch M**1** to generate a current sense signal Vcs, an output voltage feedback circuit **16** for detecting the output voltage Vo to generate a feedback signal VFB, a comparator **20** for comparing the feedback signal VFB with a reference voltage Vref to generate the first signal S**1**, a signal generator **18** for providing a jittering signal VL, and a comparator **22** for comparing the signal VL with the current sense signal Vcs to generate the second signal S**2**. In this embodiment, the current detector **14** comprises a current sensing resistor Rcs connected in series to the power switch M**1**, for generating the current sense signal Vcs when the current Ip passes therethrough. The pulse frequency modu-

lator **12** comprises a flip-flop **24** for generating a pulse frequency modulating signal Q responsive to the signals S**1** and S**2**, and a gate driver **26** for generating the control signal Vg responsive to the pulse frequency modulating signal Q. In the pulse frequency modulator **12**, the signals S**1** and S**2** are input to a setting terminal S and a resetting terminal R of the flip-flop **24**, respectively, so the pulse frequency modulating signal Q is to be triggered by the first signal S**1** and terminated by the second signal S**2**, thereby controlling the on time of the power switch M**1** to start and end, and in turn controlling the on-time of the power switch M**1**. More particularly, whenever the output voltage Vo decreases to become lower than the reference voltage Vref, the first signal S**1** turns to be logic "1", thereby triggering the pulse frequency modulating signal Q, and in turn turning on the power switch M**1** to make the current Ip increase. When the current sense signal Vcs increases to become higher than the signal VL, the second signal S**2** turns to be logic "1", thereby resetting the signal Q, and in turn turning off the power switch M**1**. Since the signal VL jitters, the time for the signal Q to be turned off jitters to jitter the switching frequency of the power switch M**1**. FIG. **2** illustrates the process clearly. With the rising slope of the current sense signal Vcs remaining unchanged, when the signal VL increases from VL**1** to VL**2**, the current sense signal Vcs needs more time to rise to the signal VL. Thus, the cycle of the control signal Vg increases from T**1**=1/f**1** to T**2**=1/f**2**, as shown by waveforms **28** and **29**, respectively, meaning that the switching frequency of the power switch M**1** decreases from f**1** to f**2**. On the contrary, when the signal VL decreases, the switching frequency of the power switch M**1** increases. Therefore, jittering the signal VL is an effective way to jitter the switching frequency of the power switch M**1**, in turn improving the EMI problem in the PFM power supply.

[0023] FIG. **3** is a first embodiment of the signal generator **18** of FIG. **1**. In the left part, a voltage-to-current converter **30** and a current mirror **32** are for generating the preset signal VL, while a counter **34**, a ramp generator **36**, a voltage-to-current converter **38** and a current mirror **40** in the right part of FIG. **3** are for jittering the signal VL. The voltage-to-current converter **30** converts the reference voltage Vref**1** into a current I**1**. The current mirror **32** mirrors the current I**1** to generate a current I**2**. The ramp generator **36** provides a ramp signal Vra. The counter **34** generates a count value CNT according to a clock CLK for the ramp generator **36** to adjust the ramp signal Vra. The voltage-to-current converter **38** converts the ramp signal Vra into a current I**3**. The current mirror **40** mirrors the current I**3** to generate a current I**4**. The currents I**2** and I**4** are combined into a jittering current I**5**, which passes through a resistor Ro to generate the jittering signal VL. The clock CLK may be generated by a periodic signal in the PFM power supply, such as the signal Q, Vg or VFB. In other embodiments, the counter **34** may be replaced by a different circuit, such as a random number generator.

[0024] FIG. **4** is a second embodiment of the signal generator **18** of FIG. **1**, with the left part identical to that in FIG. **3**. The rest of the circuit is composed of a variable resistor **42** and a resistance controller **44**. The variable resistor **42** includes a resistor Radj and the resistor Ro connected in series. The resistance controller **44** finely adjusts the resistor Radj to change the resistance of the variable resistor **42**, thereby jittering the signal VL. The resistance controller **44** may be realized by a counter or a random number generator.

[0025] The embodiment shown in FIG. **1** jitters the switching frequency by jittering the second signal S**2**, but the other embodiment can jitter the switching frequency by jittering the first signal S**1**. As the embodiment shown in FIG. **5**, the first signal S**1** is delayed by a programmable delay circuit **46** for a period of time before it is sent to the pulse frequency modulator **12**. A delay time controller **48** adjusts the delay time of the programmable delay circuit **46** according to the output Q of the flip-flop **24**, thereby jittering the time where the signal Q is triggered, and in turn, jittering the switching frequency of the power switch M**1**. The delay time controller **48** may be realized by a counter or a random number generator. In other embodiments, the delay time controller **48** may adjust the delay time of the programmable delay circuit **46** alternatively according to another periodic signal, such as the signal Vg or VFB.

[0026] The jitter approach of FIG. **5** may be modified into the embodiment shown in FIG. **6**, where the second signal S**2** is delayed by the programmable delay circuit **46** for a period of time before sent into the pulse frequency modulator **12**, and the delay time controller **48** adjusts the delay time of the programmable delay circuit **46** according to the output Q of the flip-flop **24**, thereby jittering the time where the signal Q is reset, and in turn jittering the switching frequency of the power switch M**1**.

[0027] While the embodiment of FIG. **1** jitters the second signal S**2** by means of jittering the signal VL, it is also feasible to jitter the second signal S**2** by jittering the current sense signal Vcs. As the embodiment shown in FIG. **7**, the current sense signal Vcs is amplified by a gain circuit **50** into a signal Vcs_m. A gain controller **52** adjusts a gain Ki of the gain circuit **50** according to the control signal Vg, thereby changing the rising slope of the current sense signal Vcs_m, and in turn changing the time where the second signal S**2** is triggered, so as to finally change the time where the signal Q is terminated. When the gain Ki of the gain circuit **50** jitters, the switching frequency of the power switch M**1** jitters accordingly. In other embodiments, the gain controller **52** may adjust the gain Ki according to another periodic signal. The gain controller **52** may be realized by a counter or a random number generator.

[0028] FIG. **8** is a quasi resonant (QR) mode PFM power supply, which includes a zero current detector **54** for detecting an output current Io of the PFM power supply and triggering the first signal S**1** for the pulse frequency modulator **12** when the output current Io decreases and reaches a threshold value. The current detector **14** detects the current Ip of the power switch M**1** to generate the current sense signal Vcs. The output voltage feedback circuit **16** detects the output voltage Vo to generate the feedback signal VFB. An error amplifier **55** amplifies the difference between the feedback signal VFB and the reference voltage Vref to generate a third signal S**3**. The comparator **22** compares the current sense signal Vcs with the third signal S**3** to generate the second signal S**2**. The pulse frequency modulator **12**, similar to the embodiment of FIG. **1**, has the signal Q triggered by the first signal S**1** and reset by the second signal S**2**. For jittering the second signal S**2**, the programmable delay circuit **46** delays the second signal S**2** for a period of time before sending it to the pulse frequency modulator **12**. The delay time controller **48** adjusts the delay time of the

programmable delay circuit **46** according to the control signal Vg. Jittering the delay time of the programmable delay circuit **46** jitters the time where the signal Q is terminated, thereby jittering the switching frequency of the power switch M**1**.

[0029] The approach to jittering the second signal S**2** as shown in FIG. **8** may be modified into the embodiment of FIG. **9**, where the gain circuit **50** amplifies the current sense signal Vcs into Vcs_m, and the gain controller **52** jitters the gain Ki of the gain circuit **50** according to the control signal Vg, thereby jittering the rising slope of the current sense signal Vcs_m, then jittering the time where the second signal S**2** is triggered, and in turn jittering the time where the signal Q is terminated, so as to finally jitter the switching frequency of the power switch M**1**.

[0030] The method for jittering the rising slope of the current sense signal Vcs_m as shown in FIG. **9** may be modified into the embodiment of FIG. **10**, where the gain circuit **50** amplifies the feedback signal VFB into VFB_m, and the gain controller **52** jitters the gain Ki of the gain circuit **50** according to the control signal Vg, thereby jittering the rising slope of the feedback signal VFB_m, in turn jittering the time where the second signal S**2** is triggered, so as to jitter the time when the signal Q is terminated and finally make the switching frequency of the power switch M**1** jitter accordingly.

[0031] The embodiments of FIGS. **8-10** all involve comparing the current sense signal Vcs related to the current Ip of the power switch M**1** with the third signal S**3** to generate the second signal S**2**. In other embodiments, another ramp signal may be implemented to replace the current sense signal Vcs. For example, the circuit of FIG. **8** may be modified into a QR voltage mode PFM power supply as shown in FIG. **11**. Therein the comparator **22** compares the internal ramp signal Vramp with the third signal S**3** to generate the second signal S**2**. The circuit of FIG. **9** may be modified into a voltage mode structure as shown in FIG. **12**. Therein the gain circuit **50** amplifies a ramp signal Vramp to generate a ramp signal Vramp_m, and the comparator **22** compares the ramp signal Vramp_m with the third signal S**3** to generate the second signal S**2**. The circuit of FIG. **10** may be modified into a voltage mode structure as shown in FIG. **13**. Therein, the comparator **22** compares the ramp signal Vramp with the third signal S**3** to generate the second signal S**2**.

[0032] The embodiment shown in FIG. **14** is a constant on-time or constant off-time mode PFM power supply. Its pulse frequency modulator **12** comprises a one-shot circuit **56** triggered by the first signal S**1** to generate a pulse signal S**4** whose pulse width is determined by the constant time Ton from a constant time generator **58**. The constant time Ton is finely adjusted by the constant time adjuster **60** according to the control signal Vg so as to become jittering. The gate driver **26** generates the control signal Vg responsive to the pulse signal S**4**. By jittering the length of the constant time Ton, the on time or off time of the power switch M**1** is jittered, thereby jittering the switching frequency of the power switch M**1**. In other embodiments, the constant time adjuster **60** may jitter the length of the constant time Ton alternatively according to another periodic signal, such as the feedback signal VFB. The constant time adjuster **60** may be realized by a counter or a random number generator.

[0033] FIG. **15** is one embodiment of the constant time generator **58** of FIG. **14**, which includes a current source **62** for providing a charging current Ic that charges a capacitor Cv to generate a charging voltage Vc, a comparator **64** for comparing the charging voltage Vc with a threshold voltage Vb provided by a voltage source **66** to determine the length of the constant time Ton. The constant time adjuster **60** adjusts at least one of the capacitor Cv, the charging current Ic and the threshold voltage Vb, thereby jittering the length of the constant time Ton.

[0034] While the present invention has been described in conjunction with preferred embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, it is intended to embrace all such alternatives, modifications and variations that fall within the spirit and scope thereof as set forth in the appended claims.

What is claimed is:

1. A frequency jittering control circuit configured to operably generate a frequency jittering control signal to switch a power switch of a pulse frequency modulation power supply to generate an output voltage, the frequency jittering control circuit comprising:

a pulse frequency modulator connected to the power switch, configured to operably trigger the control signal responsive to a first signal to turn on the power switch, and configured to operably terminate the control signal responsive to a second signal to turn off the power switch;

a signal generator configured to operably provide a jittering signal according to a count value or a random number;

a current detector configured to operably detect a current of the power switch to generate a current sense signal; and

a comparator connected to the pulse frequency modulator, the signal generator and the current detector, and configured to operably compare the current sense signal with the jittering signal to generate the second signal.

2. The frequency jittering control circuit of claim **1**, wherein the signal generator configures to operably adjust a reference signal by a ramp signal to generate the jittering signal, wherein the ramp signal is adjustable according to the count value or the random number.

3. The frequency jittering control circuit of claim **1**, wherein the signal generator comprises:

a first voltage-to-current converter configured to operably convert a reference voltage into a first current;

a first current mirror connected to the first voltage-to-current converter, and configured to operably mirror the first current to generate a second current;

a ramp generator configured to operably generate a ramp signal;

a counter or a random number generator connected to the ramp generator, and configured to operably generate the count value or the random number to adjust the ramp signal;

a second voltage-to-current converter connected to the ramp generator, and configured to operably convert the ramp signal into a third current;

a second current mirror connected to the second voltage-to-current converter, and configured to operably mirror the third current to generate a fourth current; and

a resistor connected to the first and second current mirrors, and configured to operably generate the jittering signal according to a sum of the second and fourth currents.

4. The frequency jittering control circuit of claim **1**, wherein the signal generator comprises a variable resistor having a resistance adjustable according to the count value or the random number, and the jittering signal is adjusted according to a voltage across the variable resistor.

5. The frequency jittering control circuit of claim **1**, wherein the signal generator comprises:

a voltage-to-current converter configured to operably convert a reference voltage into a first current;

a current mirror connected to the voltage-to-current converter, and configured to operably mirror the first current to generate a second current;

a variable resistor connected to the current mirror, and configured to operably generate the jittering signal according to the second current; and

a resistance controller connected to the variable resistor, and configured to operably adjust a resistance of the variable resistor according to the count value or the random number to adjust the jittering signal.

6. The frequency jittering control circuit of claim **5**, wherein the resistance controller comprises a counter or a random number generator configured to operably generate the count value or the random number.

7. The frequency jittering control circuit of claim **1**, further comprising:

an output voltage feedback circuit configured to operably detect the output voltage to generate a feedback signal; and

a comparator connected to the pulse frequency modulator and the output voltage feedback circuit, and configured to operably compare a reference voltage with the feedback signal to generate the first signal.

8. A frequency jittering control circuit configured to operably generate a frequency jittering control signal to switch a power switch of a pulse frequency modulation power supply to generate an output voltage, the frequency jittering control circuit comprising:

an output voltage feedback circuit configured to operably detect the output voltage to generate a feedback signal;

a comparator connected to the output voltage feedback circuit, and configured to operably compare the feedback signal with a reference voltage to generate a first signal;

a one-shot circuit connected to the comparator, and configured to operably be triggered by the first signal to generate a pulse signal;

a driver connected to the one-shot circuit, and configured to operably generate the control signal responsive to the pulse signal; and

a constant time generator connected to the one-shot circuit, and configured to operably provide a jittering constant time according to a count value or a random number to determine a constant on time or a non-constant on time of the control signal.

9. The frequency jittering control circuit of claim **8**, wherein the constant time generator comprises:

a capacitor;

a current source connected to the capacitor, and configured to operably provide a charging current to charge the capacitor to generate a charging voltage; and

a second comparator connected to the capacitor, and configured to operably compare the charging voltage with a threshold voltage to determine the constant time;

wherein at least one of the capacitor, the charging current and the threshold voltage is adjusted according to the count value or the random number to generate the jittering constant time.

10. A frequency jittering control method for generating a frequency jittering control signal to switch a power switch of a pulse frequency modulation power supply to generate an output voltage, the frequency jittering control method comprising steps of:

A.) triggering the control signal responsive to a first signal to turn on the power switch;

B.) terminating the control signal responsive to a second signal to turn off the power switch; and

C.) jittering the first or second signal to jitter a switching frequency of the power switch;

wherein the step C comprises steps of:

detecting a current of the power switch to generate a current sense signal;

comparing the current sense signal with a third signal to generate the second signal; and

jittering the third signal according to a count value or a random number.

11. A frequency jittering control method for generating a frequency jittering control signal to switch a power switch of a pulse frequency modulation power supply to generate an output voltage, the frequency jittering control method comprising steps of:

detecting the output voltage to generate a feedback signal;

comparing the feedback signal with a reference voltage to generate a first signal;

triggering a pulse signal responsive to the first signal; and

jittering a pulse width of the pulse signal according to a count value or a random number to jitter a switching frequency of the power switch.

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