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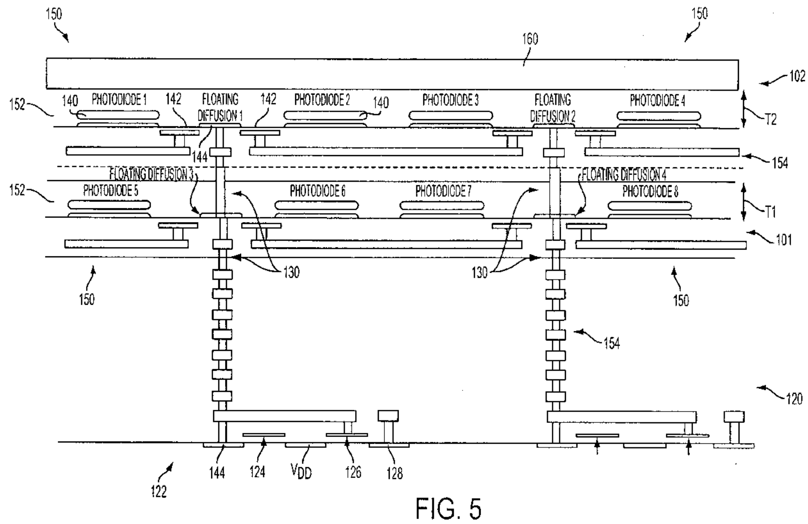

FIG. 5

(57) Abstract: An image sensor includes a first sensor layer (101) having a first array of pixels and a second sensor (102) layer having a second array of pixels. Each pixel of the first and second arrays has a photodetector (140) for collecting charge in response to incident light, a charge-to- voltage conversion mechanism (144), and a transfer gate (142) for selectively transferring charge from the photodetector to the charge- to- voltage mechanism. The first and second sensor layers each have a thickness to collect light with a first and second preselected ranges of wavelengths, respectively. A circuit layer (120) is situated below the first sensor layer and has support circuitry (122) for the pixels of the first and second sensor layers, and interlayer connectors (130) are between the pixels of the first and second layers and the support circuitry.

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IMAGE SENSOR HAVING MULTIPLE SENSING LAYERS

FIELD OF THE INVENTION

The invention relates generally to the field of image sensors, and more particularly to a stacked image sensor construction.

BACKGROUND OF THE INVENTION

A typical Complementary Metal Oxide Semiconductor (CMOS) image sensor has an image sensing portion that includes a photodiode for collecting charge in response to incident light and a transfer gate for transferring charge from the photodiode to a charge-to-voltage conversion mechanism, such as a floating diffusion. Usually, the sensing portion is fabricated within the same material layer and with similar processes as the control circuitry for the image sensor. In an effort to increase the number of pixels provided in an image sensor, pixel size has been decreasing.

However, as the pixel size shrinks, the illuminated area of the photodetector is also typically reduced, in turn decreasing the captured signal level and degrading performance.

Thus, a need exists for an improved image sensor structure.

SUMMARY OF THE INVENTION

An image sensor includes a first sensor layer having a first array of pixels. Each pixel of the first array has a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion mechanism, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism. The first sensor layer has a thickness to collect light with a first preselected range of wavelengths. A second sensor is layer situated over the first sensor layer, and has a second array of pixels. Each pixel includes a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism. The second sensor layer has a thickness to collect light with a second preselected range of wavelengths. A circuit layer is situated below the first sensor layer and has support circuitry for the pixels of the first and second sensor layers, and interlayer connectors are between the pixels of the first and second layers and the support circuitry.

The present invention has the advantage of providing an improved image sensor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

Figure 1 is a block diagram illustrating aspects of an embodiment of a digital camera.

Figure 2 is a block diagram conceptually illustrating an embodiment of an image sensor.

Figure 3 is a block diagram illustrating portions of a pixel.

Figures 4A and 4B illustrate examples of embodiments of pixel kernel configurations.

Figure 5 is a section view illustrating an embodiment of an image sensor.

Figure 6 is a section view illustrating another embodiment of an image sensor.

Figures 7 and 8 illustrate examples of color filter arrays.

Figure 9 is a section view illustrating another embodiment of an image sensor.

Figure 10 is a section view illustrating a further embodiment of an image sensor.

Figure 11 conceptually illustrates an example of binning pixels in embodiments of an image sensor.

Figure 12 is a section view illustrating another embodiment of an image sensor.

Figure 13 is a section view illustrating another embodiment of an image sensor.

Figure 14 is a block diagram conceptually illustrating another embodiment of an image sensor.

DETAILED DESCRIPTION OF THE INVENTION

In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s) being described. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Turning now to Figure 1, a block diagram of an image capture device shown as a digital camera embodying aspects of the present disclosure is illustrated. Although a digital camera is illustrated and described, the present invention is clearly applicable to other types of image capture devices. In the disclosed camera, light 10 from a subject scene is input to an imaging stage 11, where the light is focused by a lens 12 to form an image on an image sensor 20. The image sensor 20 converts the incident light to an electrical signal for each picture element (pixel). In some embodiments, the image sensor 20 is an active pixel sensor (APS) type (APS devices are often referred to as CMOS sensors because of the ability to fabricate them in a Complementary Metal Oxide Semiconductor process).

The amount of light reaching the sensor 20 is regulated by an iris block 14 that varies the aperture and the neutral density (ND) filter block 13 that includes one or more ND filters interposed in the optical path. Also regulating the overall light level is the time that the shutter block 18 is open. The exposure controller block 40 responds to the amount of light available in the scene as metered by the brightness sensor block 16 and controls all three of these regulating functions.

This description of a particular camera configuration will be familiar to one skilled in the art, and it will be apparent to such a skilled person that many variations and additional features are present. For example, an autofocus system is added, or the lens is detachable and interchangeable. It will be understood that the present disclosure applies to various types of digital cameras where similar functionality is provided by alternative components. For example, the digital camera is a relatively simple point and shoot digital camera, where the shutter 18 is a relatively simple movable blade shutter, or the like, instead of the more complicated focal plane arrangement. Aspects of the present invention can also be practiced on imaging components included in non-camera devices such as mobile phones and automotive vehicles.

An analog signal from the image sensor 20 is processed by an analog signal processor 22 and applied to an analog to digital (A/D) converter 24. A timing generator 26 produces various clocking signals to select rows and pixels and synchronizes the operation of the analog signal processor 22 and the A/D converter 24. The image sensor stage 28 includes the image sensor 20, the analog signal processor 22, the A/D converter 24, and the timing generator 26. The components of the image sensor stage 28 can be separately fabricated integrated circuits, or they could be fabricated as a single integrated circuit as is commonly done with CMOS image sensors. The resulting stream of digital pixel values from the A/D converter 24 is stored in a memory 32 associated with the digital signal processor (DSP) 36.

The digital signal processor 36 is one of three processors or controllers in the illustrated embodiment, in addition to a system controller 50 and an exposure controller 40. Although this partitioning of camera functional control among multiple controllers and processors is typical, these controllers or processors are combined in various ways without affecting the functional operation of the camera and the application of the present invention. These controllers or processors can comprise one or more digital signal processor devices, microcontrollers, programmable logic devices, or other digital logic circuits. Although a combination of such controllers or processors has been described, it should be apparent that one controller or processor can be designated to perform all of the needed functions. All of these variations can perform the same function and fall within the scope of this invention, and the term "processing stage" will be used as needed to encompass all of this functionality within one phrase, for example, as in processing stage 38 in Figure 1.

In the illustrated embodiment, the DSP 36 manipulates the digital image data in its memory 32 according to a software program permanently stored in program memory 54 and copied to the memory 32 for execution during image capture. The DSP 36 executes the software necessary for practicing image processing. The memory 32 includes of any type of random access memory, such as SDRAM. A bus 30 comprising a pathway for address and data signals connects the DSP 36 to its related memory 32, A/D converter 24 and other related devices.

The system controller 50 controls the overall operation of the camera based on a software program stored in the program memory 54, which can include Flash EEPROM or other nonvolatile memory. This memory can also be used to store image sensor calibration data, user setting selections and other data which must be preserved when the camera is turned off. The system controller 50 controls the sequence of image capture by directing the exposure controller 40 to operate the lens 12, ND filter 13, iris 14, and shutter 18 as previously described, directing the timing generator 26 to operate the image sensor 20 and associated elements, and directing the DSP 36 to process the captured image data. After an image is captured and processed, the final image file stored in memory 32 is transferred to a host computer via an interface 57, stored on a removable memory card 64 or other storage device, and displayed for the user on an image display 88.

A bus 52 includes a pathway for address, data and control signals, and connects the system controller 50 to the DSP 36, program memory 54, system memory 56, host interface 57, memory card interface 60 and other related devices.

The host interface 57 provides a high speed connection to a personal computer (PC) or other host computer for transfer of image data for display, storage, manipulation or printing. This interface is an IEEE1394 or USB2.0 serial interface or any other suitable digital interface. The memory card 64 is typically a Compact Flash (CF) card inserted into a socket 62 and connected to the system controller 50 via a memory card interface 60. Other types of storage that are utilized include, for example, PC-Cards, MultiMedia Cards (MMC), or Secure Digital (SD) cards.

Processed images are copied to a display buffer in the system memory 56 and continuously read out via a video encoder 80 to produce a video signal. This signal is output directly from the camera for display on an external monitor, or processed by the display controller 82 and presented on an image display 88. This display is typically an active matrix color liquid crystal display (LCD), although other types of displays are used as well.

The user interface, including all or any combination of viewfinder display 70, exposure display 72, status display 76 and image display 88, and user inputs 74, is controlled by a combination of software programs executed on the exposure controller 40 and the system controller 50. User inputs 74 typically include some combination of buttons, rocker switches, joysticks, rotary dials or touchscreens. The exposure controller 40 operates light metering, exposure mode, autofocus and other exposure functions. The system controller 50 manages the graphical user interface (GUI) presented on one or more of the displays, for example, on the image display 88. The GUI typically includes menus for making various option selections and review modes for examining captured images.

The exposure controller 40 accepts user inputs selecting exposure mode, lens aperture, exposure time (shutter speed), and exposure index or ISO speed rating and directs the lens and shutter accordingly for subsequent captures. The brightness sensor 16 is employed to measure the brightness of the scene and provide an exposure meter function for the user to refer to when manually setting the ISO speed rating, aperture and shutter speed. In this case, as the user changes one or more settings, the light meter indicator presented on viewfinder display 70 tells the user to what degree the image will be over or underexposed. In an automatic exposure mode, the user changes one setting and the exposure controller 40 automatically alters another setting to maintain correct exposure. For example, for a given ISO speed rating when the user reduces the lens aperture, the exposure controller 40 automatically increases the exposure time to maintain the same overall exposure.

The image sensor 20 shown in Figure 1 typically includes a two-dimensional array of light sensitive pixels fabricated on a silicon substrate that provide a way of converting incoming light at each pixel into an electrical signal that is measured. Referring to Figure 2, portions of an embodiment of the image sensor 20 are conceptually illustrated.

In Figure 2, the image sensor 20 is a Complementary Metal Oxide Semiconductor (CMOS) image sensor that includes a first sensor layer 101 having a first array of pixels 111. A second sensor layer 102 is situated over the first sensor layer 101, which has a second array of pixels 112. A circuit layer 120 is situated below the first sensor layer 101, with support circuitry 122 for the pixel arrays 111,112 of the first and second sensor layers 101,102. Interlayer connectors 130 between the pixels 111,112 of the first and second layers 101,102 and the support circuitry 122 provide electrical connections between the respective layers. The first sensor layer 101 has a thickness T1 to collect light with a first preselected range of wavelengths and the second sensor layer has a thickness T2 to collect light with a second preselected range of wavelengths. Regular silicon wafers, silicon on insulator (SOI) wafers or silicon on sapphire (SOS) wafers are all suitable materials for manufacture of the sensor layers 101, 102.

Figure 3 is a block diagram conceptually portions of a pixel 110 of the pixel arrays 111, 112. The pixel 110 includes a photodetector, such as a photodiode 140 and a transfer mechanism, such as a transfer gate 142. The photodetector 140 collects charge in response to incident light and the transfer gate 142 functions to transfer charge from the photodetector 140 to a charge-to-voltage mechanism, such as a floating diffusion sense node 144, which receives the charge from the photodetector 140 and converts the charge to a voltage signal. As noted above, the pixels 110 are typically configured in arrays of rows and columns. A row select transistor is coupled to a column bus, and the readout of charge from the pixels 110 is accomplished by selecting the desired row of the array by activating the proper row select transistor, and the information is read out from the columns of the selected row.

In some embodiments, the pixels 110 of the first and second pixel arrays 111,112 are organized into pixel kernels 150. Figures 4A and 4B illustrate examples of some pixel kernel configurations. In Figure 4A, four photodiodes 140 share a common floating diffusion 144 via respective transfer gates 142, and in Figure 4B, two photodiodes 140 share a common floating diffusion 144. In the embodiments illustrated in Figures 4A and 4B, the interlayer connectors 130 are coupled to the floating diffusions 144 of the pixel kernels 150.

Figure 5 is a cross-section view showing further aspects of an embodiment of an image sensor having two sensor layers 101,102 and a circuit layer 120. Each of the sensor layers 101, 102 and the circuit layer 120 include a silicon portion 152 and one or more metal layers 154. The support circuitry 122 of the circuit layer 120 includes a floating diffusion 144 corresponding to each pixel kernel 150, and coupled to the corresponding pixel kernel by the interlayer connectors 130. The structure illustrated in Figure 5 has an extra metal layer 154 (the metal layer corresponding to the transfer gate 142) and the wafer interconnection 130 is done through the floating diffusions 144. This allows binning the pixels onto the same floating diffusion 144.

Among other things, the support circuitry 122 also includes a reset gate 124, a voltage supply VDD, and a source follower input and output 126, 128 for each pixel kernel 150. In embodiment illustrated in Figure 5, the interlayer connectors 130 electrically connect the respective floating diffusions nodes 144 on sensing layer T2, sensing layer T1, and the circuit wafer to form a collective floating diffusion 144.

In general, reducing the thickness of the silicon portion 152 can result in optical interference, which in turn can degrade quantum efficiency. To mitigate this effect and improve quantum efficiency, antireflection coatings are used on both sides of each of the sensing layers and on top on the circuit layer in some embodiments. Such antireflection coatings are known, and are used, for example, for single layer structures such as ONO stacks (silicon oxide- silicon nitride - silicon oxide) or hafnium oxide-magnesium oxide stacks. Other suitable antireflection coatings could also be used. These antireflection coatings can be deposited using any typical deposition technique before the sensing and the circuit layer are bonded together.

Figure 6 illustrates another embodiment where the interlayer connections 130 are implemented by row and column interconnects, which connect the pixels 111 to the circuit layer 120 via row and column circuitry 132. An extra two metal layers 154 are included and the wafer interconnections 130 are done through row and column interconnects placed at the periphery of the imager area. Thus, each output signal and timing line on the sensor layers are electrically coupled with the interconnects 130 to the column or row circuitry 132 on the circuit layer 120. In the illustrated embodiments, standard CMOS digital and analog circuitry is situated outside the image area on sensor layers 101, 102 and/or the circuit wafer 120.

In the embodiments illustrated in Figures 5 and 6, a color filter array (CFA) 160 is situated over the top sensor layer 102. The silicon portions 152 or the first and second sensor layers 101,102 have different thicknesses T1,T2 so that each layer collects light with in a predetermined range of wavelengths. For instance, the thickness of the sensor layers can be about 0.5 μm to collect predominantly blue light, about 1.3 μm to collect predominantly green light, and/or about 3.0 μm to collect predominantly red light. By using the first and second thicknesses T1, T2 set to collect two predetermined colors, the need for some layers of the CFA 160 are eliminated.

More specifically, the embodiments illustrated in Figures 5 and 6 having two sensor layers 101, 102 with layer thicknesses T1, T2 eliminates the need for two of the layers of the CFA 160. Figures 7 and 8 illustrate examples of two complementary CFAs 160, where Y stands for yellow, M stands for magenta and P stands for panchromatic. The silicon thickness T2 of the top sensor layer 102 is about 2μm in the illustrated embodiments.

The embodiments illustrated in Figures 9 and 10 each include an additional sensor layer 103. In Figure 9, the interlayer connections 130 connect the floating diffusions 144, and in Figure 10, the interlayer connections 130 are made using the row and column circuitry 132. In Figures 9 and 10, the silicon thickness T3 of the third sensor layer is about 0.5 μm so that it collects predominantly blue light, the silicon thickness T2 of the second sensor layer 102 is about 1.3 μm so that it collects predominantly green light, and the silicon thickness T1 of the first sensor layer is about 3 μm so that it collects predominantly red light. Such a sensor does not require wavelength selective filters to detect color, which are known to decrease quantum efficiency.

This structure also allows multiple ways of binning pixels onto a common floating diffusion. Depending on the number of photodiodes 140 within each pixel kernel 150, three or more photodiodes 140 can be connected to the same electrical interconnect 130. This allows multiple ways of binning the pixels 110. For example, as illustrated in Figure 11, the transfer gates 142 for photodiodes B1, G1, and R1 can be activated to transfer charge onto the common floating diffusion 142 and produce a binned panchromatic signal. Similarly, on a single color layer, transfer gates 142 for each photodiode 110 in the pixel kernel 150 can be activated to bin all of the color signals and produce a higher sensitivity output at lower spatial resolution. For example, binning all four of the red pixels R1+R2+R3+R4 functions like a single large (high sensitivity) red pixel. The option also exists to sacrifice spatial resolution for color response in one color plane, but not others. For example, the four red pixels could be binned together, but individual photodiode data preserved in the green channel. Another option would be to bin all photodiodes (for example using all 12 photodiodes in Figure 11 (four blue pixels B1-B4, four green pixels G1-G4, and four red pixels R1-R4) onto the shared floating diffusion 144. This would produce a high sensitivity, low spatial resolution panchromatic signal for the stacked kernel. Color separation in this case would be accomplished by preserving color separation in nearby kernels.

Figure 12 illustrates another embodiment that includes two sensor layers 101,102 and a circuit layer 120 that also contains sensing elements. This structure requires one less wafer as compared to the embodiments illustrated in Figures 9 and 10 while still providing three sensor layers. Thus, the circuit layer 120 includes pixels 110 in addition to support circuitry. The silicon thickness T1,T2,T3 circuit layer 120 and the two sensor layers 101,102 are such that each layer collects light with predetermined ranges of wavelengths. In Figure 12, the interlayer connections 130 are made through the row and column circuitry 132, though in similar embodiments the connections are made through the floating diffusions 144.

Figure 13 illustrates an embodiment having one sensor layer 101 and a circuit layer 120 that also includes sensing elements. The embodiment illustrated in Figure 113 has interlayer connections 130 through the floating diffusions 144, though the connections can alternatively be made through the row and column circuitry as disclosed in other embodiments herein. The sensor layer 101 and the circuit layer 120 each have silicon thicknesses T1,T2 to layer collect light with predetermined ranges of wavelengths. As with the embodiments illustrated in Figures 5 and 6, a complementary CFA 160 such as illustrated in Figures 7 and 8 is provided for filtering the third color.

Figure 14 conceptually illustrates another embodiment having more than three sensing layers 101-N, with each layer having a predetermined thickness for collecting light having corresponding ranges of wavelengths. This structure allows the extension of sensitivity beyond the visible spectrum. The top three layers will be responsible for capturing the light in the visible frequency range as described, for example, in the embodiments illustrated in Figures 9 and 10, while the extra layers N may be used to capture infrared light

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

PARTS LIST

10	light
11	imaging stage
12	lens
13	ND filter block
14	iris block
16	brightness sensor block
18	shutter block
20	image sensor
22	analog signal processor
24	analog to digital (A/D) converter
26	timing generator
28	image sensor stage
30	bus
32	memory
36	digital signal processor (DSP)
38	processing stage
40	exposure controller
50	system controller
52	bus
54	program memory
56	system memory
57	host interface
60	memory card interface
62	socket
64	memory card
70	viewfinder display
72	exposure display
74	user inputs
76	status display
80	video encoder

82	display controller
88	image display
101	first sensor layer
102	second sensor layer
103	third sensor layer
110	pixel
111	first pixel array
112	second pixel array
120	circuit layer
122	support circuitry
124	reset gate
126	source follower input
128	source follower output
130	interlayer connectors
132	row and column circuitry
140	photodiode
142	transfer gate
144	floating diffusion
150	pixel kernel
152	silicon layer
154	metal layer
160	color filter array (CFA)
T1	first thickness
T2	second thickness
T3	third thickness
V_{DD}	voltage supply

CLAIMS:

1. An image sensor, comprising:

a first sensor layer having a first array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion mechanism, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism, the first sensor layer having a thickness to collect light with a first preselected range of wavelengths;

a second sensor layer situated over the first sensor layer, the second sensor layer having a second array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism, the second sensor layer having a thickness to collect light with a second preselected range of wavelengths;

a circuit layer situated below the first sensor layer, the circuit layer having support circuitry for the pixels of the first and second sensor layers; and

interlayer connectors between the pixels of the first and second layers and the support circuitry.

2. The image sensor of claim 1, wherein the circuit layer includes a charge-to-voltage conversion mechanism coupled to the charge-to-voltage mechanisms of the first and second sensor layer.

3. The image sensor of claim 1, wherein the circuit layer further includes an array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism.

4. The image sensor of claim 1, wherein a plurality of photodiodes are connected to a common charge-to-voltage mechanism.

5. The image sensor of claim 1, wherein the circuit layer includes a charge-to-voltage mechanism, and wherein the interlayer connections are connected between charge-to-voltage mechanisms of the first and second sensor layers and the circuit layer.

6. The image sensor of claim 1, further comprising row and column select circuitry that provides the interlayer connections.

7. The image sensor of claim 1, further comprising a color filter array filter situated over the second sensor layer.

8. The image sensor of claim 1, further comprising a third sensor layer situated over the second sensor layer, the third sensor layer having a third array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion mechanism, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism, the third sensor layer having a thickness to collect light with a third preselected range of wavelengths.

9. The image sensor of claim 8, further comprising a fourth sensor layer situated over the third sensor layer, the third sensor layer having a thickness to collect light with a fourth preselected range of wavelengths, wherein at least one of the first, second, third or fourth preselected ranges of wavelengths are outside the visible frequency range.

10. The image sensor of claim 1, wherein the first sensor layer and the circuit layer are combined in a single layer having the first array of pixels and the support circuitry.

11. An image sensor, comprising:

a first sensor layer having a first array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion mechanism, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism, the first sensor layer having a thickness to collect light with a first preselected range of wavelengths;

a circuit layer situated below the first sensor layer, the circuit layer having a second array of pixels, each pixel including a photodetector for collecting charge in response to incident light, a charge-to-voltage conversion, and a transfer gate for selectively transferring charge from the photodetector to the charge-to-voltage mechanism, support circuitry for the first and second arrays of pixels; and

wherein the circuit layer has a thickness to collect light with a second preselected range of wavelengths;

interlayer connectors between the pixels of the first and second layers and the support circuitry;

a color filter array situated over the first sensor layer.

12. The image sensor of claim 11, wherein the interlayer connections are connected between the charge-to-voltage mechanisms of the first sensor layer and the circuit layer.

13. The image sensor of claim 11, further comprising row and column select circuitry that provides the interlayer connections.

14. A method of binning pixels of an image sensor, comprising:

providing a first pixel kernel situated in a first layer;

providing a second pixel kernel situated in a second layer above the first layer;

transferring a first charge from a pixel of the first pixel kernel to a first charge-to-voltage mechanism;

transferring a second charge from a pixel of the second pixel kernel to a second charge-to-voltage mechanism; and

transferring the first and second charges to a common charge-to-voltage mechanism.

15. The method of claim 14, further comprising:

providing a third pixel kernel situated in a third layer above the second layer;

transferring a third charge from a pixel of the third pixel kernel to a third charge-to-voltage mechanism; and

transferring the first, second and third charges to the common charge-to-voltage mechanism.

16. The method of claim 14, wherein transferring the first charge includes transferring a plurality of charges from a plurality of pixels to the first charge-to-voltage mechanism.

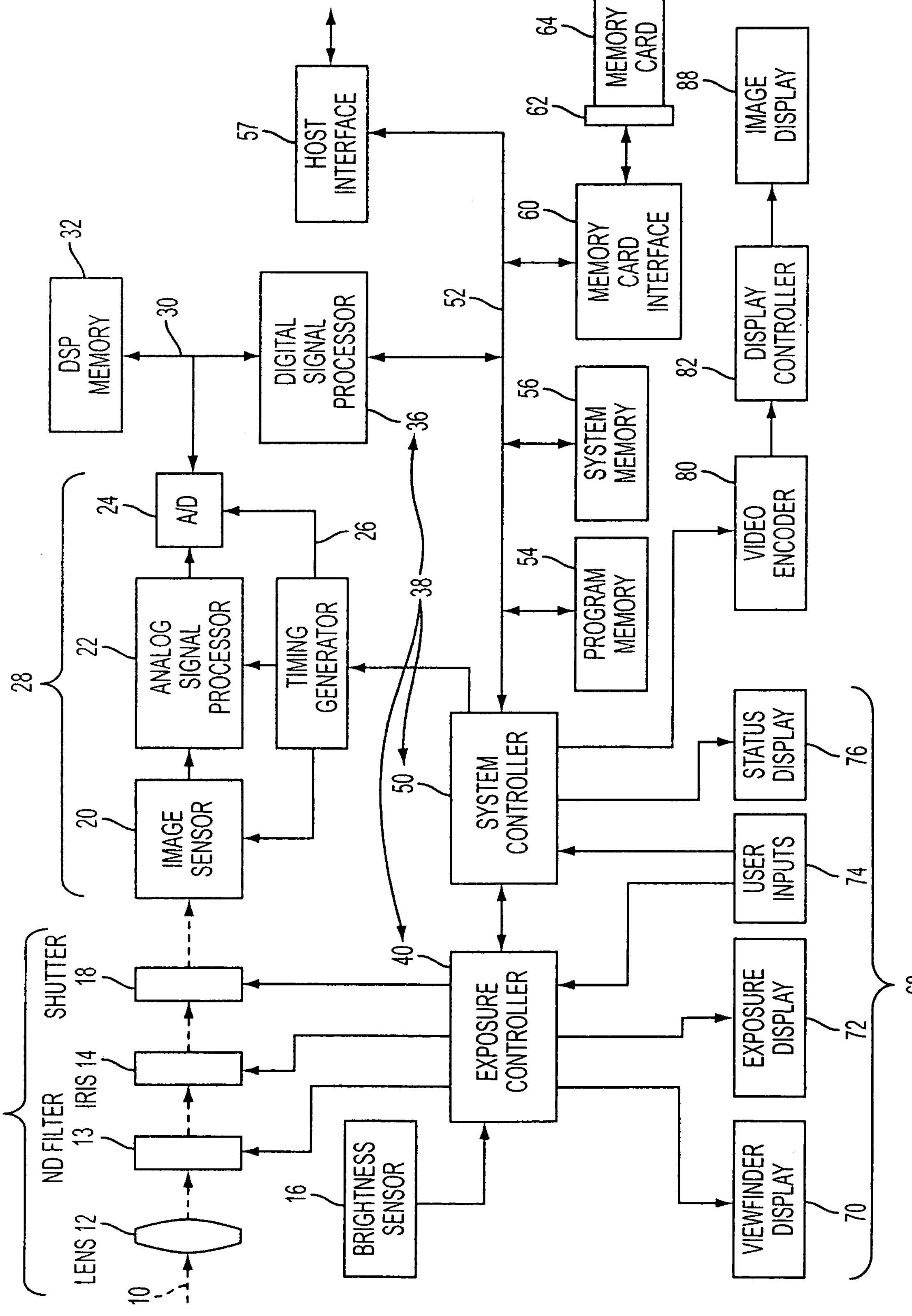

DSP MEMORY
32
30
DIGITAL SIGNAL PROCESSOR
36
HOST INTERFACE
57
MEMORY CARD
64
62
IMAGE DISPLAY
88
MEMORY CARD INTERFACE
60
52
SYSTEM MEMORY
56
PROGRAM MEMORY
54
DISPLAY CONTROLLER
82
VIDEO ENCODER
80
A/D
24
26
ANALOG SIGNAL PROCESSOR
22
TIMING GENERATOR
28
38
IMAGE SENSOR
20
SYSTEM CONTROLLER
50
STATUS DISPLAY
76
USER INPUTS
74
SHUTTER
18
IRIS 14
ND FILTER
13
LENS 12
10
40
EXPOSURE CONTROLLER
EXPOSURE DISPLAY
72
68
BRIGHTNESS SENSOR
16
VIEWFINDER DISPLAY
70

FIG. 1

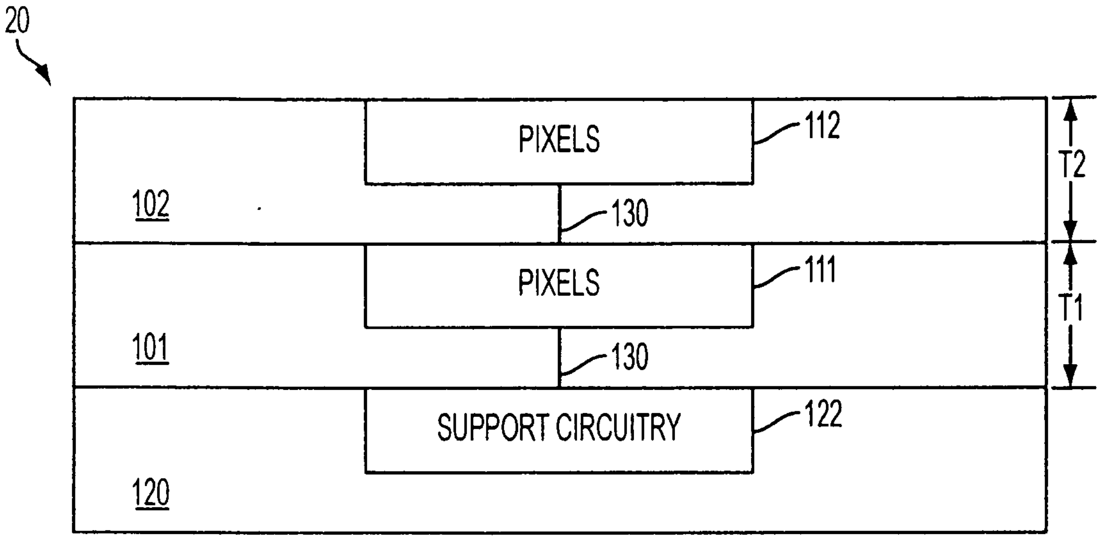


FIG. 2

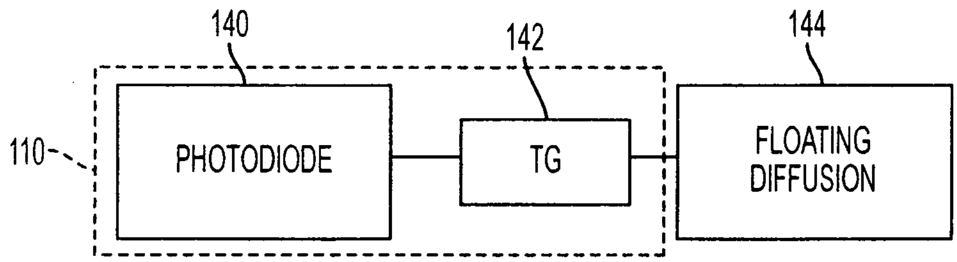


FIG. 3

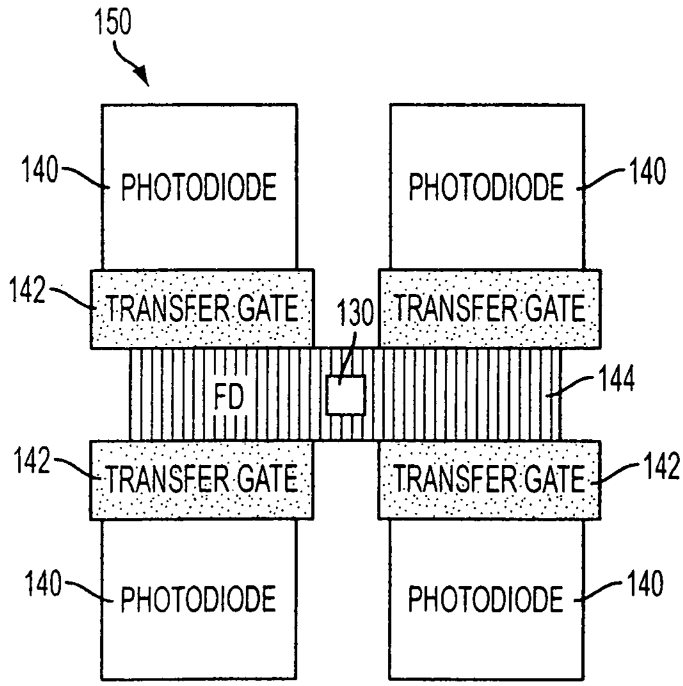


FIG. 4A

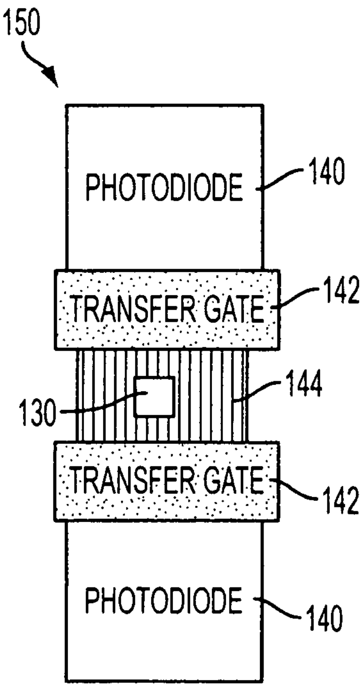
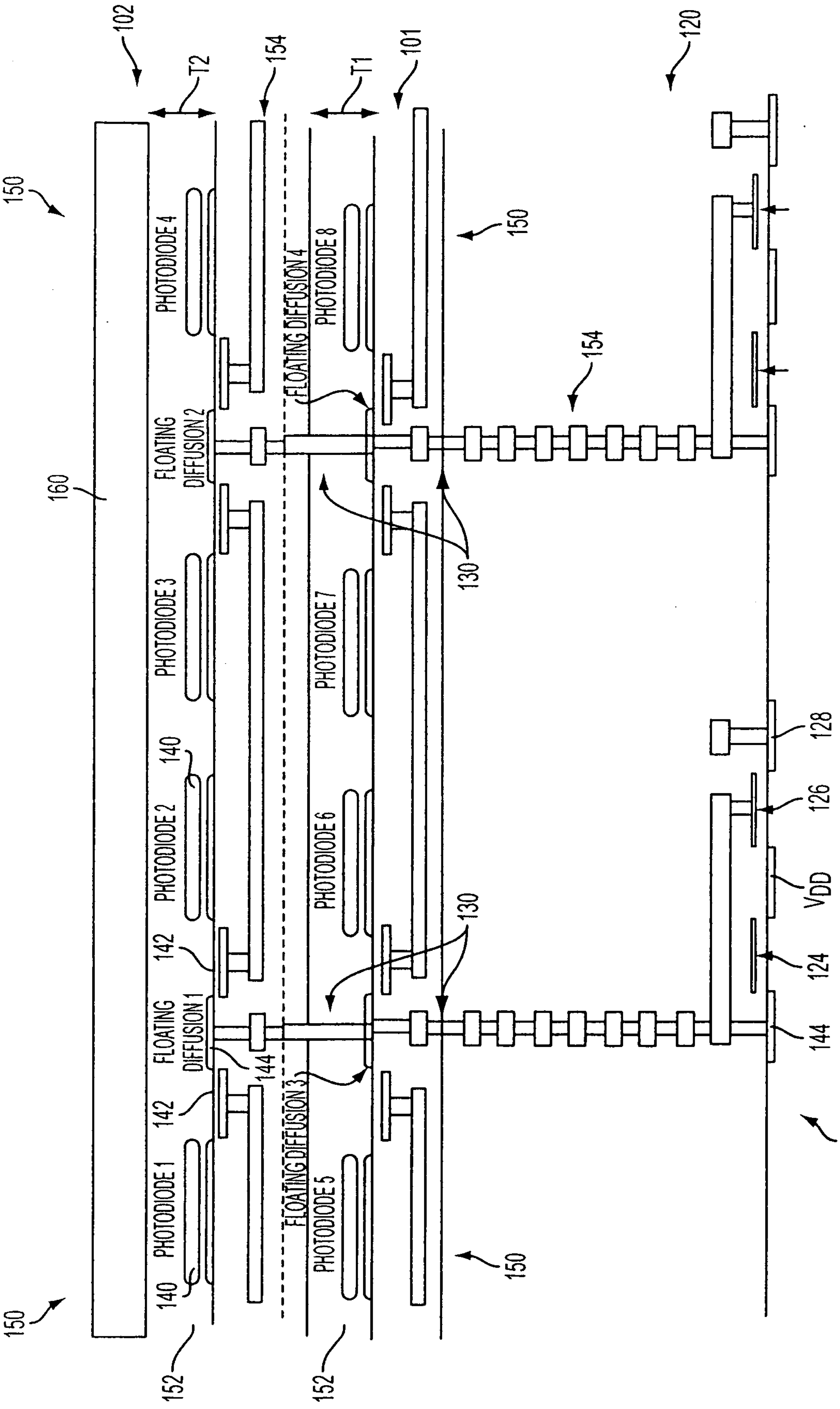


FIG. 4B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T2
154
T1
101
120
150
160
PHOTODIODE 1
PHOTODIODE 2
PHOTODIODE 3
PHOTODIODE 4
PHOTODIODE 5
PHOTODIODE 6
PHOTODIODE 7
PHOTODIODE 8
FLOATING DIFFUSION 1
FLOATING DIFFUSION 2
FLOATING DIFFUSION 3
FLOATING DIFFUSION 4
140
142
144
130
152
124
V_{DD}
126
128
122

FIG. 5

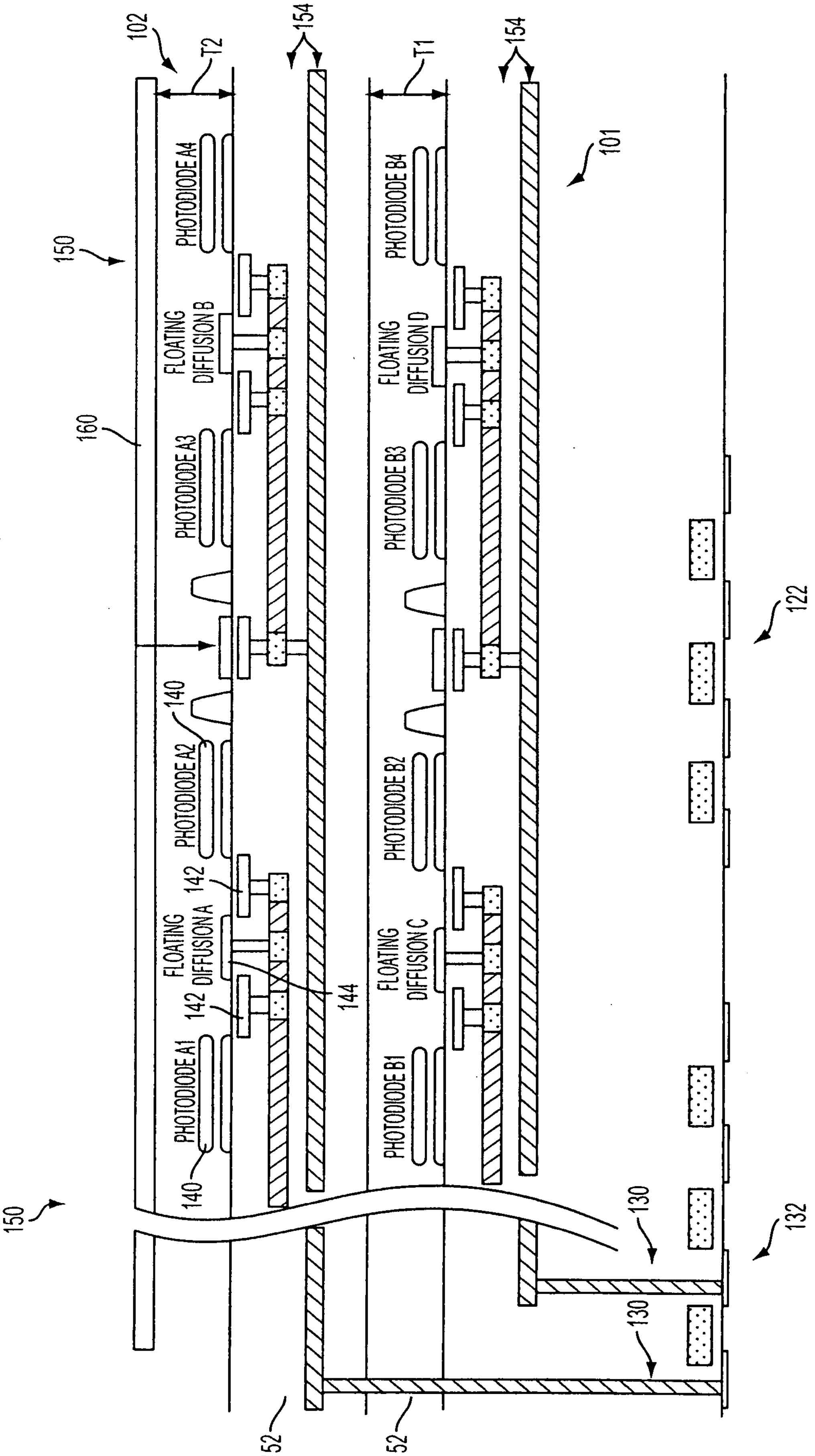

102
T2
154
T1
154
101
150
160
PHOTODIODE A4
FLOATING DIFFUSION B
PHOTODIODE A3
PHOTODIODE A2
140
142
FLOATING DIFFUSION A
142
144
PHOTODIODE A1
140
PHOTODIODE B4
FLOATING DIFFUSION D
PHOTODIODE B3
PHOTODIODE B2
FLOATING DIFFUSION C
PHOTODIODE B1
150
130
130
122
132
152
152

FIG. 6

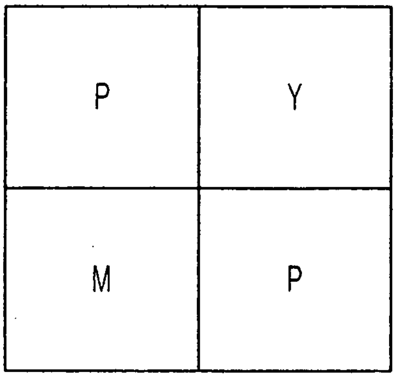


FIG. 7

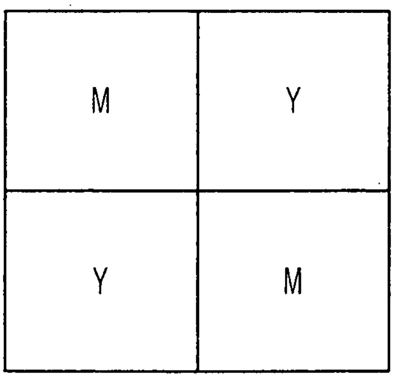
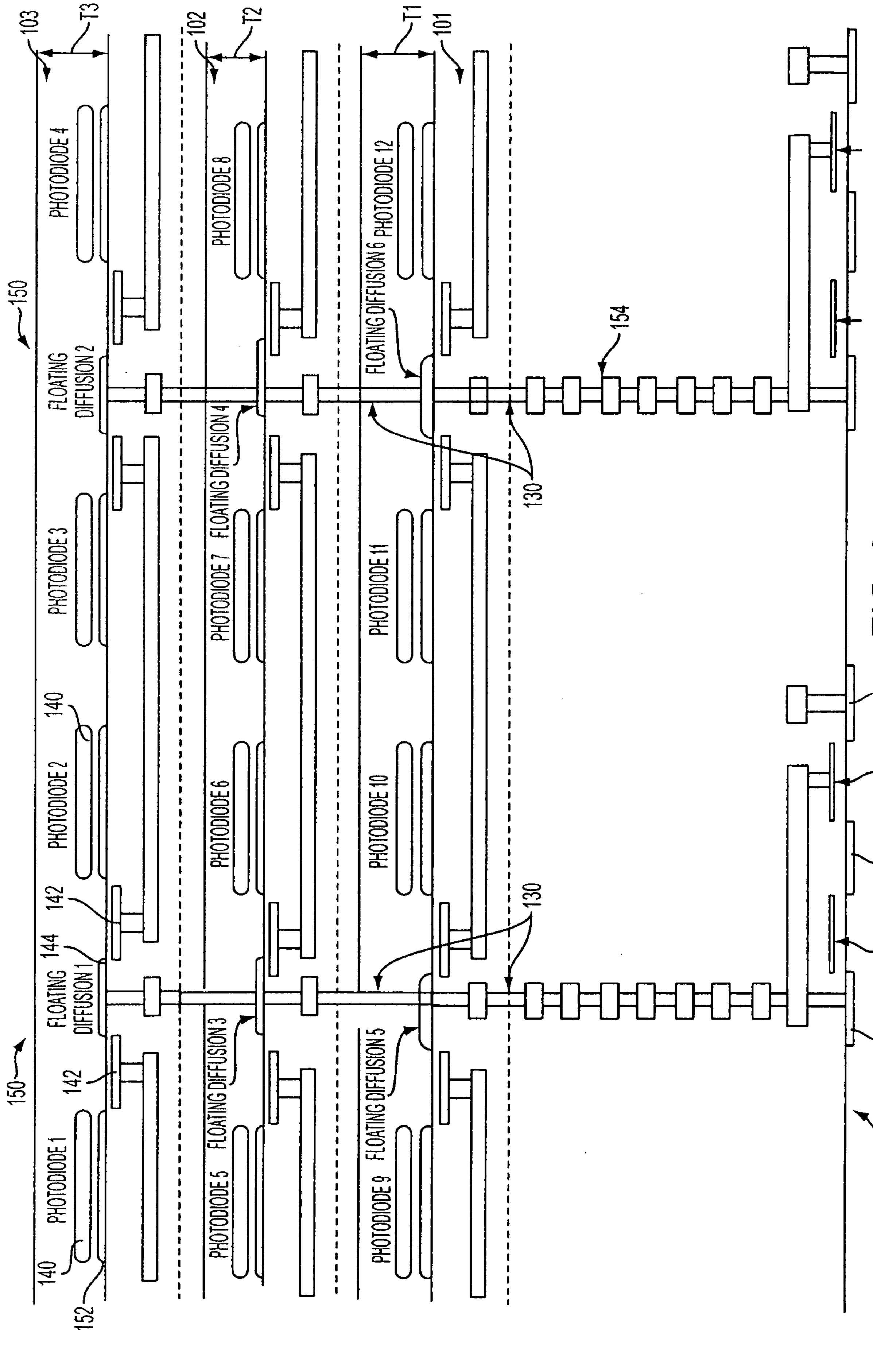


FIG. 8


103
T3
102
T2
T1
101
120
150
PHOTODIODE 4
PHOTODIODE 8
PHOTODIODE 12
FLOATING DIFFUSION 6
FLOATING DIFFUSION 2
FLOATING DIFFUSION 4
154
130
PHOTODIODE 3
PHOTODIODE 7
PHOTODIODE 11
140
PHOTODIODE 2
PHOTODIODE 6
PHOTODIODE 10
128
126
V_{DD}
142
144
FLOATING DIFFUSION 1
FLOATING DIFFUSION 3
FLOATING DIFFUSION 5
124
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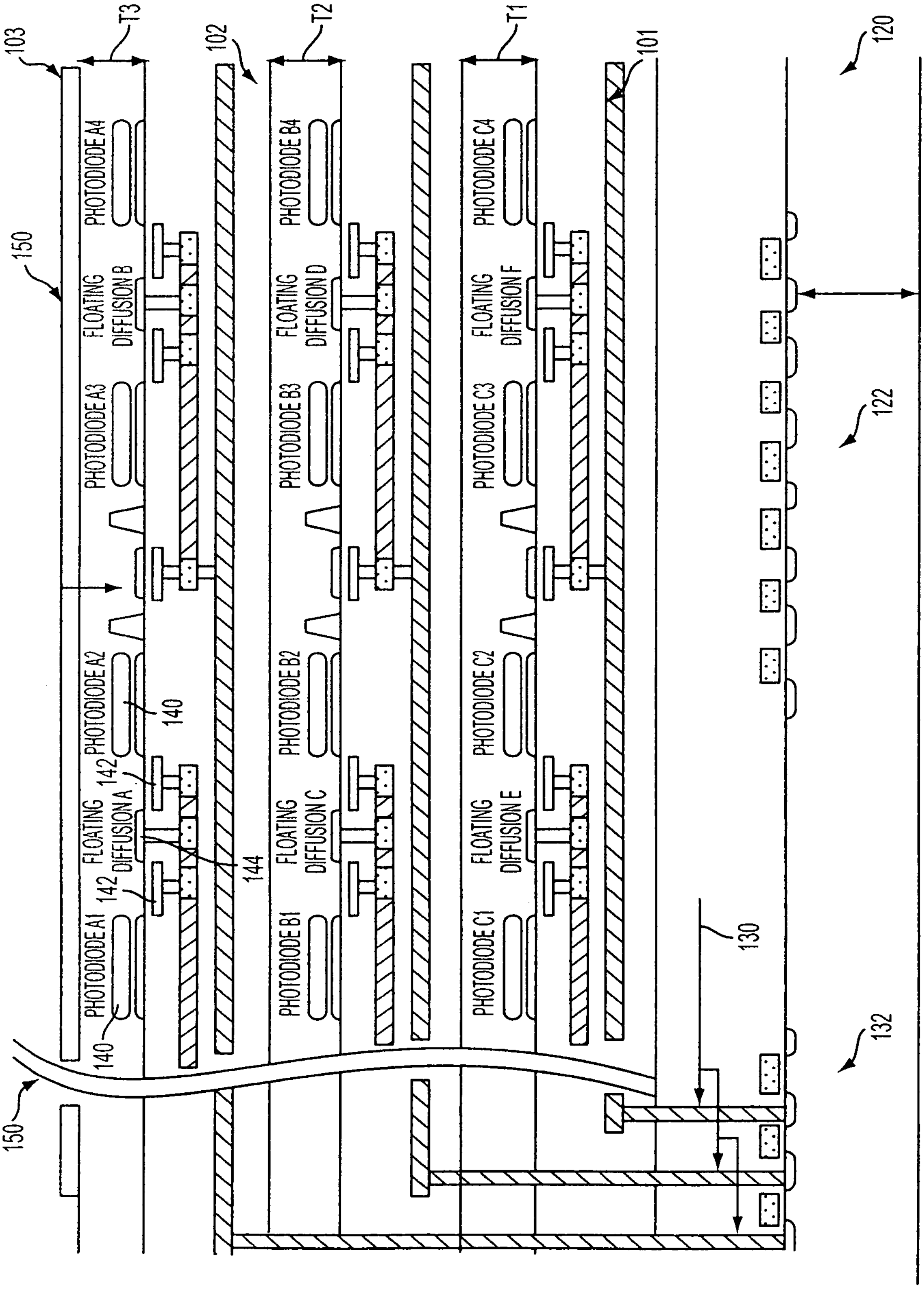
150
142
122
PHOTODIODE 1
PHOTODIODE 5
PHOTODIODE 9
140
152

FIG. 9


103
T3
102
T2
T1
101
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PHOTODIODE A4
FLOATING DIFFUSION B
PHOTODIODE A3
PHOTODIODE A2
140
142
FLOATING DIFFUSION A
144
PHOTODIODE A1
PHOTODIODE B4
FLOATING DIFFUSION D
PHOTODIODE B3
PHOTODIODE B2
FLOATING DIFFUSION C
PHOTODIODE B1
PHOTODIODE C4
FLOATING DIFFUSION F
PHOTODIODE C3
PHOTODIODE C2
FLOATING DIFFUSION E
PHOTODIODE C1
122
130
132

FIG. 10

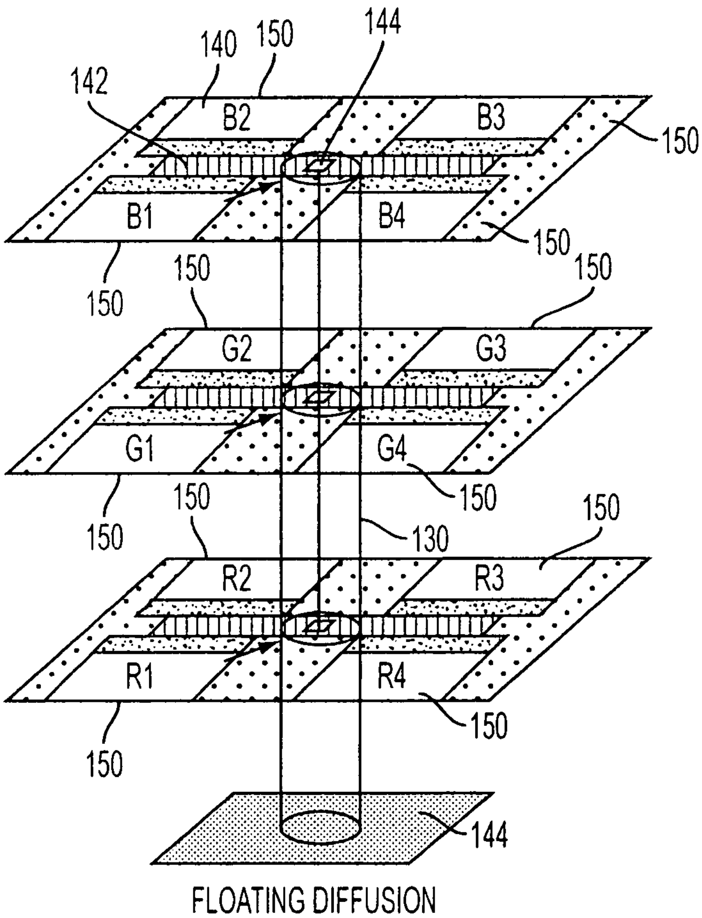

144
140
150
142
B2
B3
150
B1
B4
150
150
150
150
G2
G3
G1
G4
150
150
150
130
150
R2
R3
R1
R4
150
150
144
FLOATING DIFFUSION

FIG. 11

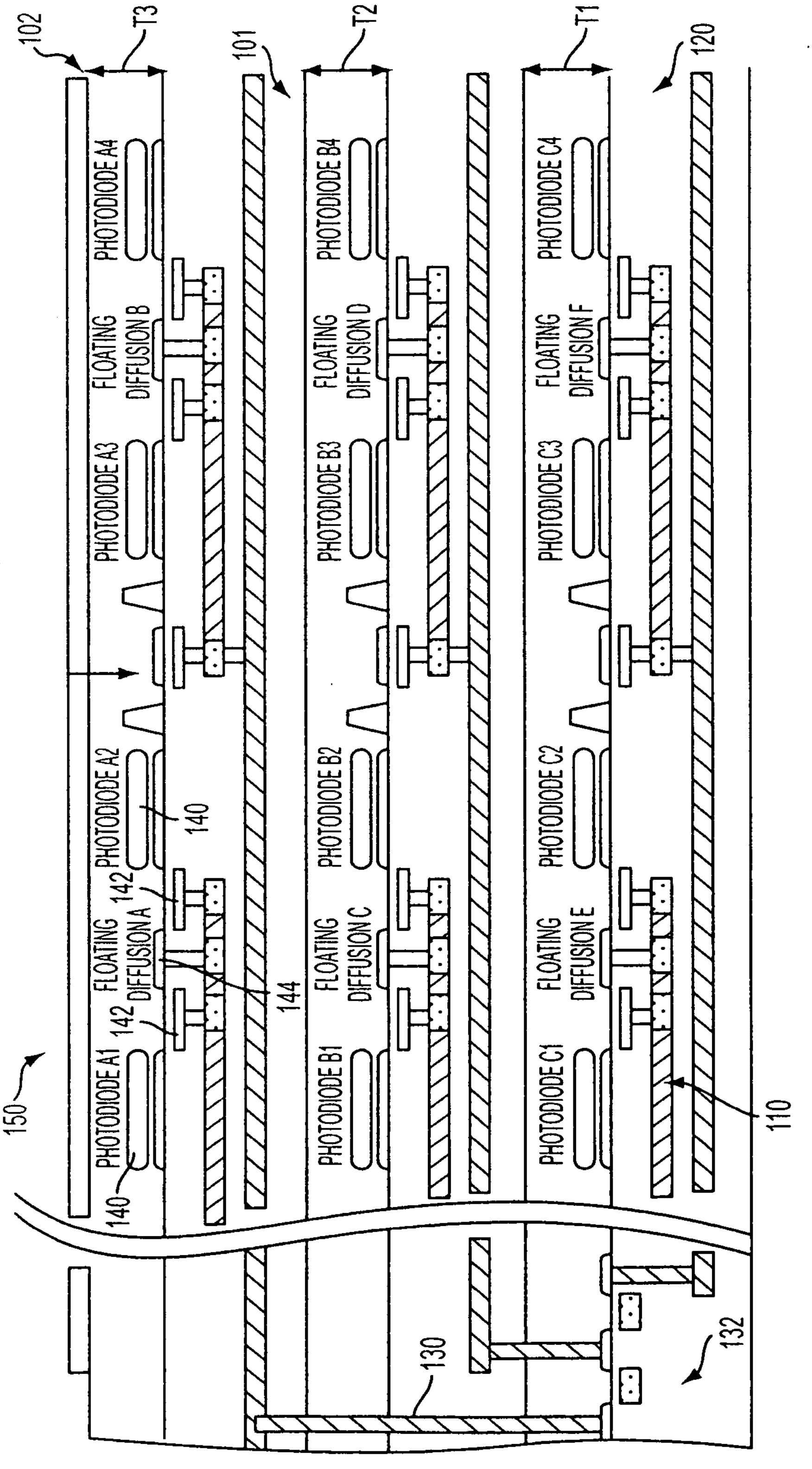
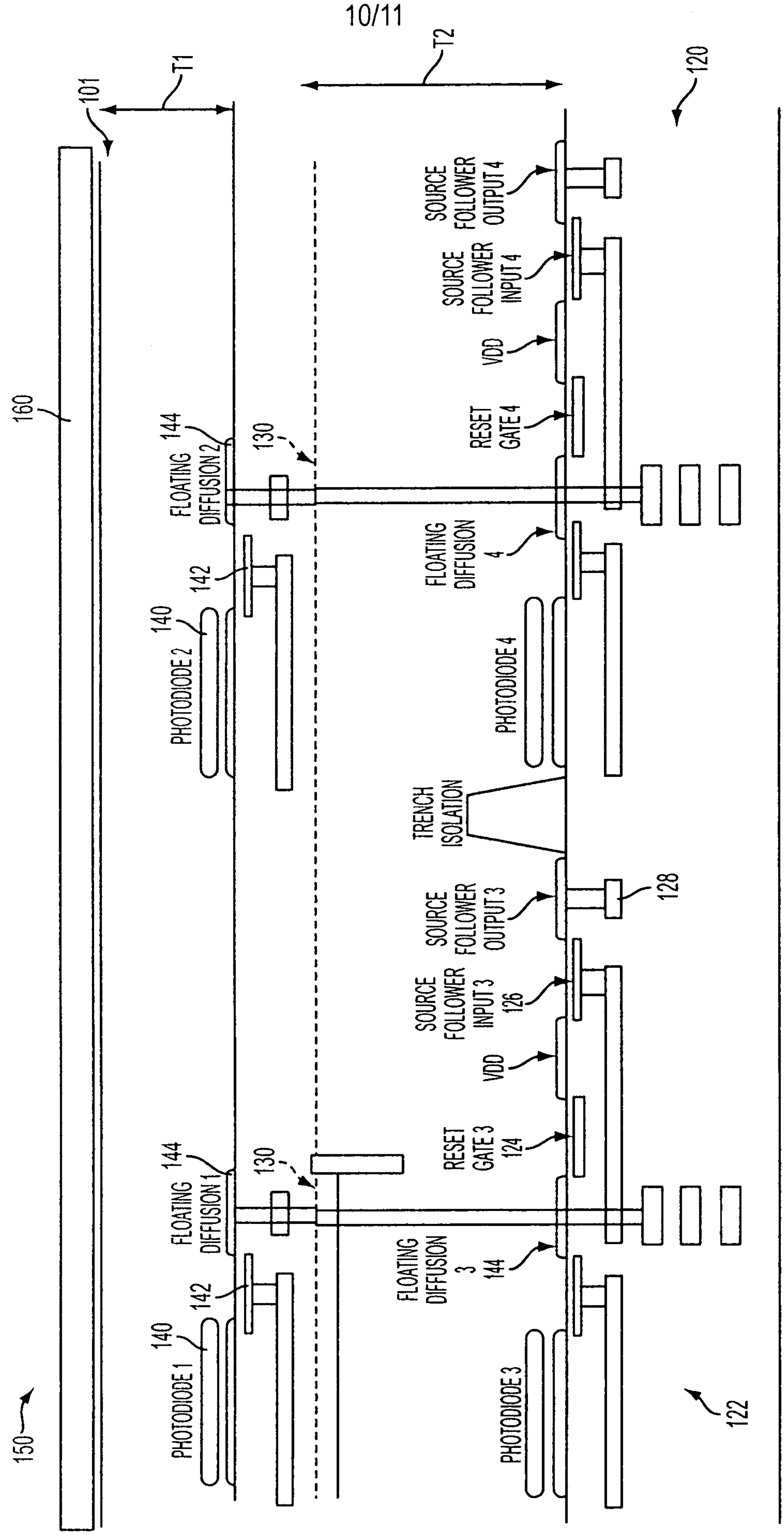

102
T3
101
T2
T1
120
PHOTODIODE A4
FLOATING DIFFUSION B
PHOTODIODE A3
PHOTODIODE A2
140
142
FLOATING DIFFUSION A
142
144
PHOTODIODE A1
140
150
PHOTODIODE B4
FLOATING DIFFUSION D
PHOTODIODE B3
PHOTODIODE B2
FLOATING DIFFUSION C
PHOTODIODE B1
PHOTODIODE C4
FLOATING DIFFUSION F
PHOTODIODE C3
PHOTODIODE C2
FLOATING DIFFUSION E
PHOTODIODE C1
110
130
132

FIG. 12



T1
T2
101
120
160
150
122
SOURCE FOLLOWER OUTPUT 4
SOURCE FOLLOWER INPUT 4
VDD
RESET GATE 4
FLOATING DIFFUSION 2
144
130
142
140
PHOTODIODE 2
FLOATING DIFFUSION 4
PHOTODIODE 4
TRENCH ISOLATION
SOURCE FOLLOWER OUTPUT 3
128
SOURCE FOLLOWER INPUT 3
126
VDD
RESET GATE 3
124
FLOATING DIFFUSION 1
144
130
142
140
PHOTODIODE 1
FLOATING DIFFUSION 3
144
PHOTODIODE 3

FIG. 13

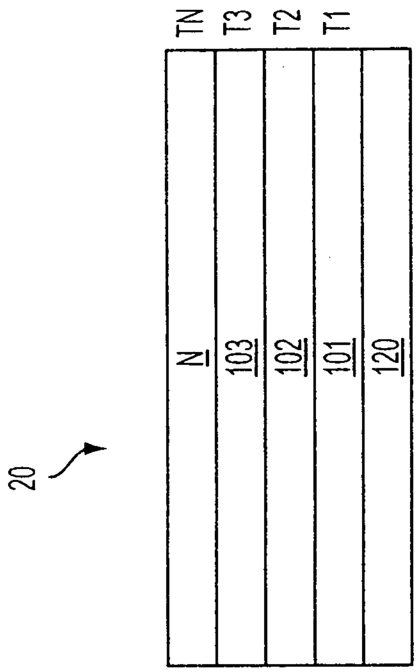


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/004051

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 10 284714 A (TOSHIBA CORP) 23 October 1998 (1998-10-23)	1,3,6,8,10
Y	paragraphs [0033] - [0035] figures 1-5	2,4,5,7,9,11-16
Y	US 2002/033892 A1 (MONOI MAKOTO [JP]) 21 March 2002 (2002-03-21) figure 6	2,4,5,14-16
Y	FR 2 888 989 A (ST MICROELECTRONICS SA [FR]) 26 January 2007 (2007-01-26)	7
A	page 9, line 28 - page 11, line 34 page 17, lines 13-18 page 12, lines 30-35	1-6,8-16

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 October 2009	04/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Markmann, Markus

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/004051

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/125222 A1 (BRADSKI GARY R [US] ET AL) 1 July 2004 (2004-07-01) paragraphs [0007] - [0013] figure 1	9
Y	US 2008/083939 A1 (GUIDASH ROBERT M [US]) 10 April 2008 (2008-04-10) paragraphs [0031] - [0036], [0040]; figures 2,5	1-16
Y	US 2005/205901 A1 (SUZUKI NOBUO [JP]) 22 September 2005 (2005-09-22) paragraphs [0009], [0066] - [0070] figure 5	1-16
A	JP 2001 339057 A (KOYANAGI MITSUMASA; FUJI XEROX CO LTD) 7 December 2001 (2001-12-07) abstract; figure 1	3,10
A	EP 1 628 348 A (HAMAMATSU PHOTONICS KK [JP]) 22 February 2006 (2006-02-22) paragraphs [0028] - [0041]	1-16
A	WO 2007/105478 A (KOYANAGI MITSUMASA [JP]) 20 September 2007 (2007-09-20) abstract; figures 28,29	1-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/004051

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
JP 10284714	A	23-10-1998	NONE		
US 2002033892	A1	21-03-2002	JP 4031901	B2	09-01-2008
			JP 2002043556	A	08-02-2002
			US 2005270595	A1	08-12-2005
FR 2888989	A	26-01-2007	US 2007018075	A1	25-01-2007
US 2004125222	A1	01-07-2004	AU 2003297017	A1	29-07-2004
			WO 2004061966	A1	22-07-2004
US 2008083939	A1	10-04-2008	EP 2067171	A2	10-06-2009
			WO 2008045356	A2	17-04-2008
US 2005205901	A1	22-09-2005	JP 2005268479	A	29-09-2005
JP 2001339057	A	07-12-2001	JP 3713418	B2	09-11-2005
EP 1628348	A	22-02-2006	CN 1795559	A	28-06-2006
			WO 2004105137	A1	02-12-2004
			KR 20060011845	A	03-02-2006
			US 2007181780	A1	09-08-2007
WO 2007105478	A	20-09-2007	JP 2007228460	A	06-09-2007