United States Patent

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[54] **PRINTER CONTROL SYSTEM**
11 Claims, 9 Drawing Figs.

[52] **U.S. Cl.** **340/172.5, 101/93**
[51] **Int. Cl.** **G06k 15/08, G06f 3/12**
[50] **Field of Search** 340/172.5; 101/93

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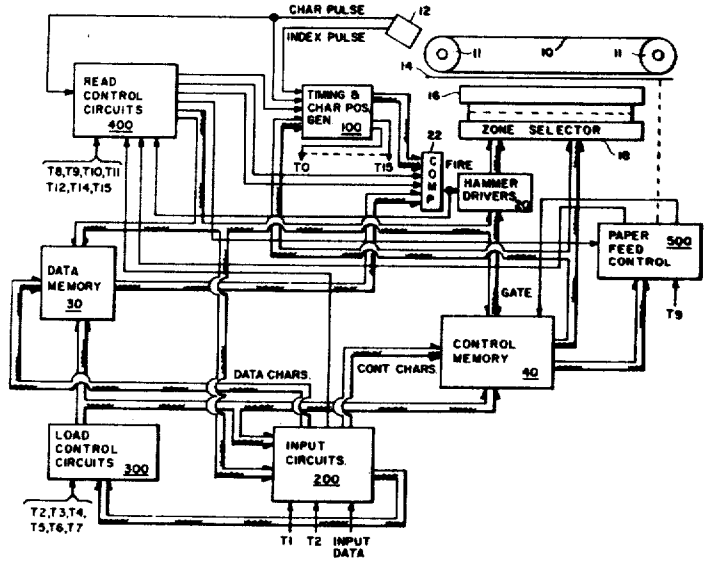
ABSTRACT: A telecommunications line-printer employs a segmented line print control and data buffering system wherein the serially received data and format control characters are temporarily stored in data groups corresponding to segments of a print line. Each group is scanned during printout operations until all data in the group have been printed. A switching matrix connects hammer driver circuits only to hammers in the line segment being printed, thus conserving hardware by time-sharing the drivers. Each data group has a control character defining format control operations, which operations are executed before printing of the group begins. In ordinary circumstances, each format control character occurring at the input opens a new data group to receive the next data characters, regardless of whether the previous group was completely filled. However, in "short line" situations memory is conserved by not closing the group until it is full and the rate of extraction of data from the memory is increased by temporarily suspending the performance of format operations. This preserves realtime printing while insuring against loss of input data. In short-line situations, received format control characters are ignored by the format control means and instead trigger the printing of a special character indicating that a format operation was deleted.



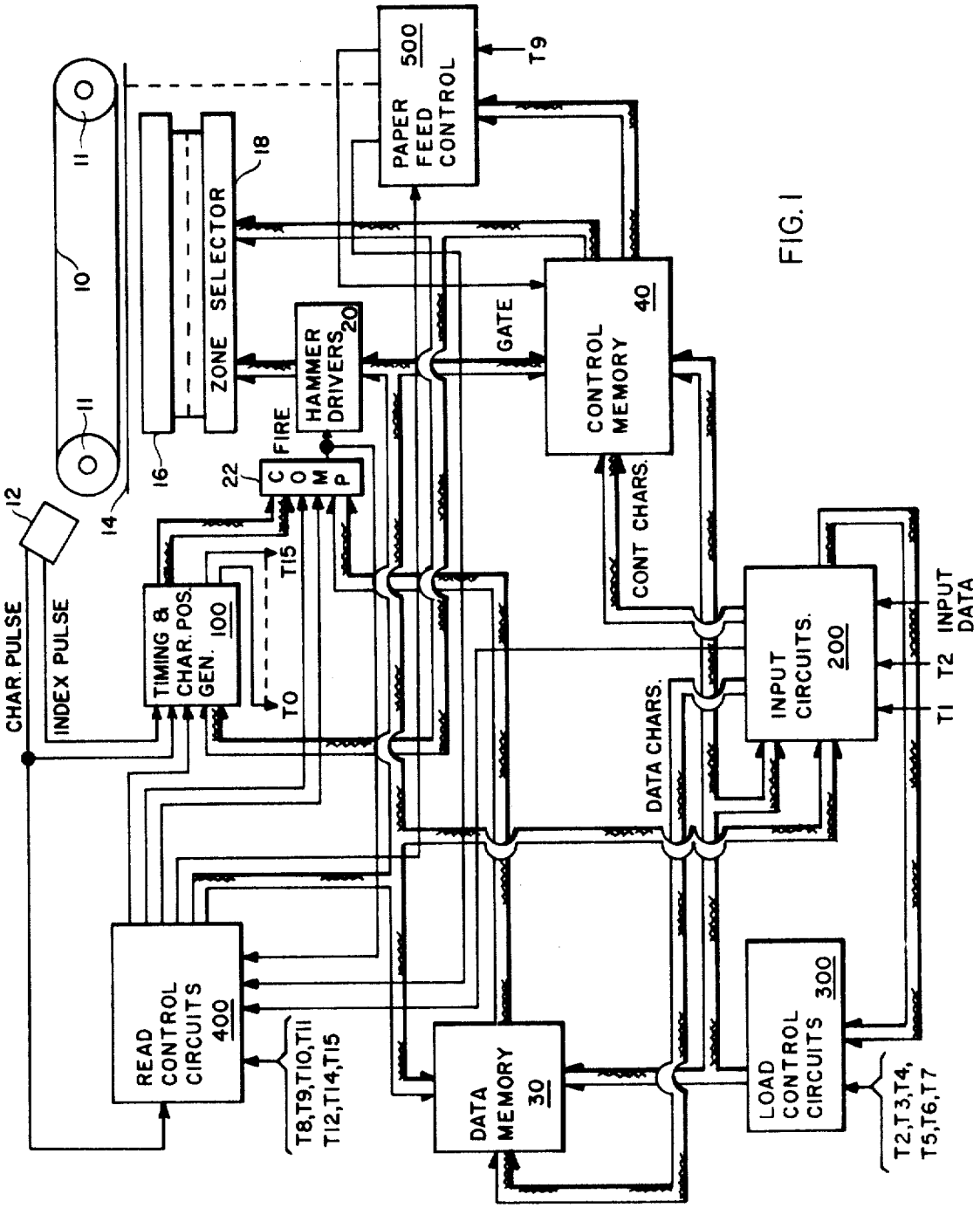


FIG. 1

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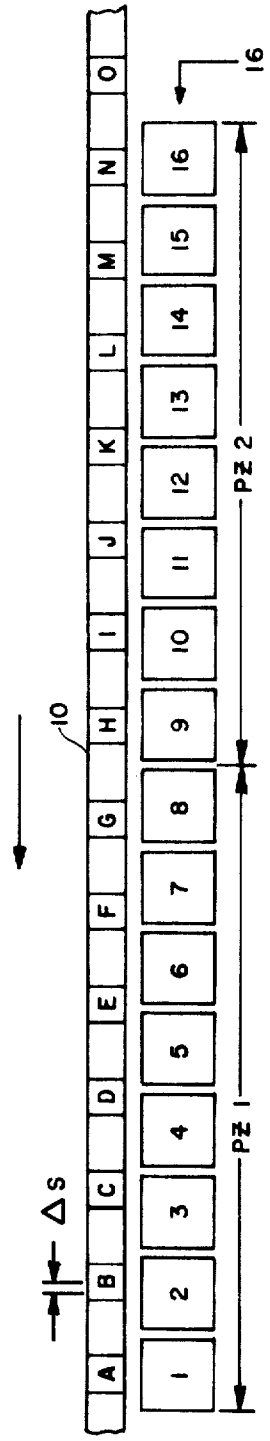
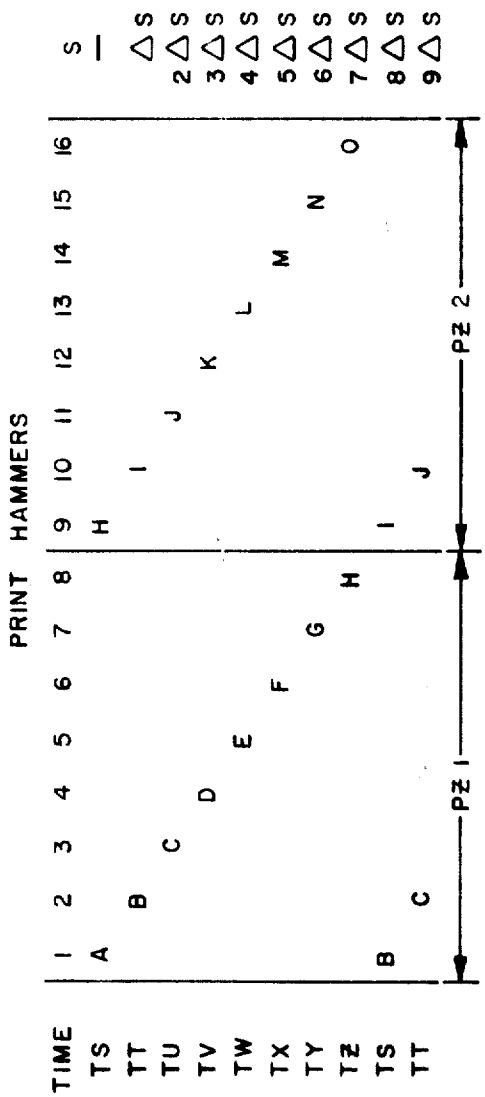

A B C D E F G H I J K L M N O
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
10
16
PZ 1
PZ 2
ΔS

FIG.6


PRINT HAMMERS
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
TIME
TS
TT
TU
TV
TW
TX
TY
TZ
TS
TT
S
ΔS
2ΔS
3ΔS
4ΔS
5ΔS
6ΔS
7ΔS
8ΔS
9ΔS
PZ 1
PZ 2

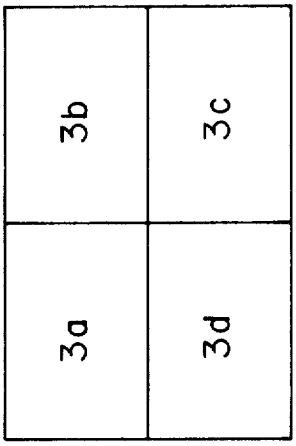

3a
3b
3c
3d

FIG. 2

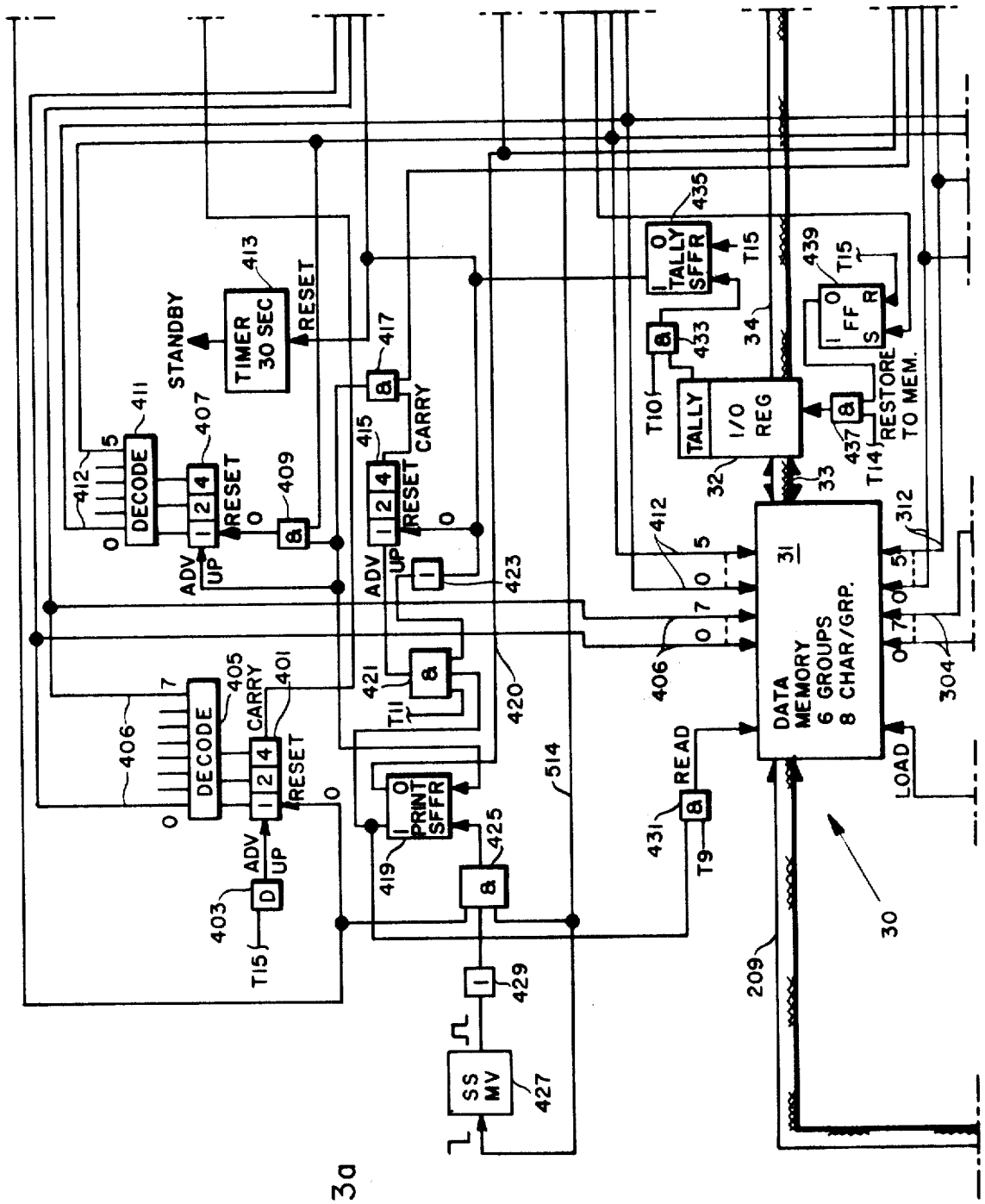

DECODE
STANDBY
TIMER 30 SEC
RESET
CARRY
ADV
UP
DATA MEMORY 6 GROUPS 8 CHAR/GRP.
TALLY I/O REG
TALLY SFFR
PRINT SFFR
READ
LOAD
RESTORE TO MEM.
SS MV
FF
30
209
304
312
401
403
405
406
407
409
411
412
413
415
417
419
420
421
423
425
427
429
431
433
434
435
437
439
514
T9
T10
T11
T14
T15

FIG. 3a

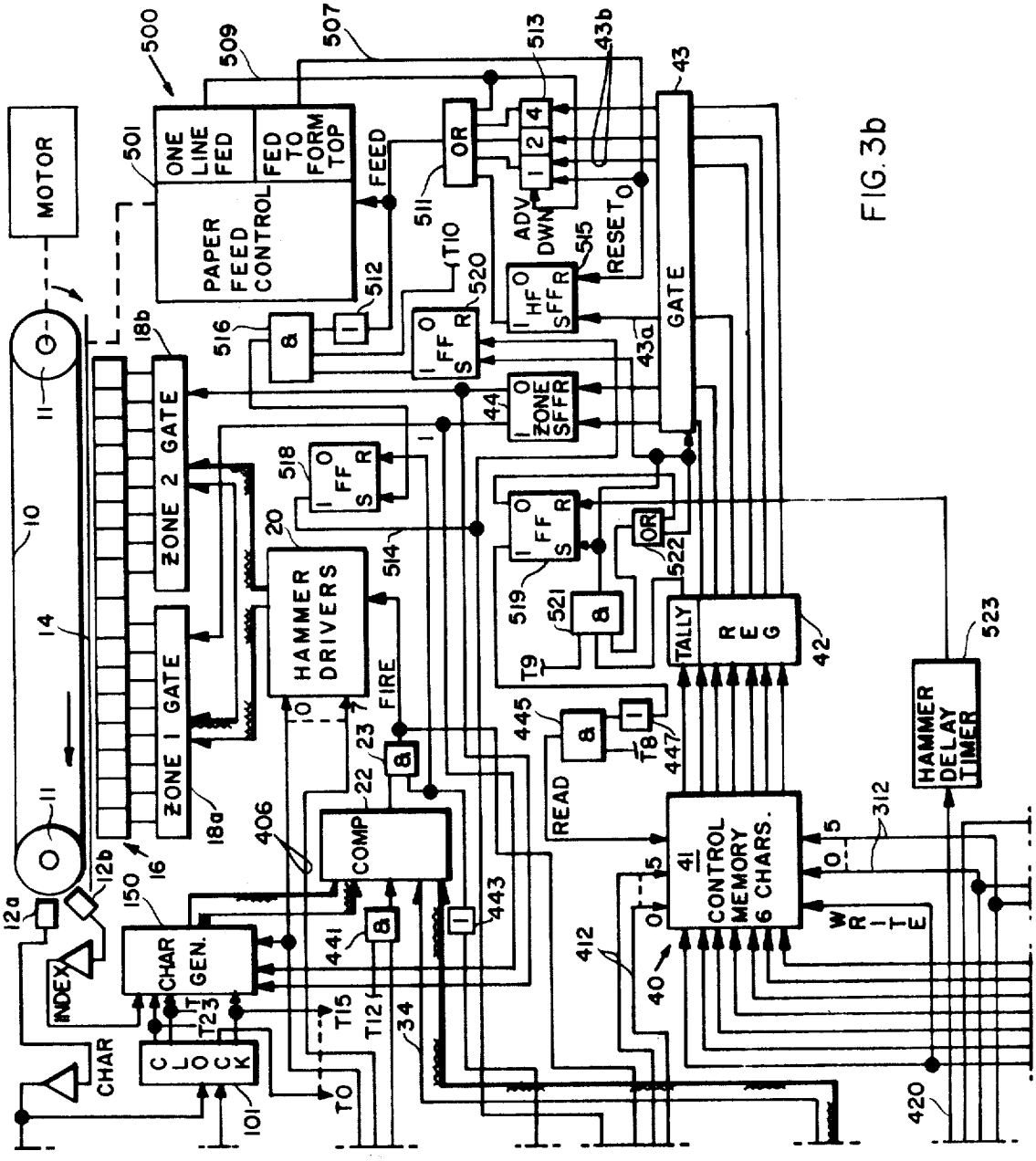
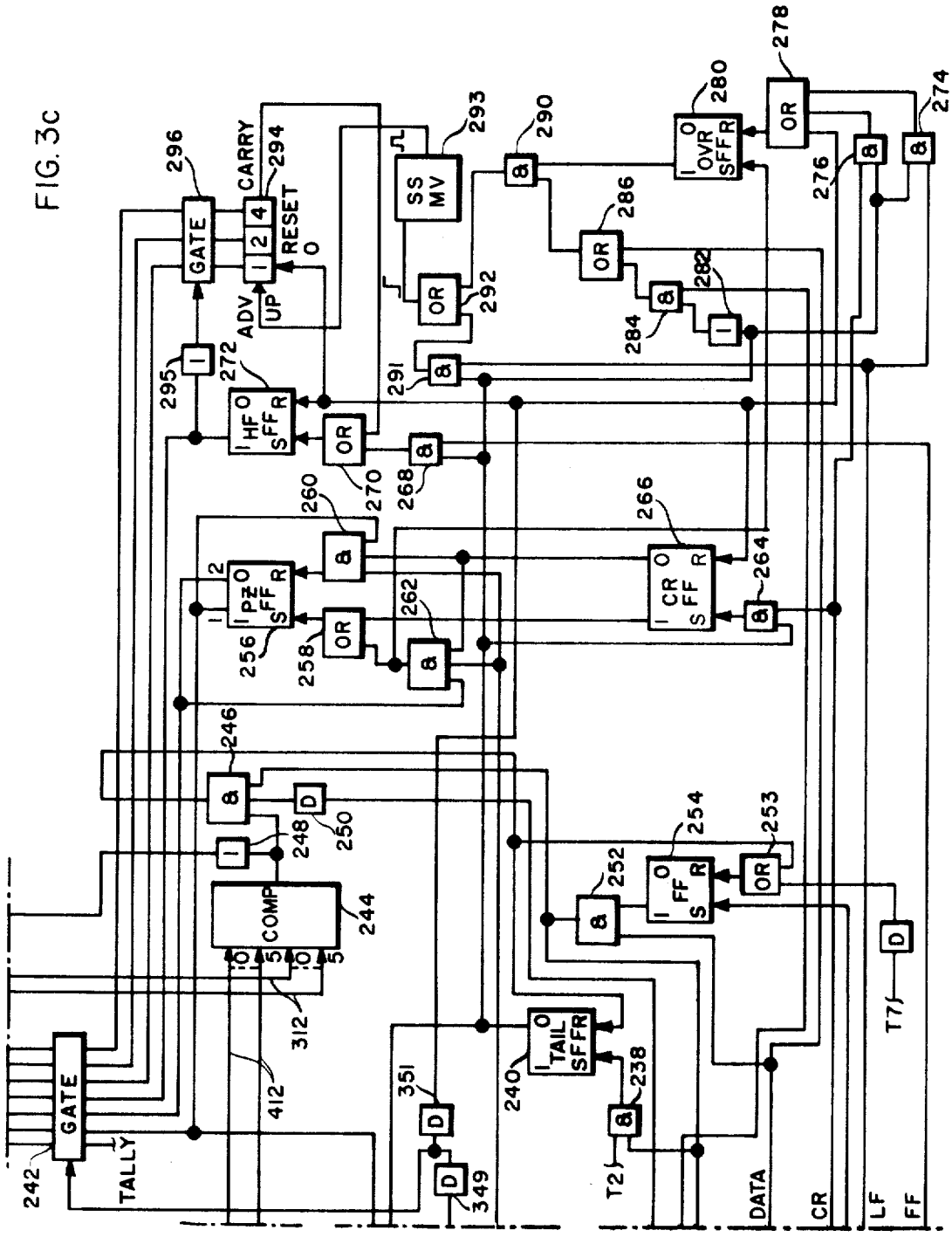

MOTOR
PAPER FEED CONTROL
ONE LINE FED
FED TO FORM TOP
FEED
ZONE 2 GATE
ZONE 1 GATE
HAMMER DRIVERS
FIRE
CHAR GEN.
CLOCK
INDEX
CHAR
COMP
READ
WRITE
TALLY
REG
GATE
OR
ADV
DWN
RESET
HF FF
ZONE FF
HAMMER DELAY TIMER
41 CONTROL MEMORY 6 CHARS.
TO

FIG. 3b

FIG. 3c


GATE
TALLY
242
412
COMP
244
312
246
248
250
PZ
HF
CR
OVR
TAIL
FF
SS MV
GATE
CARRY
RESET
ADV
UP
OR
&
D
T2
T7
DATA
CR
LF
FF

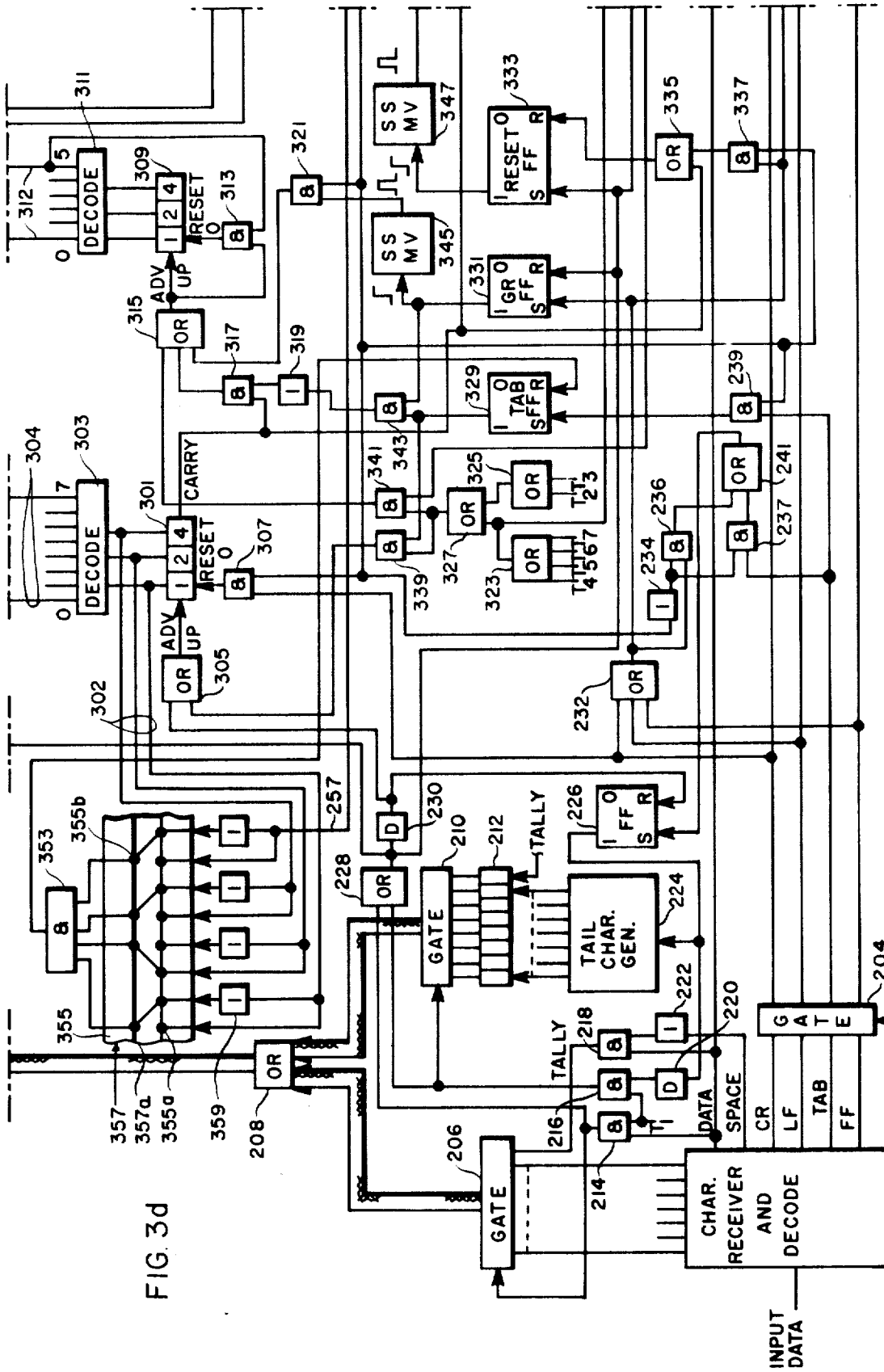

DECODE
RESET
ADV
UP
CARRY
OR
GATE
TAIL CHAR. GEN.
TALLY
SS MV
RESET FF
GR FF
TAB FF
CHAR. RECEIVER AND DECODE
INPUT DATA
CR
LF
TAB
FF
SPACE
DATA
GATE

FIG. 3d

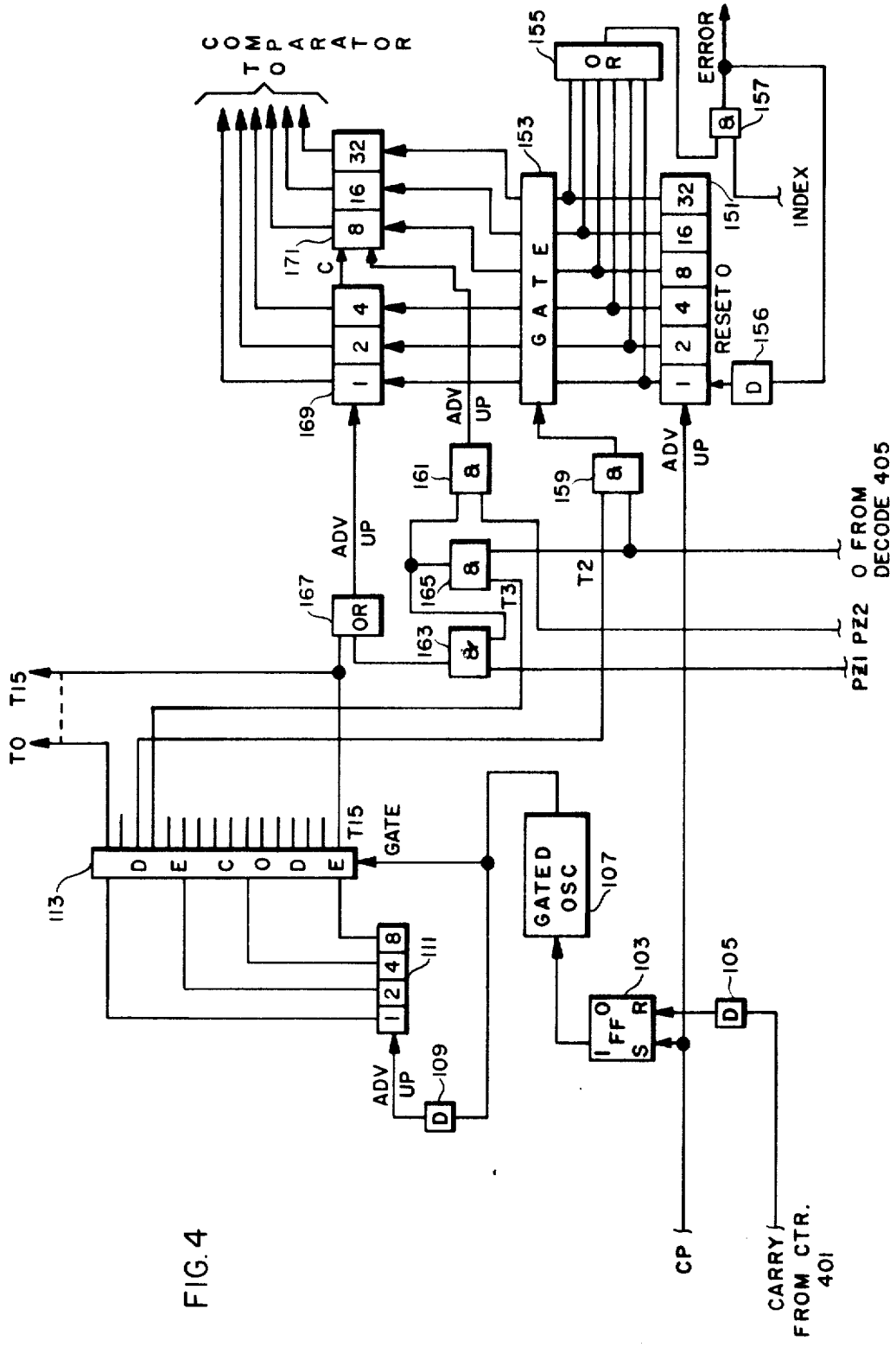
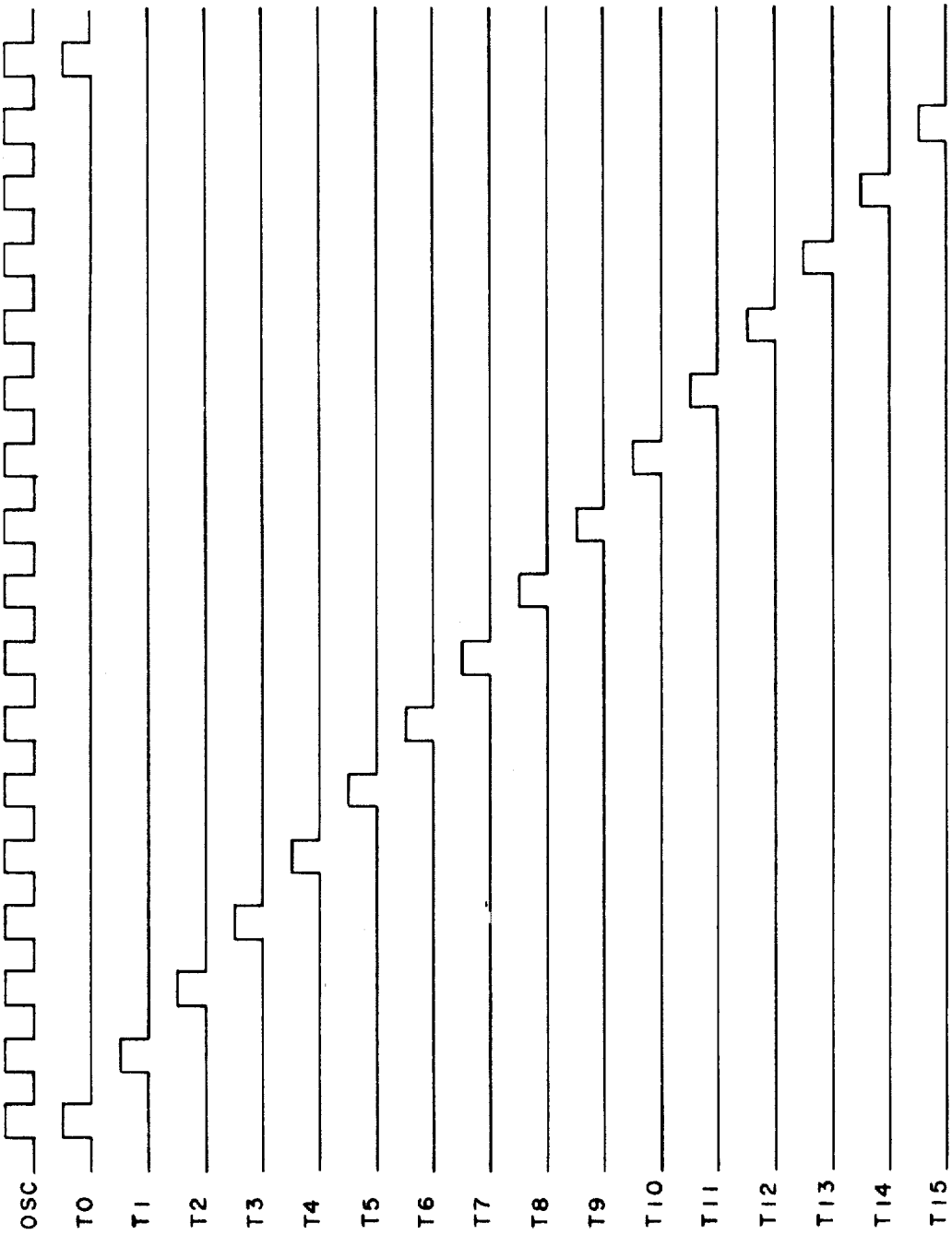

COMPARATOR
32
16
8
4
2
1
171
C
169
153
GATE
155
OR
ERROR
157
INDEX
151
RESET 0
156
D
ADV
UP
161
159
165
T2
T3
167
OR
163
T0 T15
T15 GATE
DECODE
113
111
109
GATED OSC
107
103
FF
105
CP
CARRY FROM CTR. 401
PZ1 PZ2 0 FROM DECODE 405

FIG. 4

FIG.5



PRINTER CONTROL SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to a system for controlling a high speed line printer and, more particularly, to a system for controlling a teleprinter adapted both to receive message and format control data from a communications link and to print the message in accordance with the specified format in real time.

The most practical and common type of digital telecommunication involves transmitting message data in serial form over a single transmission channel. Control data must necessarily be interspersed among the message data to enable the print apparatus at the receiving station to arrange the message in accordance with its sending format. Common control commands are: carriage return (begin a new line of print), single line feed (advance the message receiving document to the next line position), multiple line feed (advance the print document an indicated number of single lines), form feed (advance a web of connected forms to the head of the next form) and tab (skip to the next preset tab position on a line, leaving all intermediate line positions blank). These command signals are transmitted singly and in various different combinations along with the message signals, enabling the receiving printer to fully reconstruct the transmitted message.

Since teleprinters cannot execute these different control functions anywhere near as fast as they can receive and print message data, the need for data buffering is unavoidable. This is to say that when the printer is executing a command such as carriage return or line feed, it cannot at the same time be printing. Therefore, any message data received during the execution of a function command must be temporarily retained in buffer storage until it can be printed. This arrangement works very satisfactorily so long as sufficient time remains between function execution intervals to permit printing of all data received. However, when the frequency of control commands rises to a certain level, so much printer time is consumed in executing function commands that the rate of printing message data cannot keep up with the data transmission rate and message data begins to accumulate in the buffer memory.

This situation is presented by the so-called "short-line" situation where a series of consecutive short print lines are transmitted, e.g., each line having less than one-eighth the number of characters of a full line. During the time it takes the printer to execute a carriage return-line feed command, more than one line of data is received. Therefore, a backlog of message data will accumulate in the buffer memory so long as this situation persists.

One way to remedy this situation is to make the buffer memory large enough to accommodate the expected worst case short line condition. This solution amounts to placing an arbitrary restriction on the amount of short line data that can be transmitted and is therefore undesirable since it limits the transmission capabilities of the system. Similarly undesirable is a solution involving the reduction of the overall transmission rate to accommodate the short line situation. Further, it is generally impractical to interrupt data transmission or to call for a repeat transmission.

OBJECTS AND SUMMARY OF THE INVENTION

It is therefore an object of the present invention to alleviate the above-mentioned difficulties inherent in prior teleprinter systems and to provide an improved teleprinter control system that enables real time printing of high speed telecommunicated messages without loss of message data, even during extended intervals of short line transmission.

Another object is to provide an improved buffer memory control wherein a relatively small-sized memory is utilized.

Still another object is to provide an improved electronic tabulating control for a teleprinter.

Yet another object is to provide an improved teleprinter in accordance with the above-stated objectives while at the same time having a minimum amount of hardware to enable low cost fabrication and maximum reliability and durability.

In accordance with one aspect of the invention, a teleprinter buffer memory stores received message data in fractional line segments and reads out and prints the stored message data sequentially by fractional line segment. This increases the storage efficiency of the buffer in that short data lines do not consume a full line segment in the buffer.

In accordance with another aspect of the invention, the system accommodates extreme short line situations by temporarily suspending the execution of function commands while at the same time shifting to a mode of buffer loading control which ensures utilization of the buffer storage capacity at 100 percent efficiency. Special symbols are printed out to indicate that a function command was deleted and to show the point in the text where the function command should have been executed.

In accordance with yet another principle of the invention, printing is accomplished by utilizing a line printer having an individually controllable print element, e.g., a print hammer cooperating with a rotating type wheel or band, for each possible data position in a line to be printed. The number of hammer driver circuits, however, is limited to the number of data positions included in a fractional line segment of the buffer memory. Switching means are provided to enable "time sharing" of the driver circuits with the full line of print elements.

In accordance with still another aspect of the invention, fully electronic print tabbing is provided through the use of one or more tab plugs which are prewired to a predetermined data position on the print line. A plug, when inserted, causes the buffer control circuits to respond to an incoming tab character to skip the write address circuit directly to the address corresponding to the print position wired into the tab plug. This causes the next-occurring message data to be routed to the tab-specified buffer address so that it will be printed out beginning at the tab-indicated print line position.

These and other objects, features and advantages will be made apparent by the following detailed description of a preferred embodiment of the invention, the description being supplemented by the drawings as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a generalized schematic diagram of a preferred embodiment of the buffer control system in accordance with the invention.

FIG. **2** is a diagram illustrating the relationship between FIGS. **3***a*—**3***d*.

FIGS. **3***a*, **3***b*, **3***c* and **3***d*, when joined together in the manner illustrated in FIG. **2** constitute a detailed circuit schematic of the preferred embodiment shown generally in FIG. **1**.

FIG. **4** is a detailed circuit schematic of the clock and character position generator circuits shown generally in FIG. **3***b*.

FIG. **5** is a waveform diagram illustrating the timing relationship between the sixteen basic timing pulses generated by the clock circuit shown in FIG. **4**.

FIG. **6** is a schematic diagram illustrating the relationship between the print hammers and the print band of the preferred embodiment.

GENERAL DESCRIPTION

Referring to FIG. **1**, a preferred embodiment of the invention is hereinafter generally described. Printing is accomplished by a row of individually controllable print hammers **16** aligned opposite the possible data positions in a print line on a record medium **14**. A chain or band **10** carrying type slugs continuously rotates about a pair of sprockets **11**, the type slugs traversing behind the print line in a repetitive sequence. Document **14** is indexable by means of a paper feed control unit **500** so that successive print lines are positioned in alignment with hammers **16**. An inked ribbon or strip may be provided between document **14** and hammers **16** to generate the print impressions when the hammers force the document against selected type slugs on band **10** or the document may

be coated with a pressure sensitive marking surface to create the desired print impressions.

The individually controllable hammers **16** are operated through a zone selector switching matrix **18** by individual hammer drivers in the circuit **20**. The hammers **16** are divided into a plurality of print zones, the number of hammers in each zone preferably being equal. The number of hammer drivers in circuit **20** is equal to the number of hammers in a single print zone and the selector matrix **18** operates to connect the drivers to the hammers of the active zone. This arrangement results in considerable hardware saving since a small number of hammer driver circuits are "time shared" by the full row of hammers and an individual driver for each hammer is unnecessary.

Data to be printed is received serial by bit, serial by character on a single channel input data line by input circuits **200**. Received data characters are transmitted parallel by bit, serial by character under control of the load control circuits **300** to a data memory **30** where they are temporarily stored, awaiting readout for printing. Format control characters are interspersed singly and in groups among the input data characters. The format control characters consist of carriage return (CR), line feed (LF), tabulate (TAB) and form feed (FF). These characters when received are decoded by the circuits **200** and trigger the entry into a control memory **40** of predetermined control characters which govern the operation of the timing and character position generator **100**, zone selector matrix **18** and the paper feed control unit **500**.

Data memory **30** is subdivided into a plurality of memory groups, each group having a number of character storage locations equal to the number of print hammers in a print zone. Control memory **40** is subdivided into a plurality of character storage locations, there being one such character storage location for each group in memory **30**. The load and read control circuits **300** and **400** always operate such that addressing of any memory group in memory **30** automatically operates to address the associated character storage location in memory **40**. The total number of groups in memory **30** is a matter of choice but, in the instant embodiment, a number equal to three times the number of print zones is chosen to provide a total buffering capacity equal to three full print lines.

The circuits **200** decode each incoming character and provide an indication as to whether the character is a message character, i.e. DATA or SPACE, or a format control character, CR, LF, TAB or FF. In accordance with conventional communication practice each received character comprises an equal number of data pulses, each pulse being representative of a binary 1 or a binary 0. The circuits **200** include a shift register for deserializing each input character.

When a full data character has been assembled in the input circuits it is transmitted in parallel under the control of load control circuits **300** to data memory **30** for storage in a predetermined memory group. At a subsequent time the stored character is read from the memory **30** and is compared by a comparator **22** with a coded character supplied at the output of the timing and character position generator **100**. If this comparison yields a match, a "fire" signal is emitted by comparator **22**, causing printing of the character at the desired print position on document **14**.

Receipt of format control characters by input circuits **200** effects the following control operations:

1. If the format control character or the first of a series of consecutive format control characters is either a CR, LF, or FF, the group in memory **30** to which the preceding data characters had been allocated is closed (except under special "short line" circumstances described subsequently), whether or not it is full, and the next group in memory **30** is set up to store the next-received data characters.
2. If the format control character received is a TAB signal, all the character positions in the data memory lying between the character position storing the last data character and a character position representing the TAB position in the print line are automatically filled (except during operation in a short line situation) with internally generated SPACE characters.
3. If the format control character is CR, input circuits **200** automatically cause data bits to be entered into the character position in control memory **40** associated with the newly opened group in the data memory which will cause the printing of the next-received data characters to begin at the leftmost position of the print line (position 1 on print zone 1).
4. If the format control character is LF, input circuits **200** cause data bits to be entered into the character position in control memory **40** associated with the newly opened group in the data memory which will cause the paper feed control **500** to feed document **14** one line space before the printer begins printing the next-received data characters. If a plurality of LF signals are received, the data bits entered in memory **40** are such as to cause paper feed control **500** to feed the document a number of line spaces corresponding to the number of LF signals received.
5. If the format control character is FF, input circuits **200** cause a data bit to be entered into the character position in memory **40** associated with the newly opened group in the data memory which will trigger feed control **500** to feed document **14** to the first print line on the next form (assuming document **14** is a web of connected forms) before printing of the next-received data characters begin.

To achieve "real time" printing of the input data, i.e. printing each data character at substantially the same instant it is received, readout of data memory **30** under the control of read control circuits **400** must take place, in essence, simultaneously with entry into memory **30** of the received input characters. To accomplish this objective and still maintain the segregation of read and load operations which is necessary for proper operation of the memory, the system is timed by a repetitive sequence of timing pulses generated by the timing circuits **100**, each sequence defining one basic time cycle. The cycles, as described subsequently, are synchronized with the travel of band **10** and occur at a rate which is very high in comparison to the rate at which the input data is received. Each cycle is divided into two halves, the first half governing the operation of load control circuits **300** and the second half governing operation of the read control circuits **400**. Thus, input and output access to memory **30** is time—division multiplexed to enable "simultaneous" loading into and reading from the memory.

Read control circuits **400** address the data memory groups and corresponding character positions in control memory **40** sequentially, each group remaining addressed until all format operations indicated by the control character have been executed and all data stored in the group have been printed. When a new group is addressed, the control character is inspected by feed control **500** and all required feeding operations are performed before printing begins. When printing begins, the character positions in the data memory group are sequentially scanned and the characters stored therein compared with the coded output from generator **100** to effect printing. This scan sequence repeats until all characters in the group have been printed. Thereafter, the next data group is addressed for readout.

As has been previously discussed, when the printer is performing a line space operation it cannot, obviously, also be printing. During such periods, therefore, data characters may be loaded into the data memory but none can be taken out. Under normal operating conditions when the data is being printed in full lines or near full lines, enough data is extracted from the memory between line spacing operations so that the average data extraction rate will at least equal and usually exceed the average data entry rate.

However, in the so-called "short line" situation, more than one complete line of data is received at the input during the time that a paper feed operation is being performed. This creates a situation where the average data entry rate exceeds

the average data extraction rate. Ordinarily, short lines are experienced on a random and infrequent basis and the capacity of data memory **30** is adequate to provide the necessary data buffering. However, when a long succession of short lines is received data accumulates in memory **30** and, since the storage capacity of the memory is finite, there is a possibility that the buffering capacity of the system will be exceeded and data will be lost.

In the instant embodiment, this deleterious condition is prevented through the use of circuits, included in input circuits **200**, which periodically test to see how many groups in memory **30** have been emptied by readout and thus are available to receive data. If the number of available data groups is fewer than some predetermined number, the system is automatically thrown into the "tail" mode of operation. This mode of operation is designed to conserve the storage capacity of memory **30** by utilizing it at 100 percent efficiency and to increase the average rate of data extraction from memory **30** by temporarily inhibiting the performance of format control operations. When the system is operating in the tail mode, format control characters received at the input do not automatically cause the write addressing of a new group in memory **30** to receive the next data characters. Instead, successive blocks of incoming data are tailed together in memory and a new memory group is not set up until the previous memory group has been completely filled. The normal response of the system to received format control characters, as outlined above, is inhibited and the only effect such characters have is to trigger the entrance into memory **30** of an internally generated special character. This special character, since it is entered into memory **30**, is subsequently printed out along with the data characters and serves to indicate the fact that execution of a format control operation was deleted and further indicates the position in the printed text at which the format operation should have occurred.

The system continues to operate in the tail mode until the testing circuits indicate that the criticality of the short line condition has passed and an adequate number of memory groups have been freed. While this tailing arrangement necessarily sacrifices the format of the message it guarantees against any loss of the actual message itself and still provides an intelligible output having as much format information as the original message, the format simply being indicated in a different way.

DETAILED DESCRIPTION

Terminology

In the detailed circuit schematics of FIGS. **3** and **4**, which depict an exemplary embodiment of the subject invention, standard logic circuits are represented by labeled blocks, a brief description of each of which is given below. The specific circuit implementation of each block is well within the skill of the electronic digital circuit technician. In order to prevent undue cluttering of the drawings with arrowheads, all lines connected either to the left or bottom side of a circuit block represent input lines and all lines connected either to the top or right side of a circuit block represent output lines unless the contrary is indicated by an arrowhead on the line.

A block labeled with the & symbol represents a logical AND circuit wherein a signal of the upper voltage level (more positive) employed in logic system is produced on the output line when positive level signals are present on all input lines. All other combinations of input signals produce a signal of the lower voltage level (more negative) at the output line.

A block labeled OR represents a logical OR circuit wherein a positive signal on any one or more input lines produces a positive signal at the output.

A block labeled XOR represents an exclusive OR circuit wherein a positive output is produced when a positive signal is present at either one and only one of the two input lines.

A block labeled I represents an inverter circuit wherein a positive level signal at the input line produces a negative level signal at the output and vice versa.

A block labeled D represents a delay circuit which operates to exactly reproduce at the output any voltage pattern present at the input, all voltage transitions occurring at the input being delayed by a predetermined time interval.

A block labeled SSMV represents a one-shot multivibrator or "single-shot" wherein every positive-going voltage transition at the input produces a positive pulse of predetermined fixed duration at the output.

A block labeled FF represents a flip-flop circuit which is any type of bistable circuit arrangement wherein a positive level signal at the S input causes the 1 output to go positive and stay positive while the 0 output simultaneously goes negative and stays negative and wherein a positive level signal at the R input causes the 0 output to go positive and stay positive while the 1 output simultaneously goes negative and stays negative. A flip-flop having a positive level at the 1 output is referred to as being in the "set" condition and when a positive level exists at the 0 output is referred to as being in the "reset" condition. A flip-flop, once set, will thereafter respond (change its output state) only in response to a positive signal at the R input and when it is in the reset state it responds only to a positive signal at the S input.

A block labeled GATE represents a gating circuit which comprises a plurality of logical AND circuits each of which received a signal to be gated at one of its two inputs and receives a gating signal at the other of its inputs. The gating signal input line is identified by an arrowhead and a positive signal thereon activates all AND circuits in the gate.

A block subdivided into sections **1, 2, 4**, etc. represents a binary counter wherein a positive level signal at the ADV UP input causes the binary number represented on the output lines to advance by a count of one and wherein a positive signal at the RESET 0 input causes the output state of the counter to revert to 0 (negative signals on all output lines). A pulse is generated on the CARRY output of the counter each time the output state changes from all positive to all negative output signals.

A block labeled DECODE connected to the output of a counter converts each unique combination of counter output signals into a single signal on a separate DECODE output line.

Printhead

As shown in FIG. **3***b*), a preferred form of printhead for use with the subject invention includes a continuous print chain or band **10** driven by a motor at a constant clockwise velocity about a pair of pulleys or sprocket wheels **11**. A plurality of type slugs are mounted on the band **10** and are guided in a straight line to the left behind the record medium **14** to be printed on. On the opposite side of document **14** from the moving type slugs is a row of print hammers **16** for printing a sixteen character line on the document. In the instant embodiment, for the sake of clarity, only **16** print hammers are shown. It is to be understood that in practice a much larger number of hammers e.g., **80** may be employed to print a longer print line. The hammers **16** are divided into two equal groups of eight hammers each for the purpose of printing in a first print zone (the first eight data positions in the print line) and a second print zone (the second eight data positions in the print line). Firing of a print hammer at the instant a type slug on band **10** is in exact registration with the hammer results in an on—the—fly generation of that print character on the documents. In practice, an inked ribbon is interposed between the hammers and the document to supply ink for this operation. The document is adapted to be fed upwardly (out of the plane of the drawing) by paper feed control unit **500** enabling a plurality of print lines to be generated successively.

The print band **10** supports a multiplicity of equally spaced type slugs representing the different characters of a complete alphameric font. A pair of transducers **12***a* and **12***b* detect tim-

ing marks on band **10** and generate a pulse in response to each mark. The transducers **12** may be, for example, magnetic pick-ups detecting slots or gear teeth on the band or they may be photocells detecting apertures in the band. Transducer **12***a* detects a single timing mark on the band for each type slug and each pulse thus generated is termed a character pulse (CP). Transducer **12***b* detects a single timing mark on the band and the pulse produced in response thereto is called an index pulse. As will become apparent, subsequently, these pulses are instrumental in timing the operation of the logic circuits, which must be accurately synchronized with the speed of movement of the print band.

The spacing between adjacent type slugs on the print band is exactly one and one-seventh times the spacing between adjacent print hammers. This relationship is illustrated in greater detail in FIG. **6**. There, the 16 print hammers are shown as blocks numbered 1 through 16 and a segment of band **10** is shown moving to the left past the hammers.

Since the spacing of the slugs from each other is exactly 1 1/7 times the spacing of adjacent print hammers, it can be seen that there are only two print hammers which are in exact registry with a type slug at the instant depicted in FIG. **6**. These are hammers **1** (the first hammer in print zone 1) and **9** (the first hammer in print zone 2), which register with slugs A and H, respectively. After the print band has moved to the left a distance Δ S (The distance between the centerline of type slug B and the centerline of hammer **2**), hammers **2** and **10** are in registry with type slugs B and I, respectively. An instant later, type slugs C and J move into registration with hammers **3** and **11**, respectively. The full eight hammer scan sequence is depicted in the chart in FIG. **6**, which illustrates the order in which the type slugs come into registration with the hammers during the scan cycle. One complete scan cycle consumes eight time intervals TS through TZ shown to the left on the chart. The condition on band **10** as show FIG. **6** is that which pertains at time TS. The total amount of band movement is shown in column S at the right of the chart. Note that at the beginning, TS, of the next scan cycle type slugs B and I are in registration with hammers **1** and **9**, respectively, and as the cycle continues, the type slug presented to each hammer is that type slug to the right of the slug presented to the same hammer on the preceding cycle. Thus, if there are **64** different type slugs in the font, it takes **64** TS through TZ time cycles to present the complete type font to each hammer. This, therefore, is the maximum amount of time required to print a full eight character zone of data.

As will be explained in detail subsequently, each of the eight major time intervals TS through TZ is subdivided by the timing circuits **100** into 16 minor time intervals TO through T**15**. One "major time cycle" thus constitutes the time required to run through a single progression of major time intervals TS through TZ (the time required for one-eighth hammer scan) and one "minor time cycle" is the time required to run through one progression of the time intervals TO through T**15** (the time which elapses between the instant when a type slug is in registration with a given hammer and the instant in which the next type slug comes into registry with the next print hammer to the right). Therefore, each major time cycle is divided into **128** minor time intervals. It can be seen, then, that for proper printing no two print hammers in the active print zone can be fired at exactly the same time since within a print zone no two hammers are in exact alignment with type slugs at the same instant. As is well known, this arrangement conserves on hardware since a single comparator may be used to generate hammer firing pulses and these pulses do not have to be stored temporarily in "secondary storage" but instead may be used to trigger the hammer at the instant they are generated. Of course, in keeping with this scheme, the data characters stored in memory **30** for each print position in the print zone must be readout and presented to comparator **22** in sync in the order which the corresponding print hammers in the zone come into registration with the type slugs.

Referring back to FIG. **3***b*, the hammer driver circuit **20** includes eight separate hammer drivers. These eight drivers correspond to the eight print hammers of the print zone. Consequently, each driver output line is connected through the gates **18***a* and **18***b* to a print hammer in each print zone, e.g., the first hammer driver is connected through gate **18***a* to hammer **1** and through gate **18***b* to hammer **9**, etc. Gates **18***a* and **18***b* are activated by the mutually exclusive outputs from a zone flip-flop **44**. Printing can thus take place in only one print zone at a time.

Each hammer driver in the circuit **20** is conditioned for operation by one of eight input lines **406** coming from the read control circuits **400**. As explained, below, conditioning signals occur sequentially on these input lines in sync with the occurrence of the major cycle intervals TS through TZ.

Comparator **22** receives a six parallel-bit input from character position generator **150** and compares it with a six parallel-bit input from an input-output (I/O) register **32** associated with the data storage matrix **31** of memory **30**. At T**12** of each minor time cycle at which there is data to be printed present in I/O register **32** AND **441** generates a signal which activates comparator **22** and causes it to produce a pulse at its output if the two six bit inputs to the comparator match. The output from comparator **22** is fed to AND **23** which responds during print time (all preparatory line spacing operations having been completed) by transmitting a "fire" pulse to the driver circuits **20**. This activates the selected hammer driver circuit to print a character in the active print zone. The firs signal is also transmitted back to the read control circuit **400** to prevent return of the data character in I/O register **32** to its slot in memory matrix **31**.

Timing and Character Position Generator **100**

As shown in FIG. **3***b*, the timing and character position generator **100** includes a clock circuit **101** for generating the **16** minor cycle timing signals TO through T**15** and a character position generator **150** for generating a six-bit output signal for representing to comparator **22** the type slug which is coming into registration in the active print zone each minor time cycle during a printing operation.

The details of the circuit **101** and **150** are shown in FIG. **4**. The circuit **101** includes a flip-flop **103** having its 1 output connected to a gated oscillator **107** which produces a train of square waves so long as the output from flip-flop **103** is positive. The oscillator output is transmitted to gate the output from a decode circuit **113** and to advance a counter **111** through delay circuit **109**. Flip-flop **103** is set by the character pulse CP generated by transducer **12***a* (FIG. **3***b*) and is reset by the carry output from a counter **401** in the read control circuits **400**.

Decode circuit **113** responds to each combination of binary signals on the four output lines of counter **111** by producing a positive level output signal on one of the 16 output lines TO through T**15**. Outputs on these lines, which are gated by oscillator **107**, represent the 16 minor time intervals TO through T**15**. TO is produced in response to an all negative output from counter **111** and T**15** corresponds to an all positive output therefrom. The output from oscillator **107** together with the 16 timing pulses TO—T**15** are shown in the waveform diagram of FIG. **5**.

The delay produced by delay circuit **109** is approximately equal to one-half the length of negative dwell between each two positive outputs from the oscillator. This delay is required to prevent the outputs from counter **111** from being gated through the decoder during the time that the counter is switching. Further, since the signal which resets flip-flop **103** to turn off oscillator **107** is generated at T**15** of the last minor interval of a major cycle, a delay circuit **105** is required to prevent the last T**15** output from decoder **113** from being cut short.

Since the frequency of oscillator **107** is fixed, and since operation of the system depends on the output of the oscillator being synchronized with the speed of the print band, some provision must be made to account for minor fluctuations in

the band speed. This is done by setting the period of the oscillator equal to 1/130th of the time it takes the print band motor, operating at nominal speed, to drive the print band a distance exactly equal to the spacing between two adjacent type slugs (the time between CP pulses). Counter **401** (FIG. *3a*) which supplies the oscillator turn-off pulse to flip-flop **103** is a three position binary counter which is reset to zero by each CP and which is advanced one count after **T15** of each minor time cycle. The carry output from the counter is thus generated at the end of the eighth minor time cycle following the occurrence of each CP. Therefore, oscillator **107** is allowed to operate through exactly 128 cycles before it is turned off. The oscillator thus operates for 128/130ths of the time between CP pulses when the print band is moving at nominal speed. Therefore, the slight oscillator pause occurring at the end of each major time cycle insures that the oscillator will in fact be gated on exactly at the time the next CP occurs, even if the print band gains speed and the next CP occurs slightly before the time that it ordinarily should occur. Of course, if the band loses speed, the oscillator pause is simply extended a bit.

The character position generator **150** is also shown in FIG. **4** and includes a six position binary master counter **151** which is connected to feed a six position binary slave counter through a gate **153**. The slave counter is divided into two three-position halves **169** and **171** for purposes to be described subsequently.

Master counter **151** is advanced one count by each CP. Thus, master counter **151** provides a unique coded output for each of the **64** different type slugs on the print band. The sequential occurrence of these outputs represents the order of presentation of the type characters at print hammer "0" (an imaginary location one hammer space to the left of hammer **1**).

Gate **153** is activated by an output from an AND **159** to transfer the count from counter **151** in parallel to the slave counter **169, 171**. This transfer occurs at T2 time during the first time interval TS (defined by a zero output from decode circuit **405**) of each major time cycle during printing.

The immediately ensuing T3 signal activates AND circuit **165** which in turn causes AND **161** to produce an output if print zone **2** is the active print zone or causes AND circuit **163** to generate an output if print zone **1** is the active print zone. An output from AND **161** is transmitted directly into the eight position of the slave counter causing a count of eight to be added to the count that was just inserted from master counter **151**. An output from AND **163** passes through an OR **167** and feeds directly into the one position of the slave counter causing a count of one to be added.

The reason for the addition of one or eight to the slave counter at the beginning of each major time cycle during printing lies in the fact that the master counter **151** provides a code reference for the imaginary "0" print hammer and to provide a proper reference for the first hammer in print zone **1** a count of one must be added while to provide a proper reference for the first hammer in print zone **2** a count of eight must be added. The number one is used since print hammer **1** is one type slug removed from hammer O and the number eight is used because hammer **9** is eight type slugs removed from hammer O.

Therefore, by time TS3 (minor interval T3 of major interval TS), the output from slave counter **169, 171** represents the character code of the print character just coming into alignment with hammer **1** if print zone **1** is active or hammer **9** if print zone **2** is active. At time TS15 OR circuit **167** adds another single count to the slave counter so that during the ensuing interval TT the count in the slave counter represents the character code of the character coming into alignment with print hammer **2** if print zone **1** is active or print hammer **10** if print zone **2** is active. Similarly, at time T15 of each of the following major intervals TT through TY another single count is added to the slave counter to generate an indication of the character coming into alignment with hammers **3** through **8** if print zone **1** is active or hammers **11** through **16** if print zone **2** is active.

When the next major time cycle is initiated by occurrence of the next CP, master counter **151** is advanced one and the slave counter is properly adjusted by a repeat of the above described cycle. It can therefore be seen that when printing is taking place the output from the slave counter **169, 171** is a 6-bit coded character representing the type slugs which sequentially come into alignment with the hammers of the active print zone. This 6-bit output is, as previously described, employed by comparator **22** for the purpose of generating hammer fire pulses.

Character position generator **150** also receives as an input the index pulse detected by transducer **12***b*. This signal is fed to one input of AND circuit **157**, the other input to which is supplied form an OR circuit **155** connected to all six output lines from counter **151**. AND circuit **157** provides an error output indicative of the fact that counter **151** is not in sync with the print band. When the two are in sync, the index pulse will always occur when counter **151** is in its zero output state, and all inputs to OR **155** are negative. If at index time any input to OR **155** is positive (master counter **151** not at zero) the error signal from AND **157** causes reset of counter **151** to zero through delay **156**. Such error signal normally occurs once (during turn on of system) to accomplish initial sync as the band comes up to speed initially. Since it is beyond the scope of the present invention, no means are shown with the present embodiment for acting additionally on the error signal. However, it is apparent that a succession of error signals is indicative of faulty equipment and detection of such a succession may be used, for example, to light an error indicator and inhibit further printing while an off-line tape recording unit or the like is activated to preserve the input message for later printout after appropriate correction has been made in the system.

Input Circuits **200**

Input circuits **200** are shown in FIGS. *3c* and *3d* and comprise all the circuit elements labeled with a number in the **200** series. A character receiver and decode circuit **202** receives the transmitted input data serial-by-bit, serial-by-character from the input data line and accumulates each character in a single serial input-parallel output deserializing register. Each time this register is loaded with a full character, the circuit **202** generates a positive output on one or two of the six output lines DATA, SPACE, CR, LF, TAB, or FF to indicate which type of character has been received (both DATA and SPACE go positive in response to a space character). Data and space characters are transmitted parallel-by-bit out of the deserializing register and through a gate **206** and an OR circuit **208** into the character storage location of memory matrix **31** which is then being addressed by one of the eight character address lines **304** and one of the six memory group address lines **312**. Gate **206** is activated by an AND circuit **214** which is energized by the first T1 signal which occurs after the DATA line goes positive. The same output from AND **214** causes an OR circuit **228** to generate a "load" signal to enter the data or space character into the memory matrix **31**. The output from OR **228** serves diverse other purposes (explained in detail subsequently), such as advancing character address counter **301**, resetting flip-flop **226**, resetting flip-flop **331**, setting flip-flop **333** and conditioning one input of AND **284**.

If the received data character is not a space character, an AND circuit **218** causes an eighth character bit, which is a "tally" bit, to be entered through gate **206** along with the character. As will be described subsequently in connection with the memory readout operation, this tally bit is employed to determine the presence in memory **30** of characters to be printed. If the received data character is a space character, an inverter circuit **222** connected to the SPACE output from decoder **202** deconditions AND **218** and thus prevents the addition of the tally bit. The space character is thus, in effect, an "empty" character location in the memory **30**.

If the received character is any one of the format control characters CR, LF, or FF, a gate **204** operates on the first T1 after the output of circuit **202** goes positive causing an output to be transmitted from an OR circuit **232** to set group flip-flop

331. This output also acts to reset the reset flip-flop 333 through an AND circuit 337 and an OR circuit 335 and to set a flip-flop 254. Further, the output from OR 232 partially conditions an AND circuit 236 which is used to trigger the gating of a special tail character into memory 30 under conditions described in a subsequent section of this specification.

The setting of flip-flop 331 triggers a single-shot 345 whereupon a pulse is transmitted through an AND gate 321 and an OR circuit 315 to advance memory group address counter 309 one count. Counter 309 is a three position binary counter the outputs of which are fed to a decode circuit 311 to generate a signal on one of the six memory group address lines 312. Each of these lines, when activated, sets up a different memory group to receive input data. Thus, under normal operating conditions the receipt of a CR, LF, or FF character automatically causes the addressing of the next memory group in sequence whether or not the preceding memory group had been completely filled with data characters. Since there are only six groups in matrix 31, the "5" output line 312 is returned to the input of an AND circuit 313 to reset counter 309 to zero every sixth counter advance pulse.

The setting of flip-flop 331 also partially conditions an AND circuit 343 to set up a counter inhibit function during a tabulate operation as described subsequently.

Gating of a CR output by gate circuit 204,

The resetting of flip-flop 333 conditions that circuit to respond to a subsequent set input from OR 228 to gate a control character into control memory matrix 41 as described subsequently. The setting of flip-flop 254 readys the system to run through a "tail test" sequence at a subsequent time, as described below, to determine the number of memory groups in matrix 31 available to receive data.

Gating of a CR output by gate circuit 204, besides accomplishing the functions just described, also causes a flip-flop 266 to be set through AND gate 264 and further causes a flip-flop 280 to be reset through an AND gate 276 and an OR circuit 278. This latter flip-flop functions in an "overrun" situation, as described subsequently, to automatically cause the generation of a line space control bit for inclusion in the control character entered into memory matrix 41.

The setting of flip-flop 266 causes an OR circuit 258 to set the print zone flip-flop 256 whereby the set output thereof goes positive to set up the inclusion into the control character of a bit designating print zone 1 as the active zone. This will cause, as explained below, the next data character received at the input to be subsequently printed by the first print hammer in zone 1.

The gating of an LF output by gate 204, besides accomplishing the above-described functions, also activates an AND circuit 291 to cause an OR circuit 292 to trigger a single-shot 293, generating a pulse which advances the line space counter 294 by one count. The output form counter 294 is gated by a gate circuit 296 for inclusion in the control character to be entered into control memory matrix 41. The LF signal passed by gate 204 also activates an AND circuit 274 and an OR circuit 278 to reset the overrun flip-flop 280.

The gating of an FF output by gate 204 besides accomplishing the above-described functions, also activates AND circuit 268 to cause OR circuit 270 to set flip-flop 272. The set output from flip-flop 272 generates a bit for inclusion into the control character which bit indicates that feeding of the document to the first print position of the next form is required. Also the output from flip-flop 272 deconditions, through an inverter 295, the gate circuit 296 whereby a zero line space count is forced into the control character regardless of the number set up at the output of counter 294. Receipt of eight or more consecutive LF characters causes a carry output to issue from counter 294, whereby flip-flop 272 is set. Thus, more than seven consecutive LF commands automatically generates a head-of-form command.

Summarizing the operation of the input circuits 200 as thus far described, each DATA and SPACE character received at the data input is gated by gate 207 into the memory matrix 31 and is stored at the particular character and group location defined by the load address lines 304 and 312.

Receipt of any of the format control characters CR, LF or FF causes the load control circuits 300 to address the next memory group and the various control flip-flops 256, 266, and 272 as well as the line space control counter 294 are set up to indicate the various format control operations called for by the received format control characters.

Thereafter, as soon as the next data character is gated into memory by the output from AND 214, OR 228 (by setting flip-flop 333) triggers single-shot 347 to activate a gate 242. This enters the character (including a tally bit) into the control memory matrix 41. A delay circuit 349 is provided at the output of single-shot 347 to allow time for the output pulse from OR 228 to set a count into counter 294 when such an operation is called for by the set condition of overrun flip-flop 280.

When gate 242 opens, a 7-bit control character is entered into memory matrix 41, the seven bits of the character consisting of: one tally bit, two bits (mutually exclusive) from the output of print zone flip-flop 256, one bit from the output of head-of-form flip-flop 272, and three bits supplied by line space counter 294. The character location in memory matrix 241 at which this control character is stored is determined by the memory group address lines 312. The active address line of this group, of course, corresponds to the memory group in memory matrix 31 which is then being addressed.

After the gating function of gate 242 has terminated, a delay circuit 351 passes the gating pulse to reset the flip-flops 272, 266 and 280 and to return counter 294 to zero. The control circuits are thus restored in preparation for generating the next control character in response to the next-received format control character or characters at the input.

Also provided in input circuits 200 are the testing circuits which periodically determine the state of availability of memory groups in memory matrix 31 to establish whether or not the system must be switched into the tail mode of operation. The primary circuits in this group are flip-flop 254 and 240, comparator 244 and AND circuit 246. Each time an output is generated from OR 232 in response to the passage through gate 204 of a CR, LF, or FF signal, flip-flop 254 is set, conditioning the right-hand input to AND circuit 252. Thereafter, as soon as the DATA line goes positive in response to the receipt of a data character, AND 252 generates an output which conditions AND 341, AND 238, and AND 246. When AND 341 has thus been conditioned, the next ensuing T2, T3, T4, T5, T6, and T7 timing signals, which are applied to OR circuit 327 from ORs 323 and 325, are gated by AND 341 to OR circuit 315 connected to the input of the load group address counter 309. These six advance pulses therefore drive the state of the six output lines 312 of decode circuit 311 through one full cycle, leaving, at the completion of T7, the same output line energized that was energized at the beginning of the test cycle.

Also, the same T2 pulse which initiates the testing cycle also activates AND 238 to set a flip-flop 240.

Comparator 244 compares the pattern of signals on the six load group address lines 312 with the pattern of signals on the six read group address lines 412 transmitted from the read control circuits 400. The active one of these latter address lines indicates the memory group of the storage matrix 31 which is currently being read from. Comparator 244 produces a positive signal at its output when a match is obtained. If the comparator output goes positive at either T2 or T3 time of the testing cycle it is then known that there are less than two empty memory groups in matrix 31 available to receive input data. However, should the output of comparator 244 go positive during any of the time intervals T4, T5, T6, or T7 of the testing cycle then it is known that there are more than two available memory groups.

The reasoning behind these determinations is as follows: the read control circuits 400, in addressing memory groups for readout, can never get ahead of the group which is currently

being loaded under control of the load control circuits **300**. This, of course, is apparent for the basic reason that the memory **30**, like any buffering memory, operates on a first in-first out basis. Therefore, when the readout operation is fully "caught up" with the load operation, the read control circuits **400** are addressing the same memory group as the load control circuits **300**. There can thus be no data in any of the other five memory groups and all five are thus available for buffering. This means that when the load group address counter **309** is driven through the six step testing cycle, an output is not obtained from comparator **244** until T7. Comparator outputs at T6, T5 or T4 mean that there are, respectively, four, three and two available (empty) memory groups.

When the read control circuits are four memory groups behind the load control circuits, only one memory group is free to receive new input data. In this situation comparator **244** produces an output during the second interval, T3, of the testing cycle. In the worst situation when the read control circuits are five memory groups behind the load control circuits the buffering capacity of the memory has been reached and no memory groups are available to receive new input data. In this instance the output from comparator **244** is obtained T2, the first interval of the testing cycle.

In the present embodiment, either of these last two buffering states are defined as critical and require the system to be thrown into the tail mode of operation to prevent loss of data.

This is done as follows: AND **246** receives an input from OR circuit **323** which is active during each of the timing signals T4, T5, T6, and T7. An output from comparator **244** during any one of these time intervals thus causes AND **246** to generate an output after a slight delay imposed by a delay circuit **250**. The latter is provided to allow the signals on comparator input lines **312** to settle before the comparison result is sampled. The output from AND **246** resets the flip-flop **240** which had been set by the output from AND **238** at the beginning of the testing cycle, and also resets flip-flop **254** through an OR circuit **253** to terminate the testing sequence.

As has been previously described, the reset output from flip-flop **240** conditions AND gates **307**, **337**, **321**, **239**, **264**, **268**, **291**, **276** and **274**. The conditioning of these AND gates is necessary to permit the functioning of input circuits **200** and load control circuits **300** in the normal mode of operation. However, when the tail mode of operation is determined to be necessary, i.e., an output from comparator **244** at either T2, or T3, no output is generated by AND **246** and flip-flop **240** remains in the set condition at the end of the test cycle. Therefore, the previously mentioned AND gates remain deconditioned and normal operation of the system is inhibited. Flip-flop **254** is reset by timing pulse T7 acting through an OR **253**.

Once the system is switched into the tail mode, operation is as follows: data characters received by input circuit **202** are gated as previously described into storage matrix **31**. When any of the format control characters CR, LF, or FF are received the ensuing output from OR **232** sets FLIP-flop **331** as previously described except that the following output from single-shot **345** has no effect due to the deconditioned state of AND **321**. Flip-flop **254** is also set in the usual manner so that upon receipt of the next data input character, AND **252** is enabled to initiate a tail testing cycle. This, or course, is necessary in order to remove the system from the tail mode of operation when that action is justified by the freeing up of the necessary number of memory groups.

The output from OR **232** also enables AND **236** which had been conditioned through an inverter **234** by the output from flip-flop **240**. The output from AND **236**, acting through an OR **241**, sets a flip-flop **226** whereupon an output issues therefrom to activate a tail character generator circuit **224** and to condition an AND circuit **216** after a delay imposed by delay circuit **220**. The length of the delay imposed by D **220** must exceed the length of T1 to prevent premature generation of a tail character in certain circumstances.

Tail character generator **224** produces at its output a 7-bit code character indicative of a desired special character, such as, for example an asterisk, which is stored in a register **212** along with a tally bit. The next T1 signal that occurs following this sequence of operation activates AND **216** to produce a gating pulse to transfer the special character through gate **210** for storage in memory matrix **31**. The output from AND **216** also causes OR **228** to generate a "load" pulse to enter the character in memory, resets flip-flop **331** and sets flip-flop **333**. Also, this output from OR **228** enables AND **284**, causing AND **290** to trigger single-shot **293** if the overrun flip-flop **280** is in the set state. This sets up a line space control bit under certain circumstances described subsequently for inclusion into the control character. An instant later the output from single-shot **347** acting through delay circuit **349**, gates the control character into memory matrix **41** and, thereafter, the same pulse acting through delay circuit **351** sets counter **294** back to zero. The output from OR **228** also passes through delay circuit **230** and OR **305** to advance the load character address counter **301**. Further, the output from delay circuit **230** resets the flip-flop **226**, preparing the latter to be set by the next format control character received during the tail mode whereby another tail character is generated and entered into storage.

Each of the format control characters CR, LF and FF received while the system is in the tail mode of operation sets flip-flop **254** and triggers another tail testing cycle. When the tail condition has been relieved flip-flop **240** will be returned to its reset state at the end of a testing cycle and thus the tail character generating AND circuit **236** is deconditioned and the gating AND circuits **307**, **337**, **321**, **239**, **264**, **268**, **291**, **276**, and **274** are conditioned whereby the system is allowed to resume its normal response to format control characters.

Memories **30** and **40** and Load Control Circuits **300**

The data memory **30** includes a random access data storage matrix **31**, such as a magnetic core storage matrix, having six groups of data storage locations, each such group having storage capacity for eight data characters. Each memory group is individually addressable during a data load operation by one of the six load group address lines **312**. Each group is individually addressable during a read operation by one of the six read group address line **412**. Each character storage location within the addressed group is individually addressable for loading by one of the eight load character address lines **304** and for reading by one of the eight read character address lines **406**. An input data character present on cable **209** from the load circuit **200** is loaded into the addressed character location of the addressed memory group by a load signal generated, as discussed above, by OR **228**.

During a readout operation a signal from an AND circuit **431** causes the data character stored in the character position addressed by one of the lines **406** in the memory group selected by one of the lines **412** to be transferred over cable **33** to I/O register **32**. This register presents the character over cable **34** to the comparator **22**. A signal from AND circuit **437** generated at T14 causes the character in register **32** to be reentered into the storage position in matrix **31** from which it was taken.

The control memory **40** comprises a random access storage matrix **41**, such as a magnetic core storage matrix, an output register **42**, an output gate circuit **43**, and a zone flip-flop **44**. The matrix **41** has six 7-bit character storage locations, each location being individually addressable for load operations by one of the six address lines **312**. Each character location in matrix **41** is also individually addressable for readout operations by one of the six address lines **412**.

When gate **242** is opened, a 7-bit control character is entered into the control memory at the storage location then being addressed by one of the address lines **312**. When AND circuit **445** is activated at T8, the character present in the character location then being addressed by one of the lines **412** is transferred into the output register **42**. During the ensuing T9, AND **521** generates an output which opens gate **43** and causes zone flip-flop **44** to be set or reset, depending upon the print zone bits stored in the control character. Also, gate

43 passes the head-of-form and line space control bits into the paper feed control circuits 500.

The load control circuits 300 are shown in FIGS. 3c and 3d and include those circuit elements labeled with a number in the 300 series. In the course of the above description of input circuits 200, all of the functions of the circuits 300 except those relating to the tab input operation have been described. Therefore, in this section a brief summary of the structure and operation of the load control circuits 300 is given followed by a detailed explanation of those portions of the circuit pertaining to the tab input function.

The primary elements of the circuits 300 are the load character address counter 301 and decode circuit 303 and the load group address counter 309 and decode circuit 311. The three position binary counter 301 produces eight unique combinations of output signals, each of which causes a different one of the eight output lines 304 of decode circuit 303 to be energized. The counter is advanced one count upwardly by each positive signal presented by OR circuit 305 from either the delay circuit 230 or the AND circuit 339, the latter of which comes into play during the tab operation, as described subsequently. Counter 301 is reset to zero by an output from AND 307 which is generated upon operation of gate 204 in gating a CR signal.

A carry output from counter 301 indicates that all eight character positions of a memory group have been loaded. This output causes AND circuit 317 to transmit a pulse, provided the output of AND 343 is negative, through OR 315 to advance the load group address counter 309 to the next count. The carry output also resets flip-flop 333 through OR 335 and changes the output state of print zone flip-flop 256. This latter action occurs as follows: if the flip-flop 256 is in its reset state, AND 262 is partially conditioned and AND 260 is disabled. If at the time the carry output occurs carriage return flip-flop 266 is in its reset state, AND 262 generates an output which causes OR 258 to set flip-flop 256 whereby a print zone 1 data bit is generated for inclusion into the control character. If flip-flop 256 is set at the time the carry output occurs while flip-flop 266 is in its reset state, AND 260 generates an output to reset flip-flop 256, setting up a print zone 2 data bit for inclusion into the control character. Thus, assuming carriage return flip-flop 266 remains in its reset state, each carry output from counter 301 reverses the output state of print zone flip-flop 256. Of course, as was above explained, when flip-flop 266 is set in response to a CR signal the print zone flip-flop is forced to the set state and any carry output generated before flip-flop 266 has been reset has no effect on the print zone flip-flop.

Counter 309 has a six count cycle for sequentially energizing the six address lines 312. After the "5" output line 212 goes positive AND 313 is activated by the next counter input pulse to reset the counter to zero. Counter 309 is advanced one count by the output of AND 317 which goes positive in response to each carry pulse from counter 301 which occurs, as explained above, when the output from AND 343 is negative. Counter 309 is also advanced one count in response to each output from AND 321 which is activated each time the stream of input data characters is interrupted by one or more format control characters CR, LF or FF. Counter 309 is also advanced upwardly one count by each output from AND 341, which outputs occur during the tail testing sequence explained previously.

A tab loading operation is triggered by the gating of a TAB output from circuit 202 by gate 204 unless inhibited by AND 239 when in tail mode. This gated output signal sets a flip-flop 329 which in turn conditions AND circuits 339 and 343. Immediately thereafter, AND 339 emits an output pulse during each of the ensuing minor time intervals T2 through T7. Each of these pulses advances the load character address counter 301 one count. The outputs from counter 301 are transmitted over the lines 302 to the input of a prewired tab selection jack 357. Also, this unit receives an input via line 257 from the set output of print zone flip-flop 256.

The prewired tab selector jack includes a socket member 355 having eight input contact terminals 355a distributed along its lower wall and having four output contact terminals 355b distributed along it upper wall. Jack Plug 357a is inserted in socket 355 and has a set of contacts matching the input and output contacts of socket 355. The plug is prewired to connect four selected input contacts to the four output contacts. The four selected input contacts define a given one of the 16 print hammers in terms of a particular character address in a selected print zone. As shown in FIG. 3d the plug 357a defines print hammer 10 since it connects the right-hand contact 355b to the input contact 355a representing print zone 2 and it connects the other three output contacts to the input contacts representing a binary count of two in the load character address counter 301.

An AND circuit 353 is connected to the four output contacts and generates an output signal to reset the tab flip-flop 329 when all four of the selected inputs are positive. Thus, after the flip-flop 329 has been set by a TAB signal, AND 339 begins gating a sequence of timing pulses to step counter 301 upwardly. When the counter reaches the address specified by plug 357a AND 353 resets flip-flop 329 to terminate the outputs from AND 339, leaving counter 301 at the address called for by the plug. Therefore, the next-received input data character is gated into the data memory at the specified character address and is subsequently printed by hammer 10. Therefore, the tab input circuits operate to cause a sequence of input data characters which is received immediately following a TAB control character to be printed out beginning at the specified prewired data position, regardless of where printing of the preceding data characters had left off.

If after all six timing pulses T2 through T7 have been gated by AND 339 and an output from AND 353 has not yet been generated, flip-flop 329 remains set and timing pulses beginning at T2 of the next succeeding minor time cycle are gated to drive the counter 301. If during the counter driving operation a carry output is generated it operates in the normal manner to reverse that state of the print zone flip-flop 256 and to advance the write group address counter 309 by one count. However, in the situation where the TAB input is received immediately after one or more of the format control CR, LF or FF, AND 343 acts to inhibit AND 317 and any carry output from counter 301 generated during the TAB entry operation does not advance counter 309 but does, as usual, reverse the state of print zone flip-flop.

This is done to conserve storage space in memory matrix 31. Since flip-flop 331 was in its set state when the TAB signal was received this meant that no data characters had been received following the last-received format control character. Since the last-received format control character had advanced counter 309 to set up a new memory group, the TAB input character obviously occurred at a time when no data had yet been stored in the new group. To allow the carry output from counter 301 to advance counter 301 again would simply result in wasting a memory group. Therefore, AND 343 and inverter 319 inhibit such premature closing of the group and the only effect of the carry output is to switch the output of the print zone flip-flop to 256 and to reset flip-flop 333.

Every time a data character is loaded into the eighth storage position of a memory group allocated to print zone 2, the next-received data character must be loaded into a new memory group which is accompanied by a control character in storage matrix 41 calling for feeding of document 14 by at least one space. This condition is necessary to prevent overprinting. The only exception to this rule is when it is desired to add some special additional characters such as underlining or accent characters to a line of data already printed. In this situation the special characters are immediately preceded at circuit 202 by a CR, unaccompanied by any LF characters. In all situations except that just mentioned, the circuits of the present invention automatically add a line space command to the control character associated with the data immediately following data allocated for printing by print hammer 16, pro-

vided that the required LF command is not supplied by one or more LF format control characters received at the input in the normal manner. This automatic line space feature of the present embodiment is particularly necessary to prevent overprinting by the system when it is operating in the tail mode, since, as has already been discussed, the system ignores externally supplied LF control characters at such times.

Allocation of a data character to the memory **30** for subsequent printing by hammer **16** is defined by the occurrence of an output from AND **262** which sets the print zone flip-flop **256**. This output is also used to set the overrun flip-flop **280** whereby AND **290** is partially conditioned. Should the other input to AND **290** go positive before flip-flop **280** is reset, OR **292** operates to trigger single-shot **293** to introduce a count of one into the line space counter **294**. This insures the presence of the necessary line space command in the control character associated with the next-received data characters. When the system is in tail mode, the gating of the next-received (or internally generated) data character causes an output to issue from OR **228**, which output enables AND **284**, activating AND **290** to trigger the advancement of counter **294**. Immediately thereafter, an output issues from delay circuit **349** to gate the control character, including the line space bit, into memory **41** and to reset flip-flop **280** through OR **278**.

When the system is not in tail mode, a positive signal on the DATA output from circuit **202** enables AND **29**o through OR **286** to cause the entry of the line space bit. However, if before the data character is received, a CR is received (in the performance of the above discussed underlining or accenting operation) AND **276** generates an output which resets flip-flop **280** to prevent the generation of the line space bit. By the same token, if the LF format control character is received before the data character AND **274** issues an output which resets flip-flop **280** to prevent the control character then being compiled from calling for one too many line spaces.

Read Control Circuits **400**

The read control circuits **400** are illustrated in FIGS. **3***a* and **3***b* and include all circuit elements labeled with numbers in the **400** series. Two of the basic circuit elements are read character address counter **401** and read group address counter **407**. Counter **401** operates a decode circuit **405** which generates a positive signal on one of eight output lines **406** for each unique combination of binary outputs from the counter. A delay circuit **403** generates an output signal after every T**15** time, causing advancement of counter **401** one count. The counter is reset to zero by each character pulse generated by the character mark transducer **12***a*. Each time the counter switches from an all positive to an all negative output a carry signal is generated and fed to clock circuit **101** where it is employed in the manner previously described in connection with FIG. **4**. The output lines **406** from decode circuit **405** are used to address a character for readout from memory matrix **31** and to condition the individual hammer driver circuits **20** for operation. Also "0" output line **406** is used in character position generator **150** in the manner previously described.

The read group character counter **407** is advanced upwardly by each signal generated by an AND circuit **417**. Decode circuit **411** receives the output from the counter and produces a positive signal on a different one of the six output lines **412** for each different output combination. The output lines **412** address the different groups for readout from data memory matrix **31** and address the different characters for readout from control memory matrix **41**. Also, the signals on output lines **412** are used, as previously described, by comparator **244** in the performance of the tail testing sequence. An AND circuit **409** receives inputs from AND **417** and from the "5" output line **412** to generate a signal for resetting counter **407** to zero.

At T**10** of each minor time cycle AND **433** inspects the tally bit storage position of register **32** to determine whether or not a data character is present in the character storage position of memory matrix **31** then being addressed by lines **406** and **412**. If a character is present AND **433** generates an output pulse which sets a tally flip-flop **435**. The set output from flip-flop **435** conditions AND **441** to enable comparator **22** to perform a print comparison during the following T**12**, resets a three position binary counter **415** to zero, deconditions (via inverter **423**) an AND circuit **421** to inhibit advancement of counter **415**, and resets a standby timer **413**. At the following T**15** flip-flop **435** is reset. This action initiates the operation of timer **413**, deconditions AND **441** to inhibit comparator **22** and conditions AND **421** to permit advancement of counter **415**.

Counter **415** is advanced one count upwardly at T**11** of each minor time cycle when flip-flop **435** is reset and when print flip-flop **419** is set. Counter **415** thus performs the function of indicating when eight consecutive minor time cycles (one full major time cycle) have elapsed without detection of a data character in the addressed group of memory matrix **31**. Since during each of the minor time cycles a different character location in the group had been sampled, a carry output from counter **415** indicates that the memory group is empty and causes AND **417** to generate an output pulse to advance the read group address counter **407** to the next group. It should be noted that AND **417** cannot produce this output unless the output from comparator **244** (FIG. **3***c*) is negative. This prevents advancement of counter **407** when the memory group being addressed for readout is the same memory group being addressed for writing. This prevents the readout circuits from getting ahead of the load circuits.

Flip-flop **419** performs the basic readout supervision function in that when it is in its reset state ANDs **431**, **421** and **23** are deconditioned, thus inhibiting any advancement of the counter **415**, preventing any readout operations and inhibiting generation of any "fire" pulse from comparator **22**. Flip-flop **419** is reset by the output of AND **417** which, as just described, indicates that all data from one memory group has been printed out and causes addressing of the next memory group and its associated control character in control memory **41**. The printing operation cannot resume until an output is generated from an AND circuit **425** to set flip-flop **419**. This cannot occur until a positive signal appears on input line **514**. Such a signal on line **514**, which comes from the paper feed control **500**, indicates that all format control operations required by the newly addressed control character have been executed.

When line **514** goes positive it triggers a single-shot multivibrator **427** which causes the output form an inverter circuit **429** to go negative. AND **425** thus cannot generate its output until the occurrence of the first character pulse (CP) following the timing out of single-shot **427**. Single-shot **427** thus provides sufficient delay for the switches in the print zone gates **18***a* and **18***b* to be set up and for the paper to settle and also insures that the next print cycle will begin with counter **401** in its zero state, thus initiating the memory group scan at the first character in the group.

Each time a fire pulse is gated to the hammer driver circuits from comparator **22**, the data character stored in register **32** is printed. The fire pulse is transmitted to set a flip-flop **439** whereupon AND **437** is disabled. When the next T**14** occurs, AND **437** therefore generates no output pulse and the printed character is not returned to the memory **31** and the character storage location is left empty.

If a long period of time e.g., 30 seconds, elapses without detection of any tally bits in register **32**, a presumption is made that all data in the memory **31** has been printed and no new data has been received. The "standby" output generated at this time by timer **413** is used to turn the print band motor off in order to reduce wear of the high speed mechanical elements of the system.

Paper Feed Control **500**

The circuit elements of paper feed control **500** are illustrated in FIG. **3***b* and are indicated by the circuit blocks labeled with numbers in the **500** series. When flip-flop **419** is

reset to terminate a print cycle, its reset output line **420** goes positive and initiates operation of a hammer delay timer **523**. After a predetermined delay the output from timer **523** operates to reset a flip-flop **519** whereupon AND circuit **521** is conditioned through OR **522** to inspect the control memory output register **42** during each **T9** for the presence of a tally bit. When a tally bit is found, an output is generated by AND **521** to set flip-flop **519** whereupon an inverter circuit **447** deconditions AND **445** to prevent any further readout of the control memory. The output from AND **521** is also used to activate gate **43**, transferring the print zone, head-of-form and line space bits from the control character in register **42** to the flip-flops **44** and **515** and the counter **513**, respectively. OR **522** serves a "latch back" function to hold AND **521** positive for the full duration of **T9**. The loading of zone flip-flop **44** with the new print zone control data in most cases causes activation of a different one of the gates **18***a* and **18***b*. The need for hammer delay timer **523** is thus apparent since it allows time for the last data character of the previous memory group to be printed before the state of the switches in gates **18***a* and **18***b* begin to change in response to the control character associated with the new memory group.

The output of AND **521** is also used to set a "Paper Feed Now" flip-flop **520** which partially conditions AND **516** to permit determination of the end of paper feed, if any. At the first **T10** time after gate **43** has been activated and wherein no (further) line feeding is required, an output is obtained from AND **516** which sets flip-flop **518**. The set output line **514** goes positive, initiating the timing delay of SSMV **427** and subsequently resulting in setting print flip-flop **419**, as previously discussed, and resetting flip-flop **520** to inhibit any further output from AND **516** until after the next control character has been read.

As soon as the print flip-flop **419** is set (to initiate this print cycle) the output from an inverter **443** goes positive and resets flip-flop **518**. The set output line **514** thereof goes negative and prevents subsequent setting of the flip-flop **419** until an output has been generated by AND **516** signalling that all paper feed operations called for by the next control character have been performed. Two cases must be considered, the first being that wherein the control character requires no paper feeding and the second being that wherein paper feeding is called for.

1.In the case where the control character contains no line spacing data, gate output lines **43***a* and **43***b* remain negative when gate **43** opens at **T9** and flip-flop **515** remains in its reset state and counter **513** remains at zero. Thus, the output from OR circuit **511** stays negative causing no actuation of the feed unit and when AND **516** samples the output of inverter **512** at **T10** an output is generated to set flip-flop **518**. This causes output line **514** to go positive to permit a new print cycle to begin subsequently.

2. In the case where the control character requires line spacing operations, a positive signal is gated either on line **43***a* or on one or more of the lines **43***b* to set the flip-flop **515** or to enter a count into counter **513**. In this case the output of OR **511** goes positive and at **T10** immediately following the opening of gate **43** AND **516** does not go positive and flip-flop **518** remains in its reset state suppressing printing.

A positive output from OR **511** causes paper feed control unit **501** to begin advancing the document **14**. A conventional type of format control unit included in the feed control produces a positive pulse on a line **509** each time the document has been advanced one line space and produces a positive pulse on a line **507** when the document has been fed to the first print line of the next form.

As was described previously in connection with input circuits **200**, the head-of-form and line space control bits are mutually exclusive i.e., when gate **43** gates a positive level signal to line **43***a* all of the lines **43***b* must be negative and if any one of the lines **43***b* is positive line **43***a* must be negative. Thus, when flip-flop **515** is set by gate **43**, OR **511** energizes the feed control unit **501** and the document is fed until the head of the next form is reached. At that time the signal on line **507** resets flip-flop **515**, causing OR **511** to go negative to terminate the feeding operation. At **T10** following termination of feeding AND **516** generates an output to set flip-flop **518** to enable the print cycle to begin.

When gate **43** enters a count into counter **513**, the output of OR **511** goes positive to initiate feeding and each time the document is fed one line space the output signal on line **509** reduces the count to counter **513** by one. When the counter reaches zero the required number of lines spaces have been fed and the output of OR **511** goes negative, terminating feeding and conditioning AND **516** to trigger a print cycle subsequently.

Arrival of the document at the head of the next form is defined as an unconditional requirement for stopping paper feed. Accordingly, occurrence of a form top signal on line **507** resets counter **513** to zero (and resets flip-flop **515**, as discussed above), causing the document to stop and conditioning AND **516**.

Operation-Normal Condition

The following description briefly summarizes the sequence of operations performed when the system is operating in its normal mode, the various sub-operations having already been covered in detail above. For the following, reference is made to FIGS. **3***a*—**3***d*.

Assume the following block of data is received at the data input: CR, LF, LF, D, D, D, D, D, D, D, D, D, D, D, D, D, D. This message calls for a carriage return and double line feed followed by a **15** character line of data. The D symbols stand for either data or space characters.

As soon as the CR character is received and decoded by circuit **202**, the CR line goes positive and on the following **T1** gate **204** transmits a positive signal to OR **232**, AND **307**, AND **264** and AND **276**. AND's **307**, **264**, and **276** are already partially conditioned since the system is not operating in tail mode (the reset output from flip-flop **240** is positive). Therefore the gated CR signal causes AND **307** to reset the load character address counter to zero, AND **264** to set the carriage return flip-flop **266** and AND **276** to reset the overrun flip-flop **280** (if it is not already in its reset state). Setting of flip-flop **266** forces the print zone flip-flop **256** to its set state, indicating that the next received data character should be printed in print zone **1**.

Activation of OR **232** sets the group flip-flop **331**, resets flip-flop **333** and sets flip-flop **254**. The setting of flip-flop **331** triggers single-shot **345** to advance the load address group counter **309** one count, setting up the next memory group to receive data characters. The resetting of flip-flop **333** prepares it to cause single-shot **347** to generate the control character gating and reset pulse the next ensuing output from OR **228**. The setting of flip-flop **254** partially conditions AND **252**, preparing it to trigger a tail testing operation the next time the DATA output line from circuit **202** goes positive.

The first LF character causes the LF output line to go positive whereupon the next **T1** causes gate **204** to gate a signal to OR **232**, AND **291** and AND **274**. The output thus triggered from OR **232** has no effect since flip-flops **331**, **333**, and **254** are already in their set, reset, and set states, respectively. AND **291** generates an output signal which triggers single-shot **293** and advances line space counter **294** to a count of one. AND **274** generates an output which is ineffective since flip-flop **280** is already in its reset state.

The second LF character causes generation of the same array of signals just mentioned, the net result being that AND **291** triggers single-shot **293** to advance the counter **294** to a count of two.

When the first DATA signal is received in circuit **202**, the DATA output line goes positive and AND **214** is energized the following **T1** to open gate **206** to pass the data character in parallel to the first character storage position of the newly ad-

dressed memory group. Also, OR 228 generates an output to effect the loading of the character into the matrix and to reset flip-flop 331, set flip-flop 333 and to partially condition AND 284. Resetting flip-flop 331 prepares it for triggering the next load group counter advance pulse in response to the next-received format control character. The setting of flip-flop 333 triggers single-shot 347 to produce a pulse which, after a slight delay, opens gate 242 to transfer the format control character to memory 41 and which, after another delay, operates to reset the line counter 294 and the flip-flops 272, 266 and 280.

The control character transferred by gate 242 is 1100010. The first (left-hand) bit of this character is a tally bit, the second two bits indicate print zone 1, the fourth bit indicates no head-of-form operation is required and the last three bits indicate a line space count of two. This character is stored in matrix 41 at a character storage position corresponding to the newly addressed memory group in matrix 31 (set up when counter 309 was advanced in response to the previously received CR character).

The above-described sequence of operations began, it will be recalled, with the activation of AND 214 during T1. The occurrence of the following "load" signal from OR 228 and the gate signal from the delay circuit 349 takes place during the same T1 time interval to load the data and control characters into their respective storage locations. The following T2 time pulse causes AND 238 to set the tail flip-flop 240 and energizes AND 341 to advance load group address counter 309 upwardly one count to initiate the tail testing cycle. The following T3—T7 signals cause a similar advancement of counter 309 and during one of the final four intervals, T4—T7 (assuming the tail mode of operation is not required) an output is generated by comparator 244 whereupon AND 246 generates an output to reset flip-flops 240 and 254, completing the tail testing sequence. Upon completion of this sequence, of course, counter 309 is left in the state which it possessed prior to the testing cycle.

The next seven data characters which are received at the input are allocated through gate 206 to the remaining seven character storage locations in the addressed memory group. The gating of the seventh of these data characters causes counter 301 to "turn over" from its all-one to its all-zero state, whereupon a carry output is produced. This carry output activates AND 317 to cause the load group address counter 309 to address the next memory group, resets flip-flop 333 and switches the print zone flip-flop 256 to its reset state representative of print zone 2.

When the next data character comes in (the ninth data character in the fifteen character sequence being received) it is gated by gate 206 into matrix 31 at the first character location of the newly opened memory group and the output from OR 228 sets flip-flop 333 whereupon gate 242 is opened to transfer the control character 1010000 into the memory 41. The first 1 in this character is a tally bit and the other 1 indicates print zone 2. No format control operations are called for.

The remaining six data characters in the sequence are successively allocated to character storage locations two through seven in the addressed memory group.

So far, the description of operation has been concerned solely with data and control character loading. All of these operations are timed by time signals T1—T7 and thus occur during the first halves of the generated minor time cycles. During the second halves, i.e. T8—T15, of each of the occurring minor time cycles the read control circuits 400 are operative to cause the printing of the stored data. However, before the read control circuits can operate the required format operations must be performed.

As will be recalled from above, during the T1 interval in which the first received data character was gated into memory, gate 242 also operated to gate the control character 1100010 into memory 41. During the ensuing T8 time interval (assuming that no data characters other than the one just gated are present in memory 31) AND 445 generates an output which transfers the just-entered control character into register 42. At T9 AND 521 is activated, setting flip-flops 519 and 520. The output from AND 521 also opens gate 43, setting zone flip-flop 44 and entering a count of two broadside into counter 513. This causes the output from OR 511 to go positive whereupon paper feed control 501 begins feeding document 14.

After the document has been fed two line spaces, counter 513 reaches zero and the output from OR 511 goes negative. The first T10 signals to occur after this activates AND 516 whereupon flip-flop 518 is set and output line 514 goes positive. This positive signal resets flip-flop 520 and presents, after single-shot 427 times out, positive inputs to the lower two inputs of AND 425. When the next character pulse occurs AND 425 issues an output which sets the print flip-flop 419 and resets flip-flop 518 through inverter 443.

At T9 following the setting of flip-flop AND 431 causes the first data character received to be transferred to register 32. At T10 AND 433 sets flip-flop 435 whereupon AND 441 is partially conditioned. At T12 AND 441 activates comparator 22 and the data character is compared with the character then just coming into alignment with print hammer 1. If the two characters are the same, an output is generated by comparator 22 and is gated by AND 23 to cause the hammer driver circuit associated with hammer 1 to print the character. If the two characters are not the same AND 437 operates at T14 to restore the data character back to its position in matrix 31.

At T15 AND 403 advances the read character address counter 401 by one count so that the second data character in the memory group is addressed. The following T9 AND 431 causes that character to be entered into register 32 and at T12 comparator 22 compares the character with the character then just coming into alignment with print hammer 2. Again, if comparator 22 generates an output AND 23 produces a "fire" pulse which, in this instance, causes the hammer driver circuit associated with hammer number 2 to print the character. If no output is issued form comparator 22 AND 437 operates at T14 to restore the data character to its position in memory and at T15 AND 403 advances address counter 401 so that the third character in the group is addressed and the hammer driver associated with hammer three is conditioned to operate in response to an output from comparator 22.

The eight characters in the group are thus sequentially addressed and compared with the characters on print band 10 until all characters of the memory group have been printed out. As described previously, this condition is determined to exist when counter 415 produces a carry output indicating that all eight character positions of the memory group have been inspected and no tally bits have been found, provided that comparator 244 shows that the positions have all been filled. The carry output from counter 415 enables AND 417, generating a signal which advances the read group address counter 407 one count and resets the print flip-flop 419. This action activates line 420 and initiates the hammer delay timer 523. When the latter times out, flip-flop 519 is reset whereupon AND 521 is conditioned to inspect, during the next T9 interval, for the presence of the control character associated with the memory group which is then being addressed by counter 407.

In the example being discussed, the control character now in register 42 is 101000. At T9 AND 521 generates its output which sets flip-flops 519 and 520 and opens gate 43 whereupon zone flip-flop 44 is switched to its reset state, indicating that the next printing is to occur in print zone 2. Since lines 43*a* and 43*b* do not go positive with the new control character, the output from OR 511 stays negative and no feeding is initiated. At T10 AND 516 generates an output which sets flip-flop 518 causing line 514 to go positive. This conditions AND 425 to set the print flip-flop 419 after the delay imposed by single-shot 427. As previously discussed, the period of this delay permits the switches in zone 2 gate 18*b* to be set up before printing is allowed to begin.

After flip-flop **419** is set, the newly addressed memory group is sequentially scanned beginning at character position **1** by the read control circuits **400** in the manner described above and the final seven data characters are printed in zone **2** by hammers **9** through **15** to complete the data line.

If, in either zone, printing of previously stored characters is completed before the following data characters are received, AND **417** will have a negative input from comparator **244** through inverter **248** due to the same (group) address being used for loading data into and reading data out of memory **31**. Print FF **419** cannot be reset and print cycles will continue, awaiting the data that is still to be received for printing within the extant print zone.

Operation-Tail Mode

In the above description it was noted that when the tail testing cycle was initiated by AND **252** in response to the receipt of the first data character following a format control character, the need for tailing was determined not to exist and tail flip-flop **240** was returned to its reset state at completion of the cycle.

However, if tailing is determined to be necessary, i.e., less than two memory groups in matrix **31** are available to receive input characters, flip-flop **240** remains in its set state at completion of the testing cycle. This means that AND **236** becomes partially conditioned and AND's **307**, **337**, **321**, **264**, **268**, **291**, **274**, and **276** become deconditioned. With the system in this condition and assuming that the same sequence of 15 data characters is presented at the input, operation of the input circuits **200** and write control circuits **300** is as follows.

The 15 data characters are loaded into memory **30** in exactly the same manner previously discussed. However, when the next format control characters, assuming them to be for example CR, LF, are presented to the input to set up the next line of print, the following occurs: the CR signal gated by gate **204** at T1 does not reset the character address counter **301** since AND **307** is deconditioned and it is further prevented from setting flip-flop **266** or resetting flip-flop **280**. The output which is caused to issue from OR **232** does set flip-flops **331** and **254** but it does not reset flip-flop **333** since AND **337** is deconditioned.

The output from OR **232** activated AND **236** and sets flip-flop **266** whereupon tail character generator **224** inserts the code of the special tail character into register **212**. Thereafter, AND **216** generates an output at T1 to open gate **210** to transfer the tail character into the the eighth character position of the addressed memory group (the first seven character positions of the group are taken up by the final seven characters of the previously received line of data).

The output from AND **216** also activates OR **228** to generate the "load" signal for entering the tail character into matrix **31**, for resetting flip-flop **331**, setting flip-flop **333** and enabling AND **284** to trigger the setting up of a line space control character in the event flip-flop **280** is in its set state. Also, the output from OR **228**, after the delay imposed by delay circuit **230**, advances the character address counter **301** by one count and resets flip-flop **226**. In the example being discussed, this advancement of counter **301** switches it from a count seven to a count of zero and thus causes a carry output to issue. This carry output advances the group address counter **309**, resets flip-flop **333** and reverses the state of print zone flip-flop **256**, causing it to switch back to its set state representative of print zone **1**.

In switching flip-flop **256**, AND **262** generates a signal which sets the overrun flip-flop **280**. When the next input character, LF, is received OR **232** again triggers the tail character generator and another special character is entered, this time into the first character position of the newly addressed memory group. Also, flip-flop **254** is set to condition the tail testing circuits to run another tail testing cycle in response to receipt of the next data character.

When the second tail character is gated into memory the output of OR **228** sets flip-flop **333** and thereby triggers single-shot **347**. The same output pulse from OR **228** also activates AND **284** and this in turn activates AND **290**, flip-flop **280** being in its set state. The output from AND **290** triggers single-shot **293** and the line space counter **294** is advanced to a count of one.

Immediately thereafter, the pulse from single-shot **347** issues from delay circuit **349** and opens gate **242**. This enters a control character 1100100 into control matrix **41** at the character location corresponding the newly addressed memory group. Immediately following that, delay circuit **351** causes counter **294** to be reset to zero and also resets flip-flop **280**.

The next seven consecutive input characters, regardless of whether they are data characters or format control characters (assuming the system continues in tail mode), are allocated to the remaining seven character positions of the addressed memory group. Thereafter, counter **301** produces a carry output to set up the next group memory and after that group has been filled by the next **8** input characters, overrun flip-flop **280** again causes an automatic line space bit to be included in the control character for the following memory group.

The read control circuits **400** and paper feed control **500** operate in exactly the same manner discussed above to cause printing of the characters stored in memory **30**. However, due to the just-summarized operation of the input circuits and load control circuits while in the tail mode, printout of the data always occurs in full **16** character lines (space characters being included as valid characters in this context), with each deleted format operation being indicated in the print line by the special tail symbol.

Therefore, when the system is operating in the tail mode, the only line spacing operations performed are those necessary to prevent overprinting and since data is printed in full **16** character lines between line spacing operations the average data extraction rate is increased well beyond the average data input rate. This causes the backlog of unprinted characters in memory **30** to be reduced, alleviating the critical buffering situation in due time.

When this has been done tail flip-flop **240** is once again restored to its reset state at the end of a tail testing cycle and the system is allowed to resume operation in the normal mode.

If a TAB input character occurs while the system is operating in the normal mode as outlined above, the following occurs: the TAB output line from circuit **202** goes positive and gate **204** produces an output pulse the following T1 which sets the tab flip-flop **329** through AND **239**. This causes AND **339** to generate a sequence of output pulses which advance the load character address counter **301** a count at a time until it arrives at a count representative of the tab position wired into plug **357***a*. When the tab count is reached AND **353** produces an output signal which resets flip-flop **329** and terminates the tab address operation. This operation, in effect, loads a sequence of blank spaces into memory **30**, the blanks extending from the position following the last entered data character to the position just before that corresponding to the tab position. While the system is in its normal mode of operation, this results in the usual type of tabulation format. However, while the system is in tail mode the TAB operation is ignored, AND **239** inhibiting entry into tab flip-flop **329**. A special symbol is loaded into memory **30** for each TAB character so ignored.

This is done when AND **237**, conditioned by the output of inverter **234**, generates an output through OR **241** to set flip-flop **226**, triggering entry of the special symbol from generator **224** into the memory matrix **31**.

It will be appreciated that various changes in the form and details of the above-described preferred embodiment may be effected by persons of ordinary skill without departing from the true spirit and scope of the invention.

I claim:

1. In a printer for printing message characters on a document, said characters being serially transmitted to said printer

along with print format command characters, the combination comprising:

a plurality of message memories for storing transmitted message characters prior to the printing thereof;

a control memory;

first control means for applying transmitted message characters to a first of said message memories;

means responsive to a transmitted print format command character for causing said first control means to apply the next-transmitted message characters to a second of said message memories; and

entry means for entering a predetermined control character corresponding to said print format command character into said control memory.

2. The combination set forth in claim 1 further comprising:

message readout means operable to read said message characters out of said second message memory for printing on said document; and

second control means operable just prior to said message readout means for reading said control character out of said control memory and for initiating a corresponding print format control operation whereby said message characters are printed on a selected portion of said document.

3. The combination set forth in claim 1, further comprising:

a plurality of groups of print elements adapted to print said message characters in a plurality of zones arranged in a line across said document;

additional control memories whereby there is a control memory corresponding to each said message memory;

overrun means for detecting the filling of a message memory with message characters to be printed in the last zone of said line;

means responsive to said overrun means for generating a control character representative of the first zone of said line; and

means also responsive to said overrun means for causing said first control means to apply the next-transmitted message characters to a second message memory and for entering said control character into the control memory corresponding to said second message memory.

4. The combination set forth in claim 3 wherein said generated control character is further representative of a document feed operation.

5. The combination set forth in claim 1, further comprising:

test means for periodically determining the number of message memories available to receive transmitted message characters; and

means responsive to said test means for causing said first control means to apply said next-transmitted message characters to said first message memory when the number of available message memories is below a predetermined quantity.

6. The combination set forth in claim 5, further comprising:

means responsive to an indication from said test means that the number of available message memories is below said predetermined quantity for generating a special message character in response to a transmitted print format command character; and

means for applying said special message character to said first message memory.

7. The combination set forth in claim 1, further comprising:

a plurality of print elements adapted to print the data stored in said message memories;

message memory address means included in said first control means for generating, in response to a transmitted print format command character representative of a tab operation, a sequence of message memory addresses;

print zone means responsive to said address means for generating code characters relating each said memory address to one of said print elements;

tab storage means for storing a predetermined memory address-code character combination representative of a predetermined print element;

means for comparing the outputs of said address means and said print zone means with the contents of said tab storage means and for generating a match signal upon an equal comparison;

additional control memories whereby there is a control memory corresponding to each said message memory; and

means responsive to said match signal for causing said first control means to apply the next-transmitted message character to a storage position in said second message memory corresponding to said memory address stored in said tab storage means and for causing a control character corresponding to said code character stored in said tab storage means to be applied to the control memory corresponding to said second message memory.

8. The combination set forth in claim 2, further comprising:

document feeding means; and

means included in said second control means for actuating said feeding means when the control character readout of said control memory corresponds to a print format command character representative of a document feeding operation.

9. The combination set forth in claim 2, further comprising:

a plurality of groups of print elements adapted to print, in predetermined print zones on said document, the message characters stored in said message memories;

actuation means for selectively energizing said groups of print elements a group at a time; and

means included in said second control means for energizing a selected group of said print elements when the control character readout of said control memory corresponds to a print format command character representative of said group of print elements.

10. In a printer for printing message characters on a document, said characters being serially transmitted to said printer along with line feed format command characters, the combination comprising:

a plurality of message memories for storing transmitted message characters prior to the printing thereof;

a plurality of control memories corresponding to said message memories;

input means for loading transmitted message characters into said message memories in a predetermined sequence and for loading a line feed control character into one of said control memories in response to each said transmitted line feed format command character; memory readout means for effecting printing of said stored message characters on said document and for effecting feeding of said document in accordance with said stored line feed control characters; and

means for inhibiting the loading of said line feed control characters into said control memories when the capacity of said message memories to store new message characters is reduced to a predetermined level.

11. The combination set forth in claim 10, further comprising:

means operable in response to operation of said inhibit means for automatically entering a line feed control character into one of said control memories when a message character is stored for printing in the last print position of a line on said document.