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(54) **HIGH-K DIELECTRIC MATERIALS UTILIZED IN DISPLAY DEVICES**

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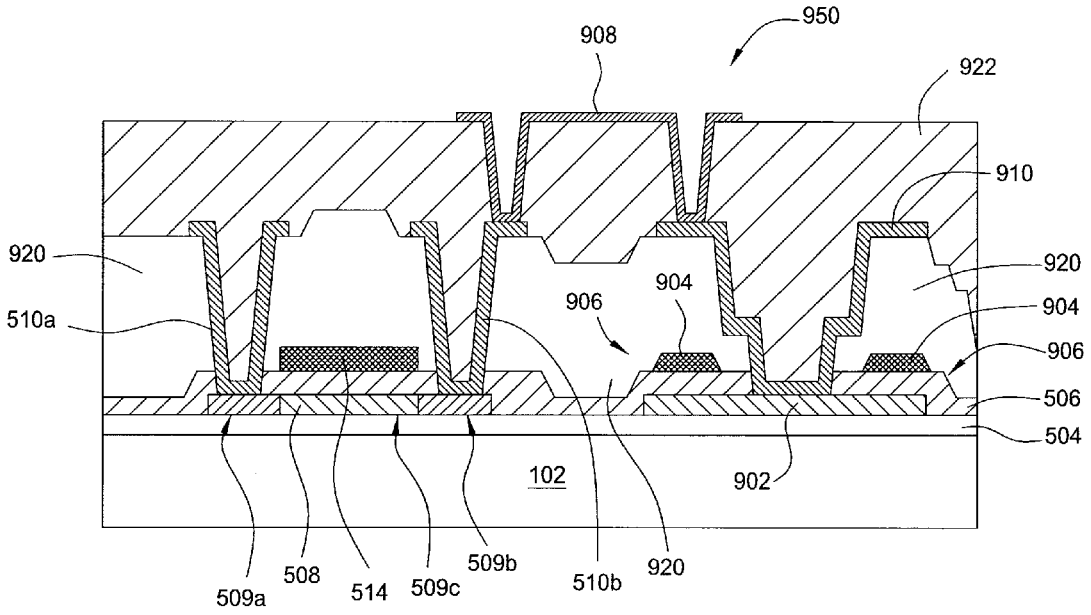
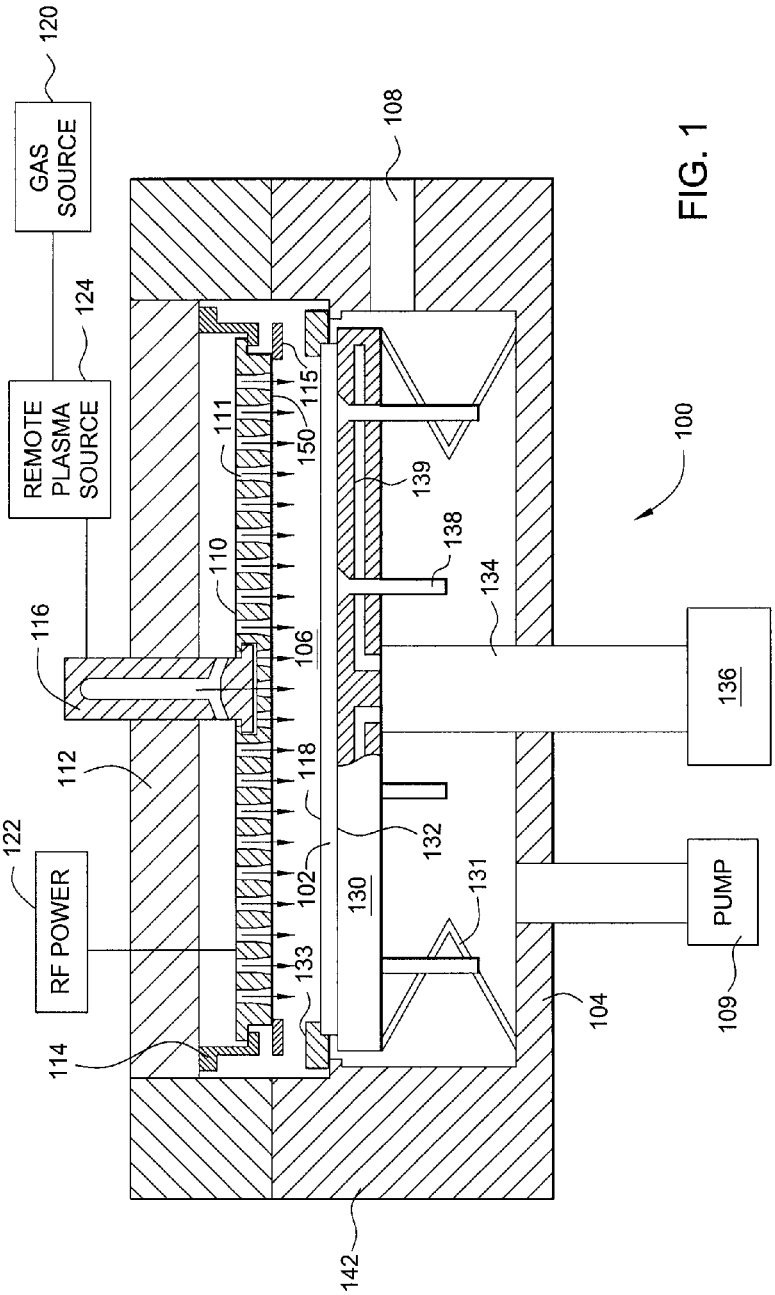
(57) **ABSTRACT**

Embodiments of the disclosure generally provide methods of forming a capacitor layer or a gate insulating layer with high dielectric constant as well as film qualities for display applications. In one embodiment, a thin film transistor structure includes source and drain electrodes formed on a substrate, a gate insulating layer formed on a substrate covering the source and drain electrodes, wherein the gate insulating layer is a high-k material having a dielectric constant greater than 10, and a gate electrode formed above or below the gate insulating layer.




GAS SOURCE
120
REMOTE PLASMA SOURCE
124
RF POWER
122
PUMP
109
136
130
100
104
108
142
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110
111
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114
115
116
118
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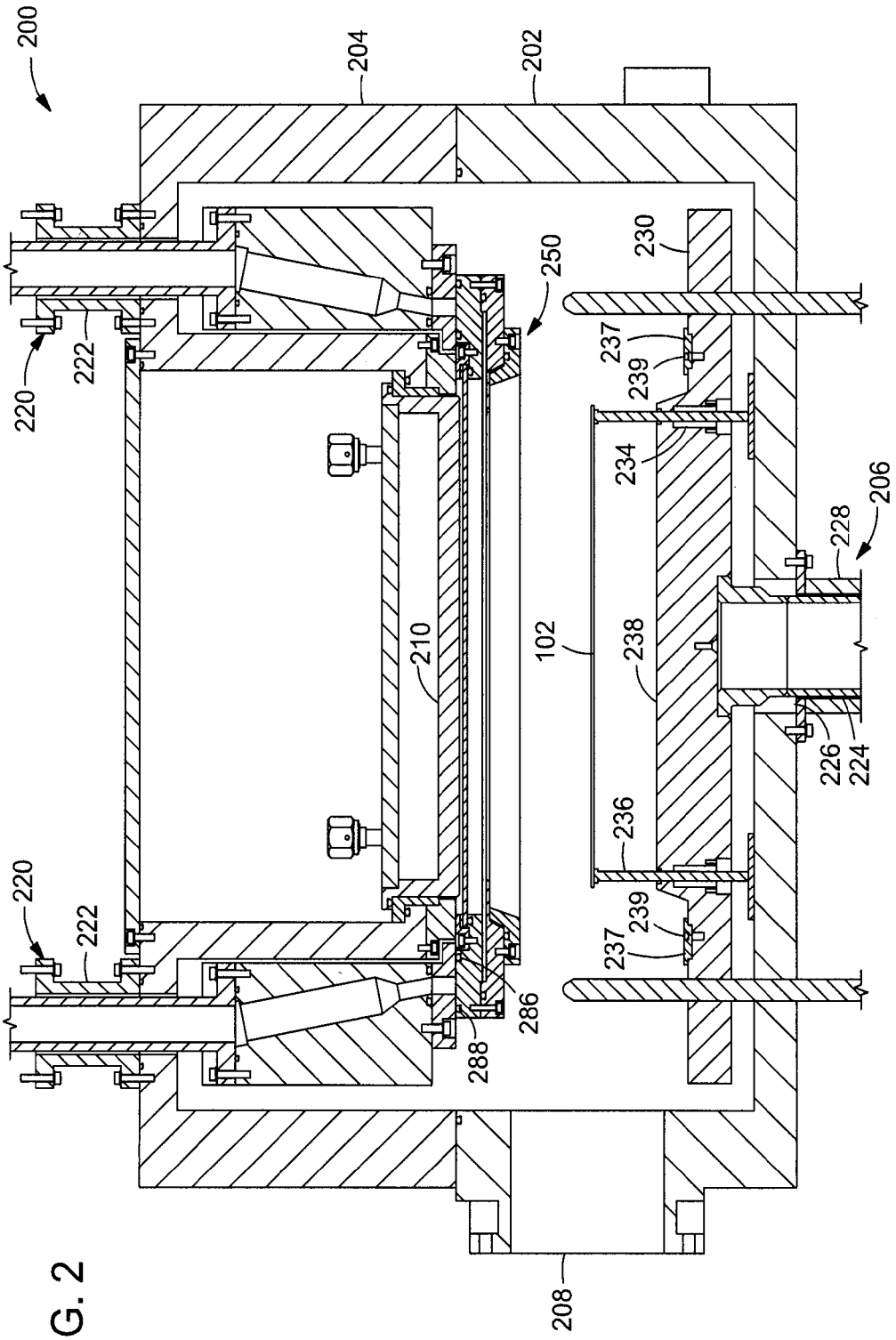
134
138
139
150

FIG. 1


200
204
202
250
230
220
222
237
239
234
206
228
210
102
238
226
224
236
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222
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239
286
288
208

FIG. 2

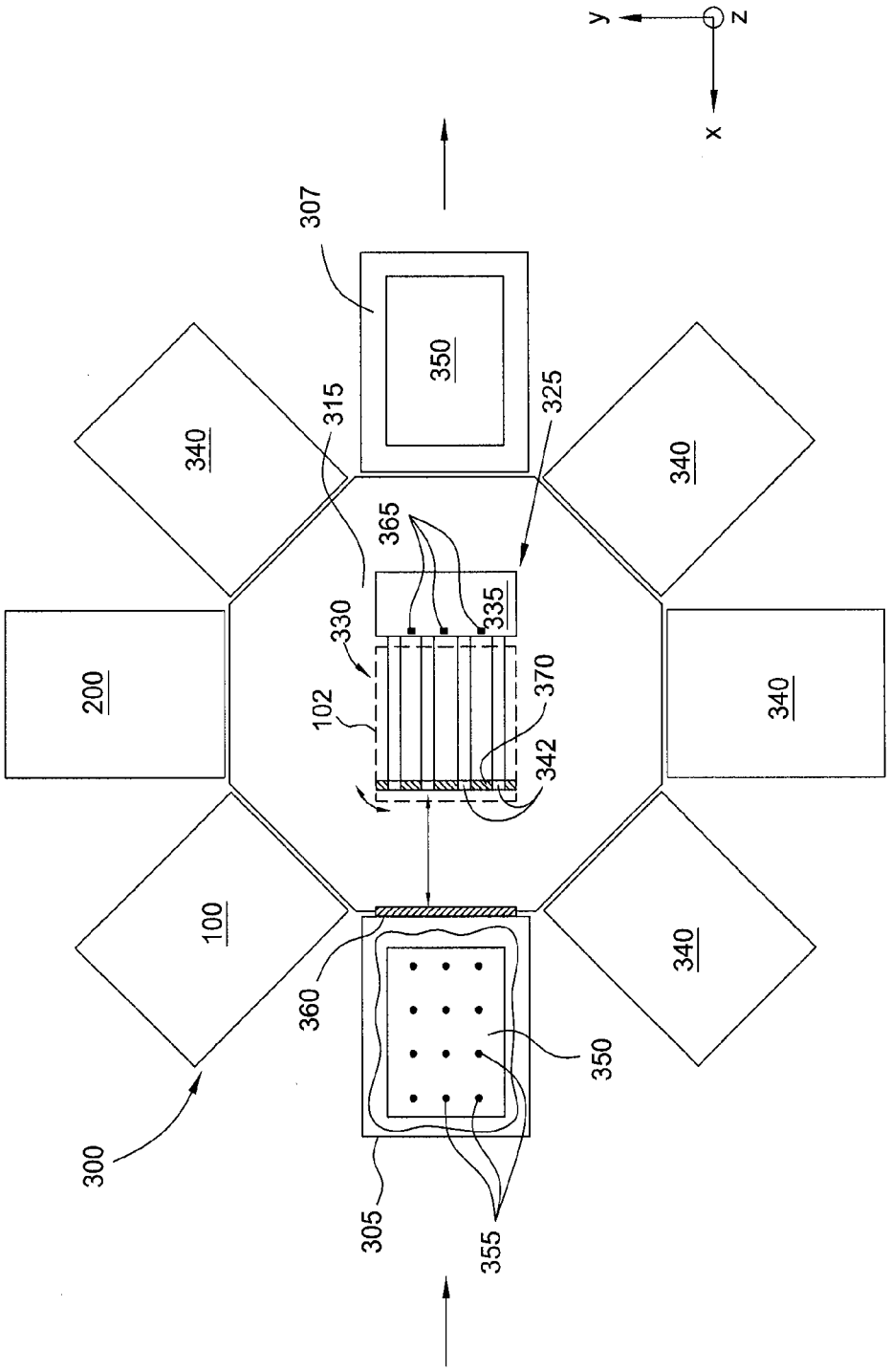

y
z
x
307
350
315
325
340
340
365
335
330
200
340
102
370
342
100
340
360
350
300
305
355

FIG. 3

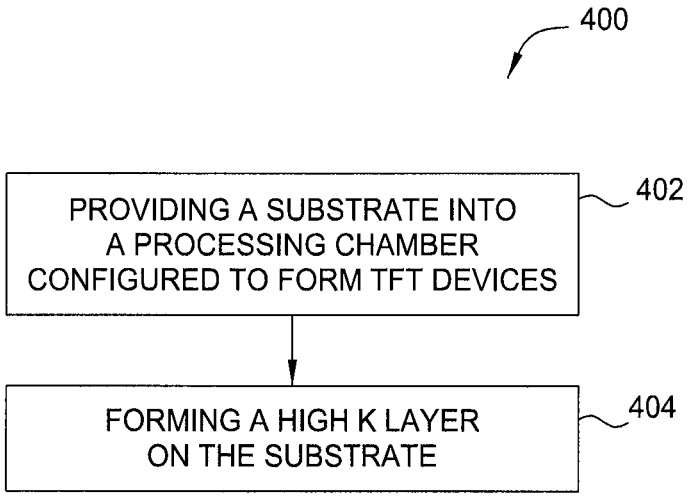

400
PROVIDING A SUBSTRATE INTO A PROCESSING CHAMBER CONFIGURED TO FORM TFT DEVICES
402
FORMING A HIGH K LAYER ON THE SUBSTRATE
404

FIG. 4

FIG. 5D

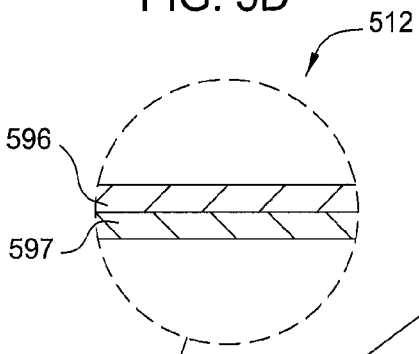
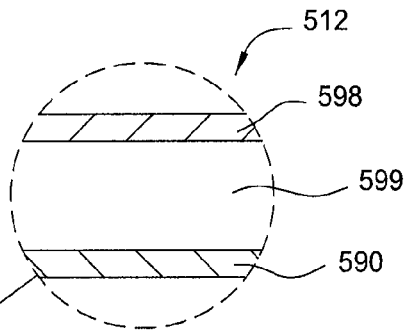


FIG. 5E



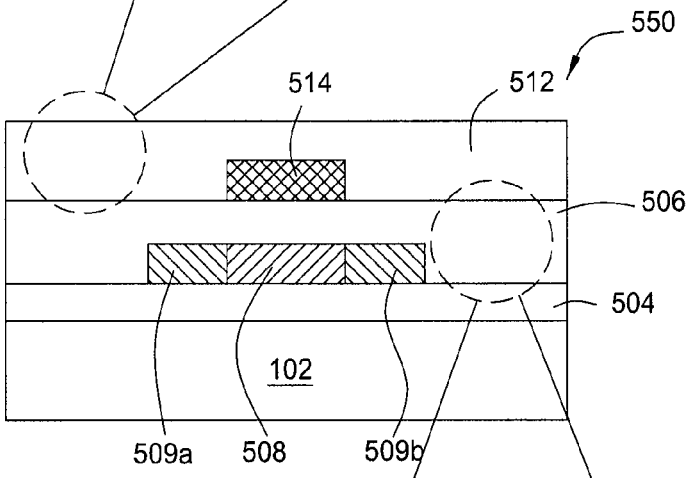


FIG. 5A

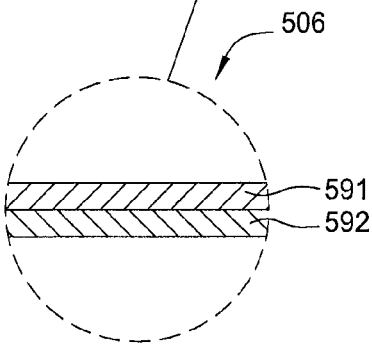


FIG. 5B

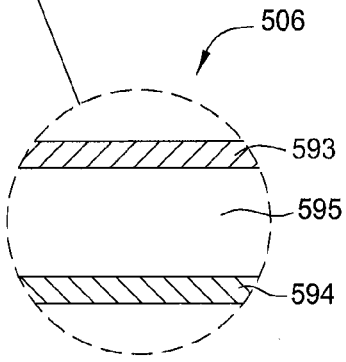
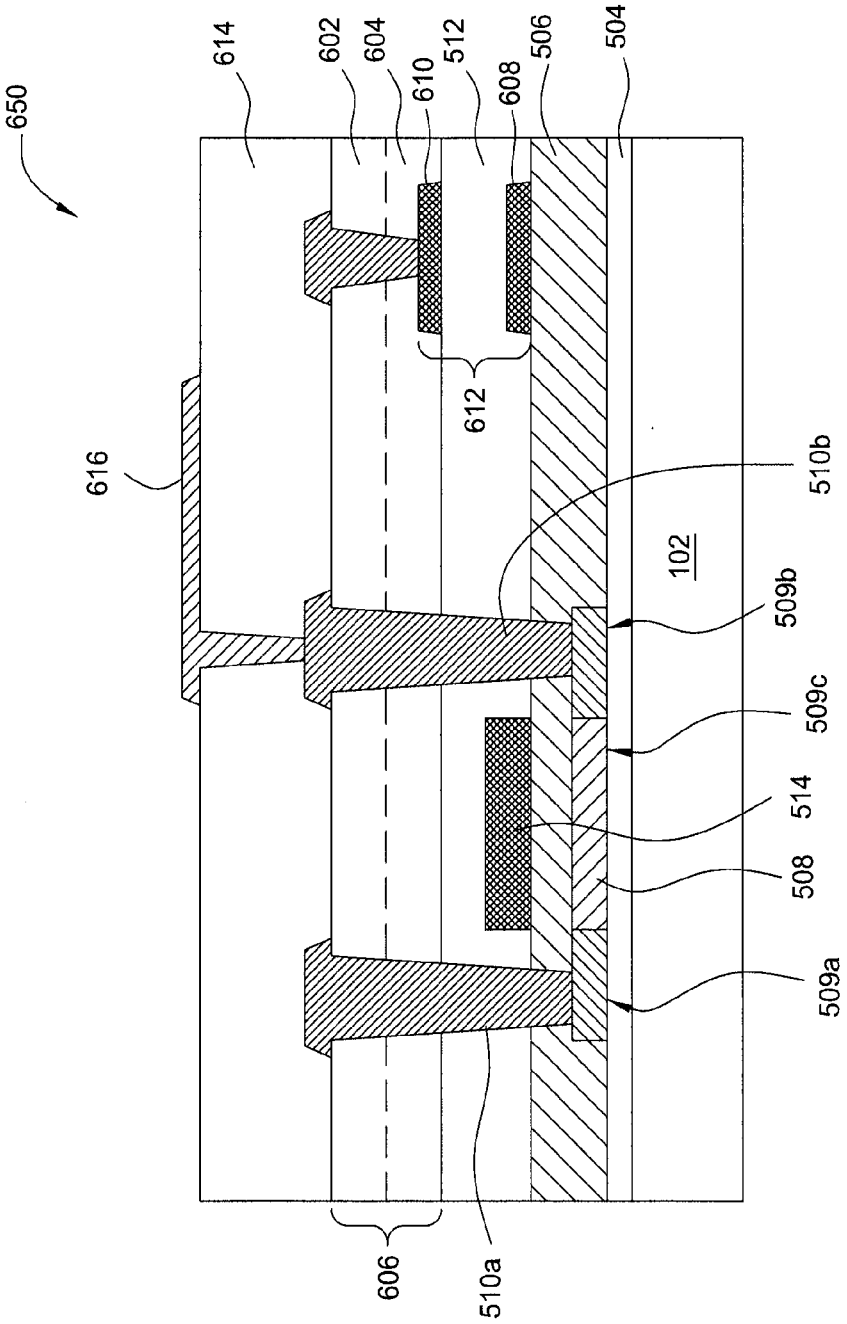


FIG. 5C


650
614
602
604
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512
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616
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510b
102
509b
509c
514
508
509a
606
510a

FIG. 6A

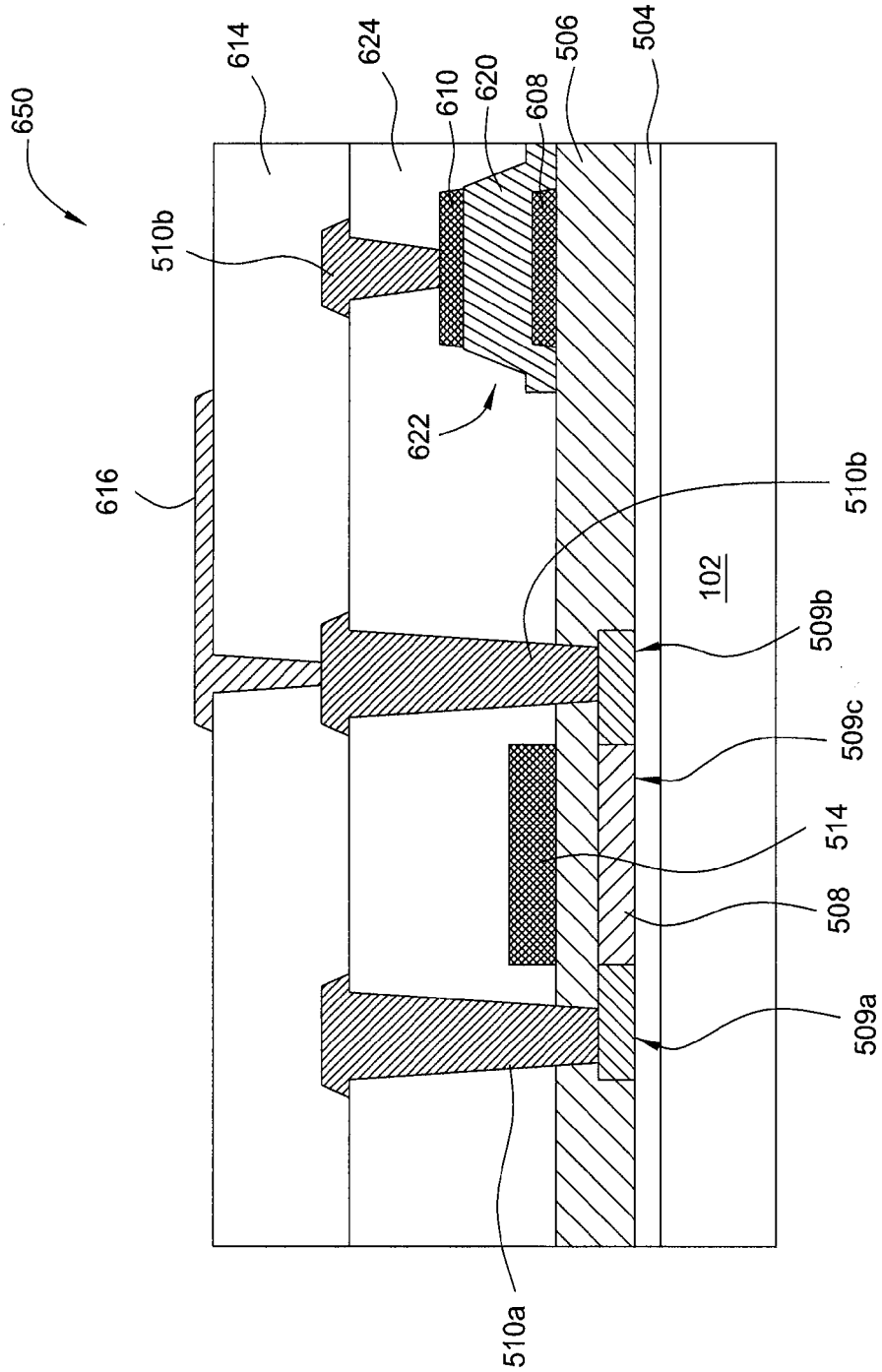
650
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FIG. 6B

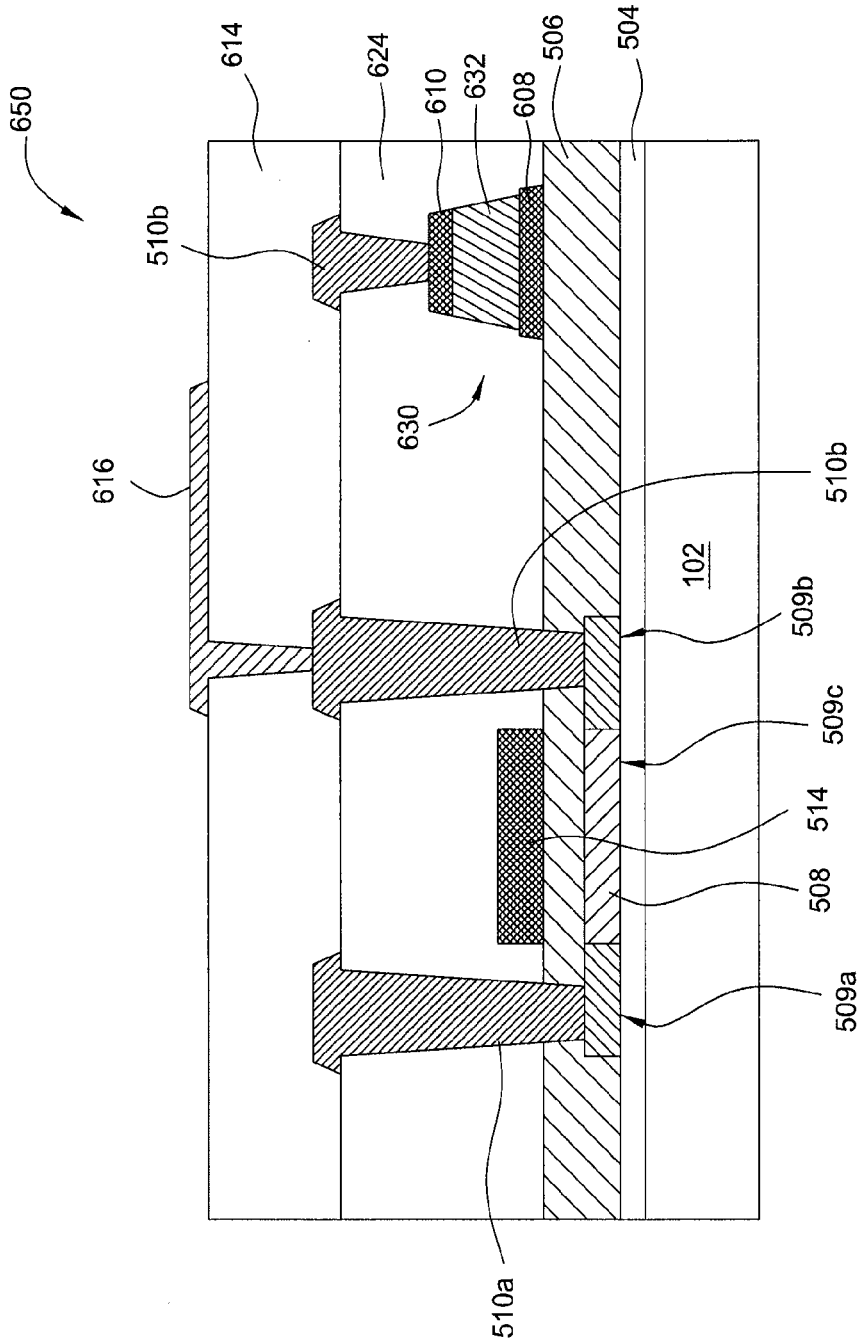
650
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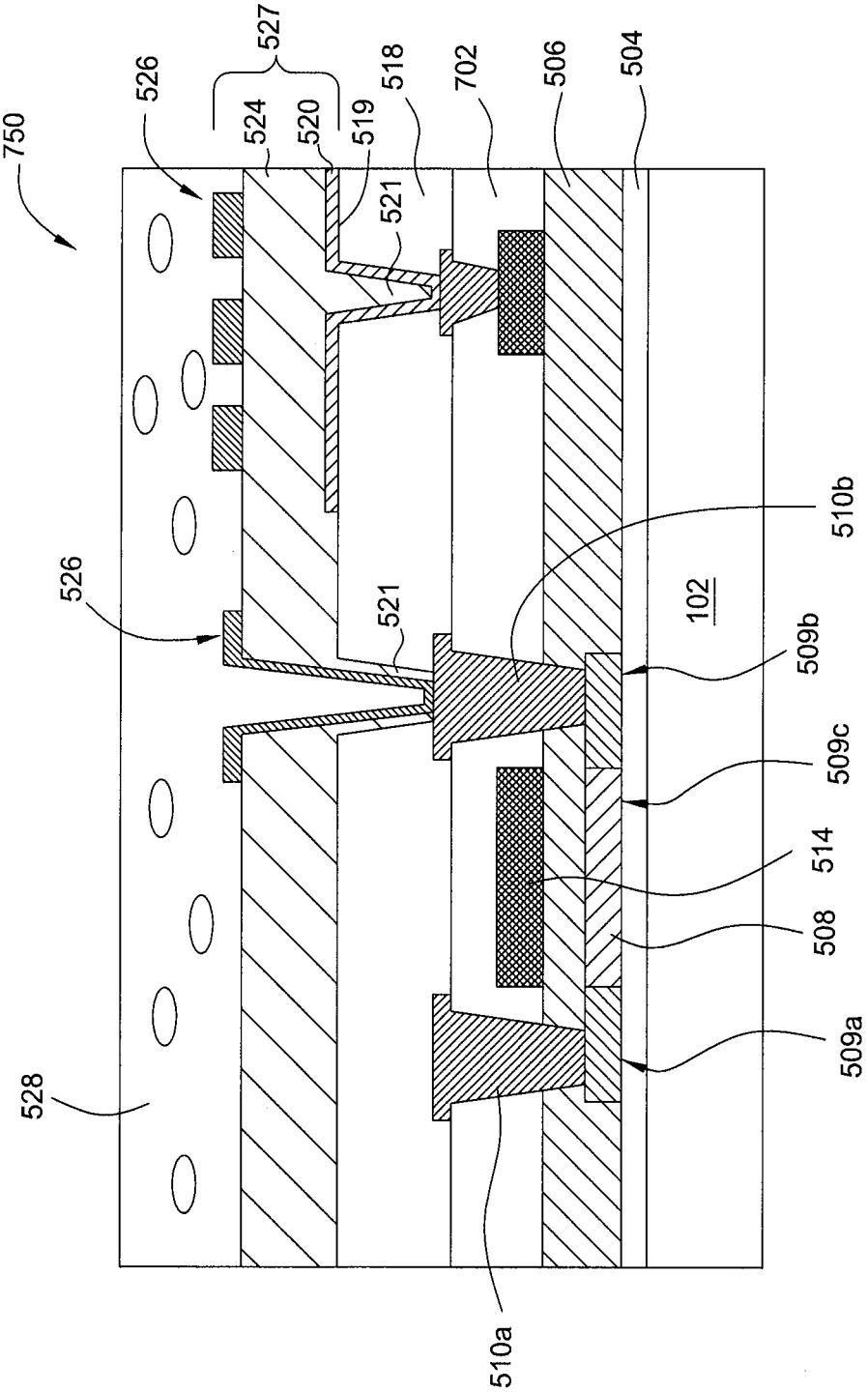
FIG. 6C


750
526
527
524
520
519
518
702
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521
526
521
510b
102
509b
509c
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508
509a
528
510a

FIG. 7

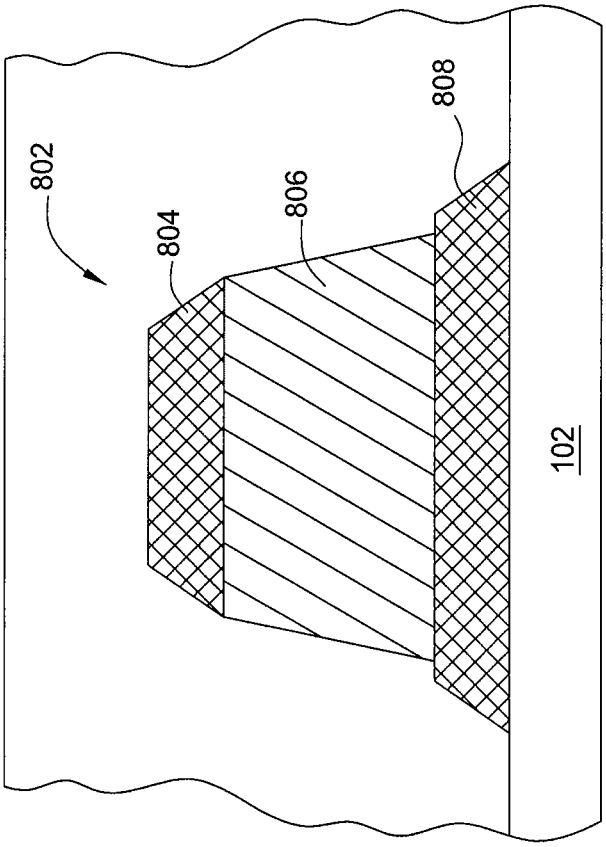
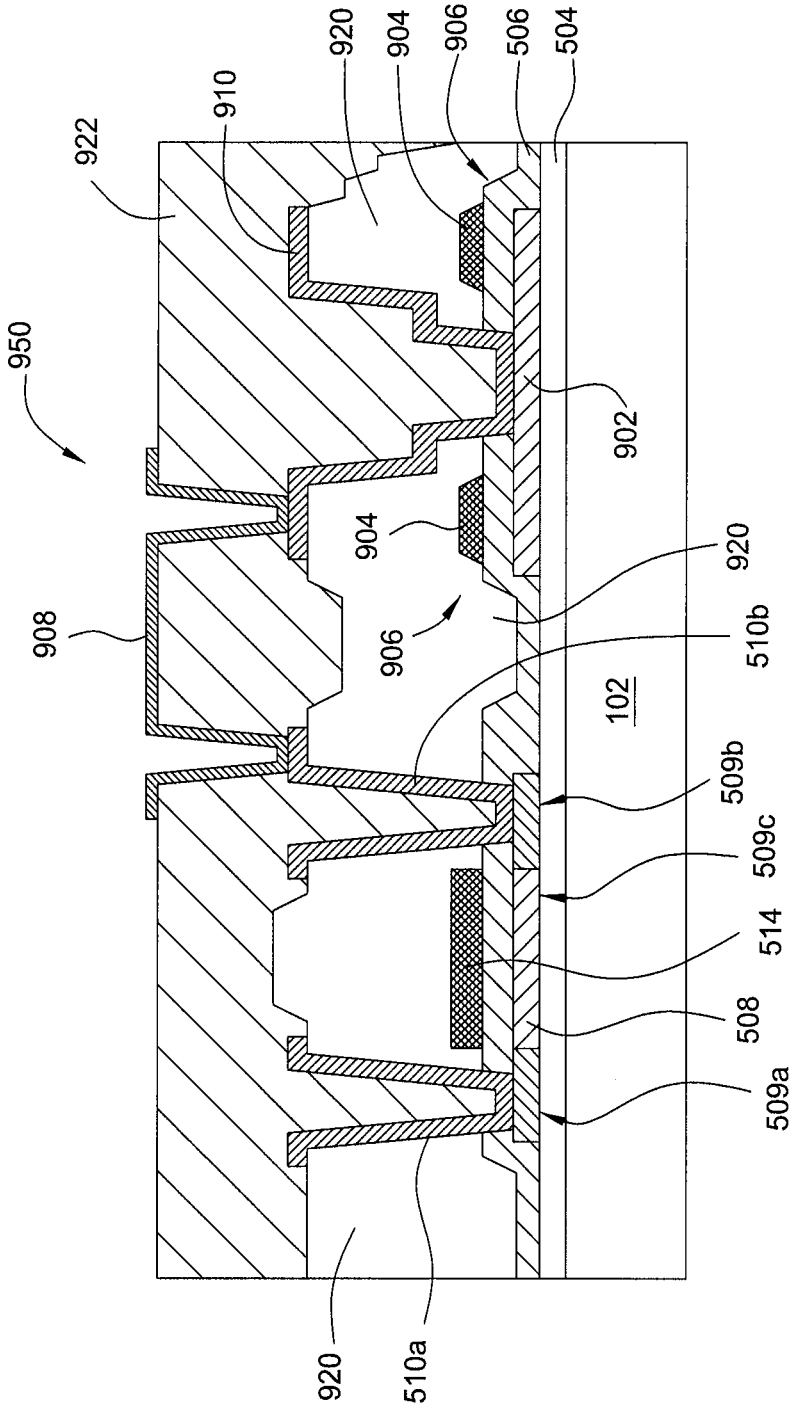


FIG. 8


950
922
910
920
904
906
506
504
902
908
904
906
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510b
102
509b
509c
514
508
509a
920
510a

FIG. 9

HIGH-K DIELECTRIC MATERIALS UTILIZED IN DISPLAY DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of U.S. Provisional Application Ser. No. 62/292,017 filed Feb. 5, 2016 (Attorney Docket No. APPM/23649L), which is incorporated by reference in its entirety.

BACKGROUND

[0002] Field

[0003] Embodiments of the present disclosure generally relate to forming a dielectric layer having a high dielectric constant for display devices. More particularly, embodiments of the disclosure relate to methods for forming a dielectric layer having a high dielectric constant by an atomic layer deposition (ALD) process with high film density and low film leakage for display applications.

[0004] Description of the Related Art

[0005] Display devices have been widely used for a wide range of electronic applications, such as TV, monitors, mobile phone, MP3 players, e-book readers, and personal digital assistants (PDAs) and the like. The display device is generally designed for producing desired image by applying an electric field to a liquid crystal that fills a gap between two substrates (e.g., a pixel electrode and a common electrode) and has anisotropic dielectric constant that controls the intensity of the dielectric field. By adjusting the amount of light transmitted through the substrates, the light and image intensity, quality and power consumption may be efficiently controlled.

[0006] A variety of different display devices, such as active matrix liquid crystal display (AMLCD) or an active matrix organic light emitting diodes (AMOLED), may be employed as light sources for display devices which utilize touch screen panels. In the manufacturing of display devices, an electronic device with high electron mobility, low leakage current and high breakdown voltage, would allow more pixel area for light transmission and integration of circuitry, thereby resulting in a brighter display, higher overall electrical efficiency, faster response time and higher resolution displays. Low film qualities of the material layers, such as dielectric layer with impurities or low film densities, formed in the device often result in poor device electrical performance and short service life of the devices. Thus, a stable and reliable method for forming and integrating film layers with in TFT and OLED devices becomes crucial to provide a device structure with low film leakage, and high breakdown voltage, for use in manufacturing electronic devices with lower threshold voltage shift and improved the overall performance of the electronic device are desired.

[0007] In particular, the interface management between a metal electrode layer and the nearby insulating materials becomes critical as improper material selection of the interface between the metal electrode layer and the nearby insulating material may adversely result in undesired elements diffusing into the adjacent materials, which may eventually lead to current short, current leakage or device failure. Furthermore, the insulating materials with different higher dielectric constant often provide different electrical performance, such as providing difference capacitance in the device structures. Selection of the material of the insulating materials not only affects the electrical performance of the device, incompatibility of the material of the insulating materials to the electrodes may also result in film structure peeling, poor interface adhesion, or interface material diffusion, which may eventually lead to device failure and low product yield.

[0008] In some devices, capacitors, e.g., a dielectric layer placed between to electrodes, are often utilized and formed to store electric charges when the display devices are in operation. The capacitor as formed is required to have high capacitance for display devices. The capacitance may be adjusted by changing of the dielectric constant and dimension of the dielectric layer formed between the electrodes and/or thickness of the dielectric layer. For example, when the dielectric layer is replaced with a material having a higher dielectric constant, the capacitance of the capacitor will increase as well. As the resolution requirement for display devices is increasingly challenging, e.g., display resolution greater than 800 ppi, only limited areas are remained in the display devices to allow forming capacitors therein to increase electrical performance. Thus, maintaining the capacitor formed in the display devices in a confined location with a relatively small area has become crucial.

[0009] Therefore, there is a need for improved methods for forming a dielectric layer with high dielectric constant with high film qualities and low leakage for manufacturing display devices that produce improved device electrical performance.

SUMMARY

[0010] Embodiments of the disclosure generally provide methods of forming an insulating layer, e.g., a capacitor layer or a gate insulating layer, with high dielectric constant as well as film qualities for display applications. In one embodiment, a thin film transistor structure includes source and drain electrodes formed on a substrate, a gate insulating layer formed on a substrate covering the source and drain electrodes, wherein the gate insulating layer is a high-k material having a dielectric constant greater than 10, and a gate electrode formed above or below the gate insulating layer.

[0011] In another embodiment, a method of forming a capacitor layer in display devices includes performing an atomic layer deposition process to form a capacitor layer on a substrate, wherein the capacitor layer has a dielectric constant greater than 10, wherein the capacitor layer is formed between two electrodes utilized in a thin film transistor device or an OLED device.

[0012] In yet another embodiment, a method for forming a hybrid layer in display devices includes forming a hybrid layer in display devices, wherein the hybrid layer includes a first dielectric layer formed by a chemical vapor deposition process and a second dielectric layer formed by an atomic layer deposition process, wherein the hybrid layer is formed as a capacitor layer or a gate insulating layer in the display devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] So that the manner in which the above recited features of the present disclosure are attained and can be understood in detail, a more particular description of the

disclosure, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0014] FIG. **1** depicts a sectional view of a processing chamber that may be used to deposit a dielectric layer in accordance with one embodiment of the present disclosure;

[0015] FIG. **2** depicts a sectional view of a processing chamber that may be used to deposit a dielectric layer in accordance with one embodiment of the present disclosure;

[0016] FIG. **3** is a schematic view of a multi-chamber substrate processing system including processing chambers described herein

[0017] FIG. **4** depicts a process flow diagram of one embodiment of a method of forming a dielectric layer on a substrate;

[0018] FIG. **5**A-**5**E is a sectional view of one example of a portion of a thin film transistor device structure having a dielectric layer of FIG. **4** formed therein;

[0019] FIGS. **6**A-**6**C are cross sectional view of different examples of a display device structure having a dielectric layer of FIG. **4** formed therein; and

[0020] FIG. **7** is a sectional view of one example of a display device structure having a dielectric layer of FIG. **4** formed therein;

[0021] FIG. **8** is a sectional view of a capacitor structure formed in a display device structure having a dielectric layer of FIG. **4** formed therein; and

[0022] FIG. **9** is a sectional view of one example of a display device structure having a dielectric layer of FIG. **4** formed therein.

[0023] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

[0024] It is to be noted, however, that the appended drawings illustrate only exemplary embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

DETAILED DESCRIPTION

[0025] Embodiments of the disclosure generally provide methods of forming a dielectric layer with enhanced electrical performance, such as high capacitance and low leakage, or an insulating layer with high dielectric constant for display devices. Such dielectric layer with high dielectric constant may be formed as a capacitor in display devices. The dielectric layer may be manufactured by an atomic layer deposition (ALD) process that may provide a film layer with low defect density, low impurities, low film leakage and high dielectric constant. The dielectric layer formed by the ALD process may be utilized in any insulating structure and/or capacitor structures in TFT devices or OLED devices. Additionally, the dielectric layer may be a hybrid layer as well formed by a combination of chemical vapor deposition (e.g., PECVD or MOCVD) process and an atomic layer deposition (ALD) process. In one example, the dielectric layer with the high dielectric constant may be used in any suitable layers, such as a gate insulating layer, a capacitor layer formed between two electrodes, an inter-insulating layer, an etching stop layer or an interface protection layer in display devices for electric performance enhancement and improvement.

[0026] FIG. **1** is a schematic cross-section view of one embodiment of a chemical vapor deposition processing chamber **100** in which a dielectric layer, such as an insulating layer, a capacitor layer formed between two electrodes, a gate insulating layer, an etch stop layer, a passivation layer, an interlayer insulator, a dielectric layer for capacitors or passivation layer in display device structures, may be deposited. One suitable chemical vapor deposition chamber, such as plasma enhanced CVD (PECVD) or metal organic CVD (MOCVD), is available from Applied Materials, Inc., located in Santa Clara, Calif. It is contemplated that other deposition chambers, including those from other manufacturers, may be utilized to practice the present disclosure.

[0027] The chamber **100** generally includes walls **142**, a bottom **104** and a lid **112** which bound a process volume **106**. A gas distribution plate **110** and substrate support assembly **130** are disposed with in a process volume **106**. The process volume **106** is accessed through a valve **108** formed through the wall **142** such that a substrate **102** may be transferred in to and out of the chamber **100**.

[0028] The substrate support assembly **130** includes a substrate receiving surface **132** for supporting the substrate **102** thereon. A stem **134** couples the substrate support assembly **130** to a lift system **136** which raises and lowers the substrate support assembly **130** between substrate transfer and processing positions. A shadow frame **133** may be optionally placed over periphery of the substrate **102** when processing to prevent deposition on the edge of the substrate **102**. Lift pins **138** are moveably disposed through the substrate support assembly **130** and are adapted to space the substrate **102** from the substrate receiving surface **132**. The substrate support assembly **130** may also include heating and/or cooling elements **139** utilized to maintain the substrate support assembly **130** at a desired temperature. The substrate support assembly **130** may also include grounding straps **131** to provide an RF return path around the periphery of the substrate support assembly **130**.

[0029] The gas distribution plate **110** is coupled at its periphery to a lid **112** or wall **142** of the chamber **100** by a suspension **114**. The gas distribution plate **110** may also be coupled to the lid **112** by one or more center supports **116** to help prevent sag and/or control the straightness/curvature of the gas distribution plate **110**. The gas distribution plate **110** may have different configurations with different dimensions. In an exemplary embodiment, the gas distribution plate **110** has a quadrilateral plan shape. The gas distribution plate **110** has a downstream surface **150** having a plurality of apertures **111** formed therein facing an upper surface **118** of the substrate **102** disposed on the substrate support assembly **130**. The apertures **111** may have different shapes, number, densities, dimensions, and distributions across the gas distribution plate **110**. In one embodiment, a diameter of the apertures **111** may be selected between about 0.01 inch and about 1 inch.

[0030] A gas source **120** is coupled to the lid **112** to provide gas through the lid **112** and then through the apertures **111** formed in the gas distribution plate **110** to the process volume **106**. A vacuum pump **109** is coupled to the chamber **100** to maintain the gas in the process volume **106** at a desired pressure.

[0031] An RF power source **122** is coupled to the lid **112** and/or to the gas distribution plate **110** to provide a RF power that creates an electric field between the gas distribution plate **110** and the substrate support assembly **130** so that a plasma may be generated from the gases present between the gas distribution plate **110** and the substrate support assembly **130**. The RF power may be applied at various RF frequencies. For example, RF power may be applied at a frequency between about 0.3 MHz and about 200 MHz. In one embodiment the RF power is provided at a frequency of 13.56 MHz.

[0032] In one embodiment, the edges of the downstream surface **150** of the gas distribution plate **110** may be curved so that a spacing gradient is defined between the edge and corners of the gas distribution plate **110** and substrate receiving surface **132** and, consequently, between the gas distribution plate **110** and the upper surface **118** of the substrate **102**. The shape of the downstream surface **150** may be selected to meet specific process requirements. For example, the shape of the downstream surface **150** may be convex, planar, concave or other suitable shape. Therefore, the edge to corner spacing gradient may be utilized to tune the film property uniformity across the edge of the substrate, thereby correcting property non-uniformity in films disposed in the corner of the substrate. Additionally, the edge to center spacing may also be controlled so that the film property distribution uniformity may be controlled between the edge and center of the substrate. In one embodiment, a concave curved edge of the gas distribution plate **110** may be used so the center portion of the edge of the gas distribution plate **110** is spaced farther from the upper surface **118** of the substrate **102** than the corners of the gas distribution plate **110**. In another embodiment, a convex curved edge of the gas distribution plate **110** may be used so that the corners of the gas distribution plate **110** are spaced farther than the edges of the gas distribution plate **110** from the upper surface **118** of the substrate **102**.

[0033] A remote plasma source **124**, such as an inductively coupled remote plasma source, may also be coupled between the gas source and the gas distribution plate **110**. Between processing substrates, a cleaning gas may be energized in the remote plasma source **124** to remotely provide plasma utilized to clean chamber components. The cleaning gas entering the process volume **106** may be further excited by the RF power provided to the gas distribution plate **110** by the power source **122**. Suitable cleaning gases include, but are not limited to, NF_3, F_2, and SF_6.

[0034] In one embodiment, the substrate **102** that may be processed in the chamber **100** may have a surface area of 10,000 cm^2 or more, such as 25,000 cm^2 or more, for example about 55,000 cm^2 or more. It is understood that after processing the substrate may be cut to form smaller other devices.

[0035] In one embodiment, the heating and/or cooling elements **139** may be set to provide a substrate support assembly temperature during deposition of about 600 degrees Celsius or less, for example between about 100 degrees Celsius and about 500 degrees Celsius, or between about 200 degrees Celsius and about 500 degrees Celsius, such as about 300 degrees Celsius and 500 degrees Celsius.

[0036] The nominal spacing during deposition between the upper surface **118** of the substrate **102** disposed on the substrate receiving surface **132** and the gas distribution plate **110** may generally vary between 400 mil and about 1,200 mil, such as between 400 mil and about 800 mil, or other distance required to obtain desired deposition results. In one exemplary embodiment wherein the gas distribution plate **110** has a concave downstream surface, the spacing between the center portion of the edge of the gas distribution plate **110** and the substrate receiving surface **132** is between about 400 mils and about 1400 mils, and the spacing between the corners of the gas distribution plate **110** and the substrate receiving surface **132** is between about 300 mils and about 1200 mils.

[0037] FIG. **2** is a schematic cross sectional view of an ALD (atomic layer deposition) chamber **200** that may be used to perform a deposition described herein. The ALD deposition process may be utilized to form a dielectric layer, such as an insulating layer, a gate insulating layer, an etch stop layer, an interlayer insulator, a dielectric layer for capacitor or passivation layer in display devices as described herein. The chamber **200** generally includes a chamber body **202**, a lid assembly **204**, a substrate support assembly **206**, and a process kit **250**. The lid assembly **204** is disposed on the chamber body **202**, and the substrate support assembly **206** is at least partially disposed within the chamber body **202**. The chamber body **202** includes a slit valve opening **208** formed in a sidewall thereof to provide access to the interior of the processing chamber **200**. In some embodiments, the chamber body **202** includes one or more apertures that are in fluid communication with a vacuum system (e.g., a vacuum pump). The apertures provide an egress for gases within the chamber **200**. The vacuum system is controlled by a process controller to maintain a pressure within the ALD chamber **200** suitable for ALD processes. The lid assembly **204** may include one or more differential pumps and purge assemblies **220**. The differential pump and purge assemblies **220** are mounted to the lid assembly **204** with bellows **222**. The bellows **222** allow the pump and purge assemblies **220** to move vertically with respect to the lid assembly **204** while still maintaining a seal against gas leaks. When the process kit **250** is raised into a processing position, a compliant first seal **286** and a compliant second seal **288** on the process kit **250** are brought into contact with the differential pump and purge assemblies **220**. The differential pump and purge assemblies **220** are connected with a vacuum system (not shown) and maintained at a low pressure.

[0038] As shown in FIG. **2**, the lid assembly **204** includes a RF cathode **210** that can generate a plasma of reactive species within the chamber **200** and/or within the process kit **250**. The RF cathode **210** may be heated by electric heating elements (not shown), for example, and cooled by circulation of cooling fluids, for example. Any power source capable of activating the gases into reactive species and maintaining the plasma of reactive species may be used. For example, RF or microwave (MW) based power discharge techniques may be used. The activation may also be generated by a thermally based technique, a gas breakdown technique, a high intensity light source (e.g., UV energy), or exposure to an x-ray source.

[0039] The substrate support assembly **206** can be at least partially disposed within the chamber body **202**. The substrate support assembly **206** can include a substrate support member or susceptor **230** to support a substrate **232** for processing within the chamber body. The susceptor **230** may be coupled to a substrate lift mechanism (not shown) through a shaft **224** or shafts **224** which extend through one or more openings **226** formed in a bottom surface of the

chamber body **202**. The substrate lift mechanism can be flexibly sealed to the chamber body **202** by a bellows **228** that prevents vacuum leakage from around the shafts **224**. The substrate lift mechanism allows the susceptor **230** to be moved vertically within the ALD chamber **200** between a lower robot entry position, as shown, and processing, process kit transfer, and substrate transfer positions. In some embodiments, the substrate lift mechanism moves between fewer positions than those described.

[0040] In some embodiments, the substrate **232** may be secured to the susceptor using a vacuum chuck (not shown), an electrostatic chuck (not shown), or a mechanical clamp (not shown). The temperature of the susceptor **230** may be controlled (by, e.g., a process controller) during processing in the ALD chamber **200** to influence temperature of the substrate **232** and the process kit **250** to improve performance of the ALD processing. The susceptor **230** may be heated by, for example, electric heating elements (not shown) within the susceptor **230**. The temperature of the susceptor **230** may be determined by pyrometers (not shown) in the chamber **200**, for example.

[0041] As shown in FIG. **2**, the susceptor **230** can include one or more bores **234** through the susceptor **230** to accommodate one or more lift pins **236**. Each lift pin **236** is mounted so that they may slide freely within a bore **234**. The support assembly **206** is movable such that the upper surface of the lift pins **236** can be located above the substrate support surface **238** of the susceptor **230** when the support assembly **206** is in a lower position. Conversely, the upper surface of the lift pins **236** is located below the upper surface **238** of the susceptor **230** when the support assembly **206** is in a raised position. When contacting the chamber body **202**, the lift pins **236** push against a lower surface of the substrate **232**, lifting the substrate off the susceptor **230**. Conversely, the susceptor **230** may raise the substrate **102** off of the lift pins **236**.

[0042] In some embodiments, the susceptor **230** includes process kit insulation buttons **237** that may include one or more compliant seals **239**. The process kit insulation buttons **237** may be used to carry the process kit **250** on the susceptor **230**. The one or more compliant seals **239** in the process kit insulation buttons **237** are compressed when the susceptor lifts the process kit **850** into the processing position.

[0043] FIG. **3** is a top plan view of a multi-chamber substrate processing system **300** suitable for the fabrication of any suitable display devices, such as organic light emitting diodes (OLEDS), thin-film transistors (TFT), and solar cell fabrication on flat media. The system **300** includes a plurality of processing chambers **100**, **200**, **340** and one or more load lock chambers **305**, **307** positioned around a central transfer chamber **315**. The processing chambers **100**, **200**, **340** may be configured to complete a number of different processing steps to achieve a desired processing of flat media, such as a large area substrate **102** (outlined in dashed lines). The load lock chambers **305**, **307** are configured to transfer a substrate in a quadrilateral form from an ambient environment outside the multi-chamber substrate processing system **300** to a vacuum environment inside the transfer chamber **315**.

[0044] Positioned within the transfer chamber **315** is a transfer robot **325** having an end effector **330**. The end effector **330** is configured to be supported and move independently of the transfer robot **325** to transfer the substrate **102**. The end effector **330** includes a wrist **335** and a plurality of fingers **342** adapted to support the substrate **102**. In one embodiment, the transfer robot **325** is configured to be rotated about a vertical axis and/or linearly driven in a vertical direction (Z direction) while the end effector **330** is configured to move linearly in a horizontal direction (X and/or Y direction) independent of and relative to the transfer robot **325**. For example, the transfer robot **325** raises and lowers the end effector **330** (Z direction) to various elevations within the transfer chamber **315** to align the end effector **330** with openings in the processing chambers **100**, **200**, **340** and the load lock chambers **305**, **307**. When the transfer robot **325** is at a suitable elevation, the end effector **330** is extended horizontally (X or Y direction) to transfer and/or position the substrate **102** into and out of any one of the processing chambers **100**, **200**, **340** and the load lock chambers **305**, **307**. Additionally, the transfer robot **325** may be rotated to align the end effector **330** with other processing chambers **100**, **200**, **340** and the load lock chambers **305**, **307**.

[0045] In one example, the processing chambers **100**, **200**, **340** incorporated in the multi-chamber substrate processing system **300** may be the chemical vapor deposition (PECVD or MOCVD) chamber **100** depicted in FIG. **1** and the atomic layer deposition (ALD) chamber **200** depicted in FIG. **2** or other suitable chambers, such as HDP-CVD, MOCVD, PECVD, thermal CVD, thermal annealing, PVD, surface treatment, electron beam (e-beam) treatment, plasma treatment, etching chambers, ion implantation chambers, surface cleaning chamber, metrology chambers, spin-coating chamber, polymer spinning deposition chamber or any suitable chambers as needed. In one example depicted in the multi-chamber substrate processing system **300**, the system **300** includes the chemical vapor deposition (such as a PECVD) chamber **100**, the atomic layer deposition (ALD) chamber **200** and other suitable chambers **340** as needed. By such arrangement, the dielectric layer formed by the ALD process and/or the PECVD process may also be integrated to perform in a single chamber without breaking vacuum so as to maintain cleanliness of the substrate without undesired contamination and residuals from the environment.

[0046] A portion of the interior of load lock chamber **305** has been removed to expose a substrate support or susceptor **350** that is adapted to receive and support the large area substrate **102** during processing. The susceptor **350** includes a plurality of lift pins **355** that are movable relative to an upper surface of the susceptor **350** to facilitate transfer of the large area substrate **102**. In one example of a transfer process of the large area substrate **102**, the lift pins **355** are extended away from or above the upper surface of the susceptor **350**. The end effector **330** extends in the X direction into the processing chamber **100**, **200**, **340** or load lock chambers **305**, **307** above the extended lift pins. The transfer robot **325** lowers the end effector **330** in the Z direction until the large area substrate **102** is supported by the lift pins **355**. The lift pins **355** are spaced to allow the fingers **340** of the end effector **330** to pass the lift pins **355** without interference. The end effector **330** may be further lowered to assure clearance between the large area substrate **102** and the fingers **340** and the end effector **330** is retracted in the X direction into the transfer chamber **315**. The lift pins **355** may be retracted to a position that is substantially flush with the upper surface of the susceptor **350** in order to bring the large area substrate **102** into contact with the susceptor **350** so the susceptor **350** supports the large area substrate **102**. A

slit valve or door **360** between the transfer chamber **315** and the load lock chamber **305**, **307** (or the processing chamber or **100**, **200**, **340**) may be sealed and processing may be commenced in the load lock chamber **305**, **307** (or the processing chambers **100**, **200**, **340**). To remove the large area substrate **102** after processing, the transfer process may be reversed, wherein the lift pins **355** raise the large area substrate **102** and the end effector **330** may retrieve the large area substrate **102**. In one example, the substrate **102** may be transferred into the multi-chamber substrate processing system **300** through the first load lock chamber **305**. After the substrate **102** is oriented and aligned to a desired position, the substrate **102** is then transferred to any one of the processing chambers **100**, **200**, **340** through the transfer chamber **315** to perform any suitable processes as needed to form a device structure on the substrate **102**. After the processes are completed in the processing chambers **100**, **200**, **340**, then the substrate **102** is removed from and transferred out of the multi-chamber substrate processing system **300** from the second load lock chamber **307** as needed.

[0047] The environment in the substrate processing system **300** is isolated from ambient pressure (i.e. pressure outside the system **300**) and is maintained at a negative pressure by one or more vacuum pumps (not shown). During processing, the processing chambers **100**, **200**, **340** are pumped down to pre-determined pressures configured to facilitate thin film deposition and other processes. Likewise, the transfer chamber **315** is held at a reduced pressure during transfer of the large area substrates to facilitate a minimal pressure gradient between the processing chambers **100**, **200**, **340** and the transfer chamber **315**. In one embodiment, the pressure in the transfer chamber **315** is maintained at a pressure lower than ambient pressure. For example, the pressure in the transfer chamber may be about 7 Torr to about 10 Torr while the pressure in the processing chambers **100**, **200**, **340** may be lower. In one embodiment, the maintained pressure within the transfer chamber **315** may be substantially equal to the pressure within the processing chambers **100**, **200**, **340** and/or load lock chambers **305** and **307** to facilitate a substantially equalized pressure in the system **300**.

[0048] During the transfer of the large area substrate **102** in the transfer chamber **315** and the processing chambers **100**, **200**, **340**, proper alignment of the large area substrate **102** is crucial to prevent collisions and/or damage of the large area substrate **102**. Additionally, the interior of the system **300** must be kept clean and free from debris such as broken pieces of a substrate, broken equipment, and other particulate contamination. While some conventional systems include view windows allowing line of sight viewing into the interior of the various chambers **100**, **200**, **340**, the windows may not allow a full view and/or precise inspection of the large area substrates and the interior of the various chambers **100**, **200**, **340**. Also, the conventional systems are not configured to view the large area substrate **102** and provide a metric of processing results while the large area substrates are in the system.

[0049] The transfer robot **325** includes one or more optical image sensors **365** and **370** disposed on the transfer robot **325** as needed. The one or more optical image sensors **365**, **370** may be optical scanners, imagers or cameras, such as a charged-coupled device (CCD), a complimentary metal oxide semiconductor (CMOS) device, a video camera, and the like. In one embodiment, one or more of the optical image sensors **365**, **370** are mounted on the transfer robot **325** in a position to view the large area substrate **102**, the fingers **340** and any object in the line of sight view of the sensors **365**, **370**. In this embodiment, the image sensors **365**, **370** may be oriented to view objects substantially in the X and Y direction as well as the Z direction as the transfer robot **325** is stationary or moving in the system **300**. The image sensors **365**, **370** may include wide angle optics, such as a fisheye lens, to enable a greater field of view.

[0050] FIG. **4** depicts a flow diagram of one embodiment of a process **400** for forming an insulating layer suitable for use in display devices, such as thin-film transistor devices or OLED devices. Such insulating layer may be formed as a capacitor layer disposed between two metal layers to form a capacitor. Suitable examples of the insulating layer used in display devices include a gate insulating layer, a capacitor layer disposed between two metal layers, an interface layer, a dielectric layer utilized to form a capacitor, an etch stop layer or a passivation layer where an insulating material is needed. The insulating layer may be formed by a plasma enhanced chemical vapor deposition (PECVD) process or a metal organic chemical vapor deposition (MOCVD) process, which may be practiced in the processing chamber **100**, as described in FIG. **1**, or an atomic layer deposition (ALD) process, which may be practiced in the processing chamber **200**, as described in FIG. **2**, or other suitable processing chamber, or in combination thereof.

[0051] The process **400** begins at operation **402** by providing the substrate **102** in a processing chamber, such as the processing chamber **100** (a PECVD chamber) or processing chamber **200** (an ALD chamber) depicted in FIG. **3**, to form an insulating layer or a dielectric layer. The substrate **102** may include a TFT device **550** partly formed thereon readily to form a gate insulating layer **506** or an capacitor layer **512**, as shown in FIGS. **5A-5E**, or other suitable layers in the device **550**.

[0052] Referring first to FIG. **5A**, a portion of the exemplary TFT device **550** formed on the substrate **102** comprises a low temperature polysilicon (LTPS) TFT or OLED device. The substrate **102** may have different combination of films, structures or layers previously formed thereon to facilitate forming different device structures or different film stack on the substrate **102**. The substrate **102** may be any one of glass substrate, plastic substrate, polymer substrate, metal substrate, singled substrate, roll-to-roll substrate, or other suitable transparent substrate suitable for forming a thin film transistor thereon.

[0053] The LTPS TFT devices **550** are MOS devices built with a source region **509***a*, channel region **508**, and drain region **509***b* formed on the optically transparent substrate **502** with or without an optional insulating layer **504** disposed thereon. The source region **509***a*, channel region **508**, and drain region **509***b* are generally formed from an initially deposited amorphous silicon (a-Si) layer that is typically later thermal or laser processed to form a polysilicon layer. The source, drain and channel regions **509***a*, **508**, **509***b* can be formed by patterning areas on the optically transparent substrate **102** and ion doping the deposited initial a-Si layer, which is then thermally or laser processed (e.g., an Excimer Laser Annealing process) to form the polysilicon layer. The gate insulating layer **506** (e.g., the insulating layer or dielectric layer to be deposited by the process **400** of FIG. **4**) may be then deposited on top of the deposited polysilicon layer(s)

to isolate a gate electrode **514** from the channel region **508**, source region **509***a* and drain regions **509***b*. The gate electrode **514** is formed on top of the gate insulating layer **506**. The gate insulating layer **506** is also commonly known as a gate oxide layer. A capacitor layer **512** (e.g., also the insulating layer or dielectric layer to be deposited by the process **400** of FIG. **4**) and device connections are then made through the insulating material to allow control of the TFT devices.

[0054] The device **550** of FIGS. **5**A-**5**E is just partially formed for ease of description and explanation regarding to the corresponding process **400** depicted in FIG. **4** utilized to form either the gate insulating layer **506** or the capacitor layer **512**, or both, in the device **550**. A relatively complete device **550** will be described below with referenced to FIGS. **6**A-**6**C, **7** and **9**.

[0055] At operation **404**, a deposition process is then performed on the substrate **102** to form an insulating layer or a dielectric layer on the substrate as depicted in FIG. **4**. The deposition process may form a dielectric layer with a dielectric constant greater than 10, such as greater than 15, for example greater than 20. In one example, the deposition process may be an ALD process that may form the dielectric layer with a high dielectric constant greater than 10. In another example, the deposition may be a hybrid process including a PECVD process (or any suitable CVD processes) and an ALD process to form a hybrid layer including dielectric materials formed from both PECVD and ALD processes with high film density as well as relatively high manufacturing throughput. Alternatively, a plasma assisted ALD (PE-ALD) process may also be used to form the dielectric layer with high dielectric constant greater than 10.

[0056] It is believed that a dielectric layer formed by an atomic layer deposition (ALD) process may have film properties that may provide desired high moisture resistance, high film density, low defect density and high film transparency. It is believed that the ALD process is enabled by a slow deposition process with a first monolayer of atoms being absorbed and adhered on a second monolayer of atoms formed on a carefully selected substrate surface. Strong adherence of atoms in each layers and absorbability of the layers of atoms onto the surface of substrate provide compact and secured bonding structures in the film structures so as to render a film property with a high film density (compared to a chemical vapor deposition process) that may efficiently eliminate loose film structure in the dielectric layer that may result in current leakage. Furthermore, the high film density may also prevent moisture or contaminant from penetrating therethrough. Furthermore, the slow ALD deposition rate of the dielectric layer at operation **404** also allows the atoms from the dielectric layer to gradually fill in the pinholes, pores, pits or defects that may be occurred from the substrate surface so as to assist repairing the film defects from the substrate surface.

[0057] In contrast, the plasma enhanced chemical vapor deposition process (or other suitable chemical vapor deposition process) often provides a relatively fast deposition process with high manufacturing throughput but renders relatively porous film structures for the resultant film layer. Thus, in some example while high manufacturing throughput is desired, by forming a dielectric layer by the hybrid process (e.g., including both PECVD and ALD processes), a relatively high film density of the dielectric layer may be obtained under relatively high throughput process. In yet another example, a plasma assisted atomic layer deposition (PE-ALD) process may be utilized instead to provide a relatively higher deposition rate (compared to ALD or thermal ALD) of deposition process while still maintaining the desired degree of film density.

[0058] In one example, the dielectric layer at operation **404** may be formed as the gate insulating layer **506** and/or the capacitor layer **512** in a single layer form depicted in FIG. **5**A. The gate insulating layer **506** and/or the capacitor layer **512** may be formed on the substrate **102** by transferring the substrate **102** to a deposition chamber, such as the ALD chamber **200** depicted in FIG. **2**, to perform an atomic layer deposition process on the substrate **102**. In one example, the gate insulating layer **506** and/or the capacitor layer **512** may be a high-k material having a dielectric constant greater than 10. Suitable examples of the high-k material layer include hafnium dioxide (HfO_2), hafnium oxynitride (HfON), zirconium dioxide (ZrO_2), zirconium oxynitride (ZrON), aluminum oxide (Al_2O_3), aluminum oxynitride (AlON), hafnium silicon oxide ($HfSiO_2$), hafnium aluminum oxide (HfAlO), zirconium silicon oxide ($ZrSiO_2$), tantalum dioxide (Ta_2O_5), aluminum oxide, Y_2O_3, La_2O_3, titanium oxide (TiO_2), aluminum doped hafnium dioxide, bismuth strontium titanium (BST), and platinum zirconium titanium (PZT), among others.

[0059] In another example, the gate insulating layer **506** and/or the capacitor layer **512** may be in form of multiple layers as shown in the circles of FIGS. **5**B and **5**C or in the circles of FIGS. **5**D and **5**E respectively with different film stack arrangements or configurations.

[0060] In the example depicted in FIG. **5**B, the gate insulating layer **506** may include two layers having a first dielectric layer **592** formed by a CVD process and a second dielectric layer **591** by an ALD process, or vise versa. Both the first dielectric layer **592** and the second dielectric layer **591** could be formed as high-k materials. However, as a dielectric layer, such as a silicon oxide or silicon nitride, formed by a CVD may generally not have a film dielectric constant greater than 10, in some examples, the first dielectric layer **592** formed by a CVD process may be a regular dielectric layer (e.g., having a dielectric layer less than 10) while the second dielectric layer **591** formed as a high-k material, or vice versa.

[0061] In the example depicted in FIG. **5**C, the gate insulating layer **506** may include in total three layers **594**, **595**, **593** formed therein. For example, the gate insulating layer **506** may include the bulk gate insulating layer **595** sandwiched between the top dielectric layer **593** and the bottom dielectric layer **594**. The top dielectric layer **593** may be in contact with the capacitor layer **512** later formed thereon while the bottom dielectric layer **594** may be formed in contact with the optional insulating layer **504**. In this particular example, the bulk gate insulating layer **595** may be fabricated by a high-k material formed by an ALD or a MOCVD process while the top and the bottom dielectric layers **593**, **594** may be silicon containing dielectric materials, such as silicon nitride silicon oxide (SiO_2), silicon oxynitride (SiON), silicon oxycarbide (SiOC), silicon carbide (SiC) and the like, formed from a PECVD process. In one example, the top and the bottom dielectric layers **593**, **594** may be a silicon oxynitride (SiON) or silicon nitride (SiN) material when the bulk gate insulating layer **595** is a high-k material as depicted in FIG. **5**C.

[0062] In yet another embodiment, the deposition process performed at operation **404** may form the capacitor layer **512** on the gate insulating layer **506**. In the example depicted in FIG. **5**D, the capacitor layer **512** may include two layers having a first dielectric layer **597** formed by a CVD process and a second dielectric layer **596** by an ALD process or a MOCVD, or vise versa. Both the first dielectric layer **597** and the second dielectric layer **596** may be formed as high-k materials. However, as a dielectric layer, such as a silicon oxide or silicon nitride, formed by a CVD may generally not have a film dielectric constant greater than 10, in some examples, the first dielectric layer **592** formed by a CVD process may be a regular dielectric layer (e.g., having a dielectric layer less than 10) while the second dielectric layer **591** formed as a high-k material, or vice versa.

[0063] In the example depicted in FIG. **5**E, the capacitor layer **512** may include in total three layers **598**, **599**, **590** formed therein. For example, the capacitor layer **512** may include the bulk capacitor layer **599** sandwiched between the top dielectric layer **598** and the bottom dielectric layer **590**. The top dielectric layer **598** may be in contact with an interlayer insulator **606** (as an example shown in FIG. **6**A) later formed thereon while the bottom dielectric layer **590** may be formed in contact with the gate insulating layer **506**. In this particular example, the bulk capacitor layer **599** may be fabricated by a high-k material formed by an ALD or MOCVD process while the top and the bottom dielectric layers **598**, **590** may be silicon containing dielectric materials, such as silicon nitride silicon oxide (SiO_2), silicon oxynitride (SiON), silicon oxycarbide (SiOC), silicon carbide (SiC) and the like, formed from a PECVD process. In one example, the top and the bottom dielectric layers **598**, **590** may be a silicon oxynitride (SiON) or silicon nitride (SiN) material when the bulk capacitor layer **599** is a high-k material as depicted in FIG. **5**E.

[0064] FIGS. **6**A-**6**C depict TFT device structures **650** with the gate insulating layer **506** and/or the capacitor layer **512**, **620**, **632** comprising high-k materials. Referring first to the example depicted in FIG. **6**A, after the capacitor layer **512** is formed, an interlayer insulator **606** may be formed on the capacitor layer **512**. The interlayer insulator **606** may be any suitable dielectric layer, such as silicon oxide or silicon nitride materials. The interlayer insulator **606** may be in form of a single layer formed on the capacitor layer **512**. Alternatively, the interlayer insulator **606** may be in form of multiple layers, such as two layers **602**, **604**, as the example depicted in FIG. **6**A, as needed for different devices requirement. In the example depicted in FIG. **6**A, the interlayer insulator **606** includes a first dielectric layer **602** of silicon nitride formed on a second layer **604** of a silicon oxide layer. Subsequently, a source-drain metal electrode layer **510***a*, **510***b* is then deposited, formed and patterned in the interlayer insulator **606**, the capacitor layer **512** and the gate insulating layer **506** electrically connected to the source region **509***a* and drain regions **509***b*.

[0065] After the source-drain metal electrode layer **510***a*, **510***b* is patterned, the planarization layer **614** is then formed over the source-drain metal electrode layer **510***a*, **510***b*. The planarization layer **614** may be fabricated from polyimide, benzocyclobutene-series resin, spin on glass (SOG) or acrylate. The planarization layer **518** is later patterned to allow a pixel electrode **616** to be formed on and filled in the planarization layer **518**, electrically connecting to the source-drain metal electrode layer **510***a*, **510***b*.

[0066] In this example depicted in FIG. **6**A, the capacitor layer **512** is formed on the gate electrode **514** extending to a capacitor structure **612** (e.g., a MIM (metal-insulating-metal) structure) formed between an upper electrode **610** and a lower electrode **608**. The upper electrode **610** may be laterally coupled to the source-drain metal electrode layer **510***a*, **510***b* while the lower electrode **608** may be laterally coupled to the gate electrode **514**, or other suitable electrodes in the device structure **650**. The capacitor structure **612** formed in the device structure **650** may be a storage capacitor that may improve the display device electrical performance. It is noted that the capacitor structure **612** may be formed in any location suitable in the device structure **650** as needed for different device performance requirement.

[0067] In another example depicted in FIG. **6**B, a capacitor structure **622**, similar to the capacitor structure **612** depicted in FIG. **6**A, may be formed with different dimension and/or profile of a capacitor layer **620** formed between the upper electrode **610** and the lower electrode **608**. Unlike the capacitor layer **512** extends from the area above the gate electrode **514** to the area between the upper and the lower electrode **608**, **610**, the capacitor layer **620** depicted in FIG. **6**B is formed substantially in the area between the upper and the lower electrode **608**. Thus, a regular interlayer insulator **624** comprising silicon oxide or silicon oxide may be formed on the gate insulting layer **506** surrounding the capacitor structure **622** formed therein. The capacitor layer **620** may have a bottom surface in contact with the lower gate insulating layer **506** as needed. The interlayer insulator **624** may be in a single layer form, as depicted in FIG. **6**B, or in multiple layer form as needed.

[0068] In yet another example depicted in FIG. **6**C, a capacitor structure **630**, similar to the capacitor structure **612**, **622** depicted in FIGS. **6**A and **6**B, may be formed with different dimensions and/or profiles of a capacitor layer **632** formed between the upper electrode **610** and the lower electrode **608**. In this particular example, the capacitor layer **632** depicted in FIG. **6**C is confined in the area between the upper and the lower electrode **608**, **610** without in contact with the lower gate insulating layer **506** so as to eliminate etching selectivity issues during the patterning process. It is noted that such capacitor layers **632**, **620**, **512** may also be in a single layer form of a single high-k material or multiple layer form of multiple layers comprising high-k material, as depicted in FIGS. **5**A and **5**D-**5**E, as needed.

[0069] FIG. **7** depicts yet another example of a TFT device structure **750** with the gate insulating layer **506**, optionally a high-k material, and a regular interlayer insulator **702** comprising silicon oxide or silicon nitride. A planarization layer **518** is formed over the source-drain metal electrode layer **510***a*, **510***b* to provide a planar surface **519** where a common electrode **520** may be later formed thereon and patterned. The planarization layer **518** may be fabricated from polyimide, benzocyclobutene-series resin, spin on glass (SOG) or acrylate. The planarization layer **518** is later patterned to form a via contact hole **521** that allows the common electrode **520** along with a capacitor layer **524** and/or a pixel electrode **526** to be sequentially filled therein. It is noted the capacitor layer **524** formed in the device structure **750** may also formed by a high-k material from a PECVD or MOCVD process, such as the process in the processing chamber **100** depicted in FIG. **1**, or an ALD process, such as the process in the processing chamber **200** depicted in FIG. **2**.

[0070] It is noted that the TFT structure shown in FIG. **7** is just an exemplary embodiment of the TFT device **750**. The via contact hole **521** may be filled partly or fully by the common electrode **520**, the capacitor layer **524** or the pixel electrode **526** in any configuration as needed. The pixel electrode **526** and the common electrode **520** along with the capacitor layer **524** formed therebetween, in combination, form the capacitor structure **527** (e.g., a MIM (metal-insulating-metal) structure) in the TFT device **750**, as illustrated in the example depicted in FIG. **7**. After the pixel electrode **526** is formed, other insulating layer **528**, such as an organic layer or a liquid crystal layer, may be formed on the structure of the capacitor structure **527** to further complete the structure of the device **750**.

[0071] It is noted that the material layer formed by the operation **404** may be utilized to form the capacitor layer **524**, **512**, **620**, **632**, gate insulating layer **506**, a passivation layer or any other suitable layers that require insulating materials in the TFT device structures **650** and **750** including LTPS TFT for LCD or OLED TFT as needed, as depicted in FIGS. **6**A-**6**C and **7**.

[0072] FIG. **8** depicts a simple capacitor structure **802** (e.g., a MIM (metal-insulating-metal) structure) that may be formed on the substrate **102** utilized in any location in display devices. Similar the upper electrode **610** and the lower electrode **608**, or the pixel electrode **526** and the common electrode **520**, depicted above, the capacitor structure **802** includes a top electrode **804** and a bottom electrode **808** having a capacitor layer **806** disposed in between to form the capacitor structure **802**. The capacitor layer **806** comprises a high-k material similar to the capacitor layer **524**, **512**, **620**, **632** described above. The capacitor layer **806** may also in form of any numbers of the layers as needed.

[0073] FIG. **9** depicts yet another example of a TFT device structure **950**. Similar to the structure described above, the device structure **950** includes a regular interlayer insulator **920** disposed on the gate electrode **514**. A passivation layer **922** may be formed on the interlayer insulator **920**. Another portion of the source and drain region **902** (electrically connected to the source and drain region **509***a*, **509***b*) is shown on the optional insulating layer **504**. Another portion of the source-drain metal electrode layer **910** (electrically connected to the source and drain metal electrode **510***a*, **510***b*) is disposed on and electrically coupled to the source and drain region **902**. A pixel electrode **908** may be electrically connected to the source-drain metal electrode layer **910**, **510***a*, **510***b*. In this particular example, a portion of the gate insulating layer **506** passes through and between the gate electrode **514** and the channel region **508**, extending to the area above the source and drain region **902**. An additional electrode **904** is formed above the source and drain region **902** and the gate insulating layer **506**, forming a capacitor structure **906** in the device structure **950**. The additional electrode **904** formed on the gate insulating layer **506** (now also serves as a capacitor layer) may be electrically connected to the gate electrode **514**. Thus, the additional electrode **904** and the source and drain region **902** along with the gate insulating layer **506** formed therebetween form the capacitor structure **906** in the device structure **950**. Similarly, the gate insulating layer **506**, now also serves as a capacitor layer, may be similar to the capacitor layer **524**, **512**, **620**, **632** described above may be in form of any numbers of the layers as needed.

[0074] It is noted that the source-drain metal electrode layer **510***a*, **510***b*, **910**, the pixel electrode **526**, **908**, the common electrode **520**, the gate electrode **514**, the upper electrode **610**, the lower electrode **608**, the top electrode **804**, the bottom electrode **808**, additional electrode **904** and any electrodes in the device structures may be any suitable metallic materials, including transparent conductive oxide layer (such as ITO or the like), silver nano ink, carbon nano tube (CNT), silver nano ink and CNT, graphene, aluminum (Al), tungsten (W), chromium (Cr), tantalum (Ta), molybdenum (Mo), copper (Cu), combination thereof or any suitable materials.

[0075] It is noted that the structures above the passivation layer **922** or the insulating layer **528**, the planarization layer **614** is eliminated for sake of brevity. However, in some exemplary device structures, an additional OLED or LCD devices, or other suitable devices may be formed above the insulating layer **528**, passivation layer **922** or the planarization layer **614** to form other suitable flexible mobile display devices, such as LTPS OLED display devices with touch screen panels as needed.

[0076] Thus, the methods described herein advantageously improve the electron stability, electrical performance, low leakage and good film stack integration of display device structures by controlling the materials, particular a high-k material formed by either an ALD process and a PECVD or MOCVD process, and structures of a gate insulating layer, capacitor layer, interlayer insulator, passivation layer, insulating materials in the display devices, along with a dielectric layer formed as a capacitor in the display devices with desired high electrical performance.

[0077] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A thin film transistor structure comprising:

source and drain electrodes formed on a substrate;

a gate insulating layer formed on a substrate covering the source and drain electrodes, wherein the gate insulating layer is a high-k material having a dielectric constant greater than 10; and

a gate electrode formed above or below the gate insulating layer.

2. The structure of claim **1**, further comprising:

a capacitor layer formed on the gate electrode, wherein the capacitor layer is fabricated from a high-k material having a dielectric constant greater than 10.

3. The structure of claim **2**, wherein the high-k material of the gate insulating layer or the capacitor layer is formed by an atomic layer deposition process.

4. The structure of claim **1**, wherein the high-k material is at least one of hafnium dioxide (HfO_2), hafnium oxynitride (HfON), zirconium dioxide (ZrO_2), zirconium oxynitride (ZrON), aluminum oxide (Al_2O_3), aluminum oxynitride (AlON), hafnium silicon oxide ($HfSiO_2$), hafnium aluminum oxide (HfAlO), zirconium silicon oxide ($ZrSiO_2$), tantalum dioxide (Ta_2O_5), aluminum oxide, Y_2O_3, La_2O_3, titanium oxide (TiO_2), aluminum doped hafnium dioxide, bismuth strontium titanium (BST), or platinum zirconium titanium (PZT).

5. The structure of claim **1**, wherein the gate insulating layer comprises a bulk gate insulating layer formed on a bottom dielectric layer.

6. The method of claim **5**, wherein the gate insulating layer further comprises a top dielectric layer formed on the bulk gate insulating layer disposed on the bottom dielectric layer.

7. The structure of claim **6**, wherein the bulk gate insulating layer is formed by a high-k material and the top and bottom dielectric layer is formed by a silicon containing material.

8. The structure of claim **6**, wherein the silicon containing material is formed by a plasma enhanced chemical vapor deposition process, a MOCVD or ALD process.

9. The structure of claim **2**, wherein the capacitor further comprises a bulk capacitor layer formed on a bottom dielectric layer.

10. The structure of claim **9**, wherein the capacitor layer further comprises a top dielectric layer formed on the bulk capacitor layer formed on the bottom dielectric layer.

11. The structure of claim **2**, further comprising:

an insulating layer formed between a common electrode and a pixel electrode disposed on the interlayer insulator, wherein the insulating layer, the common electrode and the pixel electrode in combination form a capacitor, wherein the insulating layer is a high-k material fabricated by an atomic layer deposition process.

12. The structure of claim **11**, further comprising:

a passivation layer formed on the capacitor, wherein the passivation layer is a high-k material fabricated from an atomic layer deposition process.

13. A method of forming a capacitor layer in display devices, comprising:

performing an atomic layer deposition process to form a capacitor layer on a substrate, wherein the capacitor layer has a dielectric constant greater than 10, wherein the capacitor layer is formed between two electrodes utilized in a thin film transistor device or an OLED device.

14. The method of claim **13**, further comprising:

performing a plasma enhanced chemical vapor deposition process prior to the atomic layer deposition process to form a silicon containing layer between the electrode and the capacitor layer.

15. The method of claim **13**, further comprising:

performing a chemical vapor deposition process to form a silicon containing layer on the capacitor layer.

16. The method of claim **13**, wherein the capacitor layer is a gate insulating layer, an interlayer insulator, an insulating layer, or a passivation layer in a TFT device.

17. The method of claim **13**, wherein the capacitor layer and the two electrodes form a storage capacitor in display devices.

18. A method for forming a hybrid layer in display devices, comprising:

forming a hybrid layer in display devices, wherein the hybrid layer includes a first dielectric layer formed by a chemical vapor deposition process and a second dielectric layer formed by an atomic layer deposition process, wherein the hybrid layer is formed as a capacitor layer or a gate insulating layer in the display devices.

19. The method of claim **18**, wherein the hybrid layer comprises a high-k material having a dielectric constant greater than 10.

20. The method of claim **19**, wherein the high-k material is at least one of hafnium dioxide (HfO_2), hafnium oxynitride (HfON), zirconium dioxide (ZrO_2), zirconium oxynitride (ZrON), aluminum oxide (Al_2O_3), aluminum oxynitride (AlON), hafnium silicon oxide ($HfSiO_2$), hafnium aluminum oxide (HfAlO), zirconium silicon oxide ($ZrSiO_2$), tantalum dioxide (Ta_2O_5), aluminum oxide, Y_2O_3, La_2O_3, titanium oxide (TiO_2), aluminum doped hafnium dioxide, bismuth strontium titanium (BST), or platinum zirconium titanium (PZT).

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