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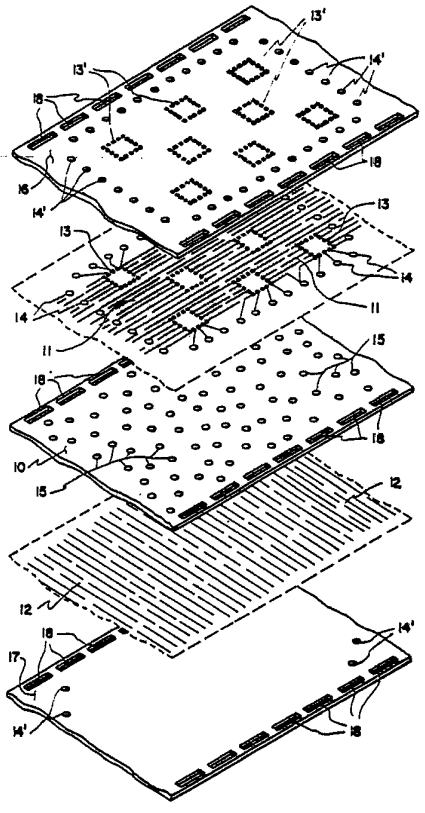
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(54) Title: MULTIPLE INTEGRATED CIRCUIT INTERCONNECTION ARRANGEMENT

(57) Abstract

A flexible chip interconnection means includes a flexible film (10) having interconnection lines (11, 12) formed on opposite sides thereof, with selected of the interconnection lines from one side connected by through-film conductors (15) to interconnection lines on the other side. Insulating layers (16, 17) cover both sets of lines on the other side. Insulating layers cover both sets of interconnection lines. Multi-chip circuits can be formed on the film with the interconnection lines directly connecting the chips.



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MULTIPLE INTEGRATED CIRCUIT INTERCONNECTION ARRANGEMENT

BACKGROUND OF THE INVENTION

The present invention relates to the electrical interconnecting of monolithic integrated circuits, and more particularly, to interconnecting monolithic integrated circuits in a preformed interconnection structure of only a small area.

Monolithic integrated circuits must be mounted in some mechanically secure manner during use, and must be electrically interconnected with other portions of the electronic system in which it is to operate. There is a desire to accomplish this in as little space as possible and at the lowest cost possible while assuring reliable interconnection during use in a chosen environment.

A typical approach is to mount such monolithic integrated circuit chips on a printed circuit board or on a ceramic substrate. Electrical interconnections to the chip electrical terminations are made from conductive tracks provided on the surface of such board or substrate. There are limits, however, to how closely monolithic integrated circuits can be arrayed on printed circuit boards due to limitations in printed circuit board track placement

technology. Closer packing is possible on ceramic substrates, but they are relatively expensive.

The density of monolithic integrated circuits across such substrates can often be increased, and the cost of mounting and interconnecting such integrated circuits on substrates and boards can be reduced through the use of chip carrier films. Such films are of an electrical insulator material having conductive interconnections provided thereon. In each "frame" along the film, an individual monolithic integrated circuit is connected to the corresponding set of interconnectors therein which radiate into the chip often bridging an opening in the film frame interior over which the chip is provided. That is, the frame interconnections from the edges of the film around the frame opening to chip electrical interconnections, the opening being provided under the ends of the tape interconnections to which the monolithic integrated circuit is interconnected and under the chip itself.

Such a film can have many frames and so many integrated circuits contained therein, one in each frame. The film with such integrated circuits can then be provided to a bonding machine which may automatically index a frame forward for each bonding, cut the tape interconnections near the edge of the film opening, and bond the remaining ends of the tape

interconnections to a board or substrate to thereby interconnect the chip in the frame thereto.

Because the tape interconnections can be made quite small, some improvement in density can be achieved at least on ceramic substrates. The use of tape carrier feed in an automatic bonding machine can aid in the reduction of cost. However, greater integrated circuit packing densities are desired along with a further reduction in cost.

SUMMARY OF THE INVENTION

The present invention provides a means for interconnecting a plurality of monolithic integrated circuits through use of a flexible insulating film with electrical interconnections on either side which are themselves interconnected at selected locations through the flexible film. There is an insulating layer over each group of interconnections on either side of the flexible film with openings in the layers to permit interconnection of monolithic integrated circuits, other circuit components, or interconnections to external circuits. The insulating layer on the side opposite that to which the monolithic integrated circuits are connected is positioned beneath the connection place for such integrated circuits to support the flexible carrier during the interconnection of the integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an exploded view of a portion of the present invention,

Figure 2 shows an integrated portion of the present invention, and

Figure 3 shows a cross section of a portion of Figure 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows an exploded view of levels of a flexible, electrical interconnection means for monolithic integrated circuits and possibly other circuit components. If to be provided as part of a tape, the portion shown would be a "frame" in such tape. The tape would consist of a repeated number of such frames.

At the center or core of the interconnection means is a polyimide film, 10, which is the flexible electrical insulating material. This film is typically one or two mils in thickness. Again, if the portion of such film shown is in the form of a tape, this portion would repeat and these duplicates would extend in an elongated fashion to the right and to the left of the break lines shown. However, though the structure shown in Figure 1, and that in Figure 2 for that matter, suggest the interconnection means in the

form of a tape, a form which is very convenient, the interconnection means could be provided in the form of a sheet having repeated patterns extending in more than one or two directions.

Adhering to a major surface on each side of film 10 are a group of fine conductive interconnection lines or interconnections, a first group, 11, shown above film 10 and a second group, 12, shown below film 10. These are shown with dashed lines around them to suggest there is a layer devoted to each group, but the interconnections are independent from each other within the group with which there is no actual physical conductive contact.

The interconnections in group 11 are shown drawn all in one direction as they are in group 12 also in an orthogonal direction, but this is a matter of design convenience and is not necessarily the only geometrical pattern which could be used. Group 11 shows an inteconnection pattern in several places, 13, adapted for accepting interconnections of monolithic integrated circuits. Furthermore, group 11 also shows a series of interconnection terminals, 14, along the sides thereof suitable for use in connecting to external circuits. Such external circuit interconnections can also be made by the group 12 interconnections.

Typically, each of the interconnections in groups 11 and 12 are formed of copper over chromium with the chromium adhering to film 10. Each interconnection may be as fine as two mils wide with a spacing of again two mils from one another, edge to edge. Such fine interconnection lines and close spacing are provided using common metal deposition and photolithography techniques. For instance, the sputtering of chromium and some copper onto film 10 can be followed by electroplating the remaining copper to the desired thickness. Then, using photolithography methods common in intergrated circuit fabrication, the patterns for each of the interconnections in groups 11 and 12 can be defined and formed. Selected registration markings may be provided in the same manner, such markings being used to determine relative positions on either side of film 10.

In addition, selected interconnections in group 11 are electrically interconnected to selected interconnections in group 12 through electrical conductors provided in openings, 15, in film 10. Copper is plated through these openings to provide such through-film interconnections.

Protecting each of interconnection groups 11 and 12, and also electrically insulating these groups

from external items, except as desired through openings provided in these layers, are protective layers. The upper one of these protective layers, 16, is over group 11 and on exposed portions of the corresponding major surface of film 10. The lower one of these protective layers, 17, is over group 12 and on exposed portions of the corresponding major surface of film 10. Protective layers 16 and 17 are of flexible electrical insulating material, again typically polyimide. Openings are provided in protective layers 16 and 17 to accommodate providing interconnections to terminations 13, for monolithic integrated circuit chips, and to terminations 14, including those terminations occurring below the interconnections in group 12, for providing interconnections to external circuits. These openings in protective layer 16 are designated 13' and 14' in accordance with the terminations in interconnection group 11. Similarly, there are some openings provided for external connection through protective layer 17 also designated 14' which correspond to terminations in interconnection group 12.

Further shown in Figure 1, for the situation in which the interconnection means portion of Figure 1 is part of a tape, are sprocket holes, 18, for sprockets to drive the tape in a machine adapted for

use in combining the portion shown in Figure 1 into a next higher assemblage in a manufacturing process. Sprocket holes 18 are precisely located with respect to the patterns of interconnections in Figure 1 including those of group 11 and 12, and with the openings for interconnections 15 in film 10. Thus, control means driving such sprockets in such a machine can precisely position such a tape along the direction this tape is driven by them.

A typical next assembly for such an interconnection means once the monolithic integrated circuit components have been mounted thereon, along with any other circuit components to be also mounted, would be to provide this interconnection means on a printed wiring board or on a ceramic substrate. Other circuits on such a board or substrate could then be interconnected to those in the integrated circuit means of Figure 1 by interconnections from terminations 14 to such circuits. Because of the very dense packing of monolithic integrated circuits and other circuit components which can be achieved with the interconnection means of Figure 1, a printed circuit board or a ceramic substrate having such interconnection means used thereon would have thereon a considerable increase in circuit component density over that which could be otherwise achieved on such a

board, and a decrease in cost over what could be achieved with such a substrate.

Figure 2 shows as an integrated item the exploded view portion of Figure 1, with the layers of Figure 1 formed into a full series of interconnection means in abbreviated tape form. Figure 2 indicates monolithic integrated circuits chips, 20, to be mated and interconnected to such an interconnection means with a form suggesting thermocompression bonding of these chips. However, other bonding technologies can be used, such as ultrasonic bonding. The patterns of Figure 1 are then repeated as "frames" along the tape shown in Figure 2 or, if a sheet rather than a tape, repeated across the sheet. Additional protective coatings or structures, including electrically insulating ones, can be provided on or over chips 20 or over other kinds of electrical circuit components mounted on the interconnection means.

Figure 3 is a cross section of a portion of Figure 2 at a location that is the place of mounting a monolithic integrated circuit chip, 30, in the interconnection means by thermocompression bonding. Protective layer 17 fully fills in about the interconnections of interconnection group 12 to provide firm support under chip 30 during bonding of the wire interconnection leads, 31, between the chip electrical termination, 32, and interconnections in interconnection group 11.

CLAIMS

The embodiments of the invention in which an exclusive property or right is claimed are defined as follows:

1. An electrical interconnection means for selected electronic circuit components also usable with selected other circuit components, said interconnection means comprising:

a flexible film of an electrical insulating material having a first major surface and a second major surface on opposite sides thereof;

a first group of electrical interconnections of a first pattern, said first group of electrical interconnections adhering to said first major surface and located entirely within a selected first area at least at one site in said flexible film, said first pattern having a plurality of places therein where portions of members of said first group of electrical interconnections are arranged in a predetermined arrangement to thereby be capable of permitting electrical contacts of a selected nature to be made to a corresponding selected monolithic integrated circuit chip;

a second group of electrical interconnections of a second pattern, said second group of electrical interconnections adhering to said second major surface and located entirely within a selected second area opposite said first area;

at least one through-film electrical interconnection, located in an opening through said flexible film, said through-film electrical interconnection serving to electrically interconnect at least one member of said first group of electrical interconnections to at least one member of said second group of electrical interconnections;

a first protective layer of an electrical insulating material disposed over said first group of electrical interconnections, except at selected interconnection locations including said portions of said members of said first group of electrical interconnections in said predetermined arrangement for permitting electrical contacts, and on said first major surface in said first area; and

a second protective layer of an electrical insulating material disposed over said second group of electrical interconnections, except

at selected contact locations, if any, and on said second major surface within said second area, said second protective layer having its resulting surface opposite that surface thereof against said second major surface and substantially parallel to said second major surface at those said places having said predetermined arrangements of said portions of said first group of electrical interconnections.

2. The apparatus of claim 1 wherein the said one site is an initial site, and said flexible film has a plurality of similar sites at each of which there is substantially a duplicate of said first group of electrical interconnections, said second group of electrical interconnections, said through-film interconnections, said first protective layer, and said second protective layer.

3. The apparatus of claim 1 wherein monolithic integrated circuit chips are electrically interconnected at those said places having said predetermined arrangements of said portions of said first group of electrical interconnections.

4. The apparatus of claim 1 wherein there is a plurality of said through-film electrical interconnections.

5. The apparatus of claim 2 wherein said duplicate sites are formed one after another repeatedly in an array.

6. The apparatus of claim 5 wherein said array is a linear array and part of a tape based on said flexible film, said tape having sprocket openings therein at opposite edges thereof in a fixed relationship with said opening for said through-film electrical interconnection.

AMENDED CLAIMS

[received by the International Bureau on 9 September 1987 (09.09.87);
original claims 1-6 replaced by amended claims 1-7 (6 pages)]

1. An electrical interconnection means for selected electronic circuit components, said interconnection means comprising:

a flexible film of an electrical insulating material having a first major surface and a second major surface on opposite sides thereof;

a first group of electrical interconnections of a first pattern, said first group of electrical interconnections adhering to said first major surface and located entirely within a selected first area at least at one site in said flexible film, said first pattern having a plurality of places therein where portions of members of said first group of electrical interconnections are arranged in a predetermined arrangement to thereby be capable of permitting electrical contacts of a selected nature to be made to a corresponding selected monolithic integrated circuit chip at least at two of said places, and wherein at least two of said chips will be directly connected by some of said first group of electrical interconnections upon said electrical contacts being made to said two of said chips at said two of said places;

a second group of electrical interconnections of a second pattern, said second group of electrical interconnections adhering to said second major surface

and located entirely within a selected second area opposite said first area;

at least one through-film electrical interconnection, located in an opening through said flexible film, said through-film electrical interconnection serving to electrically interconnect at least one member of said first group of electrical interconnections to at least one member of said second group of electrical interconnections;

a first protective layer of an electrical insulating material disposed over said first group of electrical interconnections, except at selected interconnection locations including said portions of said members of said first group of electrical interconnections in said predetermined arrangement for permitting electrical contacts, and on said first major surface in said first area; and

a second protective layer of an electrical insulating material disposed over said second group of electrical interconnections, except at selected contact locations, if any, and on said second major surface within said second area, said second protective layer having its resulting surface opposite that surface thereof against said second major surface and substantially parallel to said second major surface at those said places having said predetermined

arrangements of said portions of said first group of electrical interconnections.

2. The apparatus of claim 1 wherein the said one site is an initial site, and said flexible film has a plurality of similar sites at each of which there is substantially a duplicate of said first group of electrical interconnections, said second group of electrical interconnections, said through-film interconnections, said first protective layer, and said second protective layer.

3. The apparatus of claim 1 wherein monolithic integrated circuit chips are electrically interconnected at those said places having said predetermined arrangements of said portions of said first group of electrical interconnections.

4. The apparatus of claim 1 wherein there is a plurality of said through-film electrical interconnections.

5. The apparatus of claim 2 wherein said duplicate sites are formed one after another repeatedly in an array.

6. The apparatus of claim 5 wherein said array is a linear array and part of a tape based on said flexible film, said tape having sprocket openings therein at opposite edges thereof in a fixed relationship with said opening for said through-film electrical interconnection.

7. An electrical interconnection means for selected electronic circuit components, said interconnection means comprising:

a flexible film of an electrical insulating material having a first major surface and a second major surface on opposite sides thereof;

a first group of electrical interconnections of a first pattern, said first group of electrical interconnections adhering to said first major surface and located entirely within a selected first area at least at one site in said flexible film, said first pattern having a plurality of places therein where portions of members of said first group of electrical interconnections are arranged in a predetermined arrangement to thereby be capable of permitting electrical contacts of a selected nature to be made to a corresponding selected monolithic integrated circuit chip at least at two of said places;

a second group of electrical interconnections of a second pattern, said second group of electrical interconnections adhering to said second major surface and located entirely within a selected second area opposite said first area;

at least one through-film electrical interconnection, located in an opening through said flexible film, said through-film electrical interconnection serving to electrically interconnect at least one member of said first group of electrical interconnections to at least one member of said second group of electrical interconnections, and wherein said at least one member of said first group and said at least one member of said second group together with said at least one through-film electrical interconnection, provide a direct connection between two of said chips upon said electrical contacts of a selected nature being made to said two chips at two of said places;

a first protective layer of an electrical insulating material disposed over said first group of electrical interconnections, except at selected interconnection locations including said portions of said members of said first group of electrical interconnections in said predetermined arrangement for permitting electrical contacts, and on said first major surface in said first area; and

a second protective layer of an electrical insulating material disposed over said second group of electrical interconnections, except at selected contact locations, if any, and on said second major surface within said second area, said second protective layer having its resulting surface opposite that surface thereof against said second major surface and substantially parallel to said second major surface at those said places having said predetermined arrangements of said portions of said first group of electrical interconnections.

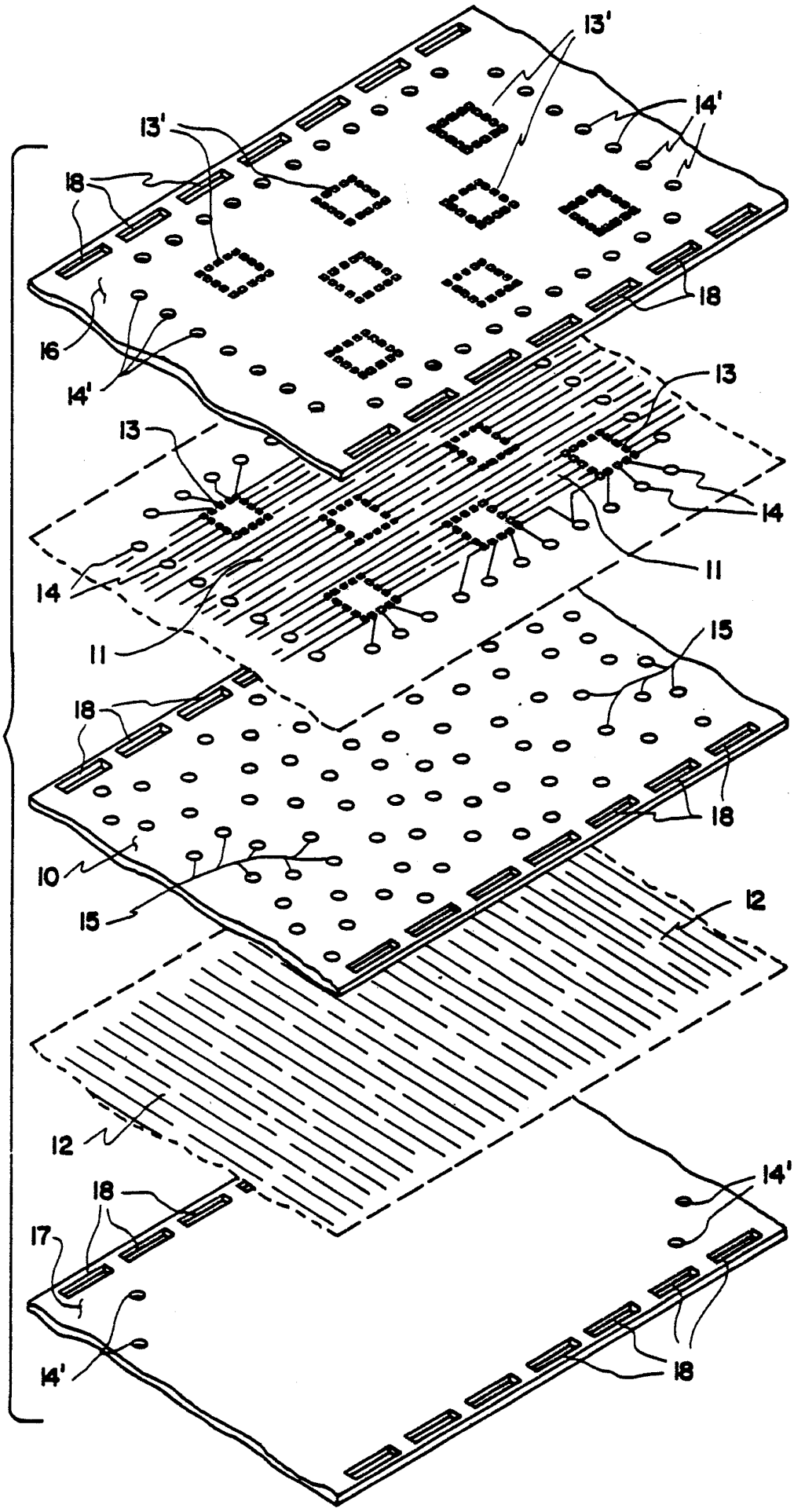

13'
14'
13'
18
18
16
14'
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14
14
11
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18
18
10
15
12
12
14'
18
17
18
14'

Fig. 1

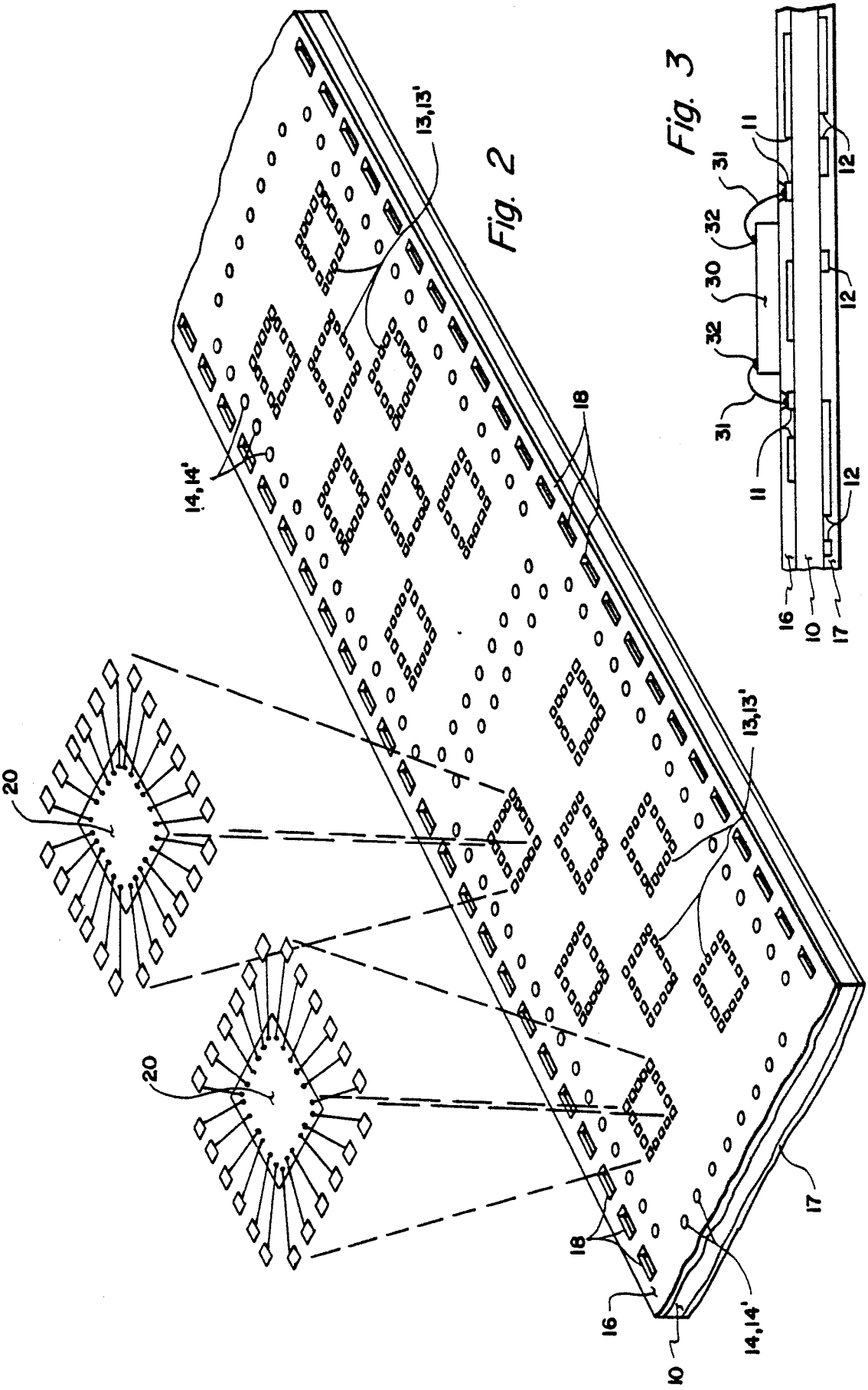

13,13'
14,14'
18
20
20
13,13'
18
16
10
14,14'
17

Fig. 2

11
12
31
32
30
12
32
31
11
12
16
10
17

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00938

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 23/52

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	GB, A, 2004127 (THOMSON) 21 March 1979 see figures 1-3; claims 1-3,7,9	1
A		2-6
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Y	EP, A, 0065425 (MATSUSHITA) 24 November 1982 see page 11, paragraph 1	1
	--	
A	IBM Technical Disclosure Bulletin, volume 24, no. 2, July 1981, (New York, US), L.V. Auletta et al.: "Flexible tape conductor interconnection for chips", pages 1214-1215	
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A	EP, A, 0178227 (FUJITSU) 16 April 1986	

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
3rd August 1987	24 AUG 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/00938 (SA 17280)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 10/08/87

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		DE-A-	2839215	22/03/79
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