



- (51) **International Patent Classification:**
H03L 7/093 (2006.01) **H03D 3/00** (2006.01)
- (21) **International Application Number:**
 PCT/EP2011/057669
- (22) **International Filing Date:**
 12 May 2011 (12.05.2011)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant (for all designated States except US):** TELEFONAKTIEBOLAGET LM ERICSSON (PUBL) [SE/SE]; S-164 83 Stockholm (SE).
- (72) **Inventor; and**
- (75) **Inventor/Applicant (for US only):** BAO, Mingquan [SE/SE]; Citrusgatan 27, S-426 54 Västra Frölunda (SE).
- (74) **Agent:** SCHLOSSMAN, Ulf; Patentor KB, Flöjelbergsgatan 8B, S-431 37 Mölndal (SE).
- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) **Title:** A PHASE LOCKED LOOP WITH TUNABLE PHASE

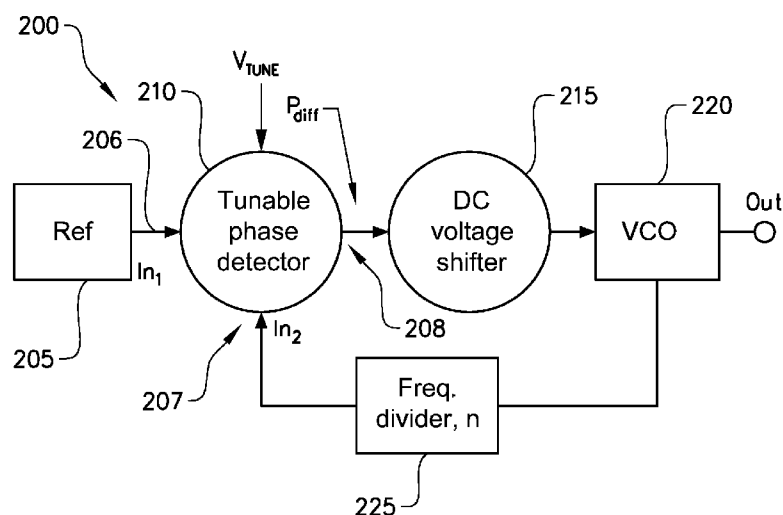


FIG. 2

(57) **Abstract:** A phase locked loop (200, 700, 800) with a phase detector (210, 710, 730) whose output signal varies between maximum and minimum points with the phase difference between input signals. A VCO (220, 720, 740) receives the output signal from the phase detector (210, 710, 730) as tuning signal. A first part of the output signal of the VCO (220, 720, 740) is an input signal to the phase detector (210, 710, 730) and a second part is the output signal of the phase locked loop. There is a DC voltage shifter (215, 715, 735) between the phase detector and the VCO, which shifts the DC voltage level of the output signal from the phase detector (210, 710, 730) so that a point at a distance from a centre point between said maximum and minimum points is shifted to zero volts (DC). The phase detector (210, 710, 730) is tunable.

A PHASE LOCKED LOOP WITH TUNABLE PHASE

TECHNICAL FIELD

The present invention discloses a phase locked loop with tunable phase.

5

BACKGROUND

Signal sources with tunable phase are used in many applications, for example in providing multiphase local oscillator, LO, signals for up-/down-conversion mixers in RF or microwave transceivers, for driving electric beam steering antenna array in radar systems, etc. The tuneability of the phase of a signal from a signal source with tunable phase is often achieved by means of a phase shifter.

There are many known kinds of phase shifters, and these can be divided into two groups, passive and active phase shifters. The first group, i.e. the passive phase shifters, often exhibit losses, and the second group, i.e. the active phase shifters, inherently have a consumption of DC power, in addition to which they generate noise and nonlinear inter-modulation.

Phase locked loops, PLLs, are a common component in, for example, transceivers and radar systems, where they are used for "locking" the phase of the output signal from the PLL to the phase of an input signal to the PLL. A traditional PLL comprises a phase detector which produces an output signal which is proportional in amplitude to the phase difference between two input signals to the phase detector. The output signal from the phase detector is used as tuning signal to a VCO, and the output from the VCO is used as one of the input signals to the phase detector, as well as being the output signal from the PLL. Sometimes, a low-pass filter is arranged between the phase detector and the VCO.

30

SUMMARY

It is an object of the present invention to provide a signal source which has a tunable phase and which overcomes the drawbacks of circuits which incorporate known phase shifters.

5

This object is addressed by the present invention in that it discloses a phase locked loop which comprises a phase detector with a first and a second input port for a first and a second input signal, respectively. The phase detector also comprises an output port, and the phase detector is arranged to deliver
10 a signal at its output port which is proportional to the phase difference between the first and the second input signals and which varies between maximum and minimum points with variations in the phase difference between the first and the second input signals.

15 The phase locked loop also comprises a Voltage Controlled Oscillator, a VCO, which receives the output signal from the phase detector as a tuning signal. A first part of the output signal of the VCO is arranged to be one of the input signals to the phase detector and a second part of output signal of the VCO is arranged to be the output signal of the phase locked loop.

20

The phase locked loop also comprises a DC voltage shifter which is arranged between the phase detector and the VCO. The DC voltage shifter is arranged to shift the DC voltage level of the output signal from the phase detector so that a point at a predefined distance from a centre point between
25 said maximum and minimum points is shifted to zero volts DC.

In addition, the phase detector is tunable with respect to the phase of its output signal.

As will be shown in the detailed description below, the phase locked loop of the invention can be used as a signal source which can be tuned in phase by means of the tunable phase detector.

- 5 In embodiments, the predefined distance from a centre point between the maximum and minimum points which is shifted to zero volts DC is zero, i.e. in embodiments, the “moved” point is the centre point.

10 In embodiments, the phase locked loop additionally comprises a frequency divider which is arranged between the VCO and the phase detector.

In embodiments of the phase locked loop, the phase detector comprises a T-network with a first and a second capacitance, each of which has a first and a second connection port and which are serially connected to each other via
15 their second connection ports. At least one of the capacitances is tunable, and an inductance connects a point between the capacitances, i.e. between their second connection ports, to ground. The first connection port of the first and second capacitance, respectively, are arranged to be used as the first and second input port of the phase locked loop. The first of the capacitances
20 also has its first connection point connected to the input port of a power detector. In the phase detector, the output port of the power detector is arranged to be output port of the phase detector.

In embodiments of the phase locked loop, the phase detector comprises a π -
25 network with a first and a second capacitance, each of which capacitance has a first and a second connection port. At least one of the capacitances is variable, and the capacitances are connected via an inductance at their first connection ports and have their second connection port connected to ground. The first connection port of the first and second capacitance,
30 respectively, are arranged to be used as the first and second input port of the

phase locked loop. The first of the capacitances also has its first connection port connected to the input port of a power detector. In the phase detector, the output port of the power detector is arranged to be output port of the phase detector. In addition, it should be pointed out that in both the versions
5 with T and π networks, the inductors can be exchanged for capacitors if the capacitors are exchanged for inductors.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail in the following, with reference
10 to the appended drawings, in which

Fig 1 shows a prior art Phase Locked Loop, and
Fig 2 shows a basic embodiment of a signal source of the invention, and
Fig 3 shows a characteristic of a phase detector, and
15 Fig 4 shows a first tunable phase detector, and
Fig 5 shows a second tunable phase detector, and
Fig 6 shows a characteristic of the phase detector of fig 5, and
Figs 7 and 8 show further embodiments of signal sources.

20 DETAILED DESCRIPTION

Embodiments of the present invention will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. The invention may, however, be embodied in many different forms and should not be construed as being limited to the
25 embodiments set forth herein. Like numbers in the drawings refer to like elements throughout.

The terminology used herein is for the purpose of describing particular embodiments only, and is not intended to limit the invention.

As reference, fig 1 shows a block diagram of a prior art Phase Locked Loop 110, commonly abbreviated as PLL. As shown in fig 1, the PLL 110 has as a first input signal a reference signal which has a certain phase φ_1 . The first input signal with the phase φ_1 is received by a phase detector in the PLL 110, and the phase detector also receives a second input signal which has the phase φ_2 .

The phase detector produces an output signal, an "error signal", denoted as Δ , which is proportional in amplitude to the difference between the phases of the input signals, i.e. φ_1 and φ_2 .

The error signal from the phase detector is passed through a low pass filter, LPF, and is then used as the tuning signal to a VCO, thereby "driving" the VCO, and creating an output signal from the VCO with a certain phase. The output signal from the VCO is either used "straight off" as the second input signal to the phase detector, or, as shown in fig 1, the output signal from the VCO is passed through a frequency divider before being used as input signal to the phase detector. If a frequency divider is used, the phase of the signal from the VCO will be divided by the division factor n of the divider, i.e. if the phase from the VCO is φ , then the phase φ_2 from the frequency divider will be φ/n .

The output signal from the VCO is also used as the output signal from the PLL 110 and from the signal source 100. In total, this design serves to create a control loop in which the phase of the output signal from the signal source 100 is "locked" to the phase of the reference signal, i.e. locked to φ_1 .

Fig 2 shows an embodiment of a phase locked loop 200 of the invention, and also shows a source 205 for a reference signal: the phase locked loop 200 has a first input port 206 for a first input signal and a second input port 207

for a second input signal. The first and second input ports are used as input ports to a phase detector 210. As described above in connection with the PLL 110, the phase detector 210 produces an output signal P_{diff} at an output port 208, which is proportional in amplitude to the phase difference between the input signals at the first and second input ports 206, 207. The reference
5 signal from the source 205 is used as the first input signal at the first input port 206.

In the phase locked loop 200, the phase detector 210 is tunable, i.e. the
10 amplitude of the output signal from the phase detector 210 for one and the same phase difference between the input signals to the phase detector 210 is tunable by means of a tuning signal shown as V_{TUNE} in fig 2. The tuning signal V_{TUNE} is used to tune the capacitance of the varactors in the T or π network, consequently, to tune the phase of the output signal from the PLL
15 200 in a manner which will be described in more detail later in this text.

As shown in fig 2, the phase locked loop 200 also comprises a DC voltage shifter 215 connected to the output of the tunable phase detector 215. The output signal from the phase detector 210 is used as input signal to a DC
20 voltage shifter 215. The role of the DC voltage shifter 215 will be described in more detail later in this text, but, as the name implies, a basic function of the DC voltage shifter 215 is to shift the DC level of the output signal from the phase detector 210 and to deliver the "DC-shifted" signal as its out signal.

As shown in fig 2, the output signal from the DC voltage shifter 215 is used
25 as the input signal or tuning signal to a Voltage Controlled Oscillator, a VCO 220. The tuning signal to the VCO 220 controls the frequency of the VCO's 220 output signal. Since frequency is the derivative of phase, the tuning signal to the VCO can also be seen as controlling the phase of the output
30 signal from the VCO 220. The output signal from the VCO 220 is used in one

part as the output signal from the entire PLL 200, and in another part as the second input signal to the phase detector 210 at the second input port 207.

In fig 2, the PLL 200 is shown as comprising a frequency divider 225 between the output of the VCO 220 and the phase detector 210. The frequency divider is however optional, i.e. it is used in some embodiments and not in some other embodiments, depending on the frequency of VCO and the frequency of reference source.

Fig 3 shows the amplitude of the output signal from the tunable phase detector 210 as a function of the phase difference Φ between the input signals to the tunable phase detector 210. Three different curves are shown, numbered as 1, 2 and 3, one for each of three different values of the tuning signal V_{TUNE} , i.e., different capacitances of the varactors of the tunable phase detector 210. The curves numbered 1, 2 and 3 correspond, respectively, to the varactors 315, 320 being tuned to a capacitance of 3, 4 and 5 pF.

As can be seen, the amplitude shown in fig 3 varies between maximum and minimum values, in this example as a sine/cosine-function. The role of the DC voltage shifter 215 is to shift the DC-level of the output of the tunable phase detector so that a certain point on the amplitude curve is shifted to zero V DC. The point which is moved to zero V DC is a point between the maximum and the minimum point on the curve, i.e. a point on the “downward” (negative) slop of the curve; it should be stressed that such a point is not to be confused with a point between the minimum and the maximum point on the curve, i.e. a point on the “upward” slope of the curve.

Suitably, the point which is moved to zero V DC is a point in the middle of the maximum and minimum points of the curve, i.e. a centre point between the maximum and minimum points of the curve, although other points at a

certain distance from the centre point can also be used, in order to create other effects.

The point which is moved to zero V DC is here referred to as the “zero gain point”, and is the point whose output phase the PLL will be “locked” to. However, since the phase detector 210 is tunable, the phase of the output signal from the VCO 220 can also be altered, thereby altering the phase difference Φ between the two input signals to the tunable phase detector 210.

Denote the frequency of the signal from the VCO 220 as f_0 and the signal from the frequency divider 225 as f_0/n , where n is the division factor of the divider. If the phase of the reference signal, i.e. the input signal at the input port 206, remains constant, then, when the phase difference Φ changes by an amount here denoted as $\Delta\Phi$, the phase of the signal f_0/n will change by $\Delta\Phi$ as well, while the phase of the signal from the VCO 220, i.e. f_0 , will change by $\Delta\Phi \cdot n$.

As an example, assume a VCO 220 with an output signal at a frequency of 7 GHz, so that $f_0=7$ GHz, and assume further a division factor in the frequency divider 225 of 8, i.e. $n=8$. In such an example, the frequency of the signal from the frequency divider 225 will be $f_0/8$, i.e. 875 MHz. If, as is preferable, the reference signal is at the same frequency as the signal from the frequency divider 225, the frequency of the reference signal will also be 875 MHz.

If, by tuning of the tunable phase detector 210, the phase difference Φ shown in fig 3 is altered from curve 1 to curve 3, the “zero gain point” will move from 284° to 329° . Hence, the variation of ϕ , “ $\Delta\phi$ ”, is 45° , and as explained above, the phase of the VCO’s signal will change $45^\circ \times 8 = 360^\circ$. If,

instead, we move from curve 1 to curve 2, i.e. to the curve which represents 4 pF, then the change in phase difference Φ will be from 284 degrees to 305 degrees, and the phase of the output signal from the VCO change by $8 \times 21 = 168$ degrees.

5

Fig 4 shows an embodiment of a tunable phase detector 410 for use in the PLL 200 in fig 2: as shown in fig 4, the tunable phase detector 410 comprises a so called "T-network" 310 with an inductor 325 connect to ground at one end, and at its other end connected to a point in between two capacitors 320, 315, which are serially connected to each other. At least one of the capacitors, and suitably both of them, are varactors, i.e. tunable capacitances, which are tuned by means of a tuning voltage shown in fig 4, and which is the tuning voltage V_{TUNE} from fig 2.

15 The two capacitors 320, 315, are connected to each other at one of their respective ends. As is also shown in fig 4, the capacitor 320 has its other end connected to the input port of a power detector 305, where the output port of the power detector 305 is arranged to be output port of the phase detector, shown as 208 in figs 2 and 4. The same end of the capacitor 320
20 that is connected to the input port of the power detector 305 is also arranged to be one of the input ports to the phase detector 410, in this case the input port which is numbered as 206 in fig 2 as well as in fig 4. The other input port of the phase detector, i.e. the input port shown as 207 in fig 2 is the end of the capacitor 315 which is not connected to the capacitor 320. This end is
25 also shown as 207 in fig 4.

In order to facilitate recognition between the tunable phase detector 410 of fig 4 and the tunable phase detector 210 of fig 2, fig 4 also shows the reference signal source 205, connected to the input port 206 via a resistor 335, and the frequency divider 225, connected to the input port 207 via a
30

resistor 330. The resistor 335 represents the output impedance of the reference signal source 205, and the resistor 330 represents the output impedance of the frequency divider.

- 5 As shown in fig 4, both of the capacitors 315, 320 are tunable, i.e. they are so called varactors. With reference to the three curves shown in fig 3, the curves numbered 1, 2 and 3 correspond, respectively, to the varactors 315, 320 being tuned to a capacitance of 3, 4 and 5 pF.
- 10 Fig 5 shows a second embodiment 510 of a tunable phase detector for use as the tunable phase detector 210 of fig 2. In the embodiment 510, the tunable phase detector comprises a π -network 511 with a first 520 and a second 515 capacitor, connected an inductor 525 between them at one a first connection point or input port, the inductors 520, 525, being grounded at
- 15 their second connection point or input port. As with the tunable phase detector 410 of fig 4, at least one of the capacitors 515, 520 is a varactor, and suitably, this is the case for both of the capacitors 520, 515.

The first connection port 206, 207 of the first 520 and second 515 capacitor, respectively, are arranged to be used as the first and second input ports, shown as 206 and 207 in fig 2, of the tunable phase detector, and the first capacitor also has its first connection port connected to the input port of a power detector 505. The output port 205 of the power detector 505 is arranged to be output port of the tunable phase detector 510.

- 25 Fig 6 shows three curves similar to those shown in fig 3, numbered 1', 2' and 3', respectively. It can be seen that the amplitude of the output signal from the tunable phase detector 510 varies from 0.48 to 0.04 V DC along curve 1', which represents a setting of the varactors 520, 515 to a capacitance of 3
- 30 pF. The curve 2' represents a setting of the varactors 520, 515 to a

capacitance of 4.5 pF, and the curve 3' represents a setting of the varactors 520, 515 to a capacitance of 6 pF. The shift from the DC voltage shifter 215 is here chosen to be 0.27 V, or rather -0.27 V, since the shift is negative. It can be seen that the zero gain points vary from 70° to 120°, which, in this example will lead to a phase variation in the output signal from the VCO 220 of 400°.

Fig 7 shows a further embodiment 700, which is a so called two-tunable phase signal source, and which comprises two PLLs 701 and 702, where the PLL 701 is a PLL which comprises a tunable phase detector 771 with a T-network, as shown in fig 4 and explained in connection with that figure, and the PLL 702 is a PLL which comprises a tunable phase detector 730 with a π -network, as shown in fig 5 and explained in connection with that figure.

One and the same tuning signal V_{TUNE} is used for both of the phase detectors 710, 730, which leads to a phase difference between the output signals from the two PLLs 701, 702, of approximately π radians, since stable zero gain points for a T-network is in the region of between $3\pi/2$ and 2π radians, and for a π -network is between 0 and π radians. In an alternative embodiment, different tuning signals V_{TUNE} are used for the two phase detectors 710, 730, and also, it is possible to use similar T or π networks, depending on the desired range of phase differences for the PLLs 701, 702.

As shown in fig 7, the PLLs 701, 702 do not comprise a frequency divider between the VCO 720, 740, and the tunable phased detector 710, 730.

In addition, as is also shown in fig 7, the two PLLs 701, 702, share the same reference signal source 705, and thereby also share the same reference signal.

Fig 8 shows an embodiment 800 which illustrates how a Phase Locked Loop of the invention can be used to generate multi-phase signals, in a manner which is similar to the embodiment which is shown in fig 7: As shown in fig 8, in the embodiment 800, there is comprised N PLL of the invention, which all share the same reference signal source 805. Three PLLs 801-803 are shown explicitly in fig 8, with respective output signals Out_1 , Out_2 and Out_3 , and the use of N PLLs is indicated by means of a dotted line and an output signal shown as Out_N . The output signals from the PLLs in the embodiment 800 can be given different phases by means of applying a different tuning signal, show as V_{TUNE1} , V_{TUNE2} and V_{TUNE3} , to the tuneable phase detector in each of the PLLs 801-803.

Embodiments of the invention are described with reference to the drawings, such as block diagrams.

In the drawings and specification, there have been disclosed exemplary embodiments of the invention. However, many variations and modifications can be made to these embodiments without substantially departing from the principles of the present invention. Accordingly, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation.

The invention is not limited to the examples of embodiments described above and shown in the drawings, but may be freely varied within the scope of the appended claims.

CLAIMS

1. A phase locked loop (200, 700, 800) comprising a phase detector (210, 710, 730) with a first (206, 713, 716) and a second (207, 715, 714) input port
5 for a first and a second input signal, respectively, the phase detector (210, 710, 730) also comprising an output port (208, 711, 712), the phase detector (210, 710, 730) being arranged to deliver a signal at its output port (208, 711, 712) which is proportional to the phase difference between the first and the second input signals and which varies between maximum and minimum
10 points with variations in said phase difference, the phase locked loop (200, 700, 800) also comprising a Voltage Controlled Oscillator, a VCO (220, 720, 740), which receives the output signal from the phase detector (210, 710, 730) as a tuning signal, a first part of the output signal of the VCO (220, 720, 740) being arranged to be one of the input signals to the phase detector
15 (210, 710, 730) and a second part of output signal of the VCO being arranged to be the output signal of the phase locked loop, the phase locked loop (200, 700, 800) being characterized in that it also comprises a DC voltage shifter (215, 715, 735) arranged between the phase detector and the VCO, the DC voltage shifter (215, 715, 735) being arranged to shift the DC
20 voltage level of the output signal from the phase detector (210, 710, 730) so that a point at a predefined distance from a centre point between said maximum and minimum points is shifted to zero volts (DC), the phase locked loop also being characterized in that the phase detector (210, 710, 730) is tunable with respect to the phase of its output signal.
25
2. The phase locked loop (200, 700, 800) of claim 1, in which the predefined distance is zero.

3. The phase locked loop (200, 800) of claim 1 or 2, additionally comprising a frequency divider (225) arranged between the VCO and the phase detector (210).

5 4. The phase locked loop (200, 700, 800) of any of claims 1-3, in which the phase detector (210, 710, 730) comprises a T-network (310) with a first (320) and a second (315) capacitance, each of which capacitance has a first and a second connection port and which are serially connected to each other via their second connection ports, with at least one of said capacitances being
10 tunable, with an inductance (325) connecting a point between said capacitances to ground, the first connection port of the first and second capacitance, respectively, being arranged to be used as the first and second input port (206, 207) of the phase locked loop, with the first (320) of said capacitances also having its first connection point connected to the input port
15 of a power detector (305), in which phase detector (210, 710, 730) the output port of the power detector (305) is arranged to be output port of the phase detector.

5. The phase locked loop (200, 700, 800) of any of claims 1-3, in which the
20 phase detector (210, 710, 730) comprises a π -network (510) with a first (520) and a second (515) capacitance, each of which capacitance has a first and a second connection port, at least one of said capacitances (515, 520) being variable, the capacitances being connected via an inductance (525) at their first connection ports and having their second connection port
25 connected to ground, the first connection port of the first and second capacitance, respectively, being arranged to be used as the first and second input port (206, 207) of the phase locked loop, with the first (520) of said capacitances also having its first connection port connected to the input port of a power detector (505), in which phase detector (210) the output port of
30 the power detector is arranged to be output port of the phase detector.

1/5

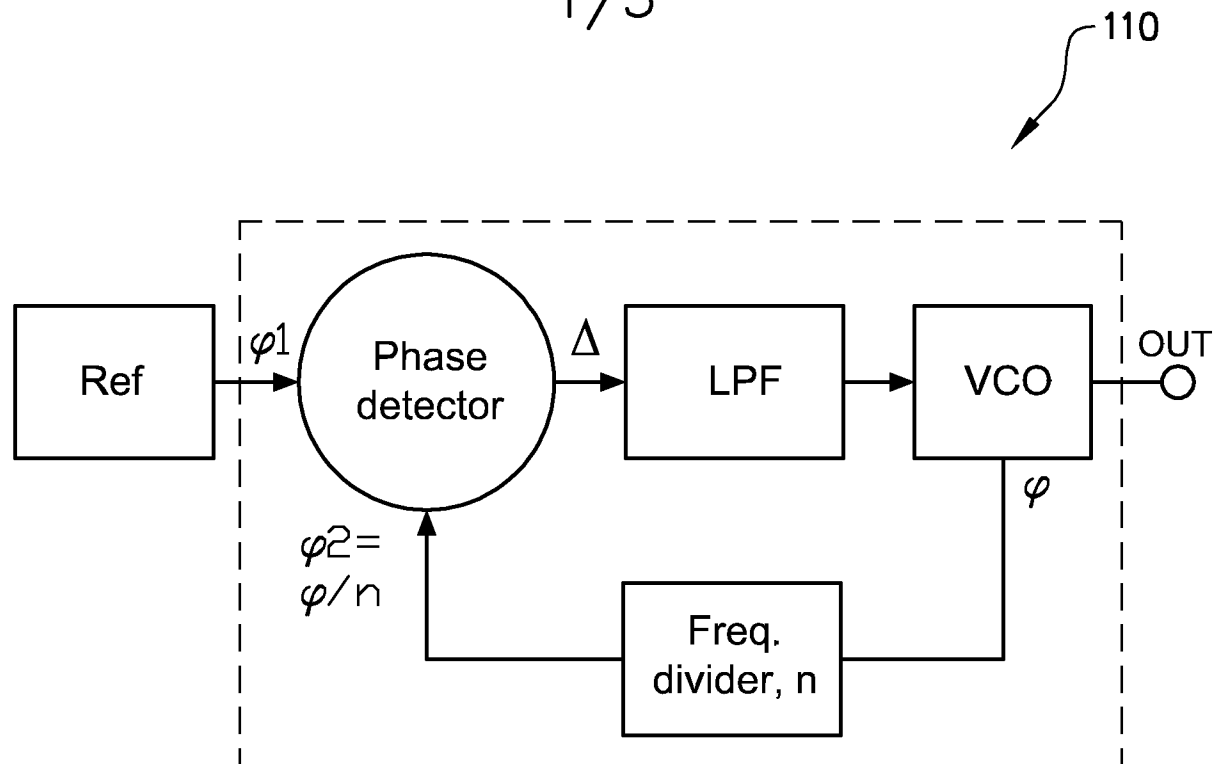


FIG. 1 Prior art

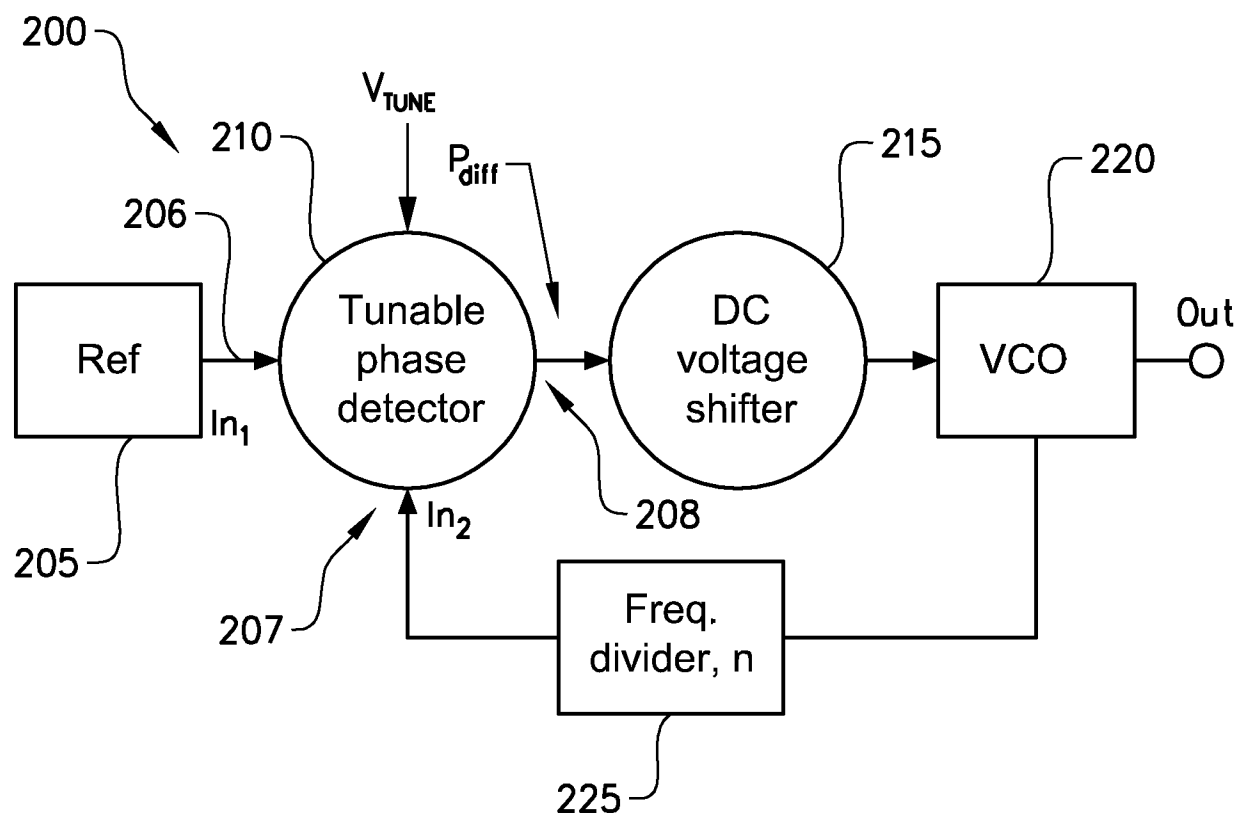


FIG. 2

2/5

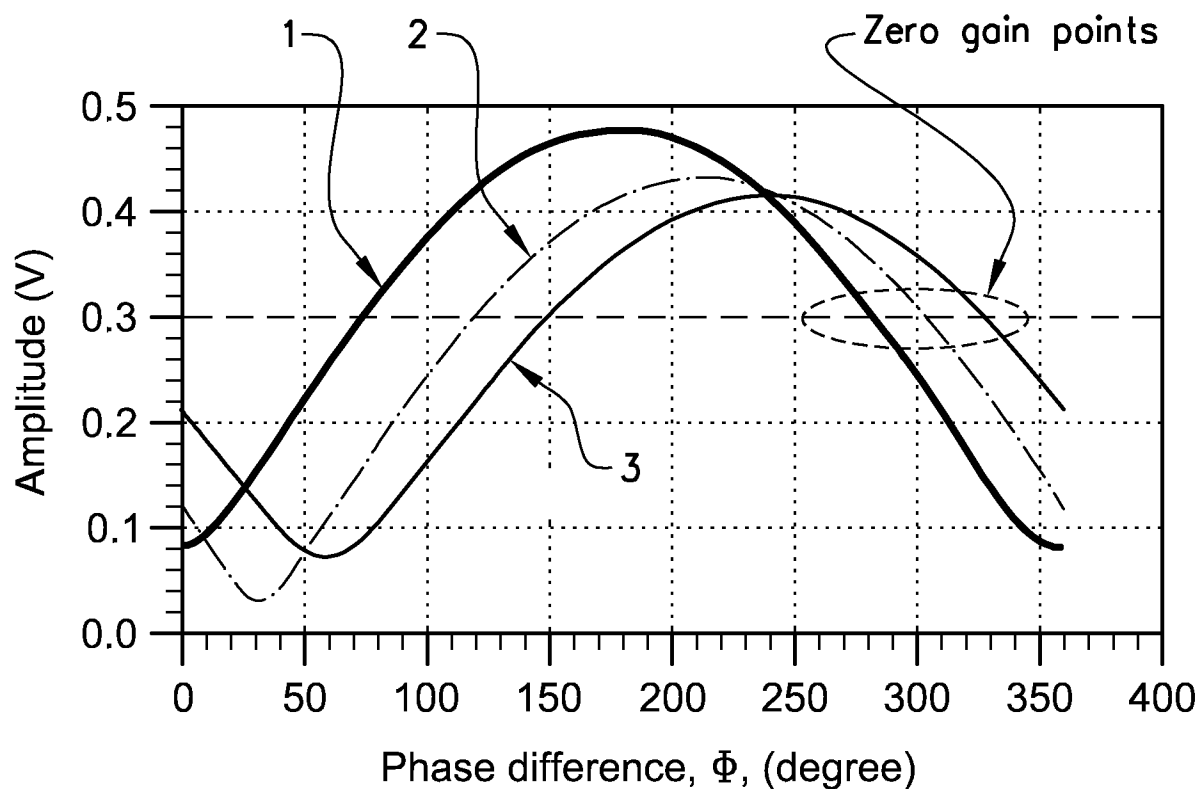


FIG. 3

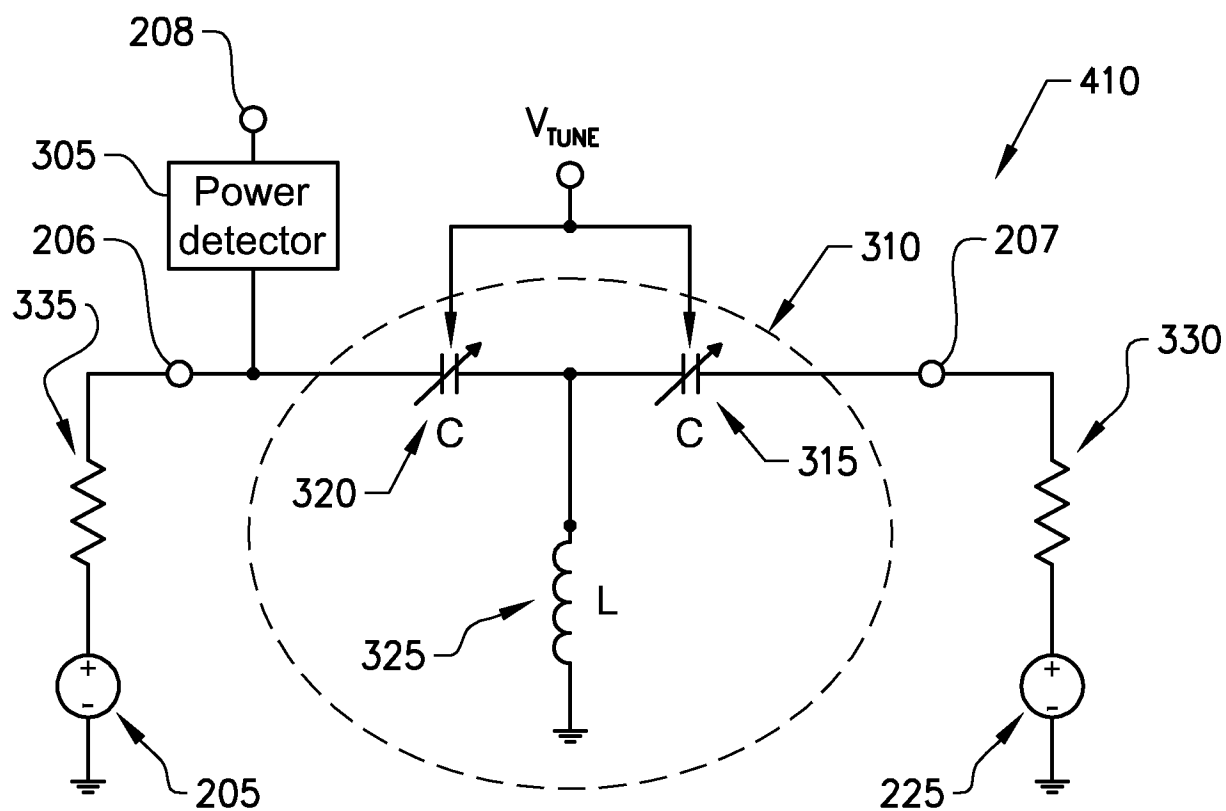


FIG. 4

3/5

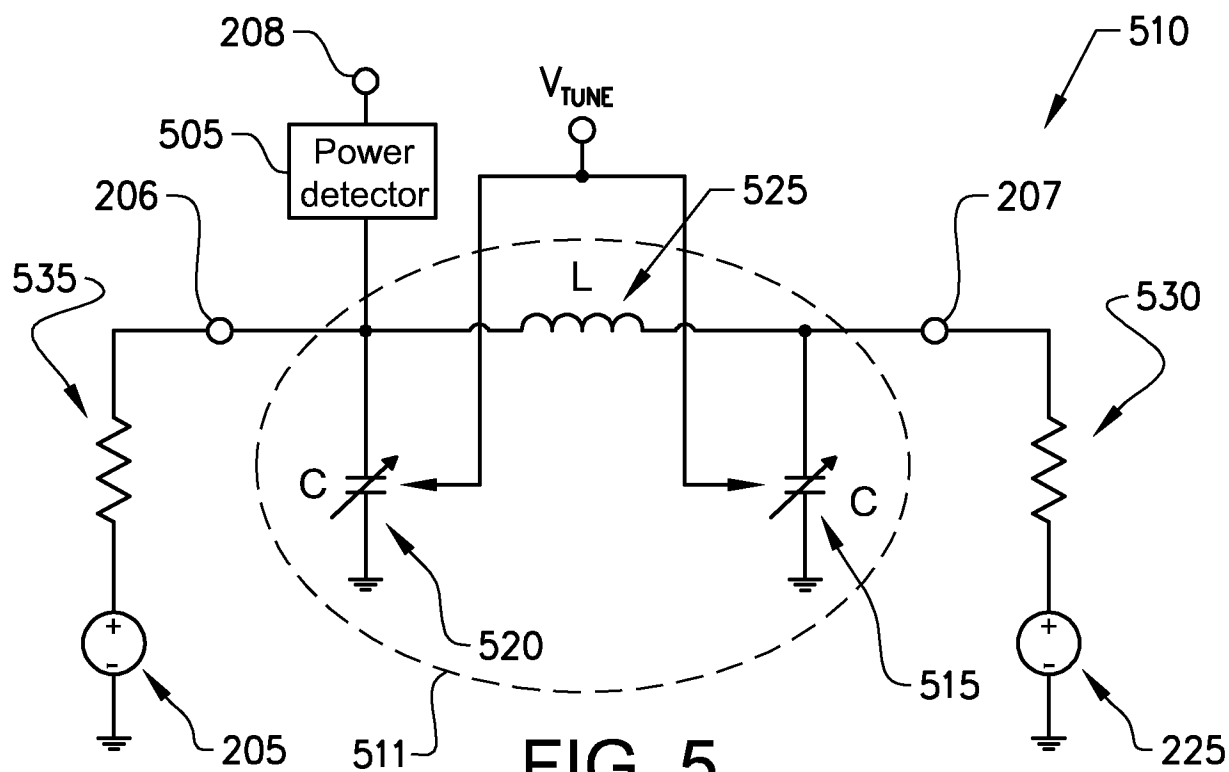


FIG. 5

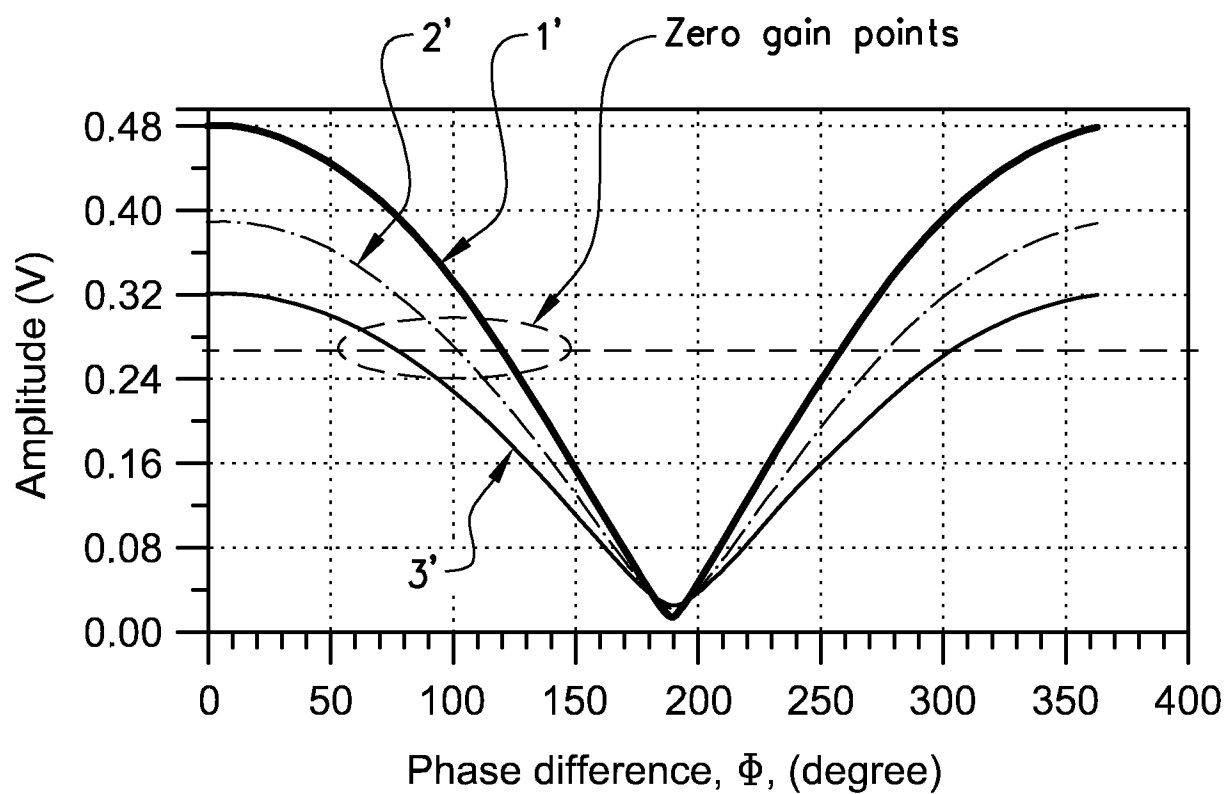


FIG. 6

4/5

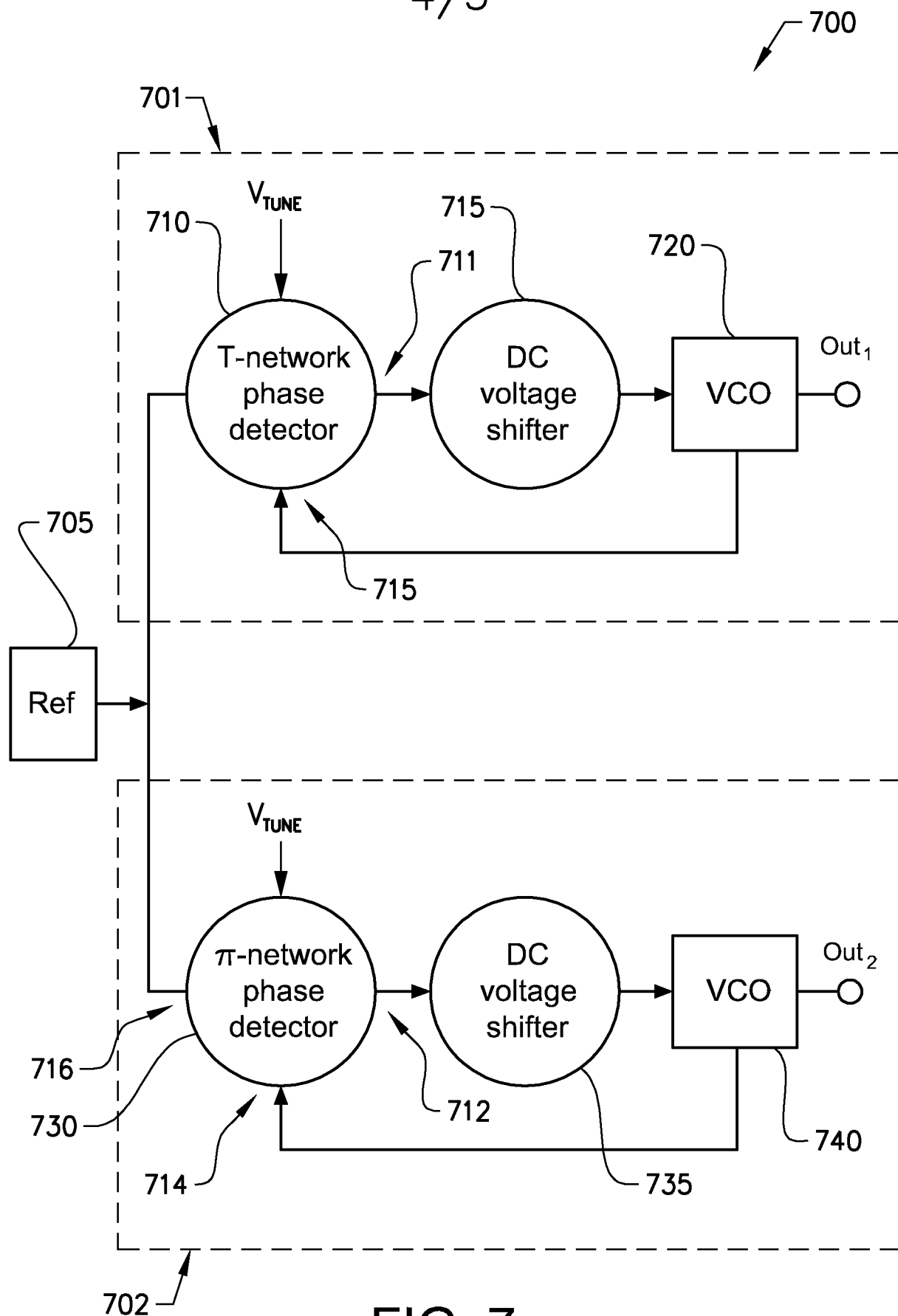


FIG. 7

5/5

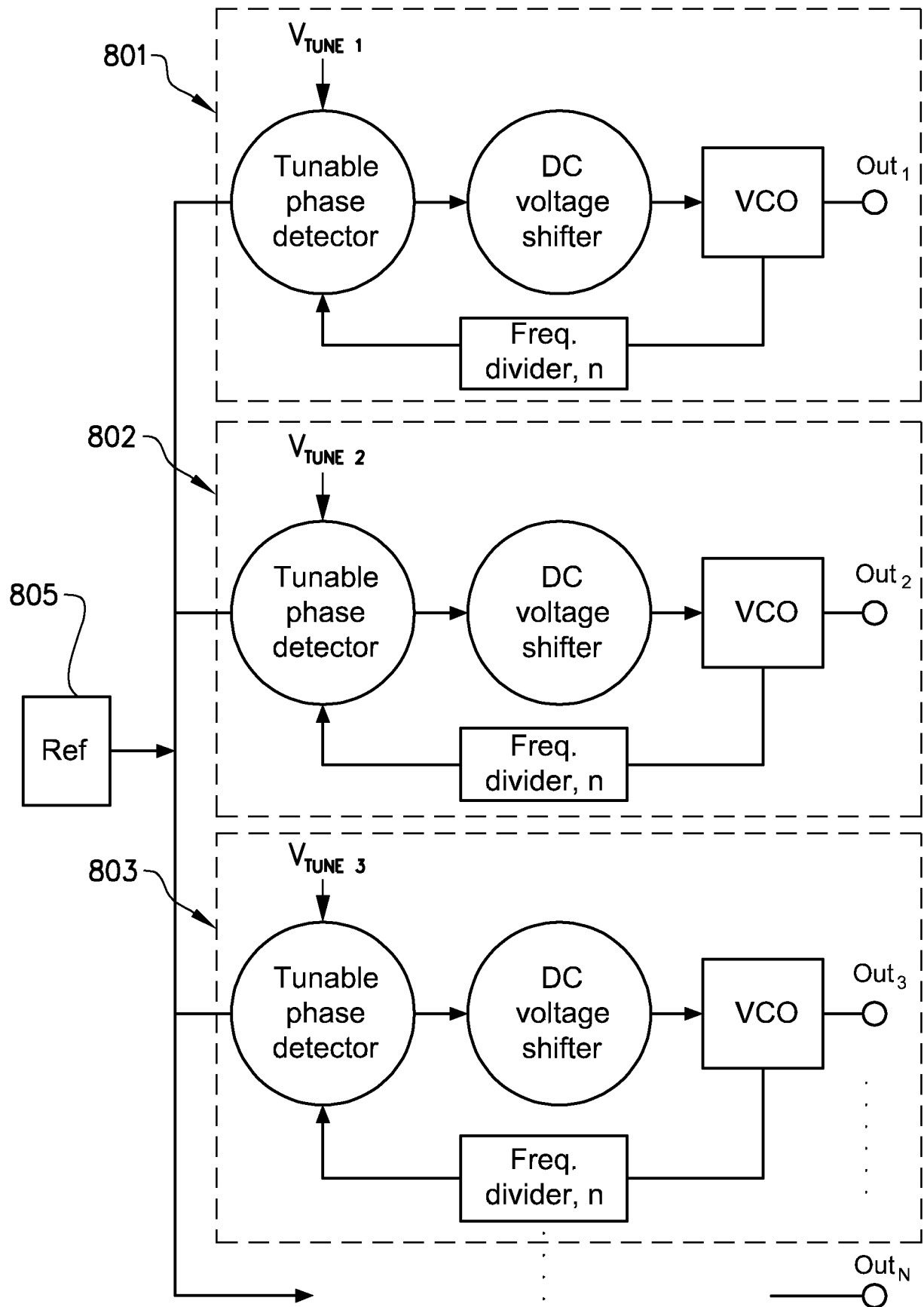


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/057669

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03L7/093 H03D3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03L H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 917 352 A (DUNLAP FRANK M [US] ET AL) 29 June 1999 (1999-06-29)	1-3
A	column 3, line 10 - column 5, line 5 -----	4,5
Y	US 4 570 130 A (GRINDEL DAVID R [US] ET AL) 11 February 1986 (1986-02-11)	1-3
A	column 7, line 55 - column 7, line 65 -----	4,5
Y	US 2009/261873 A1 (LIN KUO-KAI [TW] ET AL) 22 October 2009 (2009-10-22)	1-3
A	paragraph [0052] - paragraph [0053] -----	4,5
A	US 6 424 212 B1 (BRANDT PER-OLOF [SE]) 23 July 2002 (2002-07-23) the whole document -----	1-5



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

5 January 2012

Date of mailing of the international search report

16/01/2012

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Kahn, Klaus-Dieter

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2011/057669

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5917352 A	29-06-1999	US 5917352 A WO 9534127 A1	29-06-1999 14-12-1995
US 4570130 A	11-02-1986	DE 3375870 D1 EP 0106157 A2 JP 1723502 C JP 4001527 B JP 59075705 A US 4570130 A	07-04-1988 25-04-1984 24-12-1992 13-01-1992 28-04-1984 11-02-1986
US 2009261873 A1	22-10-2009	CN 101567687 A US 2009261873 A1	28-10-2009 22-10-2009
US 6424212 B1	23-07-2002	AU 1029201 A CN 1399812 A EP 1232564 A1 GB 2356756 A JP 2003516012 A US 6424212 B1 WO 0139365 A1	04-06-2001 26-02-2003 21-08-2002 30-05-2001 07-05-2003 23-07-2002 31-05-2001