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(54) Logarithmic amplifier

(57) The invention relates to a logarithmic amplifier for reading an input current (I_{in}) or input voltage (U_{in}) and for giving out an output voltage (U_{out}), said logarithmic amplifier including a transistor (T1) or diode for generating logarithmic amplification, said transistor (T1) or diode including an inner serial resistance. According to the invention a compensation voltage (U_c) is arranged to be subtracted from the output voltage (U_{out}) to compensate for voltage drop over the inner serial resistance.

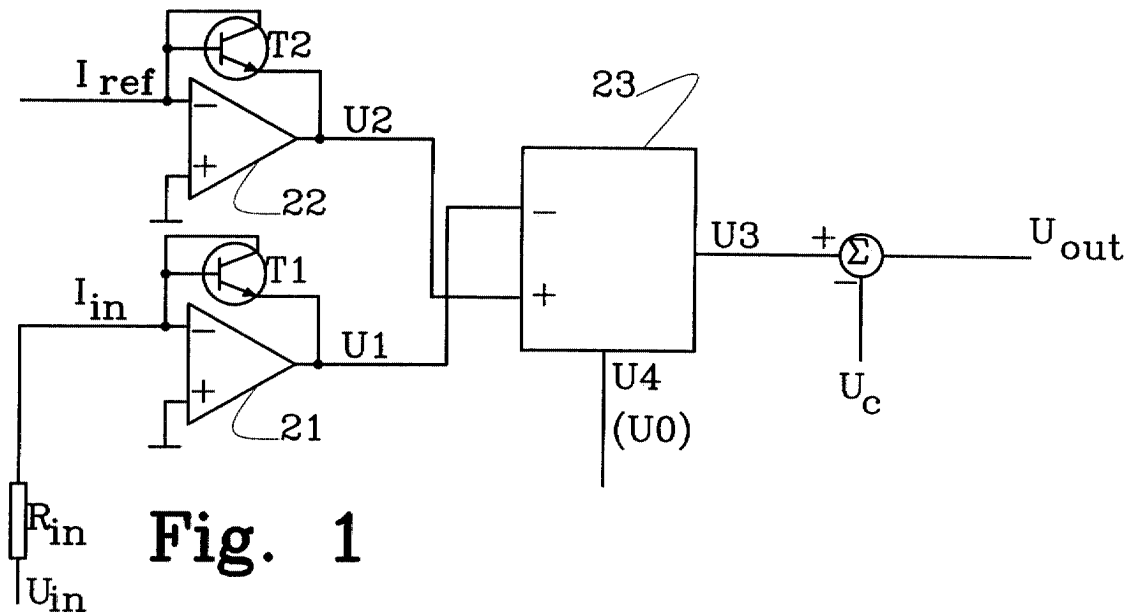


Fig. 1

Description**TECHNICAL FIELD OF THE INVENTION**

5 [0001] The present invention relates to a logarithmic amplifier.

DESCRIPTION OF RELATED ART

10 [0002] It is previously known to use the logarithmic characteristics of a diode or a transistor to accomplish a logarithmic amplifier. This may be done e.g. by taking an operational amplifier and connecting the diode or transistor between the negative input and the output of the operational amplifier. A behaviour in an ordinary transistor could be that if the temperature is stable, then the voltage over the transistor increases about 60 mV when the current flowing through it increases 10 times.

15 [0003] However, said logarithmic characteristics are highly dependent on temperature. Firstly, the absolute value of the output voltage from the operational amplifier varies typically $-2\text{mV}/^{\circ}\text{C}$. Secondly, the voltage increase over the transistor due to current increase varies proportional to the absolute temperature in Kelvin.

[0004] Logarithmic amplifier circuits have been developed to compensate for the temperature dependency. A good overview of different circuits may be found in "What's All This Logarithmic Stuff, Anyhow?", Electronic design, June 14, 1999, p 111-115.

20 [0005] To decrease the first temperature dependency the difference may be taken between the output voltage from the operational amplifier and a reference voltage. If said voltages have approximately the same temperature dependency, then they will be affected approximately equal from temperature changes and the difference between them will thus take away most of said temperature dependency.

25 [0006] Another problem is that transistors and diodes normally have an inner serial resistance, e.g. 0,5 Q, between collector and emitter or between anode and cathode, respectively. This may cause a notable error in the output voltage of the differential amplifier due to unwanted voltage drop over the inner resistance. In the case of a voltage input and a transistor this is solved in said article, Fig. 4a, by not connecting the transistor base to earth as in Fig. 3, but by connecting the base to a connection point between two resistors that are serially connected between the input voltage and ground. This pulls up the base to compensate for the voltage drop over the inner resistance. However, the compensation will not be complete, as there is also an inner resistance between the base and the emitter. Further, this only works when transistors are used and not when diodes are used and it only works with a voltage input and not with a current input.

30 [0007] Note that Fig. 4a in said article contains an evident error. It has to be a voltage input and not a current input, because the circuit would not work with a current input.

SUMMARY

35 [0008] The problems with the solution to the voltage-drop problem in the article in Electronic Design is that it does not work very well, it does not work when diodes are used and it does not work when a current input is used.

40 [0009] The object of the present invention is to provide a logarithmic amplifier that solves the voltage-drop problem better and that does not have said limitations. This is solved by subtracting a compensation voltage from the output voltage of the logarithmic amplifier to compensate for the voltage drop over the inner serial resistance.

[0010] Since the compensation is made on the output and not at the transistor base the advantage is obtained that the compensation is independent of the kind of input used and of the logarithmic element used. Thus, it works as well with a current input as with a voltage input and it works as well with a diode as logarithmic element as with a transistor.

45 [0011] A further advantage is that the compensation voltage also may be used for other purposes, such as to provide a photodiode bias voltage in the case when the input current is produced by a photodiode. This saves money, space and time.

50 [0012] The invention will now be described in detail with reference to accompanying drawings. More advantages will follow from the different embodiments described.

BRIEF DESCRIPTION OF THE DRAWINGS

55 [0013] Figure 1 discloses a schematic overview of a logarithmic amplifier according to the invention.

[0014] Figure 2 discloses an embodiment of the first differential amplifier shown in Fig. 1.

[0015] Figure 3 discloses a first embodiment of the logarithmic amplifier in Fig. 1.

[0016] Figure 4 discloses an embodiment of the second differential amplifier shown in Fig. 3.

[0017] Figure 5 discloses a second embodiment of the logarithmic amplifier in Fig. 1.

- [0018] Figure 6 discloses a third embodiment of the logarithmic amplifier in Fig. 1.
 [0019] Figure 7 discloses a practical implementation of the embodiment in Fig. 6.
 [0020] Figure 8 discloses an embodiment of the inverting amplifier in Fig. 5-7.
 [0021] Figure 9 discloses the embodiment in Fig. 6, where the input current comes from a photodiode and with an embodiment for a photodiode bias circuit.
 [0022] Figure 10 discloses an embodiment of the comparator in Fig. 9.
 [0023] Figure 11 discloses a second embodiment of the comparator in Fig. 9.
 [0024] Figure 12 discloses a second embodiment of the photodiode bias circuit.
 [0025] Figure 13 discloses a third embodiment of the photodiode bias circuit.

DETAILED DESCRIPTION OF EMBODIMENTS

[0026] In Fig. 1 is shown a logarithmic amplifier according to the invention. An input current I_{in} is fed into the negative input of a first operational amplifier 21. The positive input of the first operational amplifier 21 is connected to ground and there is a first transistor T1 connected between the negative input and the output of the first operational amplifier 21.
 [0027] In Fig. 1 the first transistor T1 is connected with its collector and base to the negative input of the first operational amplifier 21 and with its emitter to the output of the first operational amplifier 21, but other connections are possible. Especially it is possible to instead connect the base to ground. It is also possible to use a diode instead of the first transistor T1. This connection of a transistor or a diode makes the output voltage of the first operational amplifier 21 a logarithmic function of the input current. Said output voltage will from now on be called the first voltage U1 for short. It is of course possible to use an input voltage U_{in} together with an input resistor R_{in} instead of an input current.
 [0028] Since an operational amplifier has a very large input impedance the current flowing through the first transistor T1 is approximately equal to the input current I_{in} . If the first transistor T1 has a first inherent temperature dependent constant k_1 , then the first voltage U1 will become:

$$U1 = -k_1 \cdot \ln(I_{in}/I_{01}) \quad (1)$$

where I_{01} is the reverse leakage current for the first transistor T1. The formula applies only approximately and only for currents that are not very small or large.

[0029] As an example, when the first transistor T1 is connected as in Fig. 1, a behaviour in an ordinary transistor with a first constant k_1 of 0.06 V and a reverse leakage current I_{01} of 10^{-13} A could be that if the temperature is stable, then the voltage over the first transistor T1 increases about 60 mV when the current flowing through it increases 10 times, which in this case corresponds to an increase in optical power of 10 dB.

[0030] This alone makes up a logarithmic amplifier, however very temperature dependent. Firstly, the output voltage from the first operational amplifier 21 varies typically $-2\text{mV}/^\circ\text{C}$. Secondly, the voltage increase due to current increase over the first transistor T1 varies proportional to the absolute temperature in Kelvin.

[0031] To decrease the first temperature dependency the difference is taken between the first voltage U1 and a second voltage U2 that is used as a reference. If the second voltage U2 have approximately the same temperature dependency as the first voltage U1, then they will be affected approximately equal from temperature changes and the difference between them will thus take away most of said temperature dependency.

[0032] The second voltage U2 may be accomplished by using a reference current I_{ref} , which enters the negative input of a second operational amplifier 22 that has a second transistor or diode T2 connected in the same way as the first operational amplifier 21 has. The second voltage U2 is taken from the output of the second operational amplifier 22 and is thus a logarithmic function of the reference current I_{ref} . If the second transistor T2 has a second inherent temperature dependent constant k_2 , then the second voltage U2 becomes:

$$U2 = -k_2 \cdot \ln(I_{ref}/I_{02}) \quad (2)$$

where I_{02} is the reverse leakage current for the second transistor T2. The second constant k_2 will have a value that is very close to the first constant k_1 . The same comments as for formula (1) apply.

[0033] It is appropriate to chose the reference current I_{ref} in the middle of the interval where measuring is intended. This is because the measuring error due to temperature dependence will be smaller the closer the input current I_{in} is to the reference current I_{ref} . Thus, if it is a wish to measure input currents from 0,1 μA to 1 mA it is appropriate that the reference current I_{ref} is approximately 10 μA .

[0034] Further, the easiest way of implementing this circuit is to chose transistors T1 and T2 that have similar tem-

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perature characteristics and place them close together, so as to keep them in the same temperature.

[0035] The first voltage U1 and the second voltage U2 enters a first differential amplifier 23, which gives out a third voltage U3. Optionally, a fourth voltage U4 may be entered into the first differential amplifier if there is a wish to level adjust the interval within which the third voltage U3 may be. The fourth voltage U4 may be the same as a level adjust voltage U0 or something else. The level adjust voltage U0 may be ground, but it may also be used to displace the whole voltage interval used. This applies to all places where the level adjust voltage U0 is used.

[0036] The third voltage U3 may then be used as the output voltage U_{out} directly or via other circuits. If the second differential amplifier has a third inherent constant k3, then the third voltage U3 will become:

$$U3 = (U2-U1) \cdot k3 + U4 \quad (3)$$

$$U3 = [k1 \cdot \ln(I_P/I_{01}) - k2 \cdot \ln(I_{ref}/I_{02})] \cdot k3 + U4 \quad (4)$$

[0037] A problem with transistors and diodes is that they normally have an inner serial resistance, e.g. 0,5 Ω , which causes a notable error for currents larger than approximately 0,1 mA. This may be compensated by subtracting a compensation voltage U_C from the output voltage U_{out} , which is disclosed schematically in Fig. 1.

[0038] In Fig 2. is shown an example on how the first differential amplifier 23 may look. The main part includes a third operational amplifier 24 with a positive input, a negative input and an output, which gives out the third voltage U3. A second resistor R2 is connected between the negative input of the first differential amplifier 23 and the negative input of the third operational amplifier 24. A third resistor R3 is connected between the negative input of the third operational amplifier 24 and the output of the third operational amplifier 24. A fourth resistor R4 is connected between the positive input of the first differential amplifier 23 and the positive input of the third operational amplifier 24. A fifth resistor R5 is connected between the positive input of the third operational amplifier 24 and the fourth voltage U4.

[0039] It is normal to choose the resistances so that the second resistor R2 and the fourth resistor R4 are equal, and so that the third resistor R3 and the fifth resistor R5 are equal. In this case the third voltage U3 may be written as:

$$U3 = (U2-U1) \cdot R3/R2 + U4 \quad (5)$$

[0040] Thus making:

$$k3 = R3/R2 \quad (6)$$

[0041] The compensation voltage U_C should be proportional to the input current I_{in} and when there is no input current I_{in} , then the compensation voltage U_C should be equal to zero. This can be accomplished in practise in many ways. An example is shown schematically in Fig. 3. Since the third voltage U3 is level adjusted by the fourth voltage U4, see (3), said fourth voltage U4 may be used to correct the third voltage U3 and thus the output voltage U_{out} by taking:

$$U4 = U0 - U_C \quad (7)$$

[0042] Thus, the third voltage U3 becomes:

$$U3 = (U2-U1) \cdot k3 + U0 - U_C \quad (8)$$

[0043] To accomplish the compensation voltage U_C the input current I_{in} is transformed to a voltage. This is done by using a first resistor R1 through which the input current I_{in} flows. A second differential amplifier 2 or similar is connected with its negative input to one end of the first resistor R1 and with its positive input connected to the other end of the first resistor R1. Thus, the second differential amplifier reads a voltage $I_{in} \cdot R1$ over the first resistor R1. The second differential amplifier 2 gives out a fifth voltage U5, which is proportional to the photocurrent I_p . The fifth voltage U5 may be used as the compensation voltage U_C directly or after multiplication with a fourth constant k4.

[0044] In Fig. 4 is shown an example on how the second differential amplifier 2 may look. The main part includes a fourth operational amplifier 11 with a positive input, a negative input and an output, which gives out the fifth voltage

U5. A sixth resistor R6 is connected between the negative input of the second differential amplifier 2 and the negative input of the fourth operational amplifier 11. A seventh resistor R7 is connected between the negative input of the fourth operational amplifier 11 and the output of the fourth operational amplifier 11. An eighth resistor R8 is connected between the positive input of the second differential amplifier 2 and the positive input of the fourth operational amplifier 11. A ninth resistor R9 is connected between the positive input of the fourth operational amplifier 11 and ground.

[0045] It is normal to choose the resistances so that the sixth resistor R6 and the eighth resistor R8 are equal, and so that the seventh resistor R7 and the ninth resistor R9 are equal. If the resistance of the first resistance R1 is much smaller than the other resistances then the fifth voltage U5 may be written as:

$$U_5 = (R_1 \cdot I_{in}) \cdot R_7 / R_6 \quad (9)$$

[0046] This is a simplified reasoning. In practise, when the second differential amplifier 2 is to be used in the circuit in Fig. 3, then the eighth resistor R8 should be complemented with some other resistors to compensate for the resistive influence from the first resistor R1.

[0047] The compensation voltage can thus be accomplished by:

$$U_C = U_5 \cdot k_4 = R_1 \cdot R_7 / R_6 \cdot k_4 \cdot I_{in} \quad (10)$$

[0048] An alternative solution to Fig. 3 is to put an inverting amplifier 31 on the output of the first differential amplifier 23, see Fig. 5, thus making the output voltage U_{out} the inverse of the third voltage U3 according to:

$$U_{out} = (U_3 - U_0) \cdot k_5 + U_0 \quad (11)$$

where k_5 is a fifth constant inherent in the inverting amplifier 31. This means that the compensation voltage U_C may instead be added to the level adjust voltage U_0 . To make the output voltage U_{out} correct, the inputs to the first differential amplifier 23 should switch place and the result will then become:

$$U_4 = U_0 + U_C \quad (12)$$

$$U_3 = (U_1 - U_2) \cdot k_3 + U_4 \quad (13)$$

$$U_{out} = (U_0 - U_3) \cdot k_4 + U_0 = (U_2 - U_1) \cdot k_3 \cdot k_4 + U_0 - U_C \cdot k_4 \quad (14)$$

[0049] Now, there may be a wish to use the fifth voltage U5 also for other purposes than to create the compensation voltage U_C , which will be shown later in Fig. 9 ff. In that case it may be a wish to create a fifth voltage U5 with a level adjustment with the level adjust voltage U_0 . This is shown in Fig. 6, where the level adjust voltage U_0 is connected also to the second differential amplifier 2. In this case the compensation voltage should be created as:

$$U_5 = (R_1 \cdot I_{in}) \cdot R_7 / R_6 + U_0 \quad (15)$$

$$U_C = (U_5 - U_0) \cdot k_4 = R_1 \cdot R_7 / R_6 \cdot k_4 \cdot I_{in} \quad (16)$$

[0050] In Fig. 7 is shown a practical implementation of Fig. 6. To be able to trim the magnitude of the compensation voltage U_C a trimming potentiometer R_{tp} is connected with its ends between the fifth voltage U5 and the level adjust voltage U_0 . A tenth resistor R10 is connected between the fourth voltage U4 and the middle connection of the trimming potentiometer R_{tp} . A eleventh resistor R11 is connected between the fourth voltage U4 and the level adjust voltage U_0 .

[0051] To achieve the best result the third resistor R3 in the second differential amplifier 23 may then be complemented by a twelfth resistor R12 and a thirteenth resistor R13 in order to compensate for resistive influence of the tenth resistor R10 and the eleventh resistor R11.

[0052] The inverting amplifier 31 may be any inverting amplifier. However, even though the temperature dependence in the logarithmic amplifier partly is reduced by taking the difference between what is measured and a reference, there is still the second temperature dependency in the third voltage U3 that is proportional to the absolute temperature T in Kelvin. Thus, it would be good to include a circuit with a temperature dependency that is proportional to the inverse of the absolute temperature and the inverting amplifier 31 may be used for that purpose.

[0053] In Fig. 8 is shown an example of such an inverting amplifier. It includes a fifth operational amplifier 32 with a fourteenth resistor R14 on its negative input, with the level adjust voltage U0 on its positive input and a fifteenth resistor R15 between its negative input and its output. The use of only those resistors and with the third voltage U3 connected to the fourteenth resistor R14 would give an output voltage U_{out} of:

$$U_{out} = (U0 - U3) \cdot R15 / R14 + U0 \quad (17)$$

[0054] Hence, if it were possible to find a fourteenth resistor R14 that varied as $R14 = R_0 \cdot T$, where R_0 is a constant, then our problems would be solved. However, that proves difficult to find in practise. This can be solved by adding a temperature dependent resistor R_T in series, before or after, the fourteenth resistor R14. Said temperature dependent resistor R_T is preferably a PRTD, i.e. a Resistance Temperature Detector made of platinum. This type of resistor is very well characterised and standardised since it is normally used as a temperature sensor. The fourteenth resistor R14 and the fifteenth resistor R15 could then be normal resistors with no or at least low temperature dependency. Thus, the output voltage U_{out} becomes:

$$U_{out} = (U0 - U3) \cdot R15 / (R14 + R_T) + U0 \quad (18)$$

[0055] If as an example a PRTD with 1000 Ω complying with the standard DIN EN 60751 according to IEC 751 is used and the fourteenth resistor R14 is chosen as 55.77 Ω , then the maximum deviation within 0-70°C will become approximately 0.2°C. In order to achieve this the temperature dependent resistor R_T should have approximately the same temperature as the transistors T1, T2. This is easiest implemented in practise if the temperature dependent resistor R_T and the transistors T1, T2 are placed close to each other and if the circuit is so dimensioned that the power in the temperature dependent resistor R_T is not so high that self-heating occurs.

[0056] In Fig. 9 is shown the particular case when then the input current I_{in} is a photocurrent from a photodiode or phototransistor 1. The photodiode 1 is connected in series with the first resistor R1. The first resistor R1 may be connected either to the cathode or to the anode of the photodiode 1. However, since the anode is more sensitive it is preferred to connect the first resistor R1 to the cathode, as is shown in the figures. In Fig. 9 and following figures the logarithmic amplifier will be denoted with 4.

[0057] When a photodiode is used in circuits in prior art it is optimised either for high or low optical powers by using a constant bias voltage. As an example, if a photodiode of PIN-type is used and a low optical power, such as $<1 \mu W$, is to be measured, then the photodiode should have a bias voltage of 0 V. This is due to the fact that photodiodes when biased normally has a so called dark current which may disturb. The photodiode may also be seen as having a shunt resistance that conducts when the bias voltage is not 0 V and thus provides a current. The magnitude of said currents may be e.g. 25 nA at 70°C.

[0058] If on the other hand said photodiode is to measure a high optical power, such as $>0,5 \text{ mW}$, the photodiode needs to be biased with e.g. 5 V or else the photodiode will become saturated and the photo current will thus become too small.

[0059] A disadvantage with known circuits for photodiodes is thus that the range of the optical power cannot be too wide. An example of an application where the optical power range is wide is in systems using wavelength division multiplexing (WDM). This means that signals are transmitted in a line divided into channels with different wavelengths. The signals are amplified on the way and sometimes it is wished to be able to measure the total optical power before or after amplification. The development is going towards more channels in the same line, which of course leads to a higher maximum optical power and thus an urgent need exists for something that may measure a wide optical power range.

[0060] This problem may be solved with the additional features in Fig. 9. The main idea is that said photocurrent I_{in} is to be measured and compared to a threshold and that the photodiode 1 is given a bias voltage U_B depending on if the photocurrent I_{in} is above or below said threshold. It is possible to measure the photocurrent I_{in} directly and to compare it to a threshold current. However, voltages are easier to measure and compare and actually this is already done in Fig 9 - the fifth voltage U5. This is an example of when it may be good to have the fifth voltage U5 with a level adjustment.

[0061] The fifth voltage U_5 is now compared with a threshold voltage U_{th} in a comparator 3, which then gives out a sixth voltage U_6 , which will affect the bias voltage U_B . The anode of the photodiode 1 is in this example connected to a voltage at ground level, so called virtual ground.

[0062] The fifth voltage U_5 is connected to the positive input of the comparator 3 and the threshold voltage U_{th} is connected to the negative input of the comparator 3. Thus, if the fifth voltage U_5 is greater than the threshold voltage U_{th} , then the sixth voltage U_6 from the comparator 3 becomes high, e.g. 5 V. Thus, the bias voltage U_B in this case becomes a little less than 5 V. If, on the other hand, the fifth voltage U_5 is smaller than the threshold voltage U_{th} , then the sixth voltage U_6 from the comparator 3 becomes 0 V. Thus, the bias voltage U_B in this case becomes extremely close to 0 V. The magnitude of the high bias voltage is chosen to suit the particular photodiode 1 that is used, depending on its inner resistance. However, to simplify the description, the example 5 V will be used in the following.

[0063] If the voltage at the anode of the photodiode 1 should have another magnitude than virtual ground, then the values of the sixth voltage U_6 given above should be changed accordingly to give the desired bias voltage U_B .

[0064] An advantage with the invention in Fig. 9 is that it is a photodiode bias circuit that works well when the photodiode is to measure low optical powers. This is because the bias voltage U_B in this case is 0 V, which minimises both dark current and the effects of the shunt resistance and thus improves linearity. Further, the invention in Fig. 1 is also a photodiode bias circuit that works well when the photodiode is to measure high optical powers. This is because the photodiode in this case gets a bias voltage U_B of e.g. 5 V, which prevents the photodiode from becoming saturated too quickly and thus improves linearity. Thus, a photodiode bias circuit is achieved that works linearly in a wide optical power range.

[0065] In Fig. 10 is shown an embodiment of the comparator 3. It is difficult to find a commercial comparator that has a swing between 0 V and 5 V. When low optical powers are to be measured, the closer the bias voltage U_B , i.e. in this case also the sixth voltage U_6 , is to 0 V, the better, i.e. the more linear, this photodiode circuit will work. The sixth voltage U_6 should in that case preferably not be higher than a few mV. Commercial comparators often have difficulties in getting that close to 0 V.

[0066] This can be solved with the embodiment in Fig. 10, where the comparator 3 includes an inverter 13 and an inner comparator 12 with a positive and a negative input and an output. The positive input of the inner comparator 12 is used as the negative input of the comparator 3 and vice versa, due to the following inverter 13. If the inverter 13 is e.g. of CMOS-type it will have the same logical output as its supply voltage. Thus if the inverter 13 is supplied with 0 V and 5 V, its output will change between 0 V and 5 V, which is exactly what is wanted. Note that the main issue is not that it is an inverter, but that it has the output that is wanted. The same result could be achieved with e.g. another CMOS-circuit or with a comparator with CMOS-type output.

[0067] A photodiode is normally sensitive to fast changes in its bias voltage, why it is a big advantage if the positive supply voltage to the inverter 13 is carefully filtered so that there are no disturbances on the output of the inverter 13.

[0068] If the fifth voltage U_5 happens to be close to the threshold voltage U_{th} , frequent changes could occur in the sixth voltage U_6 and thus in the bias voltage U_B . That is not desired. An improved solution would then be to introduce a hysteresis with two thresholds. This may e.g. be accomplished by using a comparator with a feedback, also called a Schmitt trigger. This is represented in Fig. 11. A sixteenth resistor R_{16} is connected between the power supply voltage V_{cc} and the positive input of the inner comparator 12. A seventeenth resistor R_{17} is connected between the level adjust voltage U_0 and the positive input of the inner comparator 12. An eighteenth resistor R_{18} is connected between the positive input and the output of the inner comparator 12.

[0069] The threshold voltage U_{th} is created on the positive input of the inner comparator 12 with a level adjustment from the level adjust voltage U_0 . If the circuit should be arranged so that the threshold voltage U_{th} feeds the negative input of the inner comparator 12, then the positive input of the inner comparator 12 should be fed from a low-resistance source in order that the positive feedback is precisely determined, i.e. the resistances should be selected so that $R_{17} \ll R_{18}$.

[0070] When then the connection is as in Fig. 11 and the output of the inner comparator 12 changes state, then the positive feedback has the effect of changing the threshold voltage U_{th} slightly so that a relatively large change of input signal is then required to reverse the output state.

[0071] It is possible to change the bias voltage both fast and slow. A photodiode have a certain capacitance between its anode and cathode. This leads to that when the voltage is changed over the photodiode, then a transient current is generated proportionally to the derivative of the voltage change. Thus, one would believe that it would be better to change the bias voltage slowly. However, if the bias voltage is changed slowly, then the total circuit will become slow and rapid changes in optical power will not be measured. Thus, the preferred embodiment is to change the bias voltage fast.

[0072] When the bias voltage is raised, then said transient current will have a rather small influence compared to the large photo current. Instead there will be a problem when the optical power and thus the bias voltage is lowered. That is because the charge between the cathode and the anode of the photodiode will totally cut-off the logarithmic amplifier. Thus, the logarithmic amplifier will consider that it is measuring total darkness and will do that until the photo-

current has restored the real charge.

[0073] A solution to this problem is shown in Fig. 12. A charge compensation capacitor C1 is introduced between the anode of the photodiode 1 and the output of the comparator 3 over a second inverter 15. The purpose is to generate a second transient current with the opposite sign as the first transient current produced by the photodiode 1 when the bias voltage is changed.

[0074] Preferably, the capacitance of the charge compensation capacitor C1 is somewhat larger than the capacitance of the photodiode 1. What will happen is then this: When the bias voltage U_B suddenly goes down to 0 V, then a first transient current will come out from the input of the logarithmic amplifier 4 through the photodiode. A few ns later a somewhat larger second transient current will be produced by the charge compensation capacitor C1 in the opposite direction. If the logarithmic amplifier 4 is normally slow it will only feel a small fast sum transient current in the right direction, i.e. into its input. This means that the output voltage U_{out} will experience a fast positive transient and then regain its correct value without ever going below said correct value. Thus, the logarithmic amplifier 4 and subsequent circuits will never believe that it is dark simply because the bias voltage U_B suddenly is lowered.

[0075] In the simplest version there is simply a direct connection between the charge compensation capacitor C1 and the second inverter 15. This means that the charge compensation capacitor C1 always is connected with a low impedance to the second inverter 15. In certain applications this is a disadvantage. As an example may the bandwidth of the total circuit with photodiode and logarithmic amplifier become deteriorated due to the extra input capacitance from the charge compensation capacitor C1.

[0076] This may be solved by using an isolator 16 to isolate the charge compensation capacitor C1 from the second inverter 15 e.g. with the aid of diodes. The isolator may be implemented in numerous ways and one alternative is shown in Fig. 12. The man skilled in the art can easily adopt other versions with equivalent function.

[0077] A second capacitor C2 is on one end connected to the output of the second inverter 15 and on its other end, at the first potential V1, to the anode of a first diode, to a nineteenth resistor R19 and to a twentieth resistor R20. The twentieth resistor R20 is further connected to ground. The cathode of the first diode D1 is connected, at the second potential V2, to the charge compensation capacitor C1 and to the anode of a second diode D2. The cathode of the second diode D2 is further connected, at the third potential V3, to the nineteenth resistor R19.

[0078] In a status quo case the three potentials V1, V2, V3 will be 0 V since no currents are flowing. Further, the impedance over the isolator 16 will be high - with a low capacitance.

[0079] If the photocurrent I_{in} decreases and the sixth voltage U_6 goes down to 0 V, then the second inverter 15 will go high and the second capacitor C2 will be charged. Thus, the first potential V1 will become high and the first diode D1 starts to conduct, which means that the second potential V2 will become high. This in its turn will charge the charge compensation capacitor C1, which will discharge through the input of the logarithmic amplifier 4, as mentioned earlier.

[0080] The second capacitor C2 should be chosen with a higher capacitance than the charge compensation capacitor C1, because in that case the second capacitor C2 will discharge slower than the charge compensation capacitor C1. The second capacitor C2 discharges over the twentieth resistor R20 to ground. When it is completely discharged, the first potential V1 will once again become 0 V and the first diode D1 will stop conducting. The second potential V2 will discharge again over the second diode D2 and the nineteenth resistor R19. Thus, the status quo is once again reached.

[0081] If instead the photo current I_{in} increases and thus the sixth voltage U_6 increases and thus the second inverter goes low, then the second capacitor C2 will be charged and the first potential V1 will decrease to -5 V. The second capacitor C2 will then charge and discharge much like the previous example, but with the current in the opposite direction and the first potential will then return to 0 V.

[0082] A preferred embodiment is that the transient current from the charge compensation capacitor C1 should not be very high when the photo current I_{in} is high, as explained above. In that case the resistances of the nineteenth resistor R19 and the twentieth resistor R20 should be rather high. That is because that leads to that only a small current flows from the second potential V2 to the first potential V1 over the second diode D2 and the nineteenth resistor R19. Thus, the charge compensation capacitor C1 is charged slower and a smaller transient current will occur.

[0083] In prior art it is common to filter away disturbances with strong low-pass-filtering, which gives the effect that the bandwidth is narrowed and thus that fast changes in the optical power cannot be measured. An advantage with the last embodiments of the present invention is that the automatic change of the bias voltage is so smooth that it is possible to have a high bandwidth without getting problems with disturbances.

[0084] A further advantage with this embodiment is that the same circuit - the second differential amplifier 2 - may be used for two purposes, i.e. to create the bias voltage U_B for the photodiode and to create the compensation voltage U_C . This saves components and space and further reduces the time for manufacturing. However, it would be equally possible to have separate circuits for the two purposes.

[0085] The first resistor R1 may be connected either to the cathode or to the anode of the photodiode 1. However, since the anode is more sensitive it is preferred to connect the first resistor R1 to the cathode, as is shown in the figures.

[0086] Alternative and equivalent embodiments to those above arise if instead of the anode, the cathode of the photodiode is connected to the logarithmic amplifier. Then all the signs in the rest of the circuits would have to change.

E.g. would the sixth voltage U_6 then become -5 V at high optical powers.

Claims

1. Logarithmic amplifier for reading an input current (I_{in}) or input voltage (U_{in}) and for giving out an output voltage (U_{out}), said logarithmic amplifier including a logarithmic element (T1) for generating logarithmic amplification, said logarithmic element (T1) including an inner serial resistance, **characterized in that** a compensation voltage (U_c) is arranged to be subtracted from the output voltage (U_{out}) to compensate for voltage drop over the inner serial resistance.
2. Logarithmic amplifier according to claim 1, **characterized in that** the compensation voltage (U_c) is a function of the input current (I_{in}) or input voltage (U_{in}).
3. Logarithmic amplifier according to any of the claims 1-2, **characterized in that** the logarithmic element (T1) is a transistor.
4. Logarithmic amplifier according to any of the claims 1-2, **characterized in that** the logarithmic element (T1) is a diode.
5. Logarithmic amplifier according to any of the claims 1-4, **characterized in that** a first differential amplifier (23) is provided with three inputs and an output, in that the first voltage (U_1) is connected to the first input of the first differential amplifier (23), in that a second voltage (U_2) proportional to a reference current (I_{ref}) is connected to the second input of the first differential amplifier (23), in that a fourth voltage (U_4) proportional to the compensation voltage (U_c) is connected to the third input of the first differential amplifier and in that a third voltage (U_3) related to the output voltage (U_{out}) may be taken out from the output of the first differential amplifier (23).
6. Logarithmic amplifier according to claim 5, **characterized in that** an inverting amplifier (31) including a positive input, a negative input and an output is connected to the output of the second differential amplifier (23).
7. Logarithmic amplifier according to claim 6, **characterized in that** the inverting amplifier (31) includes a temperature dependent resistor (R_T) on its negative input.
8. Logarithmic amplifier according to claim 7, **characterized in that** the temperature dependent resistor (R_T) is a resistance temperature detector made of platinum.
9. Logarithmic amplifier according to any of the claims 7-8, **characterized in that** a resistor (R_{19}) with a resistance of 55.77 Ω is connected in series with the temperature dependent resistor (R_T), and in that the temperature dependent resistor (R_T) has a resistance of 1000 Ω .
10. Logarithmic amplifier according to any of the claims 1-9, **characterized in that** a second differential amplifier (2) with at least two inputs and at least one output is connected with two of its inputs on each side of a first resistor (R_1), in that the input current (I_{in}) is arranged to flow through said first resistor (R_1), and in that a fifth voltage (U_5) related to the compensation voltage (U_c) is provided on the output of the second differential amplifier (2).
11. Logarithmic amplifier circuit including a logarithmic amplifier and a photodiode (1) producing a photocurrent (I_p) used as the input current (I_{in}), said photodiode (1) being biased with a bias voltage (U_B) **characterized in that** the logarithmic amplifier is according to any one of the claims 1-10.
12. Logarithmic amplifier circuit according to claim 11, **characterized in that** the photodiode (1) is connected with its anode to the first resistor (R_1).
13. Logarithmic amplifier circuit according to any of the claims 11-12, **characterized in that** the logarithmic amplifier circuit further includes a comparator (3, 12) for comparing the fifth voltage (U_5) with a threshold (U_{th}) and for biasing the photodiode (1) with a bias voltage (U_B) having a magnitude depending on whether the fifth voltage (U_5) is larger than the threshold (U_{th}) or smaller.
14. Logarithmic amplifier circuit according to claim 13, **characterized in that** the bias voltage (U_B) has a first magnitude

close to 0 V if the fifth voltage (U5) is smaller than the threshold and a second magnitude corresponding to a positive voltage, such as 5 V, if the fifth voltage (U5) is larger than the threshold.

- 5 15. Logarithmic amplifying method in a logarithmic amplifier including a logarithmic element (T1), such as a transistor or a diode, with an inner serial resistance, said method including reading an input current (I_{in}) or an input voltage (V_{in}) and giving out an output voltage (V_{out}), **characterized** by compensating for voltage drop over the inner serial resistance by subtracting a compensation voltage (U_C) from the output voltage (U_{out}).
- 10 16. Logarithmic amplifying method according to claim 15, **characterized** by creating the compensation voltage (U_C) as a function of the input current (I_{in}).
- 15 17. Logarithmic amplifying method according to any of the claims 15-16, wherein a photodiode (1) is producing a photocurrent used as the input current (I_{in}), said photodiode (1) being biased with a bias voltage (U_B) **characterized** by using a fifth voltage (U5) to generate both the compensation voltage (U_C) and the bias voltage (U_B).
- 20 18. Logarithmic amplifying method according to claim 17, **characterized** by comparing the fifth voltage (U5) with a threshold (U_{th}) and giving the bias voltage (U_B) a magnitude depending on whether the fifth voltage (U5) is larger than the threshold (U_{th}) or smaller.
- 25 19. Logarithmic amplifying method according to claim 18, **characterized** by giving the bias voltage (U_B) a first magnitude close to 0 V if the fifth voltage (U5) is smaller than the threshold (U_{th}) and a second magnitude corresponding to a positive voltage, such as 5 V, if the fifth voltage (U5) is larger than the threshold (U_{th}).
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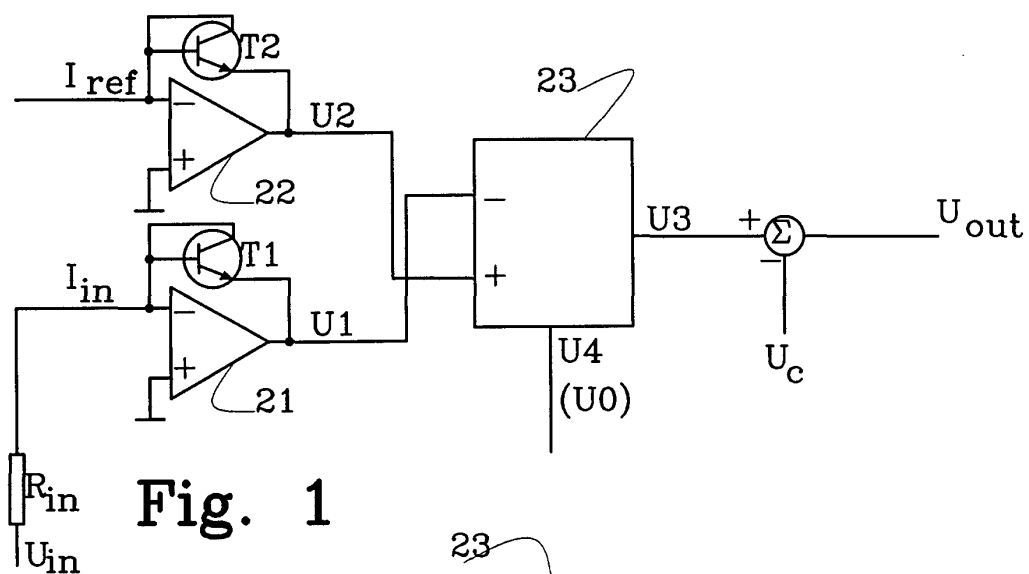


Fig. 1

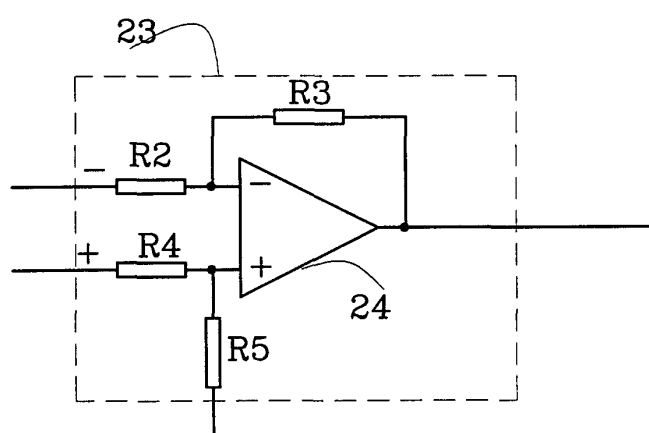


Fig. 2

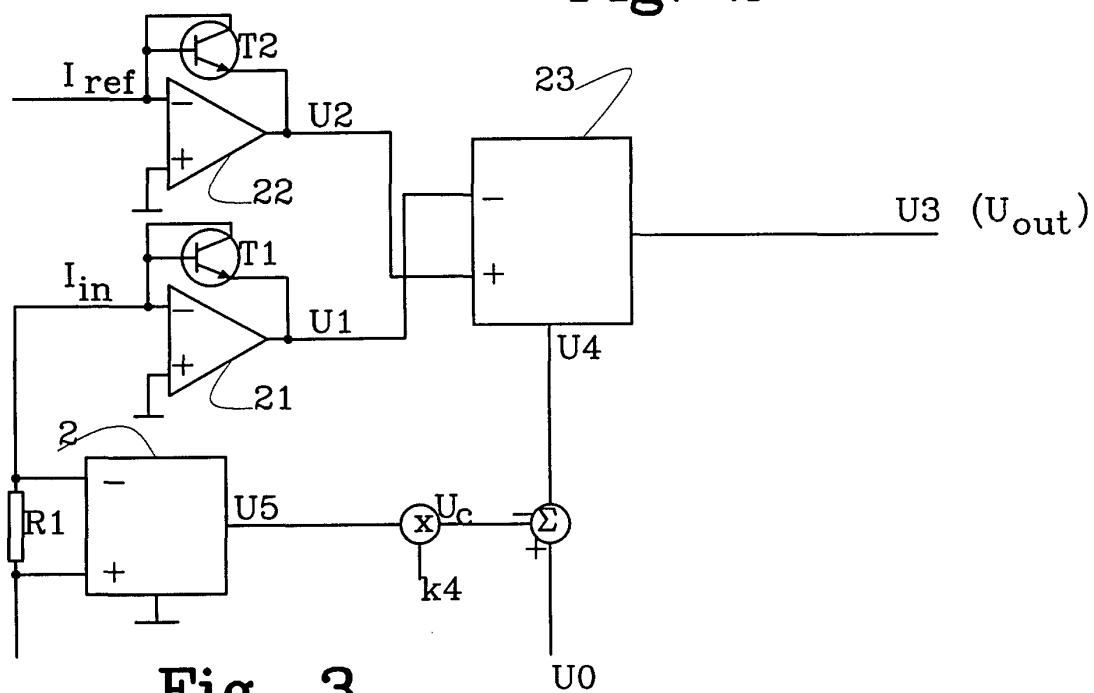


Fig. 3

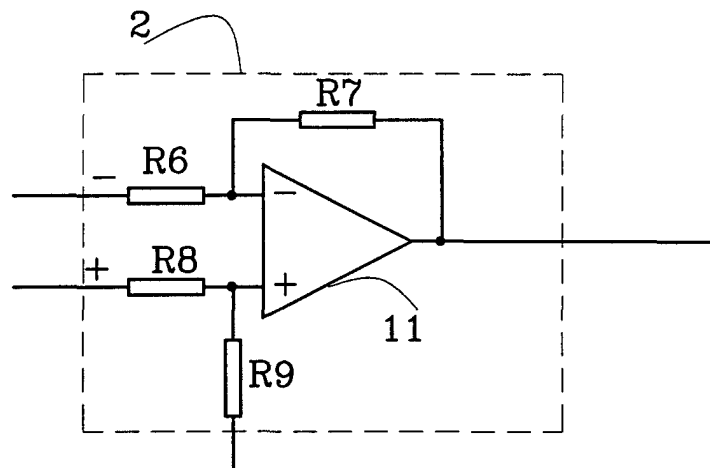


Fig. 4

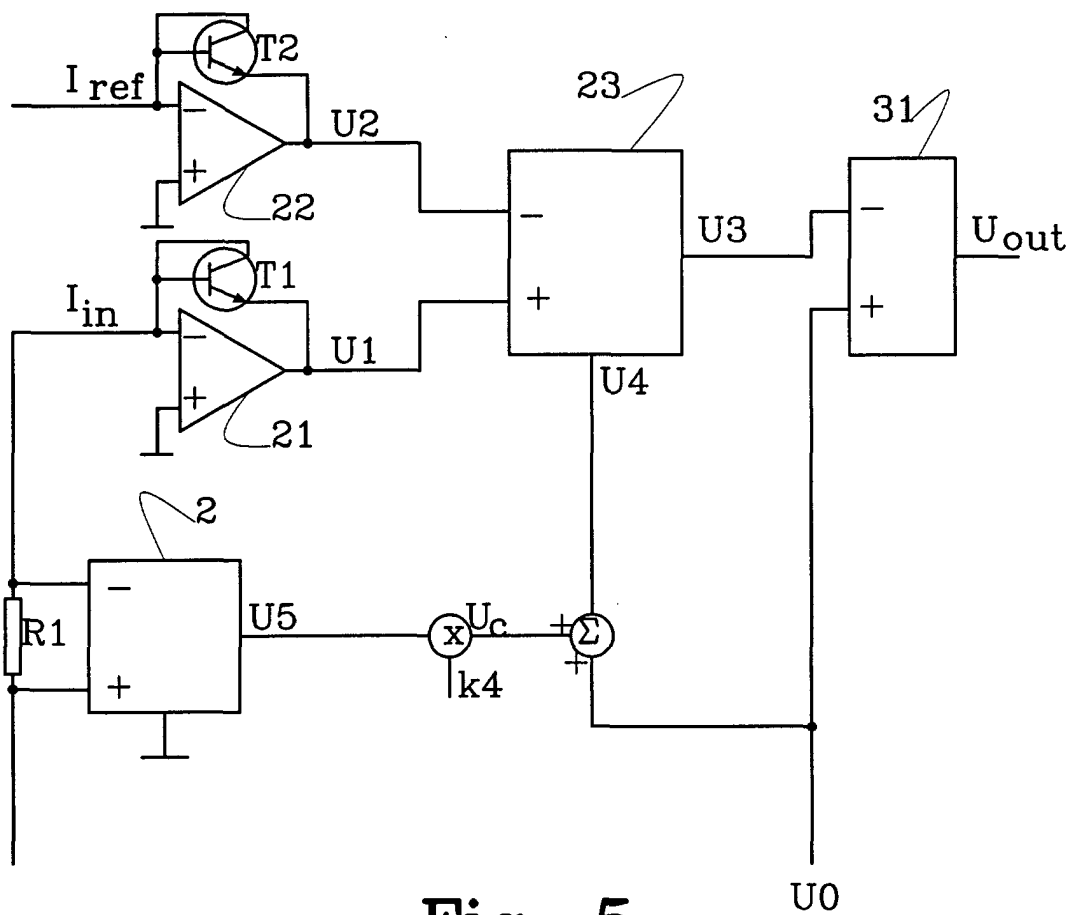


Fig. 5

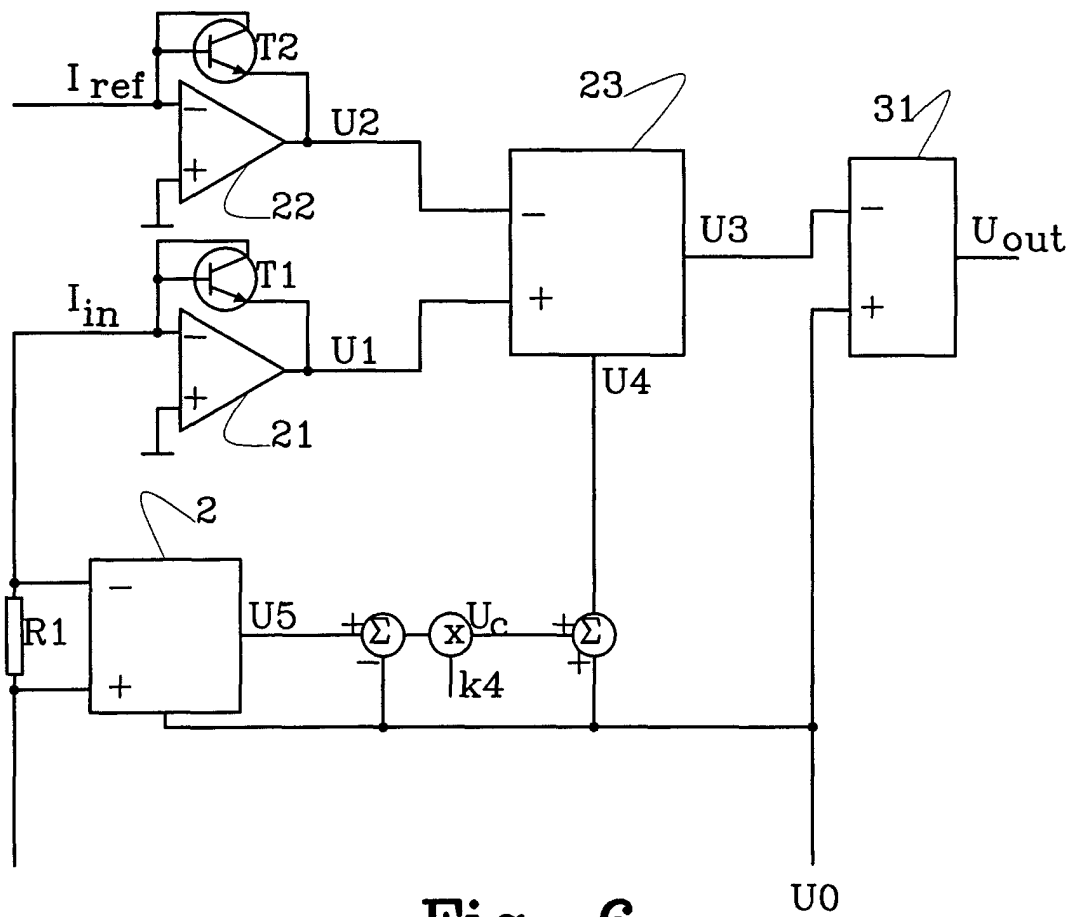


Fig. 6

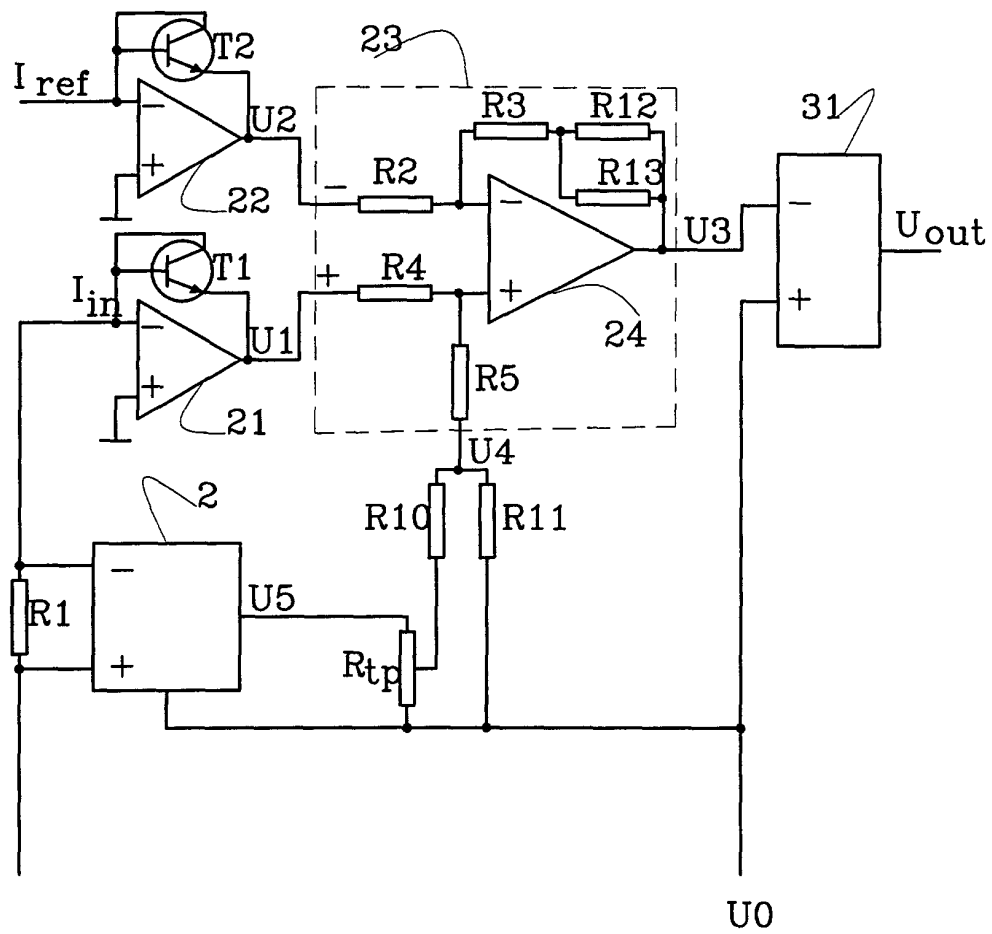


Fig. 7

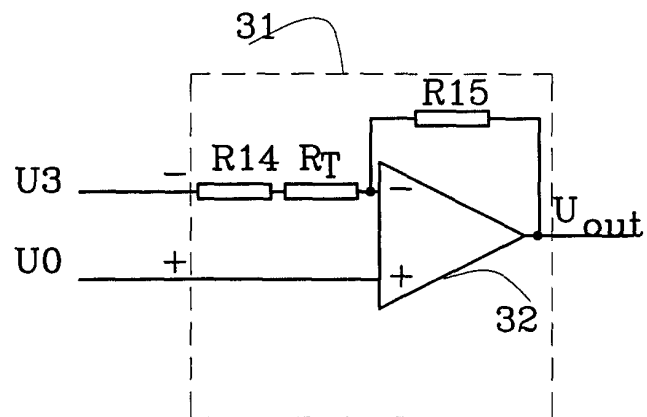


Fig. 8

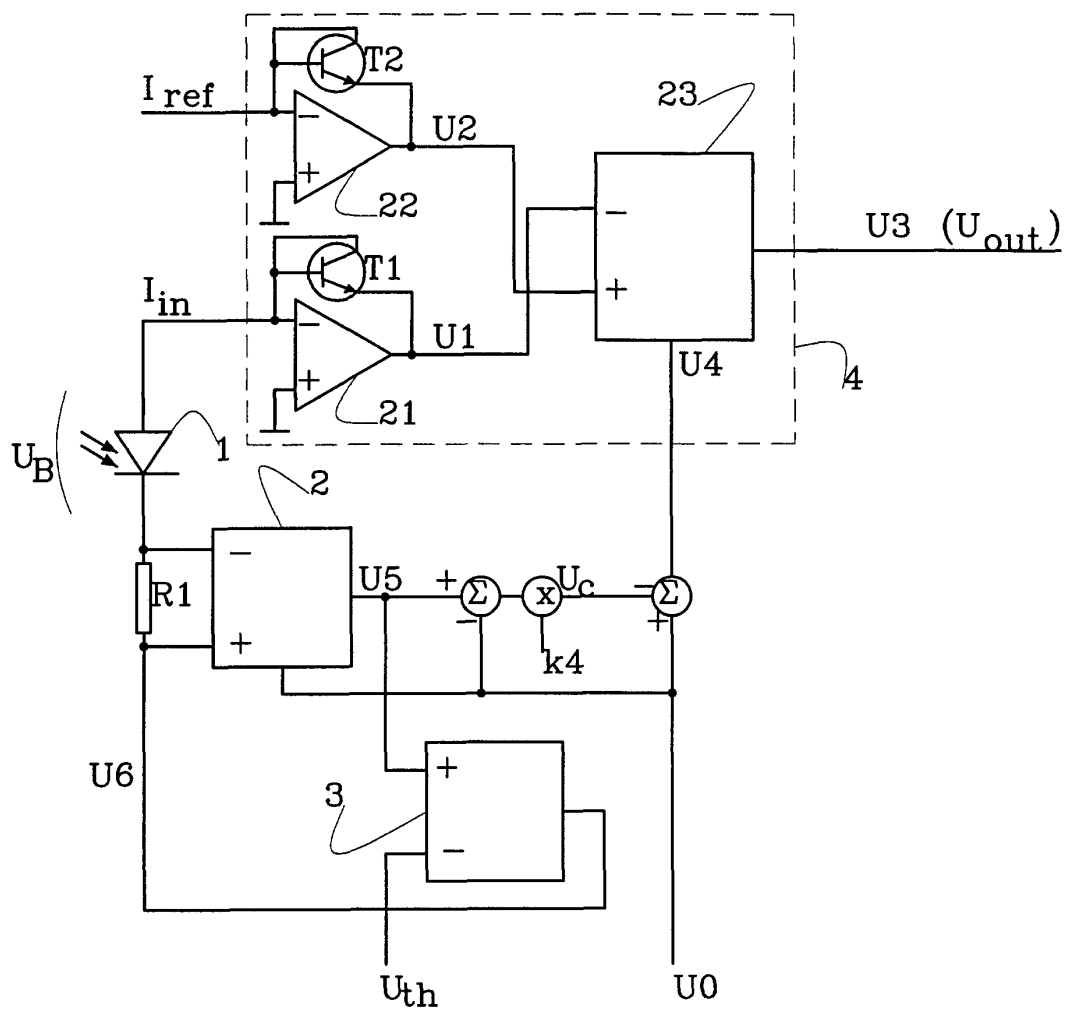


Fig. 9

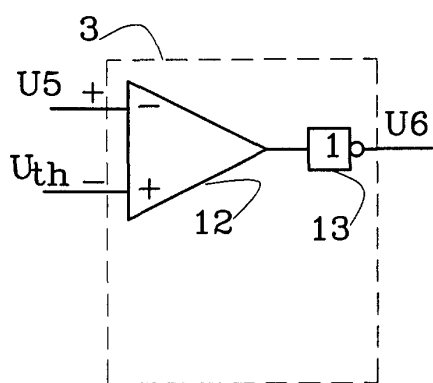


Fig. 10

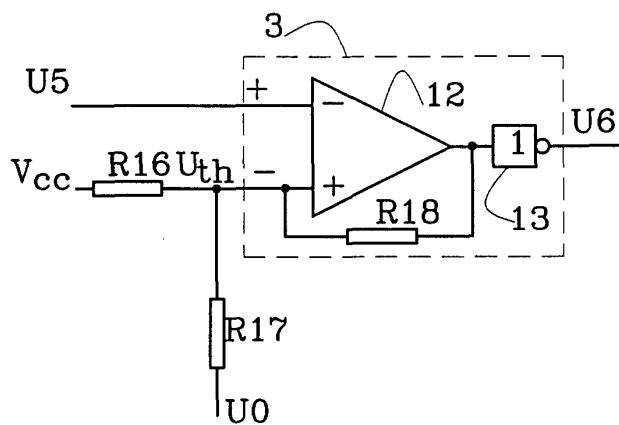


Fig. 11

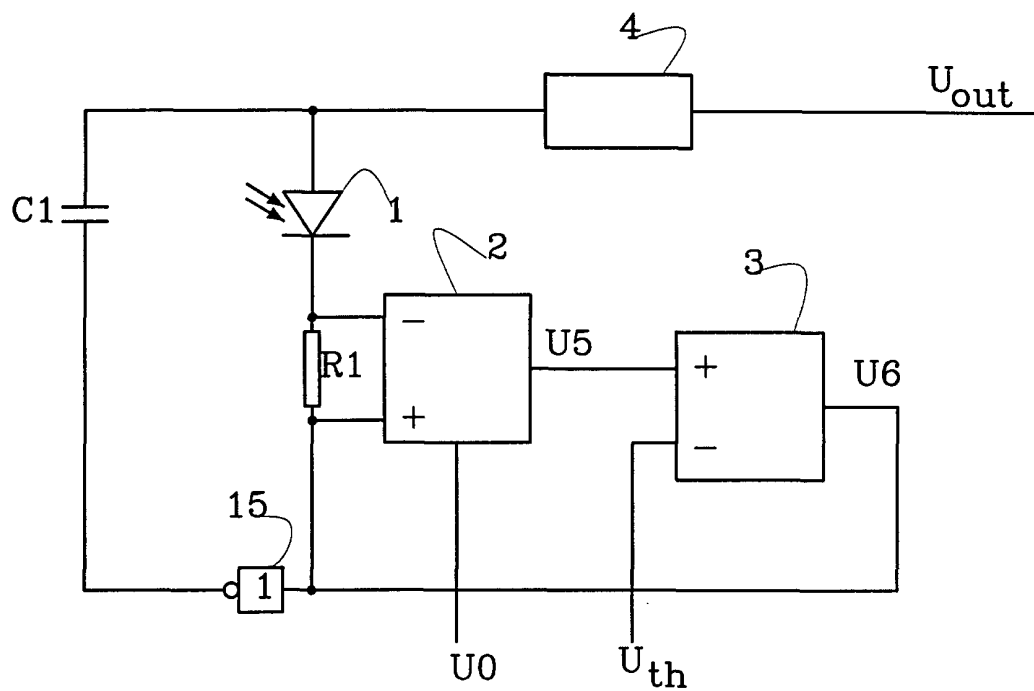


Fig. 12

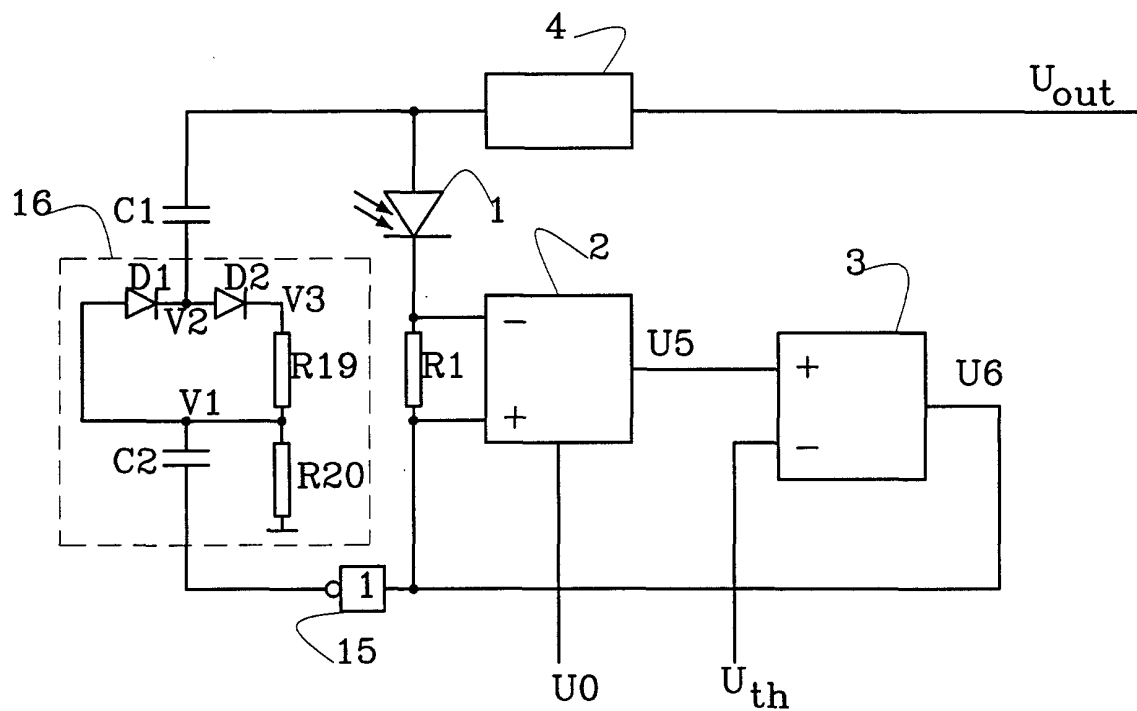


Fig. 13



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 85 0034

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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 29 June 2000	Examiner Blaas, D-L
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03/92 (P04C01)

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