

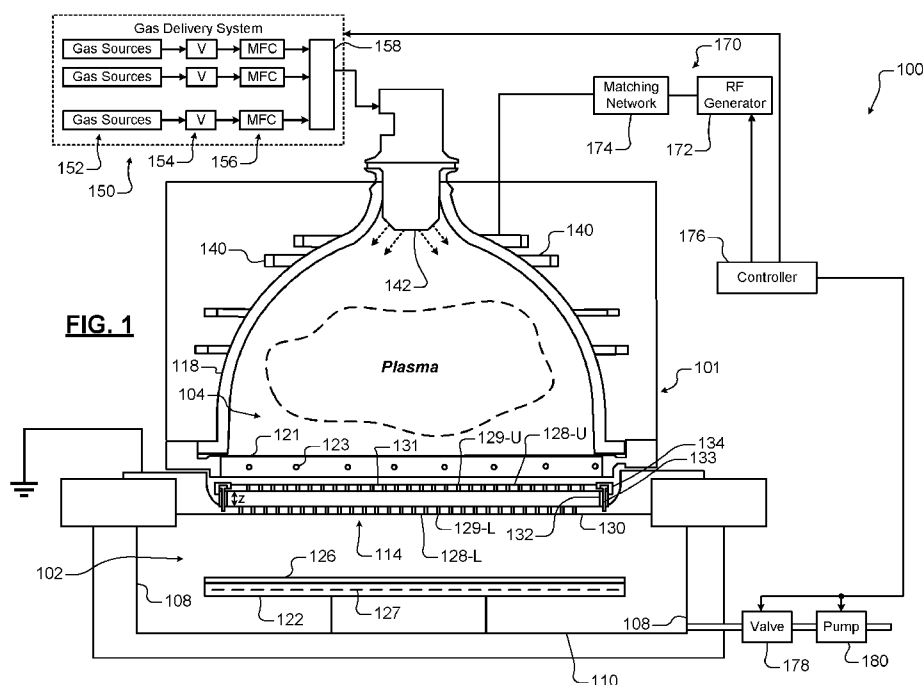
(51) International Patent Classification:
H01J 37/32 (2006.01)(21) International Application Number:
PCT/US2020/014329(22) International Filing Date:
21 January 2020 (21.01.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/795,814 23 January 2019 (23.01.2019) US(71) Applicant: **LAM RESEARCH CORPORATION**
[US/US]; 4650 Cushing Parkway, Fremont, California
94538 (US).(72) Inventors: **BRAVO, Andrew Stratton**; 2411 Burlington
St, Oakland, California 94602 (US). **HSU, Chih-Hsun**;
3940 Via Montalvo, Campbell, California 95008 (US).
KOSCHE, Serge; 155 Teresita Blvd, San Francisco, Cal-
ifornia 94127 (US). **WHITTEN, Stephen**; 3437 Clar-idge Dr, Danville, California 94526 (US). **KON, Shih-
Chung**; 48690 Taos Rd, Fremont, California 94539 (US).
KAWAGUCHI, Mark; 77 Madera Ave, San Carlos, Cali-
fornia 94070 (US). **CHOKSHI, Himanshu**; 38642 Pickering
Court, Fremont, California 94536 (US). **ZHANG, Dan**;
166 Racoon Ct., Fremont, California 94539 (US). **AM-
BUROSE, Gnanamani**; 49079 Woodgrove Common, Fre-
mont, California 94538 (US).(74) Agent: **WIGGINS, Michael D.**; HARNESS, DICKEY &
PIERCE, P.L.C., P.O. Box 828, Bloomfield Hills, Michigan
48303 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) Title: SUBSTRATE PROCESSING SYSTEM INCLUDING DUAL ION FILTER FOR DOWNSTREAM PLASMA



(57) Abstract: A substrate processing system includes an upper chamber and a gas delivery system to supply a gas mixture to the upper chamber. An RF generator generates plasma in the upper chamber. A lower chamber includes a substrate support. A dual ion filter is arranged between the upper chamber and the lower chamber. The dual ion filter includes an upper filter including a first plurality of through holes configured to filter ions. A lower filter includes a second plurality of through holes configured to control plasma uniformity.



SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

SUBSTRATE PROCESSING SYSTEM INCLUDING DUAL ION FILTER FOR DOWNSTREAM PLASMA

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/795,814, filed on January 23, 2019. The entire disclosure of the application referenced above is incorporated herein by reference.

FIELD

[0002] The present disclosure relates to substrate processing systems, and more particularly to a substrate processing system including an ion filter.

BACKGROUND

[0003] The background description provided here is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Substrate processing systems may be used to perform treatments on substrates such as semiconductor wafers. Examples of the treatments include deposition, etching, cleaning, etc. The substrate processing systems typically include a processing chamber including a substrate support, a gas delivery system and a plasma generator.

[0005] During processing, the substrate is arranged on the substrate support. Different gas mixtures may be introduced by the gas delivery system into the processing chamber. In some applications, radio frequency (RF) plasma such as inductively coupled plasma (ICP) may be used to activate chemical reactions.

[0006] ICP produces both highly reactive neutral species and ions to modify wafer surfaces. As customer devices become increasingly complicated and sensitive, controlling exposure of the substrate to the plasma is increasingly important. Ions generated within the plasma can have damaging effects on sensitive materials within device structures. The ions can modify the properties of device materials and adversely affect the performance of the overall structure.

SUMMARY

[0007] A substrate processing system includes an upper chamber and a gas delivery system to supply a gas mixture to the upper chamber. An RF generator generates plasma in the upper chamber. A lower chamber includes a substrate support. A dual ion filter is arranged between the upper chamber and the lower chamber. The dual ion filter includes an upper filter including a first plurality of through holes configured to filter ions. A lower filter includes a second plurality of through holes configured to control plasma uniformity.

[0008] In other features, a diameter of the first plurality of through holes of the upper filter is less than a diameter of the second plurality of through holes of the lower filter. A number of the first plurality of through holes of the upper filter is greater than a number of the second plurality of through holes of the lower filter. The upper filter and the lower filter are connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference.

[0009] In other features, the first plurality of through holes of the upper filter have a first diameter in a range from 0.5mm to 1.5mm. A number of the first plurality of through holes are in a range from 5,000 to 50,000. The second plurality of through holes of the upper filter have a first diameter in a range from 1mm to 4mm. A number of the first plurality of through holes are in a range from 100 to 10,000.

[0010] In other features, the upper filter is arranged parallel to the lower filter. The upper filter is spaced from the lower filter by a predetermined gap in a range from 1 mm to 50mm. At least one of the upper filter and the lower filter includes an inner cooling plenum to receive a cooling fluid.

[0011] In other features, a spacing ring is arranged between the upper filter and the lower filter. A fastener is made of a conducting material and connects the upper filter to the lower filter through a bore in the spacing ring. A protective cover is made of a plasma-resistant material and is arranged on a plasma-facing surface of the fastener.

[0012] In other features, an inductive coil is arranged around an outer surface of the upper chamber. The RF generator generates plasma in the upper chamber by supplying an RF signal to the inductive coil while the gas mixture is supplied by the gas delivery system.

[0013] In other features, the upper filter is connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference. The lower filter is connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference. The upper filter and the lower filter have a different bias.

[0014] In other features, the upper filter and the lower filter are made of aluminum and include a coating selected from a group consisting of nickel and yttria. In other features, the lower filter is made of aluminum and includes a yttria coating on a plasma-facing surface thereof and a nickel coating on a substrate-facing side thereof. The upper filter has a thickness in a range from 2 to 5 mm and the lower filter has a thickness in a range from 5 to 15 mm.

[0015] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0017] FIGs. 1 and 2 are functional block diagrams of examples of substrate processing systems including a dual ion filter according to the present disclosure;

[0018] FIGs. 3A, 3B and 4 are enlarged cross-sectional views of examples of the dual ion filter according to the present disclosure;

[0019] FIG. 5 is a graph illustrating charge receptor measurement of a single ion filter and a dual ion filter according to the present disclosure; and

[0020] FIG. 6 is a flowchart of an example of a method for using a dual ion filter to filter ions in a processing chamber according to the present disclosure.

[0021] In the drawings, reference numbers may be reused to identify similar and/or identical elements.

DETAILED DESCRIPTION

[0022] Substrate processing systems and methods according to the present disclosure include a dual ion filter arranged between an upper chamber region where plasma is

generated and a lower chamber region where the substrate is located. The dual ion filter includes an upper filter that is configured to predominantly filter ions generated by the plasma. The lower filter is configured to predominantly control plasma uniformity. The dual ion filter reduces ions reaching the substrate by increasing the electrically grounded area to capture ions, increasing surface area to help recombination, and decreasing the mean free path to assist with recombination.

[0023] Referring now to FIGs. 1 and 2, a substrate processing system 100 includes a substrate processing chamber 101. Although the substrate processing chamber 101 is shown as an inductively coupled plasma (ICP) based system, the examples disclosed herein may be applied to other types of substrate processing systems such as transformer coupled plasma (TCP) or downstream plasma systems.

[0024] The substrate processing chamber 101 includes a lower chamber region 102 and an upper chamber region 104. The lower chamber region 102 is defined by chamber sidewall surfaces 108, a chamber bottom surface 110 and a lower surface of a dual ion filter 114.

[0025] The upper chamber region 104 is defined by an upper surface of the dual ion filter 114 and an inner surface of a dome 118. In a TCP based system, the dome 118 may be replaced by a cylindrical-shaped structure. In some examples, the dome 118 rests on a first annular support 121 including one or more spaced holes 123 for delivering process gas to the upper chamber region 104. In some examples, the process gas is delivered by the one or more spaced holes 123 in an upward direction at an acute angle relative to a plane including the dual ion filter 114, although other angles/directions may be used. A gas flow channel in the first annular support 121 may be used to supply gas to the one or more spaced holes 123.

[0026] The substrate support 122 is arranged in the lower chamber region 102. In some examples, the substrate support 122 includes an electrostatic chuck (ESC), although other types of substrate supports can be used. A substrate 126 is arranged on an upper surface of the substrate support 122 during processing such as etching. In some examples, a temperature of the substrate 126 may be controlled by heating elements (or a heater plate) 127, an optional cooling plate with fluid channels and one or more sensors (not shown), although any other suitable substrate support temperature control system may be used.

[0027] In some examples, the dual ion filter 114 includes a lower filter 128-L with N_1 through holes 129-L each having a diameter D_1 . The dual ion filter 114 includes an upper filter 128-U with N_2 through holes 129-U each having a second diameter D_2 . In some examples, the lower and upper filters 128-L and 128-U include planar portions 130 and 131, respectively, that are arranged parallel to one another. In some examples, the lower and upper filters 128-L and 128-U are connected to a reference potential such as ground (FIG. 1), a positive DC reference potential (FIG. 2), or negative DC reference potential (FIG. 2). The upper and lower filters 128-U and 128-L can be biased by the same reference potential or different reference potentials. As will be described further below, the lower and upper filters 128-L and 128-U may include an internal plenum to receive cooling fluid such as a liquid or gas.

[0028] The upper filter 128-U may be supported above the lower filter 128-L by an annular ring 132 (or supported in a similar spaced relationship in another manner). Alternately, the lower filter 128-L may be supported below the upper filter 128-U by the annular ring 132 (or supported in a similar spaced relationship in another manner). In still other examples, the upper filter 128-U and the lower filter 128-L are independently supported by chamber walls or one or more other processing chamber components in a spaced relationship.

[0029] In some examples, the annular ring 132 is made of a non-conducting material. A fastener 133 may be used to provide physical and electrical connections between the lower and upper filters 128-L and 128-U. In some examples, the fastener 133 is made of metal such as bare aluminum, although other materials can be used. A protective cover 134 may be arranged over the fastener 133. In some examples, the protective cover 134 is made of a plasma resistant material such as ceramic, or a non-plasma resistant material that is coated with a plasma resistant material.

[0030] One or more inductive coils 140 may be arranged around an outer portion of the dome 118. When energized, the one or more inductive coils 140 create an electromagnetic field inside of the dome 118. In some examples, an upper coil and a lower coil are used. A gas injector 142 injects one or more gas mixtures from a gas delivery system 150. The gas delivery system 150 includes one or more gas sources 152, one or more valves 154, one or more mass flow controllers (MFCs) 156, and a mixing manifold 158, although other types of gas delivery systems may be used. Suitable gas delivery systems are shown and described in commonly assigned U.S.

Patent Application Serial No. 14/945,680, entitled "Gas Delivery System" and filed on December 4, 2015, which is hereby incorporated by reference in its entirety. Suitable single or dual gas injectors and other gas injection locations are shown and described in commonly assigned U.S. Provisional Patent Application Serial No. 62/275,837, 5 entitled "Substrate Processing System with Multiple Injection Points and Dual Injector" and filed on January 7, 2016, which is hereby incorporated by reference in its entirety.

[0031] In some examples, the gas injector 142 includes a center injection location that directs gas in a downward direction and one or more side injection locations that inject gas at one or more angles with respect to the downward direction. In some examples, 10 the gas delivery system 150 delivers a first portion of the gas mixture at a first flow rate to the center injection location and a second portion of the gas mixture at a second flow rate to the side injection location(s) of the gas injector 142. In other examples, different gas mixtures are delivered by the gas injector 142. In some examples, the gas delivery system 150 delivers tuning gas to other locations in the processing chamber.

15 **[0032]** A plasma generator 170 may be used to generate RF power that is output to the one or more inductive coils 140. Plasma 190 is generated in the upper chamber region 104. In some examples, the plasma generator 170 includes an RF generator 172 and a matching network 174. The matching network 174 matches an impedance of the RF generator 172 to the impedance of the one or more inductive coils 140. A 20 valve 178 and a pump 180 may be used to control pressure inside of the lower and upper chamber regions 102, 104 and to evacuate reactants.

[0033] A controller 176 communicates with the gas delivery system 150, the valve 178, the pump 180, and/or the plasma generator 170 to control flow of process gas, purge gas, RF plasma and chamber pressure. In some examples, plasma is sustained 25 inside the dome 118 by the one or more inductive coils 140. One or more gas mixtures are introduced from a top portion of the substrate processing chamber 101 using the gas injector 142 (and/or holes 123).

[0034] Referring now to FIG. 3A, the lower filter 128-L and the upper filter 128-U are shown in further detail. The lower filter 128-L includes a planar portion 310 that 30 includes the through holes 129-L. An annular body portion 314 is connected to the planar portion 310. An annular projecting portion 318 extends radially outwardly from the annular body portion 314. The annular ring 132 rests on an upper surface of the lower filter 128-L. The annular ring 132 includes one or more bores that receive the

fastener 133. In some examples, three or more fasteners 133 are used at spaced locations around a periphery of the lower filter 128-L.

[0035] The upper filter 128-U includes a planar portion 330 that includes the through holes 129-U. A radially outer edge 334 of the planar portion 330 is supported by an upper surface of the annular ring 132. The radial outer edge 334 may include a bore 336 for receiving the fastener 133. The fastener 133 provides an electrical connection between the upper filter 128-U and the lower filter 128-L. The protective cover 134 is arranged over the fastener 133 to protect the fastener 133 from the plasma.

[0036] In some examples, the number and diameter of the through holes 129-U and 129-L are different. The lower filter 128-L includes N_L through holes 129-L having a diameter D_L . The upper filter 128-U includes N_U through holes 129-U having a second diameter D_U . In some examples, the number N_U of the through holes 129-U is greater than the number N_L of the through holes 129-L. In some examples, the diameter D_U of the through holes 129-U is less than the diameter D_L of through holes 129-L. In some examples, the diameter D_L of the lower filter 128-L is in a range from 1mm to 4mm. In some examples, the diameter D_U of the upper filter 128-U is in a range from 0.5mm to 1.5mm. In some examples, the number N_L of through holes 129-L is in a range from 100 to 10000. In some examples, the number N_U of through holes 129-U is in a range from 5,000 to 50,000.

[0037] In some examples, the through holes 129-U and 129-L are uniformly distributed. In some examples, the through holes 129-L are vertically misaligned relative to the through holes 129-U. However in some examples, due to the large number of through holes 129-U and the uniform spacing thereof, some of the through holes 129-U may be partially or fully vertically aligned with the through holes 129-L. In some examples, the gap z is in a range from 1 mm to 50mm.

[0038] In some examples, the upper and lower filters 128-U and 128-L are made of a conducting material such as aluminum. In some examples, the upper and lower filters 128-U and 128-L include a physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD) coating. Example coating materials are selected from a group consisting of yttria, anodized Al, bare Al or nickel. In some examples, the upper filter 128-U and the lower filter 128-L are made of 6061 T6 aluminum with a yttria coating. In some examples, the lower filter 128-L is made of 6061 T6 aluminum with a yttria coating on a plasma-facing side thereof and a nickel

coating on a substrate-facing side thereof. In some examples, the coating has a thickness in a range from 500nm to 500 μ m. In some examples, the upper filter 128-U has a thickness in a range from 2mm to 5mm and the lower filter 128-L has a thickness in a range from 5 to 15 mm.

- 5 **[0039]** As can be appreciated, there are various different ways for arranging the upper and lower filters 128-U and 128-L in the processing chamber in addition to the ring shown in FIG. 3A. Referring now to FIG. 3B, the upper filter 128-U can be attached to another location in the processing chamber rather than resting on the lower filter 128-L as shown in FIG. 3A. In FIG. 3B, the upper filter 128-U is arranged on a ring 370
10 resting on a ledge located on the processing chamber sidewall (or is attached to a processing chamber sidewall). In some examples, the ring 370 is made of a conductive material. In other examples, the ring 370 is made of a non-conducting material and includes a passage 372 to receive an insulated conductor 374 to provide a connection to a reference potential.
- 15 **[0040]** In some examples, the upper and lower filters 128-U and 128-L are biased by different potentials. For example, the upper filter 128-U can be biased by a first DC reference or ground 380 and the lower filter 128-L can be biased by a second DC reference or ground 382. In some examples, the DC reference is in a range of 0 to +/- 20VDC. In some examples, the DC reference is in a range of 0 to +/-10VDC.
- 20 **[0041]** Referring now to FIG. 4, one or both of the lower and upper filters 128-L and 128-U may define plenums 410-L and 410-U for receiving a cooling fluid such as a liquid or gas to cool the lower and upper filters 128-L and 128-U, respectively. In some examples, the lower filter 128-L is cooled to suppress radical recombination. In some examples, the upper filter 128-U is cooled since it is in contact with the plasma.
- 25 **[0042]** Fluid from a fluid source 440 is supplied by a valve 444 and a pump 446 to a conduit 448 connected to the annular body portion 314. A passage 440 in the annular body portion 314 is connected to a plenum 444. The plenum 444 is connected to the plenums 410-L and 410-U. The plenum 410-U is connected to the plenum 444 by a passage 454 formed in a conduit 456 arranged between the lower filter 128-L and the
30 upper filter 128-U. While a specific cooling system arrangement is shown, other arrangements may be used to supply fluid to the plenums 410-L and 410-U.
- [0043]** In some examples, if the upper filter 128-U is cooled, the upper filter 128-U has a thickness in a range from 10mm to 15mm. In some examples, if the lower filter 128-L

is cooled, the lower filter 128-L has a thickness in a range from 10 to 20 mm. When cooled, the increased thickness allows sufficient room to accommodate the plenum.

[0044] Referring now to FIG. 5, ion current is shown as a function of DC bias voltage for a single ion filter and a dual ion filter according to the present disclosure. A current detecting probe with DC bias voltage capability was used in the processing chamber to measure ion current to a detection limit of $0.01\mu\text{A}$. With this arrangement, ion and electron current was measured as a function of DC voltage for single and dual ion filter arrangements. As can be seen in Table I below, the single ion filter has $1.9\mu\text{A}$ at zero voltage. Even without a DC bias assisting ion attraction, ions are already leaking through the showerhead and present on the wafer surface. Note that with the single ion filter, ion induced voltage does not trend dramatically with variations in hole size and pattern. However, the dual ion filter has a 100X gain in voltage performance without compromising ER.

<u>Ion Filter Configuration</u>	<u>Max Ion Flux at 0V and 5V (μA)</u>	<u>Etch Rate</u>	<u>Non-uniformity</u>
Single Ion Filter with 3.5mm holes	1.9/6.9	465	7.1
Single Ion Filter with <1mm holes (23k)	0.6/1.1	483	10.8
Dual ion filter Upper holes <1mm; Lower larger	0.02/0.29	475	5.1

Table I

[0045] The present disclosure provides improved performance by decoupling ion filtering and reactant flux. The upper filter predominantly performs ion filtering. The lower filter predominantly controls etch rate and percent non-uniformity. Also, the

volume between the upper and lower filters allows increased residence time which helps to reduce ions via collisions.

[0046] Referring now to FIG. 6, a method 600 for using a dual ion filter according to the present disclosure to filter ions during treatment of a substrate is shown. At 610, a substrate is arranged on a substrate support in the processing chamber. At 614, a process gas mixture is supplied to the processing chamber. At 616, a reference potential is applied to the dual ion filter including the lower and upper filters. At 620, plasma is struck in the processing chamber for a predetermined period to treat the substrate. At 624, ions are predominantly filtered using the upper filter and the plasma uniformity is controlled by the lower filter. At 626, the plasma is extinguished after the predetermined period.

[0047] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. It should be understood that one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the present disclosure. Further, although each of the embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0048] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including “connected,” “engaged,” “coupled,” “adjacent,” “next to,” “on top of,” “above,” “below,” and “disposed.” Unless explicitly described as being “direct,” when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are present (either spatially or functionally)

between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean “at least one of A, at least one of B, and at least one of C.”

- 5 **[0049]** In some implementations, a controller is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling
- 10 their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing
- 15 gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.
- 20 **[0050]** Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined
- 25 as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational
- 30 parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0051] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with the system, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0052] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, an ion beam etcher (IBE), a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0053] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another
5 controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

CLAIMS

What is claimed is:

1. A substrate processing system, comprising:
 - an upper chamber;
 - a gas delivery system to supply a gas mixture to the upper chamber;
 - an RF generator to generate plasma in the upper chamber;
 - a lower chamber including a substrate support; and
 - a dual ion filter arranged between the upper chamber and the lower chamber,
- the dual ion filter including:
 - an upper filter including a first plurality of through holes configured to filter ions; and
 - a lower filter including a second plurality of through holes configured to control plasma uniformity.
2. The substrate processing system of claim 1, wherein a diameter of the first plurality of through holes of the upper filter is less than a diameter of the second plurality of through holes of the lower filter.
3. The substrate processing system of claim 2, wherein a number of the first plurality of through holes of the upper filter is greater than a number of the second plurality of through holes of the lower filter.
4. The substrate processing system of claim 1, wherein the upper filter and the lower filter are connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference.
5. The substrate processing system of claim 1, wherein the first plurality of through holes of the upper filter have a first diameter in a range from 0.5mm to 1.5mm.
6. The substrate processing system of claim 5, wherein a number of the first plurality of through holes are in a range from 5,000 to 50,000.

7. The substrate processing system of claim 1, wherein the second plurality of through holes of the upper filter have a first diameter in a range from 1mm to 4mm.

8. The substrate processing system of claim 7, wherein a number of the first plurality of through holes are in a range from 100 to 10,000.

9. The substrate processing system of claim 1, wherein the upper filter is arranged parallel to the lower filter and wherein the upper filter is spaced from the lower filter by a predetermined gap in a range from 1 mm to 50mm.

10

10. The substrate processing system of claim 1, wherein at least one of the upper filter and the lower filter includes an inner cooling plenum to receive a cooling fluid.

11. The substrate processing system of claim 1, further comprising a spacing ring arranged between the upper filter and the lower filter.

15

12. The substrate processing system of claim 11, further comprising:
a fastener made of a conducting material and connecting the upper filter to the lower filter through a bore in the spacing ring; and

20

a protective cover made of a plasma-resistant material and arranged on a plasma-facing surface of the fastener.

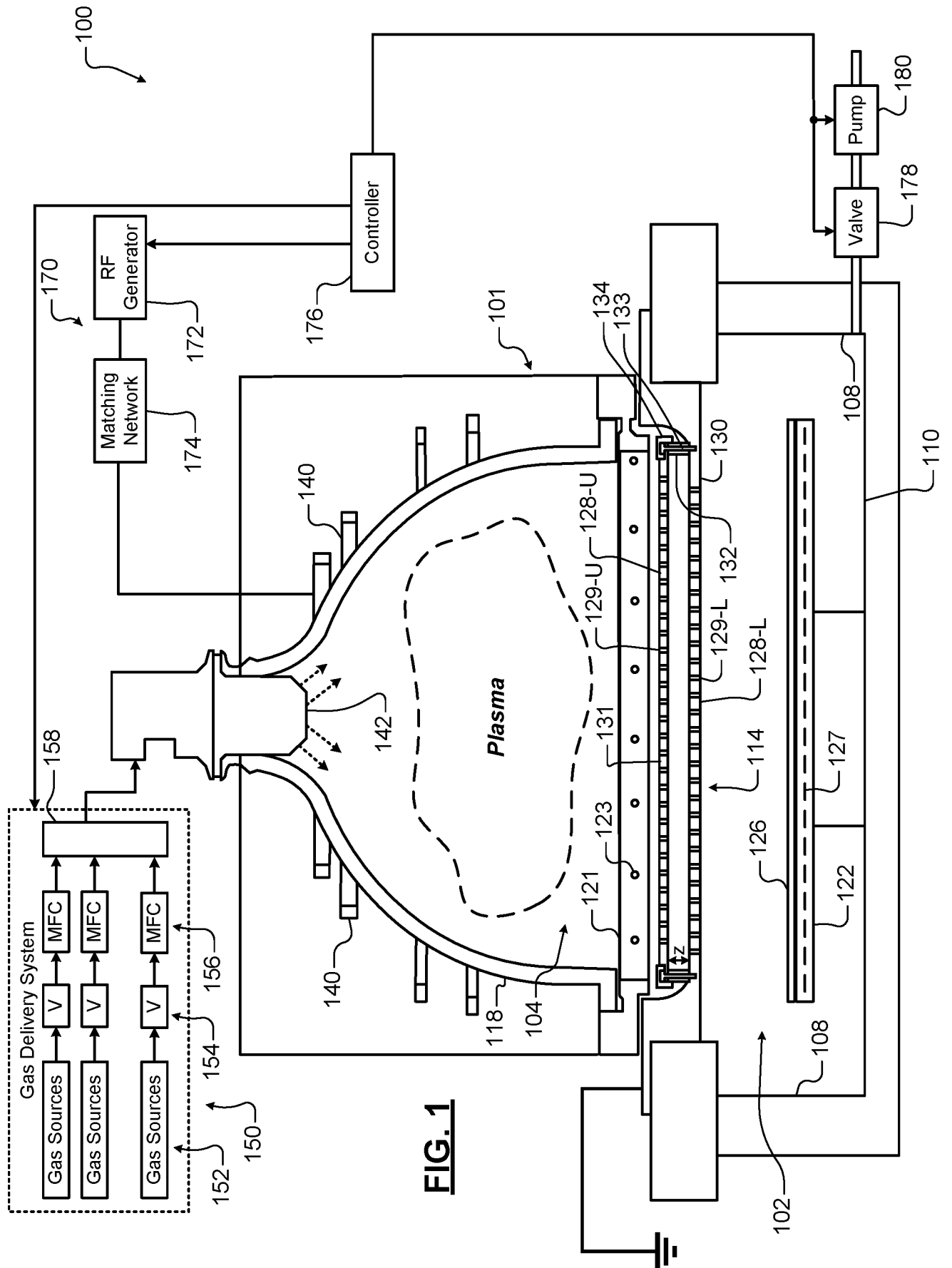
13. The substrate processing system of claim 1, further comprising an inductive coil arranged around an outer surface of the upper chamber, wherein the RF generator generates plasma in the upper chamber by supplying an RF signal to the inductive coil while the gas mixture is supplied by the gas delivery system.

25

14. The substrate processing system of claim 1, wherein:
the upper filter is connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference;
the lower filter is connected to a reference potential selected from a group consisting of ground, a positive DC reference and a negative DC reference; and
the upper filter and the lower filter have a different bias.

30

15. The substrate processing system of claim 1, wherein the upper filter and the lower filter are made of aluminum and include a coating selected from a group consisting of nickel and yttria.
- 5 16. The substrate processing system of claim 1, wherein the lower filter is made of aluminum and includes a yttria coating on a plasma-facing surface thereof and a nickel coating on a substrate-facing side thereof.
- 10 17. The substrate processing system of claim 1, wherein the upper filter has a thickness in a range from 2 to 5 mm and the lower filter has a thickness in a range from 5 to 15 mm.



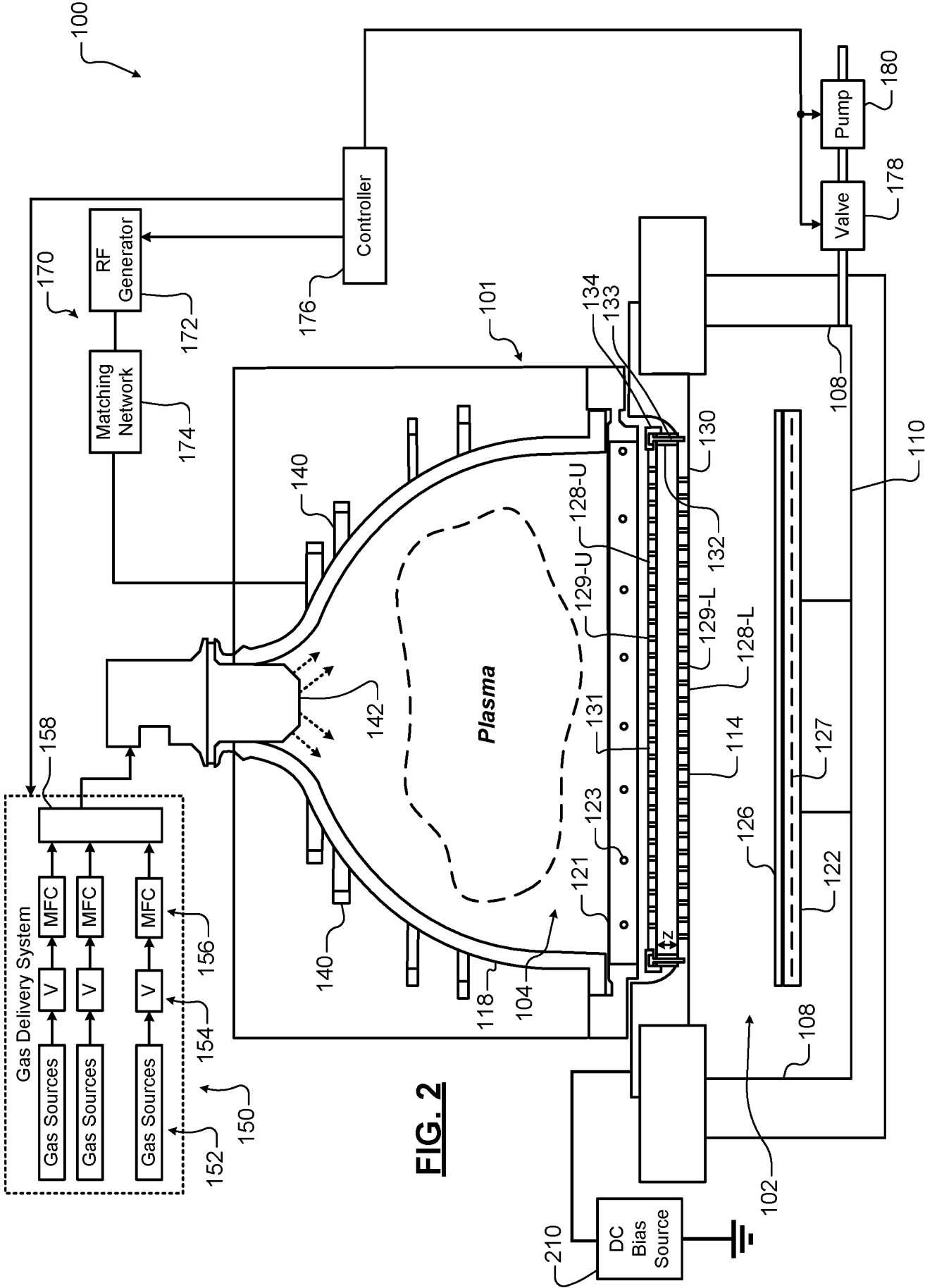


FIG. 2

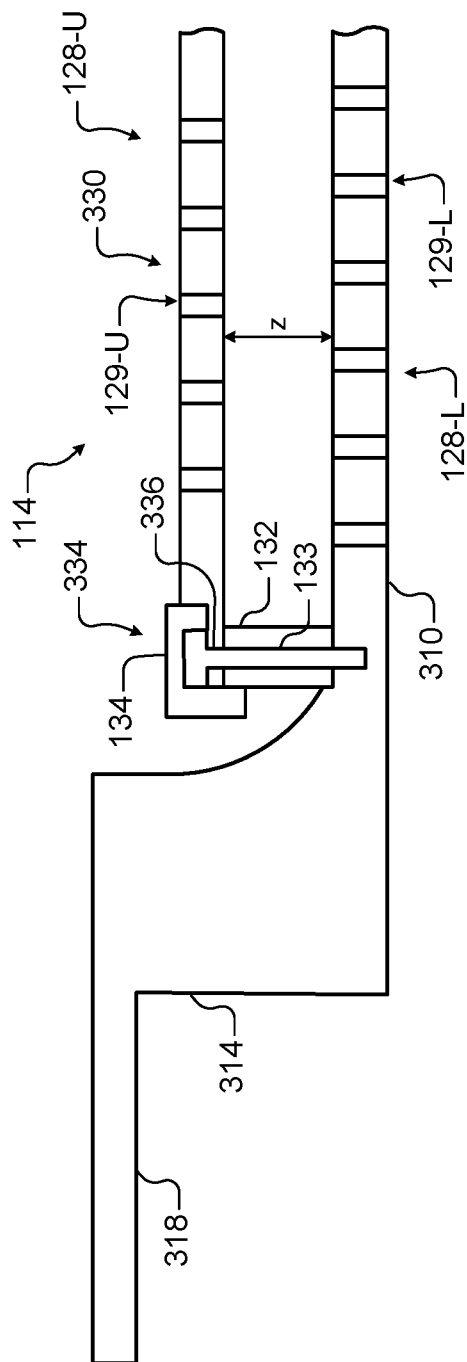


FIG. 3A

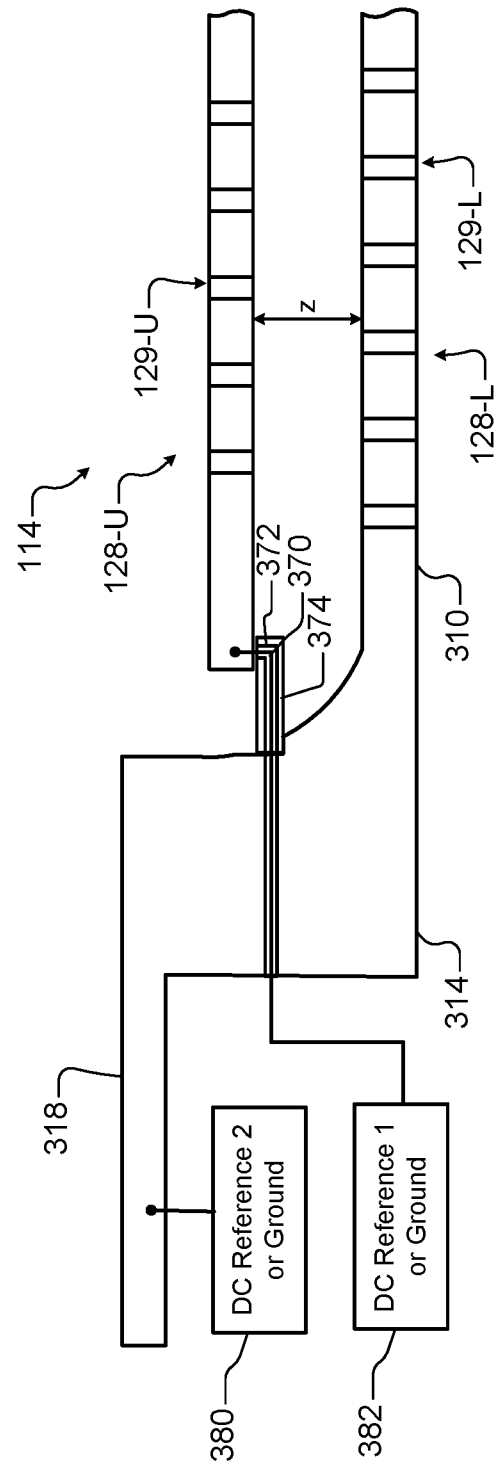


FIG. 3B

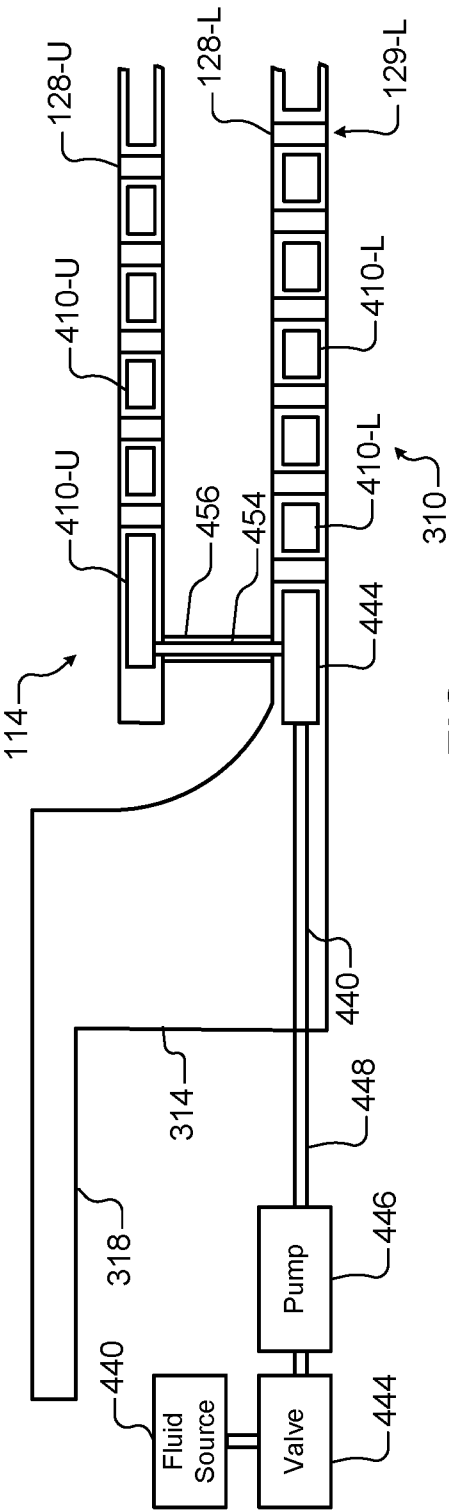


FIG. 4

Charge Receptor Measurement

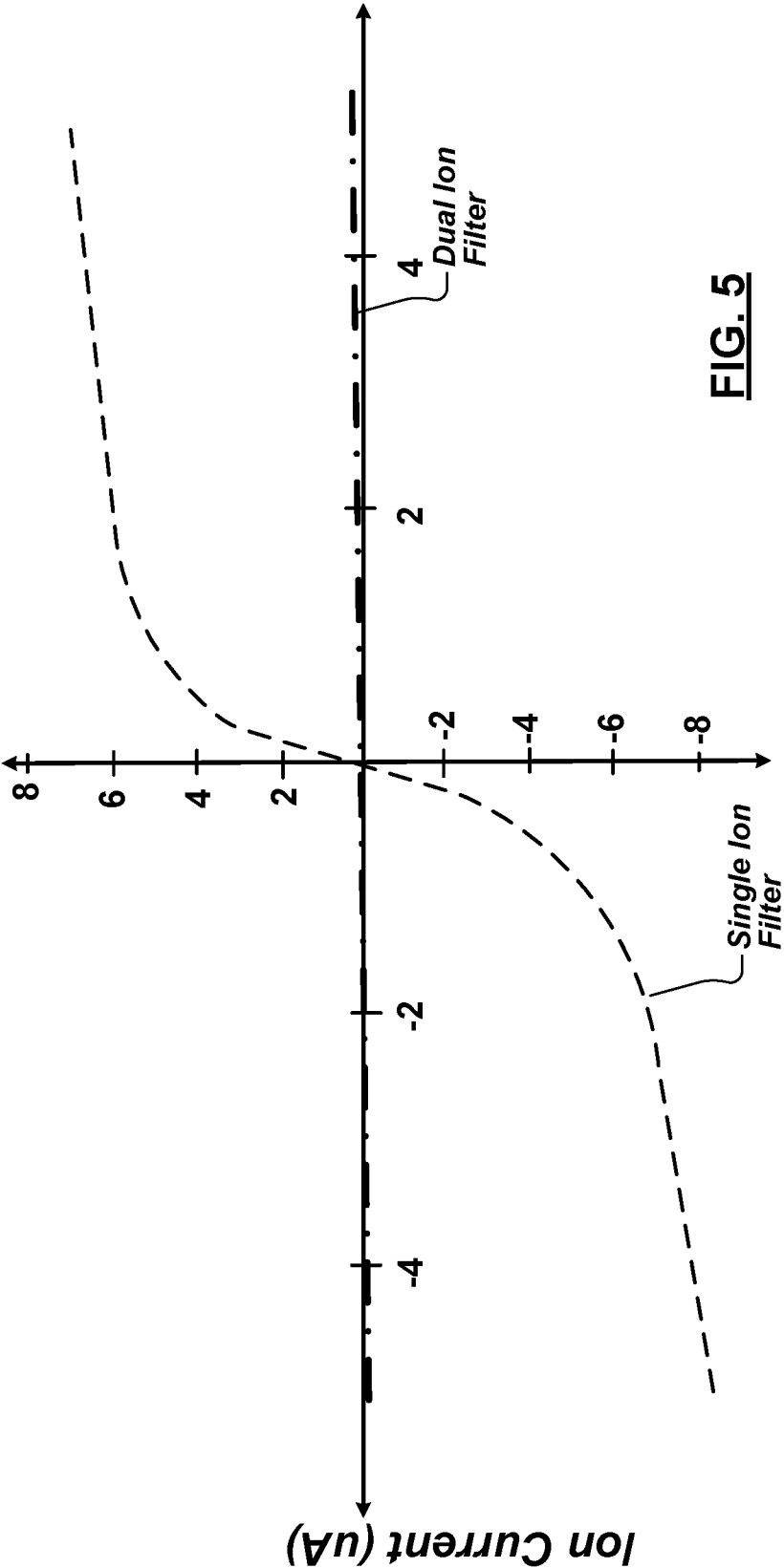
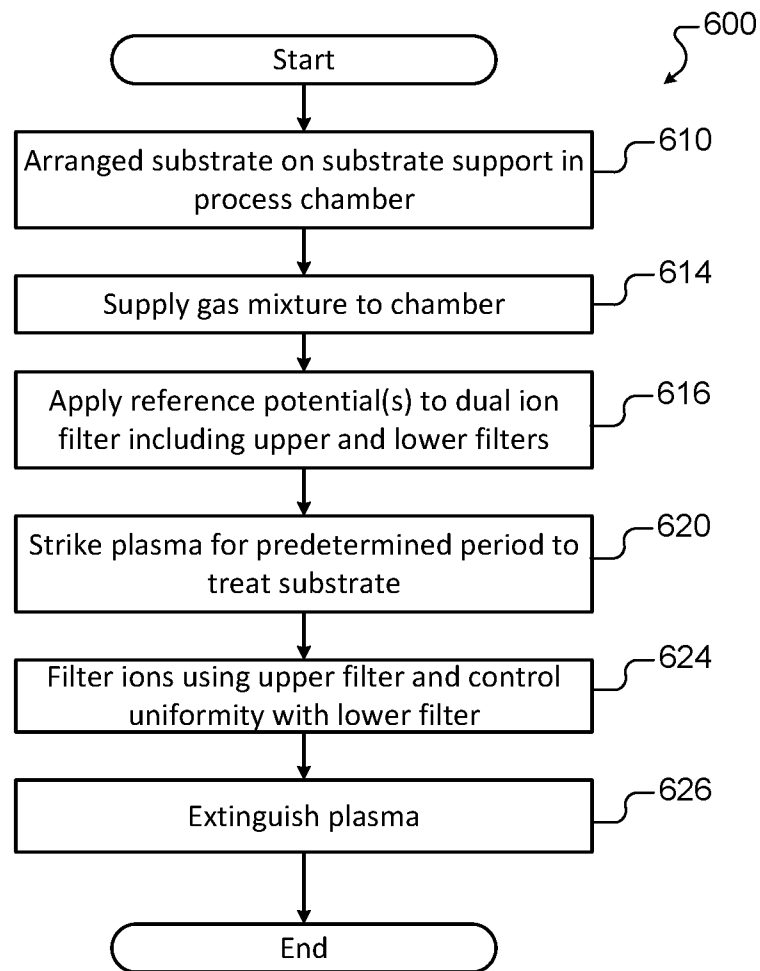


FIG. 5

Voltage (V)

Ion Current (uA)

**FIG. 6**

A. CLASSIFICATION OF SUBJECT MATTER**H01J 37/32(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01J 37/32; C23C 16/50; H01L 21/02; H01L 21/205; H01L 21/3065; H01L 21/67; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: filter, ion, plasma, chamber, uniformity, gas

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018-0122638 A1 (EUGENE TECHNOLOGY CO., LTD.) 03 May 2018 See paragraphs 32-40, 51-53, and figures 1, 9.	1-9, 13, 17
Y		10-12, 14-16
Y	US 2018-0342374 A1 (APPLIED MATERIALS, INC.) 29 November 2018 See paragraphs 70-75, and figure 1.	10, 15-16
Y	WO 2018-094064 A1 (PLASMA-THERM, LLC) 24 May 2018 See page 23, and figures 9-10.	11-12, 14
A	CN 104465457 B (LAM RESEARCH CORPORATION) 14 September 2018 See the whole document.	1-17
A	US 10079176 B2 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 18 September 2018 See the whole document.	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 May 2020 (21.05.2020)

Date of mailing of the international search report

21 May 2020 (21.05.2020)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

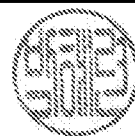


Facsimile No. +82-42-481-8578

Authorized officer

PARK, Hye Lyun

Telephone No. +82-42-481-3463



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/014329

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018-0122638 A1	03/05/2018	CN 107466421 A CN 107466421 B JP 2018-517276 A JP 6499771 B2 KR 10-1682155 B1 KR 10-2016-0124534 A TW 201705197 A TW I634587 B WO 2016-171451 A1	12/12/2017 28/05/2019 28/06/2018 10/04/2019 02/12/2016 28/10/2016 01/02/2017 01/09/2018 27/10/2016
US 2018-0342374 A1	29/11/2018	CN 110710056 A KR 10-2020-0001608 A TW 201901734 A US 10431427 B2 US 2018-0342372 A1 US 2018-0342373 A1 WO 2018-218160 A1	17/01/2020 06/01/2020 01/01/2019 01/10/2019 29/11/2018 29/11/2018 29/11/2018
WO 2018-094064 A1	24/05/2018	CN 109891548 A EP 3510624 A1 JP 2019-536279 A KR 10-2019-0085024 A TW 201826387 A US 2018-0143332 A1	14/06/2019 17/07/2019 12/12/2019 17/07/2019 16/07/2018 24/05/2018
CN 104465457 B	14/09/2018	CN 103053011 A CN 103053011 B CN 103053012 A CN 103053012 B CN 103632954 A CN 103632954 B CN 103703870 A CN 103703870 B CN 103890916 A CN 103890916 B CN 104465457 A CN 105719932 A CN 105719932 B CN 105845535 A CN 105845535 B CN 106128931 A CN 106128931 B CN 107424900 A CN 109417030 A JP 2013-541177 A JP 2014-057057 A JP 2014-531753 A JP 2015-065434 A JP 2016-167606 A	17/04/2013 23/03/2016 17/04/2013 20/04/2016 12/03/2014 11/08/2017 02/04/2014 08/06/2016 25/06/2014 07/09/2016 25/03/2015 29/06/2016 02/01/2018 10/08/2016 26/12/2017 16/11/2016 27/04/2018 01/12/2017 01/03/2019 07/11/2013 27/03/2014 27/11/2014 09/04/2015 15/09/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/014329

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		JP 2018-037668 A	08/03/2018
		JP 2019-050413 A	28/03/2019
		JP 5913312 B2	27/04/2016
		JP 6110540 B2	05/04/2017
		JP 6382719 B2	29/08/2018
		JP 6441434 B2	19/12/2018
		JP 6641077 B2	05/02/2020
		KR 10-1871521 B1	02/08/2018
		KR 10-1911562 B1	04/01/2019
		KR 10-1982364 B1	30/08/2019
		KR 10-1983866 B1	03/09/2019
		KR 10-1998542 B1	09/07/2019
		KR 10-2013-0093110 A	21/08/2013
		KR 10-2013-0136962 A	13/12/2013
		KR 10-2014-0027895 A	07/03/2014
		KR 10-2014-0046468 A	18/04/2014
		KR 10-2014-0068055 A	05/06/2014
		KR 10-2015-0032811 A	30/03/2015
		KR 10-2016-0067741 A	14/06/2016
		KR 10-2016-0067742 A	14/06/2016
		KR 10-2016-0067743 A	14/06/2016
		KR 10-2016-0068002 A	14/06/2016
		KR 10-2017-0132666 A	04/12/2017
		KR 10-2017-0132671 A	04/12/2017
		KR 10-2018-0101204 A	12/09/2018
		KR 10-2018-0118235 A	30/10/2018
		SG 10201405549V A	29/04/2015
		SG 10201505975Q A	29/09/2015
		SG 10201506065Y A	29/09/2015
		SG 10201601331P A	30/03/2016
		SG 10201602732T A	30/05/2016
		SG 11201400364R A	28/04/2014
		SG 187256 A1	28/03/2013
		SG 187610 A1	28/03/2013
		SG 2013065065 A	28/03/2014
		TW 201214557 A	01/04/2012
		TW 201222635 A	01/06/2012
		TW 201316400 A	16/04/2013
		TW 201330098 A	16/07/2013
		TW 201415560 A	16/04/2014
		TW 201528310 A	16/07/2015
		TW 201630067 A	16/08/2016
		TW 201630072 A	16/08/2016
		TW 201635334 A	01/10/2016
		TW 201639027 A	01/11/2016
		TW 201643955 A	16/12/2016
		TW 201701355 A	01/01/2017
		TW 201711110 A	16/03/2017
		TW 201806028 A	16/02/2018
		TW 201835377 A	01/10/2018

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/014329

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		TW 201842225 A	01/12/2018
		TW I546857 B	21/08/2016
		TW I552222 B	01/10/2016
		TW I562232 B	11/12/2016
		TW I578408 B	11/04/2017
		TW I605495 B	11/11/2017
		TW I608544 B	11/12/2017
		TW I609425 B	21/12/2017
		TW I621186 B	11/04/2018
		TW I647731 B	11/01/2019
		US 10170323 B2	01/01/2019
		US 10170324 B2	01/01/2019
		US 10181412 B2	15/01/2019
		US 10297459 B2	21/05/2019
		US 10304693 B2	28/05/2019
		US 10373840 B2	06/08/2019
		US 2012-0031559 A1	09/02/2012
		US 2012-0034786 A1	09/02/2012
		US 2013-0023064 A1	24/01/2013
		US 2013-0059448 A1	07/03/2013
		US 2014-0054269 A1	27/02/2014
		US 2015-0004793 A1	01/01/2015
		US 2015-0083582 A1	26/03/2015
		US 2015-0206775 A1	23/07/2015
		US 2015-0357209 A1	10/12/2015
		US 2016-0079039 A1	17/03/2016
		US 2016-0148786 A1	26/05/2016
		US 2016-0163556 A1	09/06/2016
		US 2016-0163557 A1	09/06/2016
		US 2016-0163558 A1	09/06/2016
		US 2016-0163561 A1	09/06/2016
		US 2016-0260617 A1	08/09/2016
		US 2016-0260620 A1	08/09/2016
		US 2016-0268141 A1	15/09/2016
		US 2016-0343580 A1	24/11/2016
		US 2016-0358784 A1	08/12/2016
		US 2017-0076955 A1	16/03/2017
		US 2017-0170026 A1	15/06/2017
		US 2017-0178920 A1	22/06/2017
		US 2017-0213747 A9	27/07/2017
		US 2018-0005852 A1	04/01/2018
		US 2018-0174858 A1	21/06/2018
		US 8869742 B2	28/10/2014
		US 9039911 B2	26/05/2015
		US 9117767 B2	25/08/2015
		US 9184028 B2	10/11/2015
		US 9378971 B1	28/06/2016
		US 9384998 B2	05/07/2016
		US 9418859 B2	16/08/2016
		US 9543158 B2	10/01/2017

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/014329

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 10079176 B2	18/09/2018	US 9620377 B2	11/04/2017
		US 9793126 B2	17/10/2017
		US 9793128 B2	17/10/2017
		US 9887097 B2	06/02/2018
		US 9997372 B2	12/06/2018
		US 9997373 B2	12/06/2018
		WO 2012-018448 A2	09/02/2012
		WO 2012-018448 A3	05/04/2012
		WO 2012-018449 A2	09/02/2012
		WO 2012-018449 A3	12/04/2012
		WO 2013-012591 A1	24/01/2013
		WO 2013-036371 A2	14/03/2013
		WO 2013-036371 A3	15/05/2014
		WO 2018-026867 A1	08/02/2018
		US 2015-0255330 A1	10/09/2015
		US 2016-0358814 A1	08/12/2016
		US 2019-0027404 A1	24/01/2019
		US 9396992 B2	19/07/2016