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(54) **PROCESS FOR FABRICATING SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

A process for fabricating a semiconductor device comprising the step of, after patterning the silicon film crystallized to a low degree by thermally annealing an amorphous silicon film into an island by etching, irradiating an intense light of a visible light or a near infrared radiation to effect a short-period annealing (RTA) to the silicon film of low crystallinity. Thus, the crystallinity of the silicon film is improved and the silicon film is densified in a short-period.

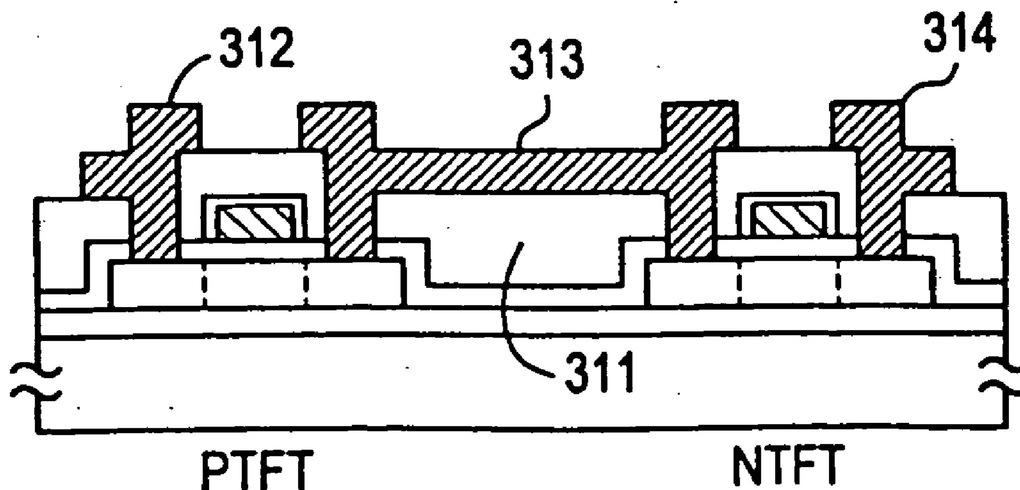


FIG.1A

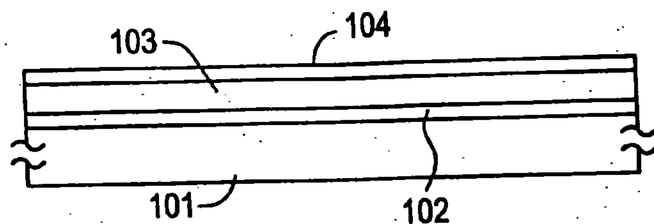


FIG.1B

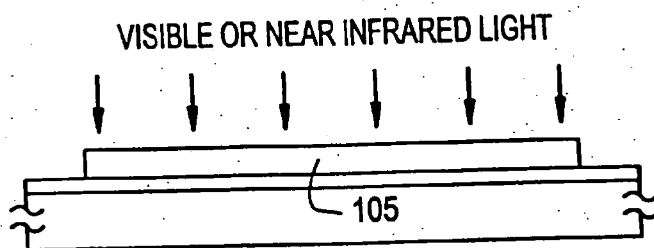


FIG.1C

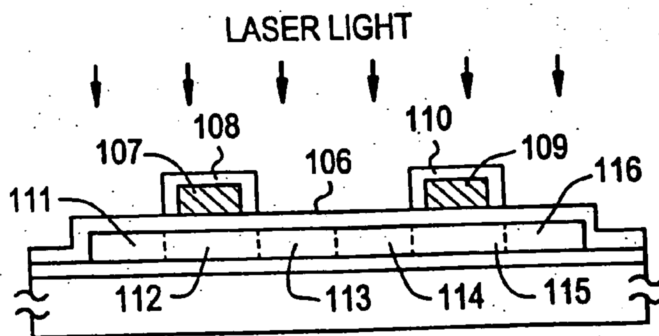


FIG.1D

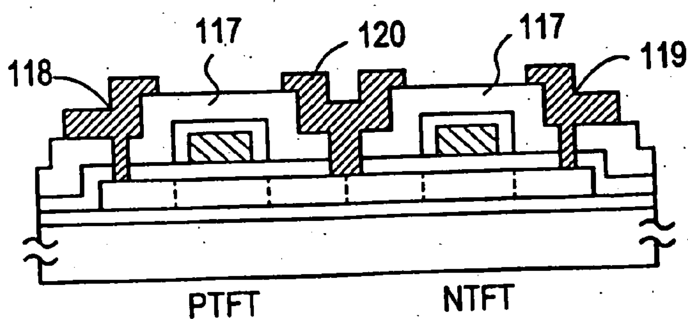


FIG.2A

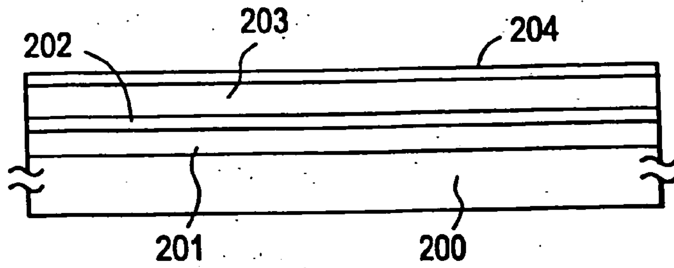


FIG.2B

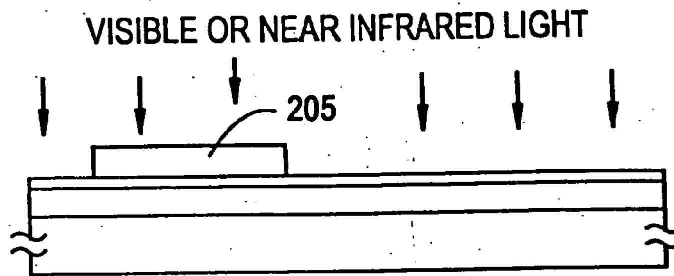


FIG.2C

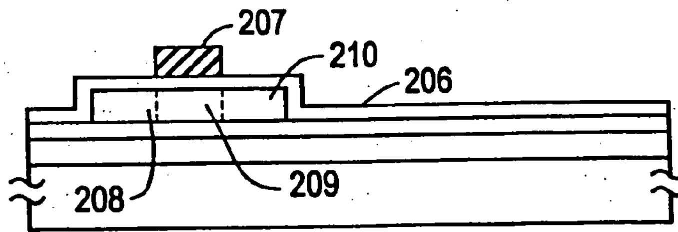


FIG.2D

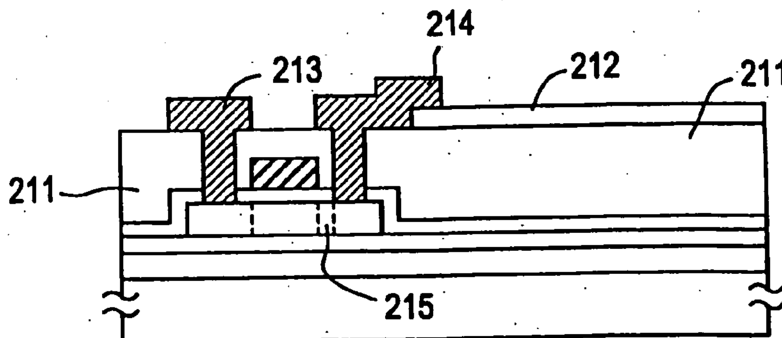


FIG.3A

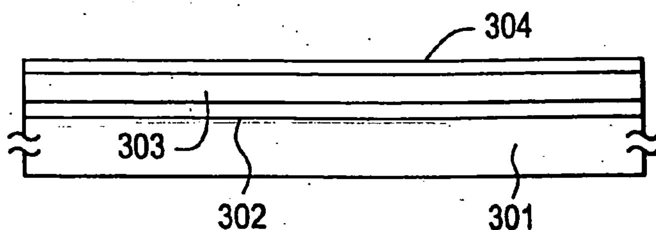


FIG.3B

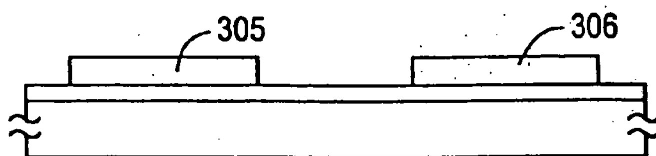


FIG.3C

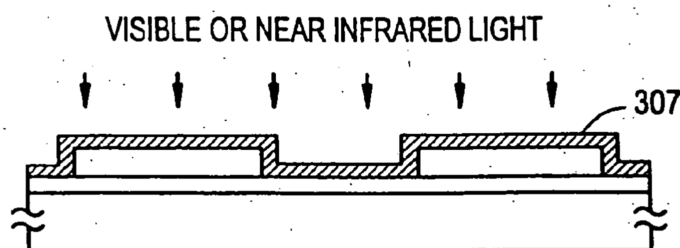


FIG.3D

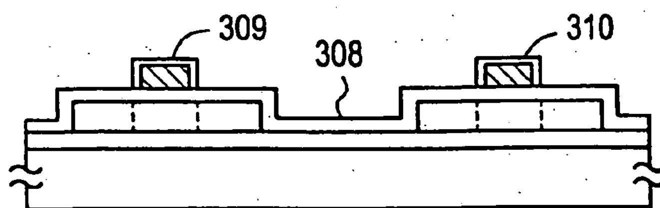


FIG.3E

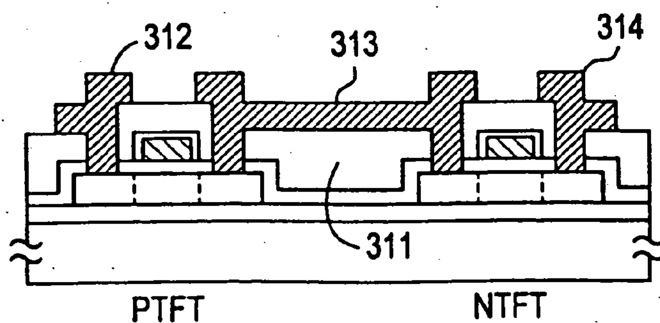


FIG 4A

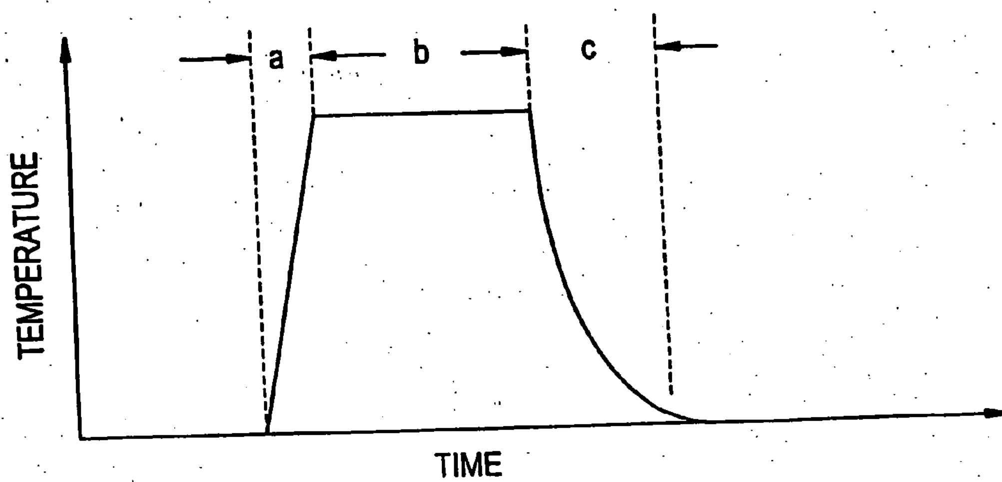
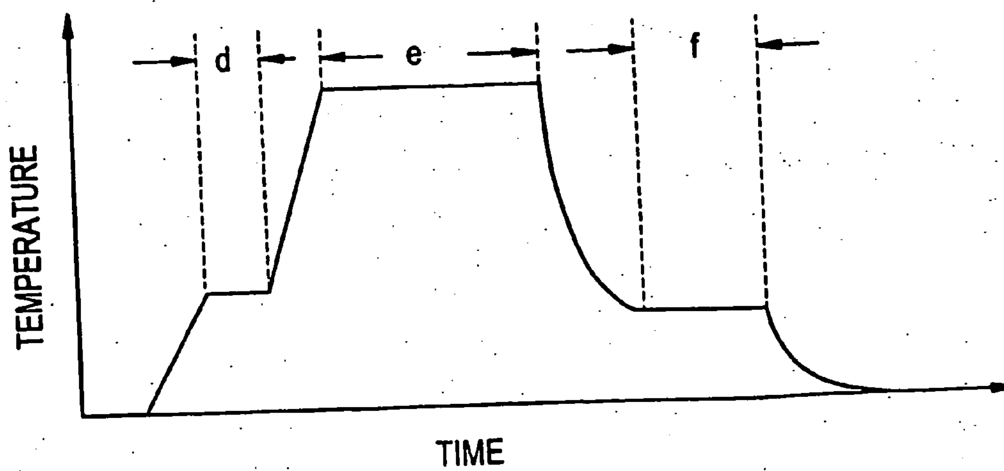


FIG.4B



PROCESS FOR FABRICATING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Industrial Field of the Invention

[0002] The present invention relates to a process for fabricating an insulated gate-structured semiconductor device such as a thin film transistor (TFT) or a thin film diode (TFD), comprising a non-single crystal silicon film formed on an insulating substrate such as a glass substrate or on an insulating film formed on various type of substrate. The present invention also relates to a process for fabricating a thin film integrated circuit (IC) to which TFT or TFD is applied, and more particularly, to a thin film integrated circuit (IC) for an active-matrix type liquid crystal displaying unit.

[0003] 2. Prior Art

[0004] Semiconductor devices developed heretofore comprising TFTs on an insulating substrate (such as a glass substrate) include an active matrix-addressed liquid crystal display device whose pixels are driven by TFTs, an image sensor, or a three-dimensional integrated circuit.

[0005] The TFTs utilized in those devices generally employ a thin film non-single crystal silicon semiconductor. The thin film non-single crystal semiconductors can be roughly classified into two; one is a type comprising amorphous silicon semiconductor (a-Si), and the other is a type comprising crystalline silicon semiconductors. Amorphous silicon semiconductors are most prevailing, because they can be fabricated relatively easily by a vapor phase process at a low temperature, and because they can be readily obtained by mass production. The physical properties thereof, such as electric conductivity, however, are still inferior to those of a crystalline silicon semiconductor. Thus, to implement devices operating at an even higher speed, it has been keenly demanded to establish a process for fabricating TFTs comprising crystalline silicon semiconductors. Known crystalline semiconductors suitable for the purpose like this include polycrystalline silicon, microcrystalline silicon, amorphous silicon partly comprising crystalline components, and semiamorphous silicon which exhibits an intermediate state between crystalline silicon and amorphous silicon.

[0006] Known process for crystalline thin film silicon semiconductors includes depositing an amorphous semiconductor film by plasma CVD or low pressure CVD, and applying thereto thermal energy for a long duration of time (i.e., thermal annealing) for crystallization.

[0007] In general, silicon semiconductors need to be heated to, a temperature of 600° C. or higher. More preferably, heating at 640° C. or higher is necessary to further enhance the crystal growth. However, such a high temperature heating has a problem of thermally influencing the substrate. Furthermore, since the heating time required for crystallization was several tens hours or longer, productivity was low. Therefore, it has been demanded to lower the heating temperature and shorten the heating time.

[0008] As a means to overcome the aforementioned problems, a process for crystallizing the film by increasing the surface temperature of the film to substantially 800° C. or higher has been developed. The process comprises irradiating an intense light such as an infrared radiation or a visible light for a duration of about 10 to 1,000 seconds to the surface of the film. This process, which is called as lamp annealing or rapid thermal annealing (RTA), is expected to be process for reducing the influence on substrates, because the duration of heating can be extremely shortened.

[0009] However, since the film formed by plasma CVD and low pressure CVD contains a lot of hydrogen combined with silicon, the decomposition reaction of hydrogen is mainly caused by RTA owing to the short time of RTA, that is, the crystallization does not sufficiently proceed. Furthermore, there is a problem that hydrogen is ejected to the exterior of the film by the decomposition reaction of hydrogen to degrade the morphology of the film surface. The present invention has been accomplished in the light of the above circumstances. Accordingly, an object of the present invention is to provide a silicon film suitable for forming a semiconductor device and having a sufficiently high crystallinity.

SUMMARY OF THE INVENTION

[0010] In one aspect of the invention, a semiconductor device comprises a substrate, a first base film comprising aluminum nitride and oxygen provided over the substrate, a second base film comprising silicon oxide provided over the first base film, and a thin film transistor provided over said second base film. The semiconductor device comprises an active layer in which 90% or more of the active layer is crystallized.

[0011] In another aspect of the invention, a semiconductor device comprises a substrate, a first base film comprising aluminum nitride and oxygen provided over the substrate, a second base film comprising silicon oxide provided over the first base film, and a thin film transistor provided over the second base film. The thin film transistor comprises an active layer including a semiconductor in which 90% or more of the semiconductor is crystallized.

[0012] In yet another aspect of the invention, a display device comprises a substrate, a first base film comprising aluminum nitride and oxygen provided over the substrate, a second base film comprising silicon oxide provided over the first base film, and a pixel thin film transistor provided over the second base film. The pixel thin film transistor comprises an active layer comprising a semiconductor, and 90% or more of the active layer comprising the semiconductor is crystallized.

[0013] In another aspect of the invention, a semiconductor device comprises a substrate, a first base film comprising aluminum nitride and oxygen provided over the substrate, a second base film comprising silicon oxide provided over the first base film, and a thin film transistor comprising an active layer. The active layer is provided over the second base film and the first base film, and 90% or more of the active layer is crystallized.

[0014] The process according to the present invention comprises a first step of forming a non-single crystal semiconductor film on a glass substrate and crystallizing the non-single crystal semiconductor film by a thermal annealing and the like to eject hydrogen from the non-single crystal semiconductor film and a second step of heating the non-single crystal semiconductor film by irradiating an intense light thereto (RTA process).

[0015] Another step of forming, on the surface of said silicon film, an insulating coating which absorbs less than 10% of the intense light used in the second step may be incorporated between the first and the second steps. It is preferred in the present invention that the silicon film obtained by the first step has a low degree of crystallinity, more specifically the degree of crystallinity is 1 to 50%, more preferably 1 to 10%. The first step can be carried out by thermal annealing or other crystallizing methods.

[0016] There may be provided a step of patterning the silicon film into at least one island by etching.

[0017] As a substrate of this invention, it is preferable to utilize a glass substrate with strain point from 550° C. to 680° C. Specifically, No. 7059 of Coming Co. (strain point 593° C.), No. 1733 of the same (strain point 640° C.), LE30 of HOYA Co. (strain point 625° C.), NA35 (strain point 650° C.) of NH Technoglass Co., NA 45 (strain point 610° C.) of NH Technoglass Co., E-8 of OHARA Co. (strain point 643° C.), OA-2 of Nihon Denki Glass Co. (strain point 625° C.), AN1 (strain point 625° C.) of Asahi Glass Co., AN2 (strain point 625° C.) of Asahi Glass Co. and the like are desirable. However, a glass substrate other than above mentioned can be utilized, too.

[0018] Moreover, an insulating film such as silicon oxide, silicon nitride, or aluminum nitride can be formed on the surface of the glass substrate and an amorphous silicon film can be formed on it. In the case that a film of a material with high heat conductivity like aluminum nitride is formed on a glass substrate, the second step above mentioned can be omitted.

[0019] In case that the crystallizing in the first step above mentioned is carried out by thermal annealing, temperature and time of the thermal annealing is varied according to the thickness, composition and the like of the semiconductor thin film. In the case of substantially intrinsic silicon semiconductor, 520 to 620° C. for example, 550 to 600° C., and 1 to 4 hours is appropriate. It is preferable if the thermal annealing is performed at a temperature lower than the strain point of the glass substrate.

[0020] In addition, it is especially preferable if silicon ions have been implanted in the silicon film by an ion implanting method at a dose of 1×10^{14} to 1×10^{16} cm^{-2} before the above-mentioned thermal annealing, because crystal growth by thermal annealing is suppressed.

[0021] Metal element promoting crystallization of the silicon film, e.g. nickel and the like, can be included in the silicon film obtained by the above-mentioned first step of the present invention. As a metal element other than nickel which can promote crystallization like this, Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Sc, Ti, V, Cr, Mn, Cu, Zn, Au, and Ag is known. In an amorphous silicon film added with these elements, crystallization proceeds enough even by low temperature short time thermal annealing of 520 to 620° C. and 1 to 4 hours. Crystal growth by RTA later has no effect if the crystallization proceeds excessively. Therefore, in the case of adding these metal elements, it is desirable if time of thermal annealing is shorter, or temperature of thermal annealing is lower, than that of the substantially intrinsic silicon film.

[0022] If these metal elements are included in the silicon film, it is also possible to crystallize the silicon film at a lower temperature in the process of RTA later. These metal elements also have an effect of promoting elimination (ejection) of hydrogen from the amorphous silicon film during thermal annealing. If silicon ions have been implanted to the silicon film as above mentioned before thermal annealing process, crystallization growth during thermal annealing can be suppressed, which is preferable, even if these metal elements are added.

[0023] These metal elements have great effects on semiconductor characteristic and reliability. A silicon film crystallized with including these metal elements at a large amount especially lacks in reliability-durability in the long run. To solve a problem like this, concentration of these metal elements existing in the Si film should be made effective in performing crystallization at a temperature needed, and will not take bad effects on the semiconductor character. Specifically, it is preferable if the minimum value of detection concentration is 1×10^{15}-1×10^{19} cm^{-3} when concentration of these metal elements included in the silicon film is analyzed through the depth of the silicon film by secondary ion mass spectrometry (SIMS).

[0024] As a light to be utilized for RTA in the second step above mentioned, it is preferable if wavelength of the light to be utilized is absorbed in the silicon film but is not substantially absorbed to the glass substrate. That is, it is preferable if the center wavelength lies in the near infrared radiation or visible light. For example, a light with wavelength of 4 μm to 0.6 μm is desirable (e.g. infrared light having a peak at wavelength 1.3 μm). By irradiating intense light like this for relatively a short time like 10 to 1000 seconds, the silicon film can be heated and crystal character can be improved. It is desirable if the silicon film is heated at 800 to 1300° C.

[0025] If the silicon film is suddenly heated from a room temperature to a high temperature like this, or on the contrary if the silicon film is suddenly cooled from a high temperature like this to a room temperature, effect of stress and the like to be taken on the silicon film is big. Therefore preheat process to heat the film at a lower temperature than this high temperature, or post heat process to heat the silicon film at a temperature between this high temperature and the room temperature for a while in the course of descending temperature from the high temperature condition can be provided. To prevent heat damage on the substrate, it is preferable if temperature of the preheat process and the postheat process is lower than the strain point of the glass substrate by 50 to 200° C.

[0026] By thermal annealing in the first process, a nucleus of crystal growth is at least generated, and a low crystallized silicon film (crystallized area is 1 to 50%, preferably 1 to 10% (the rest is amorphous condition)) can be obtained even if the crystallization is suppressed. However, it is not preferred that a semiconductor device is formed by directly using the crystalline silicon film obtained by the first step. This is because there are left a lot of amorphous components mainly in the grain boundary and characteristic of the silicon film is not preferable in bulk and surface thereof. In the present invention, this silicon film is converted to a silicon film with good crystal character by RTA of the second process. By RTA, the silicon film is heated, and crystallinity of the crystallized silicon film is improved and the film is densified simultaneously. In this time, in case that the silicon

film has a low crystallinity degree, crystallization can be expanded from the crystal nuclei formed by the first step to the surrounding amorphous region. In this case, since the crystallization proceeds relatively long distance, the effect of decreasing grain boundaries is obtained. By improving the crystallinity in this manner, the high quality silicon film with 90% or more thereof in area being crystallized can be obtained, which can be utilized for a thin film transistor (TFT).

[0027] However, in such RTA, temperature partially changes rapidly. Thus because of difference in thermal expansion coefficient between the silicon film and the substrate, and difference of temperature between the surface of the silicon film and the interface of the substrate and the silicon film, the silicon film is often peeled off. This is particularly notable in the case that the area of the film is so big that it covers the whole surface of the substrate. Therefore, peeling and the like of the film can be prevented by dividing the film in sufficiently small areas, and by making distances between the divided films sufficiently wide so that unnecessary heat would not be absorbed by the substrata. In this way, because the whole surface of the substrate will not be heated through the silicon film, thermal shrinkage of the substrate is suppressed mostly.

[0028] In the present invention, it is preferred that light with wavelength of 0.6 to 4 μm is irradiated to the silicon film formed on the glass substrate in the second step (RTA). This wavelength is efficiently absorbed to a low crystallized intrinsic or substantially intrinsic (concentration of phosphorous or boron is 10^{17} cm^{-3} or less) silicon film, and is converted to heat. Far infrared light with wavelength of 10 μm or more is absorbed to the glass substrate and heats the glass substrate. However, in the case that wavelength of far infrared light is mostly 4 μm or less, absorption by the glass is 0.01 to 10%. Thus heating of the glass is extremely small. That is, to crystallize a silicon film with low crystal character and not to take great effect on the substrate, wavelength of 0.6 to 4 μm is appropriate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] FIGS. **1**(A) to **1**(D) show the step-sequential schematically drawn views for the structures obtained in a process for fabricating a TFT according to Example 1 of the present invention;

[0030] FIGS. **2**(A) to **2**(D) show the step-sequential schematically drawn views for the structures obtained in a process for fabricating a TFT according to Example 2 of the present invention;

[0031] FIGS. **3**(A) to **3**(E) show the step-sequential schematically drawn views for the structures obtained in a process for fabricating a TFT according to Example 3 of the present invention; and

[0032] **FIG. 4A** to **4**B are graphs showing the controlled temperature during the process.

DETAILED DESCRIPTION OF THE INVENTION

EXAMPLE 1

[0033] Referring to FIGS. **1**(A) to **1**(D), the present example relates to a process for fabricating a circuit comprising a p-channel TFT (hereinafter referred to simply as a "PTFT") and an n-channel TFT (hereinafter referred to simply as an "NTFT") formed in a complementary arrangement using a crystalline silicon film formed on a glass substrate. The structure obtained in the present example is applicable to switching elements of pixel electrodes and to peripheral driver circuits of active liquid crystal display devices, as well as to image sensors and three-dimensional integrated circuits.

[0034] Referring to the cross section views in FIGS. **1**(A) to **1**(D), the fabrication process of the present example is described below. A 2,000 Å thick silicon oxide film was deposited as a base film **102** on the surface of a Coming 7059 glass substrate **101** by a sputtering process. Mask alignment in the later steps can be facilitated by annealing the substrate either before or after depositing the base film at a temperature higher than the deformation temperature (strain point) of the glass substrate, and then gradually cooling it to the deformation temperature (strain point) or lower at a rate of 0.1 to 1.0° C./min. In case of a Coming 7059 substrate, more specifically, the substrate is preferably subjected to a pretreatment comprising an annealing for a duration of from 1 to 4 hours in the temperature range of from 620 to 660° C. and a gradual cooling to a temperature in the range of from 400 to 500° C. at a rate of from 0.1 to 1.0° C./min, preferably, at a rate of from 0.03 to 0.3° C./min.

[0035] An intrinsic (I-type) amorphous silicon film **103** was deposited thereafter by plasma CVD at a thickness of from 300 to 1,500 Å, for example, 800 Å. A silicon oxide film **104** was deposited thereon by plasma CVD at a thickness of from 100 to 800 Å, for instance, at a thickness of 200 Å. This amorphous silicon film functions as a protective film to prevent surface roughening from occurring on the silicon film in the subsequent step of thermal annealing.

[0036] The resulting structure was thermally annealed at 600° C. for a duration of 4 hours under 1 atm in a nitrogen atmosphere. Hydrogen atoms that are incorporated in excess in the silicon film can be discharged by thermal annealing to provide a film with low crystallinity. However, in contrast to a polycrystalline silicon film comprising 90% or more of crystallized silicon, no peak assigned to crystalline silicon was discernible upon analyzing the silicon film by Raman scattering spectroscopy. Thus, the film obtained by annealing is presumably a film in which at least nucleation is completed, and in which crystallization had occurred over 50% or less in area, generally, from 1 to 10% in area. TEM (transmission electron microscope) observation revealed the presence of fine crystals of 1,000 Å or less, typically, from 20 to 100 Å in size. Crystals must be grown to 3 to 30 times in size, and the crystal growth was found to occur accelerated in the silicon film by previously introducing silicon ions at a dose of from 1×10^{14} to 1×10^{16} cm^{-2} by ion implantation (**FIG. 1**(A)).

[0037] The silicon film was patterned by etching thereafter to form island-like active layer **105** for the TFT. The size of the active layer **105** is determined considering the channel length and the channel width. The active layers thus formed range from the smaller ones 50 μm×20 μm in size to the larger ones 100 μm×1,000 μm in size.

[0038] Then, the active layer was crystallized by irradiating thereto an infrared radiation having a peak in a wavelength range of from 0.6 to 4 μm, for example, in a

wavelength range of from 0.8 to 1.4 μm in this case, for a duration of from 30 to 180 seconds. The temperature during the irradiation of an infrared radiation was kept in the range of from 800 to 1,300° C., representatively, in the range of from 900 to 1,200° C., for example, 1,100° C. in this case. The surface characteristics of the active layer can be further ameliorated by irradiating the infrared radiation under a hydrogen atmosphere. Since the active layer is selectively heated in the present step, the thermal influence on the glass substrate can be minimized. The present invention is particularly effective for reducing the dangling bonds and defects in the active layer (**FIG. 1**(B)).

[0039] A halogen lamp was utilized for a light source of the infrared radiation. The intensity of a visible or a near infrared light was controlled as such that the temperature on the single crystal silicon wafer provided as a monitor is to be in the range of from 800 to 1,300° C., representatively, in the range of from 900 to 1,200° C. More specifically, the temperature of the silicon wafer was monitored with a built-in thermocouple, and the result was fed back to the light source of the infrared radiation. The surface temperature of the silicon on a glass substrate is assumably lowered to about two-thirds of the monitored temperature. In the present invention, the temperature was raised and lowered in such a manner as illustrated in **FIG. 4**(A) or **4**(B). The temperature was raised at a constant rate of from 50 to 200° C./sec, and lowered by air cooling at a rate ranging from 20 to 100° C./sec.

[0040] The temperature control illustrated in **FIG. 4**(A) is a general heating cycle comprising three steps, i.e., a heating time a, a holding time b, and a cooling time c. It can be seen that the specimen is rapidly heated up from a room temperature to a temperature as high as 1,000° C., and that is cooled down from the high temperature to a room temperature, which greatly influences the silicon film and the substrate, thereby increasing possibility of causing separation between the silicon film and the substrate.

[0041] The aforementioned problem can be overcome by providing a pre-heating time d or a post-heating time f before or after the holding time as shown in **FIG. 4**(B). The pre-heating time or the post-heating time holds the structure in the temperature range that is lower than the strain point of the glass substrate by 50 to 200° C., e.g. from 400 to 700° C., preferably in the range of from 500 to 600° C., to prevent causing damage to the substrate and to the film thereon. 30 seconds to 30 minutes are preferable as the preheating time and the post-heating time. In the case where a substrate having a large area of, e.g., 300×400 mm^2 or 400×600 mm^2, is used, the pre-heating or post-heating is preferably effected at such a temperature which realizes a uniform temperature over the substrate without causing local thermal expansion or shrinking.

[0042] In case of irradiating a visible or infrared radiation, a silicon oxide film or a silicon nitride film is preferably formed as a protective film on the surface of the silicon film. The film provides a silicon film **105** having a surface of improved quality. In the present example, the irradiation was carried out under a hydrogen atmosphere to improve the surface characteristics of the silicon film. However, the irradiation can be carried out under a hydrogen atmosphere added therein from 0.1 to 10% by volume of hydrogen chloride or other hydrogen halides as well as compounds of chlorine or bromine.

[0043] The irradiation of a visible light or a near infrared light is effected for selectively heating the crystallized silicon film. Thus, the thermal influence on the glass substrate during this step can be minimized. Furthermore, this step is particularly effective for reducing the defects and dangling bonds that are present in the silicon film. Moreover, after the RTA process, it is also effective to anneal the structure in hydrogen in the temperature range of from 200 to 500° C., representatively, at 350° C., for reducing the defects. The same effect can be obtained by ion doping hydrogen at a dose of from 1×10^{13} to 1×10^{15} cm^{-2} and heat treating the structure thereafter in the temperature range of from 200 to 300° C.

[0044] A 1,000 Å thick silicon oxide film **106** as a gate insulating film was deposited by plasma CVD after the RTA process. The plasma CVD process was effected using tetraethoxysilane (TEOS; $Si(OC_2H_5)_4$) and oxygen as the starting gases while maintaining the substrate in the temperature range of from 300 to 550° C., for example, at 400° C.

[0045] Photo annealing was effected again after depositing the silicon oxide film **106** as the gate insulating film. The annealing was effected in the same manner as in the previous RTA process using a visible or a near infrared light. The levels at the boundary between the silicon oxide film **106** and the silicon film were found to disappear by the present annealing process. It can be seen that this step is extremely effective for an insulated-gate field effect semiconductor device in which the boundary characteristics between the gate insulating film and the channel forming region are particularly important.

[0046] Succeedingly, an aluminum film (containing from 0.01 to 0.25% of a rare earth element selected from Group 111a elements of the Periodic Table) was deposited by sputtering at a thickness of from 6,000 to 8,000 Å, for example, at a thickness of 6,000 Å. The aluminum film was patterned by etching to form gate electrodes **107** and **109**. The surface of the aluminum film was anodically oxidized thereafter to form oxide layers **108** and **110** on the surface thereof. The surface oxidation was effected in an ethylene glycol solution containing from 1 to 5% of tartaric acid. The thickness of the oxide layers **108** and **110** thus obtained were each 2,000 Å, respectively. The thickness of the oxide layers **108** and **110** are provided as such to determine the thickness of the offset gate region to be formed in the later step of ion doping.

[0047] Next, impurities for imparting a region either P- or N-conductive were introduced in a self-aligned manner by means of ion doping process (plasma doping process) into the silicon film **105** by using the gate electrode portions (i.e., the gate electrode **107** and the peripheral oxide layer **108**, as well as the gate electrode **109** and the peripheral oxide layer **110**) as the mask. Phosphine (PH_3) and diborane (B_2H_6) were used as the doping gases. The dose was from 1×10^{15} to 8×10^{15} cm^{-2}. Thus, in case phosphine is used, phosphorus is introduced at a dose of, more specifically 2×10^{15} cm^{-2}, while applying an accelerating voltage of from 60 to 90 kV, for example, a oltage of 80 kV. In case diborane is used, boron is introduced at a dose of 5×10^{15} cm^{-2} while applying an accelerating voltage of from 40 to 80 kV, for instance, a voltage of 65 kV. The regions were selectively doped with the respective elements by covering the other region with a photoresist. Thus, N-type impurity regions **114** and **116**, and

p-type impurity regions **111** and **113** were obtained to form a region for a p-channel TFT (PTFT) and region for an n-channel TFT (NTFT).

[0048] The regions were then annealed by irradiating a laser beam. A KrF excimer laser operating at a wavelength of 248 nm and at a pulse width of 20 nsec was used in the present invention. However, the type of the laser is not limited thereto. The laser beam was irradiated from 2 to 10 shots per site, for example, 2 shots per site, at an energy density of from 200 to 400 mJ/cm^2, for instance, at 250 mJ/cm^2. The effect of laser annealing can be further enhanced by heating the substrate in the temperature range of from about 200 to 450° C. (**FIG. 1**(C)).

[0049] Further, the step above can be effected otherwise by RTA, i.e. by irradiating a visible or near infrared radiation. A visible light or a near infrared radiation can be easily absorbed by crystallized silicon or amorphous silicon added therein from 10^{17} to 10^{21} cm^{-3} phosphorus or boron. Thus, an effective annealing well comparable to thermal annealing effected at 1,000° C. or higher can be realized. The addition of phosphorus or boron atoms accelerates the absorption of a radiation by impurity scattering effect. Accordingly, a near infrared light can be sufficiently absorbed by the silicon film. This phenomena can be easily assumed by the black-colored opaque appearance of the film. However, a radiation in the visible to the near infrared region is less absorbed by the glass substrate. Thus, the silicon film can be readily annealed in a short time without heating the glass substrate to a high temperature. This process can be said ideal for a case in which the shrinkage of a glass substrate is found problematic.

[0050] A 6,000 Å thick silicon oxide film **117** was deposited by plasma CVD thereafter as an interlayer dielectric. The interlayer dielectric may be made from a polyimide film or a double-layered film of silicon oxide and polyimide. Contact holes were formed thereafter to establish electrodes/wirings **118**, **120**, and **119** of TFT using a metallic material, for example, a multilayered film of titanium nitride and aluminum. Lastly, a semiconductor circuit comprising the TFTs in a complementary arrangement was obtained by finally annealing the structure at a temperature of 350° C. for a duration of 30 minutes under a hydrogen gas atmosphere at a pressure of 1 atm (**FIG. 1**(D)).

[0051] In the process according to the present invention, it is particularly important to add hydrogen to the dangling bonds formed during the RTA using a visible light or a near infrared radiation. This can be accomplished by heating the structure in hydrogen at a temperature in the range of from 250 to 400° C. in a step subsequent to that of RTA. Thus, the process according to the present invention provides an improved productivity, a TFT which yields a leak current (off current) reduced by two to three digits as compared with a TFT fabricated by a prior art process. The leak current in this case signifies a leak current which generates when zero voltage or a reversed bias voltage (negative voltage in case of an NTFT) is applied to the gate electrode.

[0052] The circuit thus obtained has a CMOS construction with a PTFT and an NTFT provided in a complementary arrangement, however, it is also possible to fabricate two independent TFTs by forming two TFTs simultaneously according to the process steps above, and separating them at the center.

EXAMPLE 2

[0053] The present example relates to an active-matrix type liquid crystal display device having N-channel TFTs (NTFTs) each attached as a switching element to each of the pixels. The following description refers to a single pixel only, however, a practical active-matrix type liquid crystal device comprises a great number (generally several hundred thousands) of pixels all having the same structure simultaneously. Furthermore, the TFT not necessarily be an NTFT, and a PTFT can be employed as well. The TFT need not be provided to the pixel portion of the liquid crystal display, and it can be used in the peripheral circuits. Moreover, it can be used in image sensors and in other devices. In short, the application is not limited as long as it is used as a thin film transistor.

[0054] Referring to the step sequential structures shown in FIGS. **2**(A) to **2**(D), the process for fabricating the structure according to an embodiment of the present invention is described below. A 2,000 Å thick film of aluminum nitride was deposited by sputtering as a base film **201** on a NA45 glass substrate **200** having a thickness of 1.1 mm and an area of 300×400 mm^2 and a strain point of 610° C., and a silicon oxide film **202** was further deposited thereon by plasma CVD at a thickness of 2,000 Å as another base film. Aluminum nitride has a high thermal conductivity ten times as high as that of a glass substrate or even higher. Accordingly, the aluminum nitride film deposited on the substrate was found favorable for maintaining the temperature of the entire substrate uniform. Furthermore, the adhesiveness of the aluminum nitride film to the glass substrate can be increased by adding from 0.01 to 20% by atomic of oxygen to the aluminum nitride film with respect to nitrogen, thereby bringing the thermal expansion coefficient of aluminum nitride film nearer to that of the glass substrate.

[0055] The aluminum nitride film can be deposited by plasma CVD using trimethylaluminum ($Al(CH_3)_3$) and ammonia as the starting materials. Otherwise, the aluminum nitride film can be deposited by means of reactive sputtering in a nitrogen or ammonia atmosphere using an aluminum target. The silicon oxide film **202** was deposited by CVD using TEOS and oxygen as the starting materials. A 1,000 Å thick amorphous silicon film **203** and a 200 Å thick silicon oxide film **204** were each deposited thereafter by LPCVD or plasma CVD. The resulting structure was heated at 550° C. for annealing for a duration of 1 hour (**FIG. 2**(A)).

[0056] After the step of thermal annealing, the silicon film was patterned by etching to leave only an island-like active layer **205** alone for the TFT. A visible light or a near infrared radiation was irradiated thereafter to the island-like active layer **205** to improve the crystallinity thereof. Thus, annealing was effected at 1,100° C. for a duration of 30 seconds. Since the aluminum nitride film assures a uniform thermal conduction in the silicon film, the patterning by etching can be otherwise effected after irradiating a visible light or a near infrared radiation (**FIG. 2**(B)).

[0057] A gate insulating film **206** of a silicon oxide was deposited thereafter at a thickness of from 700 to 1800 Å, typically at a thickness of 1200 Å, by plasma CVD under an oxygen atmosphere using TEOS (tetra ethoxy silane) as the starting material. The temperature of the substrate was kept at 350° C. Then, a film containing polycrystalline silicon as the principal component was formed by LPCVD and pat-

terned by etching to obtain a gate electrode **207**. Phosphorus was incorporated into the polycrystalline silicon as an impurity at an amount of from 0.1 to 5% by atomic to improve the electric conductivity thereof.

[**0058**] Then, phosphorus was incorporated as an impurity by ion doping to render the impurity-doped portion N-type conductive. Thus, a source region **208**, a channel forming region **209**, and a drain region **210** were formed in a self-aligned manner. Laser beam was irradiated to the silicon film thereafter using a KrF laser to improve the crystallinity of the film which was damaged by ion implantation. A this time, the laser beam was irradiated at an energy density of from 250 to 300 mJ/cm^2. The sheet resistance of the source/drain of the TFT was found to be in the range of from 300 to 800 Ω/cm^2. In case of forming a lightly doped drain (LDD) structure comprising impurities at a lower concentration, the sheet resistance falls in the range of from 10 to 200 kΩ/square. The annealing can be effected by lamp annealing using a visible light or a near infrared radiation instead of irradiating a laser beam (**FIG. 2**(C)).

[**0059**] Thereafter, an interlayer dielectric **211** was formed using silicon oxide or polyimide. Furthermore, a pixel electrode **212** was formed using ITO (indium tin oxide). Contact holes were formed thereafter to establish electrodes **213** and **214** for the source/drain regions of the TFT using a multilayered film of chromium and aluminum. One of the electrodes **214** was connected to the ITO **212**. Finally, the resulting structure was annealed in hydrogen for a duration of 2 hours in the temperature range of from 200 to 400° C. to obtain a complete TFT. This step is effected simultaneously on a plurality of pixel regions. Furthermore, a passivation film may be formed on the entire surface using silicon nitride and the like to improve the moisture resistance of the TFT (**FIG. 2**(D)).

[**0060**] The pixel transistors for active matrices described above in the present example need not to be operated at a high speed. In this example, accordingly, the duration of the first thermal annealing step was shortened to 1 hour. Thus, the crystallinity of the silicon film obtained in the present example was found inferior to that of the one obtained in Example **1**. Nevertheless, sufficient static characteristic and dynamic characteristic were obtained as a switching transistor of the active-matrix circuit.

EXAMPLE 3

[**0061**] Referring to FIGS. **3**(A) to **3**(E), a process for fabricating a TFT circuit according to an embodiment of the present invention is described below. A substrate of a glass having a strain point in the range of from 550 to 650° C., such as an AN2 glass substrate having a strain point of 616° C., was used. To prevent shrinking from occurring, the substrate was subjected previously to pre-annealing at 670° C. for a duration of 4 hours and to cooling to 450° C. at a rate of 0.1° C./min in a manner similar to that in Example **1**. A base film **302** was formed on the substrate **301**, and an amorphous silicon film **303** having thickness from 300 to 800 Å and a 200 Å thick silicon oxide film **304** were deposited thereafter by plasma CVD. The resulting structure was heated for annealing at 620° C. for a duration of 30 minutes. After the thermal annealing, the substrate was rapidly cooled to 450° C. at a rate of from 2 to 200° C./sec, preferably, at a rate of 10° C./sec or higher. This treatment prevents the substrate from shrinking during thermal annealing. In case an annealing furnace not suitable for rapid cooling is employed, the substrate may be taken out from the furnace and placed in the ambient temperature to obtain a similar effect as described above. Furthermore, although AN2 was used as a substrate in EXAMPLE 3, other glass substrate having a strain point of 550 to 680° C., e.g. Corning 1733 (strain point 640° C.) and LE30 (strain point 625° C.) may be used instead.

[**0062**] The substrate was subjected to a thermal annealing at a temperature higher than those of Examples 1 and 2, and yet, at a temperature higher than the strain point (616° C.) of AN2 glass. Accordingly, it was difficult to suppress the shrinking of the substrate even though a heat treatment and cooling were effected beforehand on the substrate. Rapid cooling from the annealing temperature was found effective in such a case (**FIG. 3**(A)).

[**0063**] The silicon film **303** was patterned by etching thereafter to form island-like active regions **306** and **307**. The active layer was etched by RIE (reactive ion etching) having an anisotropy along the perpendicular direction (**FIG. 3**(B)).

[**0064**] A silicon oxide film or a silicon nitride film **307** was deposited thereafter to a thickness of from 200 to 3,000 Å by plasma CVD. Otherwise, a silicon nitride film can be formed by low pressure CVD or photo CVD. Then, similar to the case in Example 1, RTA treatment was effected using a visible light or a near infrared radiation. The conditions for the RTA treatment were the same as those used in Example 1. In the present case, a protective film of silicon oxide or silicon nitride thus formed over the surface of the active layer prevented roughening or staining from occurring on the surface of the active layer on irradiating a visible light or a near infrared radiation (**FIG. 3**(C)).

[**0065**] The protective film **307** was removed after the step of irradiating a visible light or a near infrared radiation. Then, a gate insulating film **308**, and gate electrodes **309** and **310** were formed in the same manner as in Example 1, and an impurity region was formed thereafter by ion doping. The impurity region thus obtained was activated by irradiating a laser beam thereto (**FIG. 3**(D)).

[**0066**] After forming an interlayer dielectric **311**, contact holes were formed to establish metallic wirings **312**, **313**, and **314** (**FIG. 3**(E)).

[**0067**] Thus, a complementary TFT circuit was obtained. The present example is characterized in that the surface roughening or staining is prevented from occurring on the surface of the active layer by forming a protective film on the surface of the active layer upon irradiating a visible light or a near infrared radiation. Thus, the semiconductor characteristics (e.g., an electric field mobility and a threshold voltage) as well as reliability were found to be excellent. Furthermore, as described above, the process according to the present invention was particularly effective on substrate materials having a glass transition temperature (strain point) in the temperature range of from 550 to 680° C.

[**0068**] By additionally irradiating an intense light of a wavelength corresponding to visible or near infrared light to the silicon film crystallized by thermal annealing and the like, crystallinity of the silicon film can be improved and the silicon film can be densified simultaneously to obtain a

silicon film having a good crystallinity. In case of employing thermal annealing particularly, the temperature is preferably 520 to 620° C., more preferably 550 to 600° C., and the time is preferably 1 to 4 hours.

[0069] Further, in order to improve characteristic of the gate insulating film, after an insulating film is formed on the crystalline silicon film obtained by the present invention, the crystalline silicon film may be annealed by irradiating thereto a light having a wavelength corresponding to visible light or near infrared radiation in dinitrogen monoxide (N_2O) or ammonia. By this annealing, interface level can be reduced. Furthermore, after these steps, hydrogen may be added in the silicon film to neutralize or eliminate dangling bonds by hydrogenation annealing at 200 to 450° C. in hydrogen atmosphere.

[0070] In case that thermal annealing is employed in the present invention, the time required for the thermal annealing is largely shortened to 4 hours or shorter from several tens hours required conventionally. Since the annealing time is shorter than before, influence on the substrate by theannealing-step is sufficiently small. Furthermore, wavelength of the light used in the lator RTA process is 0.6 to 4 μm. Even if glass material is used for the substrate, since the substrate is cooled rapidly, the substrate is not soften and is not shrunk and is not transformed to an industrially unusable degree. Thus, the present invention is industrially useful and particularly the present invention is extremely effective for forming an insulated gate semiconductor device.

[0071] While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.

1. (canceled)

2. A method for fabricating a thin film transistor comprising steps of:

forming a non-single crystal semiconductor film over a glass substrate,

first annealing the non-single crystal semiconductor film to eject hydrogen from the non-single crystal semiconductor film, and

second annealing the non-single crystal semiconductor film to heat the non-single crystal semiconductor film at 800 to 1300° C.

3. The method according to claim 2,

wherein the first annealing is conducted at 520 to 620° C.

4. The method according to claim 2,

wherein the first annealing is conducted for 1 to 4 hours.

5. The method according to claim 2,

wherein the second annealing is conducted by rapid thermal annealing method.

6. The method according to claim 2,

wherein the second annealing is conducted using a light with wavelength of 4 μm to 0.6 μm.

7. The method according to claim 2,

wherein the second annealing is conducted for 10 to 1000 seconds.

8. The method according to claim 2,

wherein the second annealing includes a post heat process.

9. The method according to claim 2,

wherein the second annealing includes a preheat process.

10. The method according to claim 2,

wherein the method further comprises a step of patterning the non-single crystal semiconductor film in to at least one island by etching before the second annealing.

11. The method according to claim 2,

wherein the method further comprises a step of forming a protective film of silicon oxide over the non-single crystal semiconductor film before the second annealing.

12. The method according to claim 2,

wherein the method further comprises a step of forming a protective film of silicon nitride over the non-single crystal semiconductor film before the second annealing.

13. A method for fabricating a thin film transistor comprising steps of:

forming a non-single crystal semiconductor film over a glass substrate with strain point from 550° C. to 680° C.,

first annealing the non-single crystal semiconductor film to eject hydrogen from the non-single crystal semiconductor film, and

second annealing the non-single crystal semiconductor film to heat the non-single crystal semiconductor film at 800 to 1300° C.

14. The method according to claim 13,

wherein the first annealing is conducted at 520 to 620° C.

15. The method according to claim 13,

wherein the first annealing is conducted for 1 to 4 hours.

16. The method according to claim 13,

wherein the second annealing is conducted by rapid thermal annealing method.

17. The method according to claim 13,

wherein the second annealing is conducted using a light with wavelength of 4 μm to 0.6 μm.

18. The method according to claim 13,

wherein the second annealing is conducted for 10 to 1000 seconds.

19. The method according to claim 13,

wherein the second annealing includes a post heat process.

20. The method according to claim 13,

wherein the second annealing includes a preheat process.

21. The method according to claim 13,

wherein the method further comprises a step of patterning the non-single crystal semiconductor film in to at least one island by etching before the second annealing.

22. The method according to claim 13,

wherein the method further comprises a step of forming a protective film of silicon oxide over the non-single crystal semiconductor film before the second annealing.

23. The method according to claim 13,

wherein the method further comprises a step of forming a protective film of silicon nitride over the non-single crystal semiconductor film before the second annealing.

24. A method for fabricating a thin film transistor comprising steps of:

forming an insulating film over a glass substrate,

forming a non-single crystal semiconductor film over the insulating film,

first annealing the non-single crystal semiconductor film to eject hydrogen from the non-single crystal semiconductor film, and

second annealing the non-single crystal semiconductor film to heat the non-single crystal semiconductor film at 800 to 1300° C.

25. The method according to claim 24,

wherein the insulating film comprises silicon oxide.

26. The method according to claim 24,

wherein the insulating film comprises silicon nitride.

27. The method according to claim 24,

wherein the first annealing is conducted at 520 to 620° C.

28. The method according to claim 24,

wherein the first annealing is conducted for 1 to 4 hours.

29. The method according to claim 24,

wherein the second annealing is conducted by rapid thermal annealing method.

30. The method according to claim 24,

wherein the second annealing is conducted using a light with wavelength of 4 μm to 0.6 μm.

31. The method according to claim 24,

wherein the second annealing is conducted for 10 to 1000 seconds.

32. The method according to claim 24,

wherein the second annealing includes a post heat process.

33. The method according to claim 24,

wherein the second annealing includes a preheat process.

34. The method according to claim 24,

wherein the method further comprises a step of patterning the non-single crystal semiconductor film in to at least one island by etching before the second annealing.

35. The method according to claim 24,

wherein the method further comprises a step of forming a protective film of silicon oxide over the non-single crystal semiconductor film before the second annealing.

36. The method according to claim 24,

wherein the method further comprises a step of forming a protective film of silicon nitride over the non-single crystal semiconductor film before the second annealing.

37. A method for fabricating a thin film transistor comprising steps of:

forming a non-single crystal semiconductor film over a glass substrate,

adding a metal element to the non-single crystal semiconductor film,

first annealing the non-single crystal semiconductor film to eject hydrogen from the non-single crystal semiconductor film, and

second annealing the non-single crystal semiconductor film to heat the non-single crystal semiconductor film at 800 to 1300° C.

38. The method according to claim 37,

wherein the second annealing includes a post heat process.

39. The method according to claim 37,

wherein the second annealing includes a preheat process.

40. The method according to claim 37,

wherein the method further comprises a step of patterning the non-single crystal semiconductor film in to at least one island by etching before the second annealing.

41. The method according to claim 37,

wherein the method further comprises a step of forming a protective film of silicon oxide over the non-single crystal semiconductor film before the second annealing.

42. The method according to claim 37,

wherein the method further comprises a step of forming a protective film of silicon nitride over the non-single crystal semiconductor film before the second annealing.

43. The method according to claim 37,

wherein the first annealing is conducted at 520 to 620° C.

44. The method according to claim 37,

wherein the first annealing is conducted for 1 to 4 hours.

45. The method according to claim 37,

wherein the second annealing is conducted by rapid thermal annealing method.

46. The method according to claim 37,

wherein the second annealing is conducted using a light with wavelength of 4 μm to 0.6 μm.

47. The method according to claim 37,

wherein the second annealing is conducted for 10 to 1000 seconds.

48. The method according to claim 37,

wherein the metal element is one selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Sc, Ti, V, Cr, Mn, Cu, Zn, Au and Ag.

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