A fast recovery rectifier structure with the combination of Schottky structure to relieve the minority carriers during the forward bias condition for the further reduction of the reverse recovery time during switching in addition to the lifetime killer method such as Pt, Au, and/or irradiation. This fast recovery rectifier uses unpolished substrates and thick impurity diffusion for low cost production. A reduced p-n junction structure with a heavily doped film is provided to terminate and shorten the p-n junction space charge region. This reduced p-n junction with less total charge in the p-n junction to further improve the reverse recovery time. This reduced p-n junction can be used alone, with the traditional lifetime killer method, with the Schottky structure and/or with the epitaxial substrate.
Initial fabrication processes on a substrate with n-type 1005

Deposit a p-type semiconductor layer upon the substrate 1010

Form a thin film of very shallow p\textsuperscript{++} type by either implantation or diffusion upon the p-type semiconductor layer to create an early termination at p side 1015

Figure 10
METHOD OF MANUFACTURING A FAST RECOVERY RECTIFIER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 11/801,023, filed on May 8, 2007, which claims priority to U.S. provisional patent application Ser. No. 60/799,252 filed May 10, 2006 and entitled “Fast Recovery Rectifiers”, from which priority is claimed under 35 U.S.C. §119(e) and which applications are incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates generally to the structures of a fast recovery rectifier. This invention discloses the method of reducing the reverse recovery time from a conventional fast recovery rectifier by either introducing the Schottky structure at the front and/or the back of the substrate or introducing the junction termination layer to reduce the total space charge of the p-n junction. Furthermore, this invention also provides the low cost manufacturing of a very fast recovery rectifier.

[0004] 2. Description of Related Art

[0005] FIG. 1 shows the cross section of a conventional fast recovery rectifier. The doped substrate 100 is made by either n type or p type material. The doped substrate 100 used is a wafer with sawed or unpollished rough surface treatment for cost savings. The polish of the wafer surface is not required in this case. Doping of wafer can be done by either film method or by standard deep diffusion method. The p-n junction 103 can be formed on the doped substrate 100, and the depth of the p-n junction 103 is usually from less than 10 microns to over 20 microns so that the depth of the p-n junction 103 is deeper than the surface damaged region of the rough surface. Then the lifetime killer such as Pt, Au, etc. is added to the wafer with thermal treatment. The reverse recovery time is depending on doping concentration, the thermal treatment temperature, and time of the lifetime killer species. The other method for the lifetime reduction can also be done by irradiation of electrons or other species. After the irradiation treatment, the substrate is being processed by annealing.

[0006] The diffusion to the doped substrate 100 is generally using opposite polarity species at the p-n junction 103. The depth of this p-n junction 103 must be deeper than the surface damage region for the reduction of the leakage current. The diffusion to the doped substrate 100 is generally using the same polarity as at the backside layer 101. The passivation layer 104 can be formed after the formation of the p-n junction 103 as well as the life time killer process. The irradiation of the electrons and or other species can be done after the process of the wafer or even in the packaged parts. The passivation layer 104 can be done by conventional glass passivation process or multiple CVD process. The top metal layer 105 is deposited, evaporated, sputtered, or plated along with the top of the p-n junction 103. The bottom layer 105B metalization is to be done by similar metalization process or by nickel plating. After the completion of the process, the wafer is diced into chips for assembly.

[0007] FIG. 2 shows the cross section of an epitaxial based fast recovery rectifier in prior art. The epitaxial layer 102 has the same polarity and is grown on the heavily doped substrate 100. The doping concentration and the thickness of the epitaxial layer 102 are determined by the breakdown voltage. The epitaxial layer 102 can be made by single or multiple layers. The p-n junction 103 anode diffusion can be done by either ion implantation or diffusion method of the opposite polarity to the epitaxial layer 102. After the formation of the p-n junction 103 anode diffusion, the life time killer such as Pt, Au or other species with proper thermal treatment can be added to the wafer. After the p-n junction diffusion, the deep etched structure is to be done by wet etch prior to the passivation process. The passivation layer 104 is done either by the conventional glass passivation or multiple CVD layers method. The top metal layer 105 is then opened for the metalization. The top metal layer 105 can be done by the contact metalization using either Ti—TiN—Al, TiNiAg or Nickel plating for either wire bond or soldering. The backside layer 101 can be done by the implantation of similar polarity to the silicon doped substrate 100 or omitted if the doped substrate 100 is heavily doped. The bottom layer 105B metallization is done either by Ti—Ni—Ag or Cr—Au or by Ni plating. After the completion of the process, the wafer is then ready for the dicing and assembly.

[0008] U.S. Pat. No. 6,261,874, Francis and Ng disclosed the fast recovery diode structure with both beam Radiation defects and He implanted defects to reduce the reverse recovery time. With this structure, the soft recovery time can result. U.S. Pat. No. 6,486,524, Ahmed disclosed the complicated structure using p-n junction as well as the AI or Pd Schottky for the fast reverse recovery time. U.S. Pat. No. 6,603,153, Francis and Ng disclosed the fast recovery rectifier structure that is similar to U.S. Pat. No. 6,261,875. U.S. Pat. No. 6,699,755 B1 disclosed a fast recovery diode structure similar to U.S. Pat. No. 6,486,524. U.S. Pat. No. 6,870,199 Yoshikawa et al disclosed the multiple lifetime control region for the improvement of di/dt caused breakdown. U.S. Pat. No. 6,927,141 Andoh et al disclosed the termination structure by using equal metal ring.

SUMMARY OF THE INVENTION

[0009] It is therefore an objective of the present invention to provide a low cost and the improvement of the process and device structures. By using the common fast recovery rectifier, a termination structure using glass and/or CVD process is the basic structure to begin with. The substrate is an sawed or non-polished substrate instead of polished wafers for the reduction of the cost. Deep diffusion of opposite polarity to the substrate in one side and the same polarity in the other side are performed. The depth of the diffusion is from less than 10 microns to over 20 microns depending on the surface damage region of the unpolished wafer. This invention adds the etched region with either wet etches or wet/dry etches for the provision of the Schottky contact. This etched region can be a round shape, hexagon, stripe or other shapes. The metallization is then provided for the ohmic contact of the heavily doped rough surface and for Schottky contact of the etched smooth region. The purpose of the Schottky contact is to absorb the minority carrier injections at the forward bias, thus the reverse recovery time is reduced. The similar structure at the other side can also be added for the reduction of the minority carriers. Thus the reduction of the reverse recovery time can be further reduced. In order to improve the reverse recovery time, the conventional method is using the epitaxial wafers and then using life time killing method. The heavily doped substrate is used to decrease the forward voltage drop due to series resistance and in the mean time to reduce the
lifetime by reducing the thickness of the lightly doped active epitaxial region. The second objective of this invention is to form a reduced p-n junction space charge region (or depletion region) by using a thin and highly doped film of the same polarity as the top junction layer which has opposite polarity to the base silicon substrate. This early termination of the junction charge region reduces the total space charge of the p-n junction, thus the smaller reverse recovery time can be achieved. This method can be used in conjunction with the lifetime killers and/or with the Schottky structures.

**BRIEF DESCRIPTION OF THE DRAWINGS**

**[0010]** FIG. 1 shows the cross section of the conventional fast recovery rectifier.

**[0011]** FIG. 2 shows the cross section of epitaxial based fast recovery rectifier in prior art.

**[0012]** FIG. 3 is a cross-sectional view of the present invention fast recovery rectifier.

**[0013]** FIG. 4 discloses a cross section similar to FIG. 3 except the back side of the wafer is also etched like the top surface.

**[0014]** FIG. 5 discloses a cross section of epitaxial based fast recovery rectifier.

**[0015]** FIG. 6 shows a normal charge diagram of an n-p junction.

**[0016]** FIG. 7 has smaller built-in potential than FIG. 6.

**[0017]** FIG. 8 discloses a cross section of epitaxial fast recovery rectifier by using guard rings as the termination structure.

**[0018]** FIG. 9 disclosed a cross section of epitaxial based fast recovery rectifier by using guard rings as the termination structure.

**[0019]** FIG. 10 illustrates a flow chart of a method of manufacturing a reduced p-n junction of a fast recovery rectifier.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

**Embodiment One**

**[0020]** FIG. 3 is a cross-sectional view of the present invention fast recovery rectifier that is different from the FIG. 1 in the etched structure 103A. In addition, the etched structure 103A of FIG. 3 can be etched (preferred by wet etch) either in round, hexagon, strip or other shapes. The diameter or the width of the etched structure is generally larger than twice the depth of the p-n junction 103. In general, it is over 20 microns.

**[0021]** The p-n junction 103 is deposited, evaporated, sputtered, or plated along with the top metal layer 105. The p-n junction 103 is terminated early by a very thin and heavily doped layer 110 with the same polarity as 103. This layer 105 can be formed by contact metal and/or barrier metal and/or top metal for soldering or wire bonding. The backside layer 101 is to be done by similar metallization process or by nickel plating. After the completion of the process, the wafer is diced into chips for assembly.

**Embodiment Two**

**[0022]** FIG. 4 discloses a cross section similar to FIG. 3 except the back side of the wafer is also etched like the top surface. The purpose for this structure is to get the addition of the Schottky surface to absorb the minority carrier at the backside of the chip. The location of the etched structure 103B is not necessary to be aligned with the top surface structure 103A. The shape of the etched structure 103B can be round, hexagon, stripe or other structures depending on the requirement. Both FIG. 3 and FIG. 4 of the present invention offer the low cost versions of the fast recovery rectifiers.

**Embodiment Three**

**[0023]** FIG. 5 discloses a cross section of epitaxial based fast recovery rectifier. The epitaxial layer 102 has the same polarity and is grown on the heavily doped substrate 100. The doping concentration and the thickness of the epitaxial layer 102 are determined by the breakdown voltage. The epitaxial layer 102 can be made by single or multiple layers. The p-n junction anode diffusion 103 can be done by either ion implantation or diffusion method of the opposite polarity to the epitaxial layer 102 using silicon dioxide as the mask. The p-n junction 103 is terminated early by a very thin and heavily doped layer 110 with the same polarity as 103. For the ion implantation, the photo resist can be used in addition to the oxide layer as the mask. The Schottky contact region 107 is the masked region of photo resist and oxide layer. This masked Schottky contact region 107 is used for the Schottky contact.

**[0024]** In this embodiment, after the formation of the p-n junction anode layer, the lifetime killers such as P, Au or other species with proper thermal treatment can be added to the wafer. On the other hand, after the top layer diffusion, the deep etched structure is to be done by etching, preferably by wet etch prior to the passivation process. The passivation layer 104 is done either by the conventional glass passivation or multiple CVD layers method.

**[0025]** Next, the top metal layer 105 is then opened for the metallization. The top metal layer 105 can be done by the Schottky contact metallization with either Pt, Au, Ni, Mo, W, Cr, Ti etc. followed by the barrier metal layer such as TiW, TiN, and the top metal such as Al, Ag, etc. for either wire bond or soldering. The backside layer 101 can be done by the implantation of similar polarity to the silicon substrate or omitted if the substrate is heavily doped. The bottom layer 1053 is done either by Ti—Ni—Ag or Cr—Au or by Ni plating. After the completion of the process, the wafer is then ready for the dicing and assembly.

**[0026]** FIG. 6 shows a normal charge diagram of a n-p junction. The total area of qNaxxp1 at p region is equal to that of qNdxnx1 at the n region. Na is the doping concentration of the p region and xp 1 is the charge distance of the p region. By using a heavily doped p layer to make the distance xp2 of p region smaller, the total area of qNaxxp2 is smaller than that of qNaxxp1 with same doping level of Na. In order to balance the total charge, qNdxnx2 is the same as qNaxxp2. Nd is the doping concentration of n region and xn is the charge distance of the n region. Thus the built-in potential of FIG. 7 is smaller than the built-in potential of FIG. 6. In order to get good ohmic contact, this very thin layer of P++ at xp2 must be presented and the same is true for n-p junction. Reduced p-n junction is made by the following conditions: (a) The doping concentration of p region of said reduced p-n junction is in the magnitude from 2 to 10 times the magnitude of the n region, and this can be accomplished by lightly doped implant with low energy and dose—the energy of the implant is from 500 eV to 50 KeV with implant dose from 1.0E12 to 1.0E15 per cm², and light implant anneal is done by either RFA or furnace in inert ambient. Then, a very shallow p++ region is placed on the top of the p region and the implant dose is from 1.0E12 to 1.0E15 per cm² with the energy from 100V to 35
KeV, then implant anneal is done by RTA. The heavily doping concentration but very shallow p type region can be used to terminate said p-n junction; (b) Using the heavily doping concentration but very shallow p type region, the heavily doping concentration but very shallow p type region may use low temperature p++ type diffusion with the temperature from 700 deg. C. to 1100 deg. C. and time from 60 seconds to one hour with furnace or RTA diffusion. Said reduced p-n junction ranged from 0.5 ev. to 0.9 ev.

Referring to embodiments four and five to be described below. The planner termination structure for high voltage guard ring either is using single or multiple guard rings for the epitaxial wafer. The epitaxial layer or multiple epitaxial layers is deposited on the similar polarity substrate under the condition—the implant dose of the opposite polarity region ranging from less than 1E10 per cm² to 1E16 per cm² with the implant energy from 100 V to over 100 KeV and time 10 seconds to one hour with the temperature from 600 to 1100 deg. C. to form the p-n junction or the Schottky region by blocking the implant species, and the implant condition for the guard ring can be the same as the opposite polarity base material.

Embodiment Four

FIG. 8 disclosed a cross section of epitaxial based fast recovery rectifier by using guard rings as the termination structure. The insulation layer 104 is a thick oxide from 200 A to over 2 microns. This insulation layer 104 can be formed either by oxidation or CVD layers or both. The guard ring 106 structure is either single guard ring or multiple guard rings depending on the requirement of the reverse blocking voltage. The guard ring 106 can be formed either by diffusion or implant. The implant dose for the guard ring 106 is from less than 1E10 per cm² to over 1E15 per cm² and the implant energy from less than 100 V to over 100 KeV depending on the design requirement. The implant dose of the diode regions 103 is done from less than 1E10 per cm² to over 1E15 per cm² and the implant energy from less than 100 V to over 100 KeV. This implant of diode regions 103 and guard ring 106 is in the opposite polarity to the base material of epitaxial layer 102. The diode termination layer 110 is a very heavy doped region with the same polarity of diode region 103. This diode termination layer 110 can be formed either by the implant energy from 100 V to 50 KeV and the dose from 1E11 per cm² to over 1E15 per cm² or by diffusion with temperature from 700 deg. C. to over 1100 deg. C. and the time from over one hour to less than 30 seconds.

In this embodiment, the purpose of diode termination layer 103A is to terminate the p region into the narrower space, thus the total charge will be smaller. The lifetime killer such as Pt, Au, or can be added before or after the process. The top metal layer 105 can be either formed by Au, Pt, W, Mo Cr, Ni, Ti and other material or used to form the silicide.

Next, the diffusion barrier such as TiW, TiN or other layer is done before the contact layer of the 105 is deposited. The contact layer of the 105 can be either formed by Au, Pt, W, Mo Cr, Ni, Ti and other metal or used to form the silicide.

The fast recovery rectifier of this invention is accomplished by one or more of following conditions:

Schottky structure is used with the standard fast recovery rectifier by using Pt, Au and/or radiation lifetime killer.

Reduced p-n junction is used with the standard fast recovery rectifier with Pt, Au, and/or radiation lifetime killer.

Reduced p-n junction is used with Schottky structure and standard fast recovery rectifier with Pt, Au and/or radiation lifetime killer.

Reduced p-n junction alone.

Reduced p-n junction is used with Schottky structure.

Reduced p-n junction is used with Schottky structure and standard fast recovery rectifier with Pt, Au and/or radiation lifetime killer with epitaxial substrates.
[0040] The fast recovery rectifier of this invention uses the Pt, Au and/or radiation lifetime killer, and combine with Schottky structure to reduce the minority carriers at the forward bias and in the rectifying process condition. The fast recovery rectifier use unpolished rough surface doped substrate and rough diffusion to provide a low cost. This invention is to form a reduced p-n junction space charge region by using a thin and very high doped film of the same polarity as the top junction layer which is opposite polarity to the base silicon substrate. This early termination of the junction charge region reduces the total space charge of the p-n junction, thus the smaller reverse recovery time can be achieved. This method can be used in conjunction with the life time killers and/or with the Schottky structures.

[0041] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A method of manufacturing a rectifier, comprising:
   - forming a first semiconductor layer with a first type of dopant;
   - depositing a second semiconductor layer of a second type of dopant above said first semiconductor layer, wherein said first type of dopant and said second type of dopant have opposite polarity;
   - depositing a thin film of a third semiconductor layer of said second type of dopant immediately above said second semiconductor layer, wherein doping concentration of said third semiconductor layer is higher than doping concentration of said second semiconductor layer to create an early termination at the interface of said second semiconductor layer and said third semiconductor layer;
   - depositing a metal layer above said third semiconductor layer, wherein the interface between said metal layer and said third semiconductor layer is an ohmic contact.

2. The method of claim 1, further comprising epitaxial forming a fourth semiconductor layer with said first type of dopant between said first semiconductor layer and said second semiconductor layer, wherein doping concentration of said fourth semiconductor layer is lower than doping concentration of said first semiconductor layer.

3. The method of claim 1, wherein said first type of dopant is n-type.

4. The method of claim 1, wherein said first semiconductor layer further comprising one or more lifetime killer materials including Pt or Au.

5. The method of claim 1, wherein depositing a thin film of said third semiconductor layer further comprises performing an implantation.

6. The method of claim 5, wherein performing implantation includes using implant dose from about 1.0e15 per cm² to about 1.0e16 per cm².

7. The method of claim 5, wherein performing implantation includes using implant energy from about 50 eV to about 50 KeV.

8. The method of claim 5, wherein doping concentration of said second semiconductor layer is approximately 2 to 10 times of said first semiconductor layer.

9. The method of claim 1, wherein depositing a thin film of said third semiconductor layer further comprises performing a diffusion.

10. The method of claim 9, wherein performing diffusion includes using diffusion temperature from about 700° C. to about 1100° C.

11. The method of claim 9, wherein performing diffusion includes diffusion time from about 60 second to about 1 hour.

12. The method of claim 9, wherein junction voltage between said first semiconductor layer and said second semiconductor layer is from about 0.5 eV to about 0.9 eV.

13. The method of claim 2, wherein said second semiconductor layer which is above said forth semiconductor layer is formed by performing implantation with implant dose from about 1.0e15 per cm² to about 1.0e16 per cm² and implant energy from about 100 V to about 100 KeV and time from about 10 seconds to about 1 hour and temperature from about 600° C. to about 1100° C.

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