(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 August 2003 (07.08.2003)

PCT

(10) International Publication Number
WO 03/065623 A1

(51) International Patent Classification[7]: H04B 15/00, H04K 1/00, H04L 27/30

(21) International Application Number: PCT/US02/39320

(22) International Filing Date: 10 December 2002 (10.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/036,554 21 December 2001 (21.12.2001) US

(71) Applicant: **MOTOROLA, INC.** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: **SHI, Qicai**; 5462 N.W. 122nd Drive, Coral Springs, FL 33076 (US). **O'DEA, Robert, J.**; 2524 N.E. 26th Avenue, Fort Lauderdale, FL 33305 (US).

(74) Agents: **DOUTRE, Barbara, R.** et al.; 8000 West Sunrise Blvd., Rm 1610, Fort Lauderdale, FL 33322 (US).

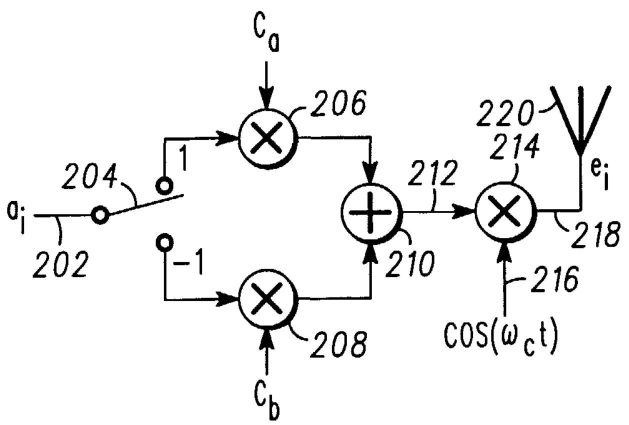
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: LOW COST DSSS COMMUNICATION SYSTEM



(57) Abstract: A method and apparatus for direct sequence spread spectrum communication having low complexity. In the transmitter (figure 2A), the data bit (202) is spreaded by a code sequence (Ca and Cb), a reference code is interleaved with the code sequence, and together (210) they are transmitted by the transmitter. The corresponding receiver recovers the data signal from the received signal by transforming the received signal to a complex base band signal and differentially decoding the base band signal at the chip level. The spreaded signal is despreaded by the chip-level differential operation, thus eliminating the decorrelation operation, and so significantly reducing the cost of the overall system. Furthermore, this system is very robust to any carrier frequency drift since the chip-level differential operation is used, thus releasing the reference clock or crystal requirements, and so further reducing the cost of the system.

WO 03/065623 A1

LOW COST DSSS COMMUNICATION SYSTEM

TECHNICAL FIELD

This invention relates to techniques and apparatus for wireless communication using Direct Sequence Spread Spectrum (DSSS) techniques.

BACKGROUND OF THE INVENTION

In the transmitter of a direct-sequence spread spectrum communication systems, a carrier waveform is modulated by a data sequence x(n) and by a spreading sequence or code sequence C(n). The code sequence may be a pseudo-noise (PN) sequence, such as a maximum length sequence (m-sequence). The PN sequence is used to reduce the sensitivity of the communication channel to noise, reduce the power spectral density of the signal and to allow multiple communication channels to operate simultaneously. In the latter case, each channel is assigned its own PN code sequence, so the technique is called code-division multiple access (CDMA).

In the receiver the data signal is recovered by removing the carrier wave and then correlating the received signal with the PN code sequence used for transmission. Decorrelation requires a large amount of computation to align the received signal with the PN code sequence, and so adds to the cost of the receiver.

In view of the preceding remarks, it is clear that there is an unmet need in the art for a receiver that avoids the high cost of performing a correlation between the received signal and a PN code sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself however, both as to organization and method of operation, together with objects and advantages thereof, may be best understood by reference to the following detailed description of the invention, which describes certain exemplary embodiments of the invention, taken in conjunction with the accompanying drawings in which:

FIG. 1 is a diagrammatic representation of the generation of spreading codes in accordance with an embodiment of the present invention.

FIGS. 2A and 2B are diagrammatic representations of embodiments of a transmitter of the present invention.

FIG. 3 is a diagrammatic representation of a digital receiver of the present invention.

FIG. 4 is a diagrammatic representation of an analog receiver of the present invention.

FIG. 5 is a diagrammatic representation of a transmitter of a further embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail specific embodiments, with the understanding that the present disclosure is to be considered as an example of the principles of the invention and not intended to limit the invention to the specific embodiments shown and described. In the description below, like reference numerals are used to describe the same, similar or corresponding parts in the several views of the drawings.

In direct sequence spread spectrum (DSSS) communication, a pseudo-noise (PN) code sequence is used to modulate a carrier waveform and thereby spread the spectrum of the transmitted signal. A PN code sequence of length N is denoted by $C = (C_1, C_2, C_3, \ldots, C_N)$, where C_i has the value 1 or -1. The PN code sequence preferably has the property that the correlation of the sequence with a cyclically time-shifted version of itself has an absolute value of one or zero, whereas the correlation of the code sequence with itself has the value N.

In a first embodiment of the present invention, the two code sequences of length 2N are generated by interleaving groups of M elements from the sequences C and ±C. The two sequences are

$$C_a(2jM+i) = C(jM+i)$$
$$C_a((2j+1)M+i) = C(jM+i)$$

and

$$C_b(2jM+i)=C(jM+i)$$
$$C_b((2j+1)M+i)=-C(jM+i)$$

where j=0,..., N/M -1 and i=1,...,M.

For example, when M=1, the two code sequences of length 2N are generated as $C_a = (C_1, C_1, C_2, C_2, C_3, C_3,\ldots, C_N, C_N)$ and $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3,\ldots, C_N, -C_N)$. These sequences may be generated, as in **FIG 1** for example, by interleaving the code sequence C with the code sequence C or -C. The transmitted signal is generated as shown in **FIG 2A**. The data signal $x = (a_1, a_2, a_3,\ldots)$ 202 is passed to selector 204. If the current signal a_i is equal to 1 it is passed to multiplier 206, where it is multiplied by the code sequence C_a. If the current signal a_i is equal to -1 it is passed to multiplier 208, where it is multiplied by the code sequence C_b. The outputs from the multipliers 206 and 208 are added at summer 210, to produce a modulation signal 212. The modulation signal 212 is passed to multiplier 214, where it multiplies (modulates) the carrier signal $\cos(\omega_c t)$ 216. Here, ω_c is the carrier frequency in radians per second, and t is the time in seconds. The resulting signal 218 is amplified and passed to antenna 220 for transmission. One element (chip) of the code sequence is generated every T_c seconds, so the chip rate is $R_c = 1/T_c$. The bit-rate is equal to $R_c/(2N)$, since 2N chips are used for each bit of information.

FIG. 2B shows a further transmitter of the present invention. A PN code sequence $C = (C_1, C_2, C_3,\ldots, C_N)$ is supplied to interpolator or up-sampler 230, that inserts zeros between the elements of the code sequence, yielding the sequence $C_{int} = (C_1, 0, C_2, 0, C_3, 0,\ldots, 0, C_N, 0)$. The sequence is delayed by one chip period in delay element 232 to give the sequence $(0, C_1, 0, C_2, 0, C_3, 0,\ldots, 0, C_N)$. The delayed signal is multiplied by the data value a_i at 234 and the result is added at 236 to the interpolated sequence to give the sequence $(C_1, a_iC_1, C_2, a_iC_2, C_3, a_iC_3,\ldots, C_N, a_iC_N)$. The gives the sequence C_a when a_I = 1, and the sequence C_b when a_I = -1. The sequence is then modulated by the carrier signal and transmitted as usual.

The corresponding receiver is shown in **FIG. 3**. Referring to **FIG. 3**, the incoming radio signal is received by antenna 302. The received signal is multiplied by the signal $\cos(\omega_c t)$ in multiplier 304 to produce an in-phase signal component. . The received signal is multiplied by the signal $\sin(\omega_c t)$ in multiplier 306 to produce a quadrature signal component. The in-phase and quadrature signal components are filtered in match filter 308, which has an impulse response matched to the transmitted pulse shape, and the resulting filtered signals are sampled by analog-to-digital converter (ADC) 310 to produce in-phase and quadrature data sequences I and Q. The sampling rate of the ADC is preferably greater than the chip rate, and is denoted by $K.R_c$, where K is bigger than or equal to 1. The n^{th} samples of the sequences are denoted by the complex baseband signal $S(n) = I(n) + iQ(n) = A(n)e^{-i\theta}$, where $i=\sqrt{-1}$ and θ is an unknown phase offset. The complex baseband signal S(n) is passed to complex delay unit 312, where the signal is delayed by an amount MT_c, where T_c is the chip period and M is the number of consecutive samples taken from each sequence during interleaving in the transmitter. The output from the complex delay unit is S(n-MK). In the sequel we consider the case M=1 without loss of generality. The complex conjugate of the signal is calculated at 314, to give the signal

$$S^*(n-k) = I(n-K) - iQ(n-K) = A(n-K).\ e^{i\theta}.$$

At multiplier 316, the signals S(n) and S*(n-K) are multiplied to give the complex product signal

$$U(n) = A(n)\ e^{-i\theta}.A(n-K)\ e^{i\theta} = A(n).A(n-K).$$

At block 318, the real part is taken to give V(n) = A(n)A(n-K). This removes any imaginary part introduced by a small mismatch between the carrier frequency in the transmitter and the receiver. The signal V(n) is then integrated at 320 and the result passed to decision logic 322.

By way of explanation, we consider the case K=1. When a bit 1 is transmitted, the current data value is $a_i=1$, the previous data value is a_{i-1}. The received signal is $I = C_a = (C_1, C_1, C_2, C_2, C_3, C_3,\ldots, C_N, C_N)$, the delayed version of I is $I'=(a_{i-1}C_N, C_1, C_1, C_2, C_2, C_3, C_3,\ldots, C_{N-1}, C_N)$, and the product of I with I' is

$$V = (a_{i-1}C_NC_1, C_1C_1, C_1C_2, C_2C_2, C_2C_3, C_3C_3, C_3C_4,\ldots, C_{N-1}C_{N-1}, C_{N-1}C_N, C_NC_N)$$

$$= (a_{i-1}C_NC_1, 1, C_1C_2, 1, C_2C_3, 1, C_3C_4,\ldots, 1, C_{N-1}C_N, 1).$$

The integration over one cycle gives

$$N + a_{i-1}C_NC_1 + C_1C_2 + C_2C_3, + C_3C_4+\ldots+ C_{N-1}C_N = N +(a_{i-1}-1)\ C_NC_1 + \varepsilon$$

where $\varepsilon = C_1C_2 + C_2C_3, + C_3C_4 + \ldots + C_{N-1}C_N + C_NC_1 = -1$ is the cyclic correlation of the PN code sequence with shift one. By carefully picking the code, we can make the product $C_NC_1 = -1$. Hence the value of the integration is $N - a_{i-1}$, which equals to N-1 or N+1 depending on the previous bit value a_{i-1}.

When the bit -1 is transmitted, the current data value is $a_i=-1$, the previous data value is a_{i-1}. The received signal is $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3, \ldots, C_N, -C_N)$, the delayed version of I is $I' = (a_{i-1}C_N, C_1, -C_1, C_2, -C_2, C_3, -C_3, \ldots, -C_{N-1}, C_N)$, The product of I with the delayed signal is

$$V = (a_{i-1}C_NC_1, -C_1C_1, -C_1C_2, -C_2C_2, -C_2C_3, -C_3C_3, -C_3C_4, \ldots, -C_{N-1}C_N, -C_NC_N)$$

$$= (a_{i-1}C_NC_1, -1, -C_1C_2, -1, -C_2C_3, -1, -C_3C_4, \ldots, -C_NC_{N-1}, -1),$$

and the integration over one cycle gives

$$-N + a_{i-1}C_NC_1 - C_1C_2 - C_2C_3, - C_3C_4 - \ldots - C_{N-1}C_N = -N + (a_{i-1}+1)\, C_NC_1 - \varepsilon,$$

where $\varepsilon = C_1C_2 + C_2C_3, + C_3C_4 + \ldots + C_{N-1}C_N + C_NC_1 = -1$ is the cyclic correlation of the PN code sequence with shift one. As discussed above, the product $C_NC_1 = -1$. Hence the value of the integration is $-N - a_{i-1}$, which equals to -N-1 or -N+1 depending on the previous bit value a_{i-1}.

The value of N is large (typically 127), so the decision logic simply compares the integration value to zero. A positive value is interpreted as a +1 bit, while a negative value is interpreted as a -1 bit. Hence the signal has been decoded without the use of a correlation. Further, the differential decoding is performed chip-by-chip, so the receiver is very robust to drift in the carrier frequency. This further reduces cost by avoiding the need for a very accurate timer or clock source. For example, if the frequency difference between the transmitter and receiver is $\Delta\omega$, the receiver signal after demodulation is

$$S(t) = A(t)\exp(-i\Delta\omega t + \theta),$$

where θ is a phase offset. The product signal is

$$U(t) = S(t)\overline{S}(t - T_c) = A(t)A(t - T_c)\exp(-i\Delta\omega T_c),$$

and the real part is

$$V(t) = A(t)A(t - T_c)\cos(\Delta\omega T_c).$$

Thus, when the product $\Delta\omega T_c$ is small, there is only a very small amplitude change. The computation can be performed using analog or digital hardware or using software running on a computer. **FIG. 4** shows an embodiment of a receiver of the invention using an analog system. In this embodiment the ADC is omitted. The discrete integration element 320 in **FIG. 3** is replaced by analog integrator 324 in **FIG. 4**. The integrator is periodically reset to zero.

A further embodiment of a transmitter is shown in **FIG. 5**. In this embodiment -1 bits are transmitted as before, but for +1 bits, the PN code sequence C is used rather than C_a. Since C is of length N while C_a is of length 2N, the data rate of this embodiment is higher. The receiver is as described above.

When a bit 1 is transmitted, the received signal is $I = C = (C_1, C_2, C_3,\ldots, C_N)$, and the real part of the product with the delayed signal is

$$V = (a_{i-1}C_NC_1, C_1C_2, C_2C_3, C_3C_4,\ldots, C_{N-1}C_N),$$

where a_{i-1} is the previous bit data value.

The integration over one cycle gives

$$C_1C_2 + C_2C_3, + C_3C_4+\ldots+ C_{N-1}C_N + a_{i-1}C_NC_1= \varepsilon + (a_{i-1} - 1)C_NC_1$$

where, as before, $\varepsilon = C_1C_2 + C_2C_3, + C_3C_4+\ldots+ C_NC_{N-1} + C_NC_1 = -1$ is the cyclic correlation of the PN code sequence with shift one. By carefully picking the code, we can make the product $C_NC_1 = -1$. Hence the value of the integration is $- a_{i-1}$, which equals to -1 or +1 depending on the previous bit value a_{i-1}.

When the bit -1 is transmitted, the current data value is a_i=-1, the previous data value is a_{i-1}. The received signal is $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3,\ldots, C_N, -C_N)$, the delayed version of I is $I'=(a_{i-1}C_N, C_1, -C_1, C_2, -C_2, C_3, -C_3,\ldots, -C_{N-1}, C_N)$, The product of I with the delayed signal is

$$V = (a_{i-1}C_NC_1, -C_1C_1, -C_1C_2, -C_2C_2, -C_2C_3, -C_3C_3, -C_3C_4,\ldots, -C_{N-1}C_N, -C_NC_N)$$

$$= (a_{i-1}C_NC_1, -1, -C_1C_2, -1, -C_2C_3, -1, -C_3C_4,\ldots, -C_NC_{N-1},-1),$$

and the integration over one cycle gives

$$-N + a_{i-1}C_NC_1 - C_1C_2 - C_2C_3, - C_3C_4 -\ldots- C_{N-1}C_N = -N +(a_{i-1}+1) C_NC_1 - \varepsilon,$$

where $\varepsilon = C_1C_2 + C_2C_3, + C_3C_4 + \ldots + C_{N-1}C_N + C_NC_1 = -1$ is the cyclic correlation of the PN code sequence with shift one. As discussed above, the product C_NC_1 =-1. Hence the value of the integration is -N - a_{i-1}, which equals to -N-1 or -N+1 depending on the previous bit value a_{i-1}.

The value of N is large (typically 127), so the decision logic simply compares the integration value to $-N/2$. A value greater than $-N/2$ is interpreted as a +1 bit, while a value less than $-N/2$ is interpreted as a -1 bit. Hence the signal has been decoded without the use of a correlation.

The first embodiment has better sensitivity than this embodiment, i.e. it is less sensitive to noise, but this embodiment has a higher data rate.

Those of ordinary skill in the art will recognize that the present invention has been described in terms of exemplary embodiments based upon use of an ideal rectangular pulse. However, the invention should not be so limited, since the present invention could be implemented using other pulse shapes. Similarly, the present invention may be implemented using general-purpose computers, microprocessor based computers, digital signal processors, microcontrollers, dedicated processors, custom circuits, ASICS and/or dedicated hard-wired logic.

Many other variations will also be evident to those of ordinary skill in the art. The embodiment disclosed can be embodied in a DSSS receiver for a location system, for instance, but it is understood that the method and apparatus of the present invention is equally applicable to all other systems using DSSS techniques.

While the invention has been described in conjunction with specific embodiments, it is evident that many alternatives, modifications, permutations and variations will become apparent to those of ordinary skill in the art in light of the foregoing description. Accordingly, it is intended that the present invention embrace all such alternatives, modifications and variations as fall within the scope of the appended claims.

What is claimed is:

CLAIMS

1. A method for generating a modulation sequence from a data value in a direct sequence spread spectrum transmitter, said method comprising:

generating a first and second code sequences by interleaving groups of M chips from a pseudo-noise sequence $C = (C_1, C_2, C_3,\ldots, C_N)$ of length N with elements $C_i = \pm 1$, said first code sequence C_a being

$$C_a(2jM+i)=C(jM+i)$$
$$C_a((2j+1)M+i)=C(jM+i)$$

and said second code sequence C_b being

$$C_b(2jM+i)=C(jM+i)$$
$$C_b((2j+1)M+i)=-C(jM+i)$$

where $j=0,\ldots,N/M-1$ and $i=1,\ldots,M$; and

selecting said modulation sequence as said first or second sequence according to the data value.

2. A method as in claim 1, wherein M=1, said first code sequence is given by $C_a = (C_1, C_1, C_2, C_2, C_3, C_3,\ldots, C_N, C_N)$ and said second code sequence is given by $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3,\ldots, C_N, -C_N)$.

3. A method for generating a modulation sequence from a data value having a value ±1 in a direct sequence spread spectrum transmitter, said method comprising:

generating a pseudo-noise sequence $C = (C_1, C_2, C_3, \ldots, C_N)$;

up-sampling the pseudo-noise sequence by a factor of two to obtain a first sequence $(C_1, 0, C_2, 0, C_3, 0, \ldots, 0, C_N, 0)$;

delaying the first sequence to give a second sequence $(0, C_1, 0, C_2, 0, C_3, 0, \ldots, 0, C_N)$;

multiplying said second sequence by the data value to obtain a third sequence; and

adding said first and third sequences to obtain said modulation signal.

4. A method for generating a modulation sequence from a data value in a direct sequence spread spectrum transmitter, said method comprising:

generating a pseudo-noise sequence $C = (C_1, C_2, C_3, \ldots, C_N)$ of length N, where $C_i = \pm 1$;

generating an interleaved code sequence C_b by interleaving groups of M chips from the pseudo-noise sequence C and the pseudo noise sequence -C as

$$C_b(2jM+i) = C(jM+i)$$
$$C_b((2j+1)M+i) = -C(jM+i),$$

where j=0,…, N/M -1 and i=1,…,M; and

selecting said modulation sequence as said pseudo-noise sequence or said interleaved sequence according to the data value.

5. A method as in claim 4, wherein M=1 and said interleaved code sequence is given by $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3, \ldots, C_N, -C_N)$.

6. A method for recovering a data value from a received signal in a direct sequence spread spectrum receiver, said received signal having a chip period T_c, a bit period T_b and being modulated by first code sequence C_a or second code sequence C_b generated by interleaving groups of M chips from a pseudo-noise sequence $C = (C_1, C_2, C_3,\ldots, C_N)$ of length N with elements $C_i = \pm 1$, said first code sequence C_a having elements

$$C_a(2jM+i)=C(jM+i)$$
$$C_a((2j+1)M+i)=C(jM+i)$$

and said second code sequence C_b having elements

$$C_b(2jM+i)=C(jM+i)$$
$$C_b((2j+1)M+i)=-C(jM+i)$$

where j=0,..., N/M -1 and i=1,...,M; said method comprising:

transforming said received signal to complex baseband signal having in-phase and quadrature components;

delaying said complex baseband signal by a time MT_c equal to M chip periods to obtain a complex delayed signal;

multiplying the complex baseband signal by the conjugate of the complex delayed signal to obtain a complex product signal;

integrating the real part of said complex product signal over the bit period T_b to obtain an integrated value; and

determining said data value from said integrated value.

7. A method as in claim 6, wherein M=1, $C_a = (C_1, C_1, C_2, C_2, C_3, C_3,\ldots, C_N, C_N)$ and $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3,\ldots, C_N, -C_N)$.

8. A method as in claim 6, wherein said determining comprises comparing said integrated value to a predetermined threshold value.

9. A method as in claim 6, further comprising sampling said baseband complex signal using an analog-to-digital converter.

10. A method for recovering a data value from a received signal in a direct sequence spread spectrum receiver, said received signal having a chip period T_c, a bit period T_b and being modulated by a code $C = (C_1, C_2, C_3, \ldots, C_N)$ or a code sequence $C_b = (C_1, -C_1, C_2, -C_2, C_3, -C_3, \ldots, C_N, -C_N)$, where $C_i = \pm 1$ and C is a pseudo-noise sequence, said method comprising:

transforming said received signal to complex baseband signal having in-phase and quadrature components;

delaying said complex baseband signal by a time equal to the chip period T_c; to obtain a complex delayed signal;

multiplying the complex baseband signal by the conjugate of the complex delayed signal to obtain a complex product signal;

integrating the real part of said complex product signal over the bit period T_b to obtain an integrated value; and

determining said data value from said integrated value.

FIG. 1A

FIG. 1B

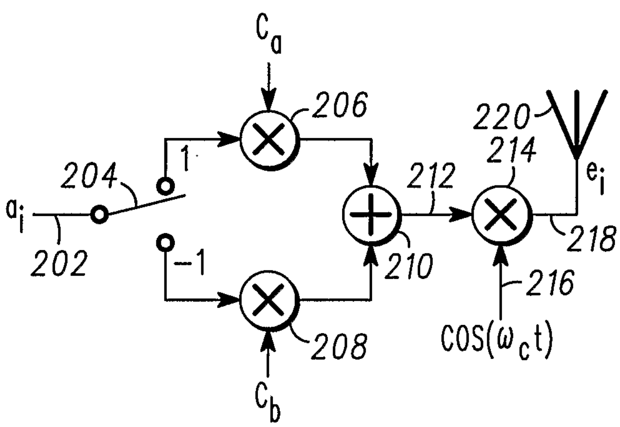


FIG. 2A

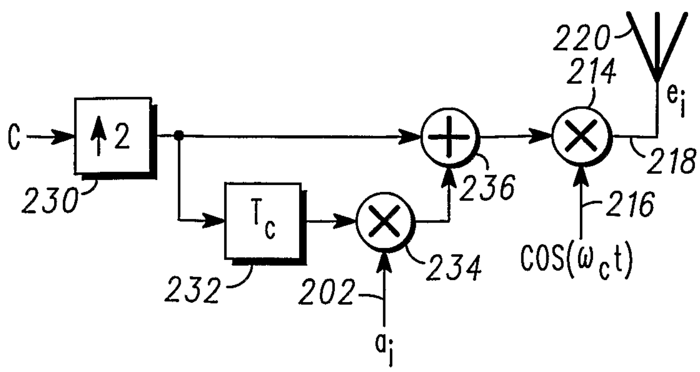


FIG. 2B

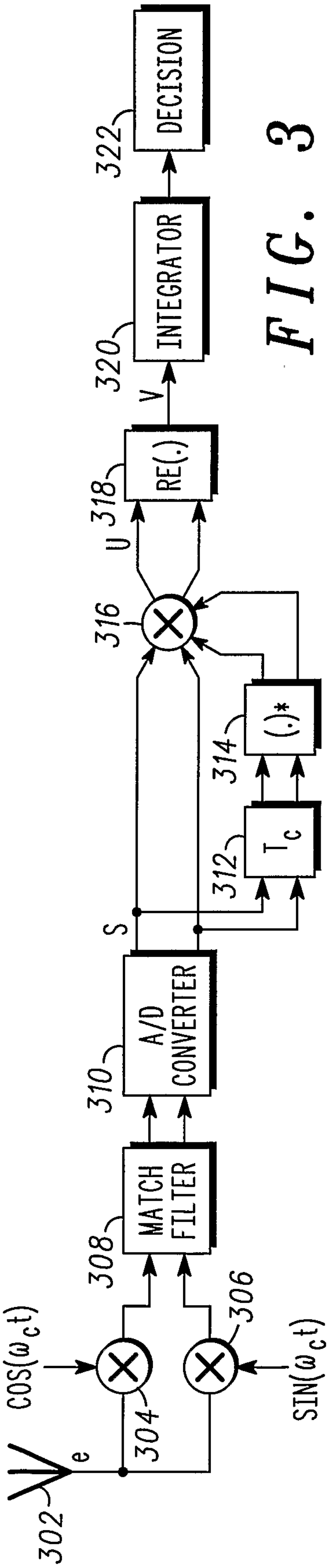


FIG. 3

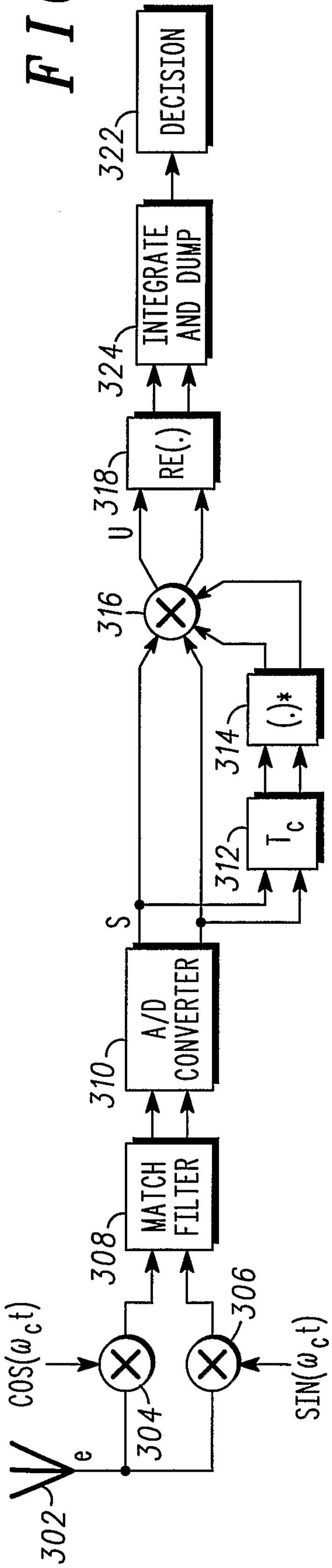


FIG. 4

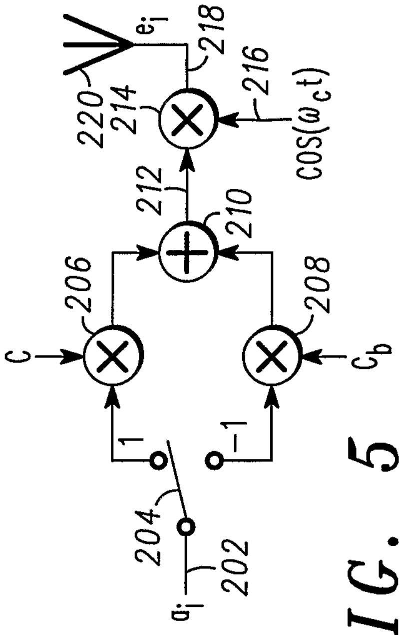


FIG. 5

INTERNATIONAL SEARCH REPORT	International application No. PCT/US02/39320

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04B 15/00; H04K 1/00; H04L 27/30
US CL : 375/140
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/140, 141, 146, 147, 149; 370/335, 342, 441

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST (code sequence interleaving, code sequence mixing, plural codes), NPL (i.e. IEEE).

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,111,911 A (SANDERFORD, JR. et al) 29 AUGUST 2000, abstract, figures 1-A, 21, 22, and related description.	6-10
A	US 5,222,075 A (RICHLEY) 22 JUNE 1993, abstract, figure 1 and the related description.	1-10
A	US 5,610,940 A (DURRANT et al) 11 MARCH 1997, figure 6 and related description.	1-5
A	US 5,412,620 A (CAFARELLA et al) 02 MAY 1995, figure 10 and related description.	6-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
05 FEBRUARY 2003	01 MAY 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MOHAMMAD GHAYOUR Telephone No. (703) 306-3034

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/39320

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-5, drawn to method for generating a modulation sequence (i.e. transmitter side).
Group II, claim(s) 6-10, drawn to method for recovering data value from a received signal (i.e. receiver side).

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: Group I (i.e. claims 1-5) is directed to a method for gnerating a modulation sequence from a data value in a spread spectrum data transmitter, whereas, Group II (i.e. claims 6-10) is directed to a method for recovering a data value from a received signal in direct sequence spread spectrum receiver.