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Weil [45] **Oct. 17, 1972**

[54] DISTANCE RANGING SYSTEM

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[21] Appl. No.: **99,429**

[52] **U.S. Cl.** ....**356/5,** 356/28, 343/7 ED, 343/7 PF, 244/3.13, 244/3.14, 244/3.16, 244/3.17, 244/3.19
[51] **Int. Cl.** **G01c 3/08,** F41g 7/00
[58] **Field of Search**..........244/3.13, 3.14, 3.16, 3.17, 244/3.19; 343/7 ED, 7 PF; 356/5, 28

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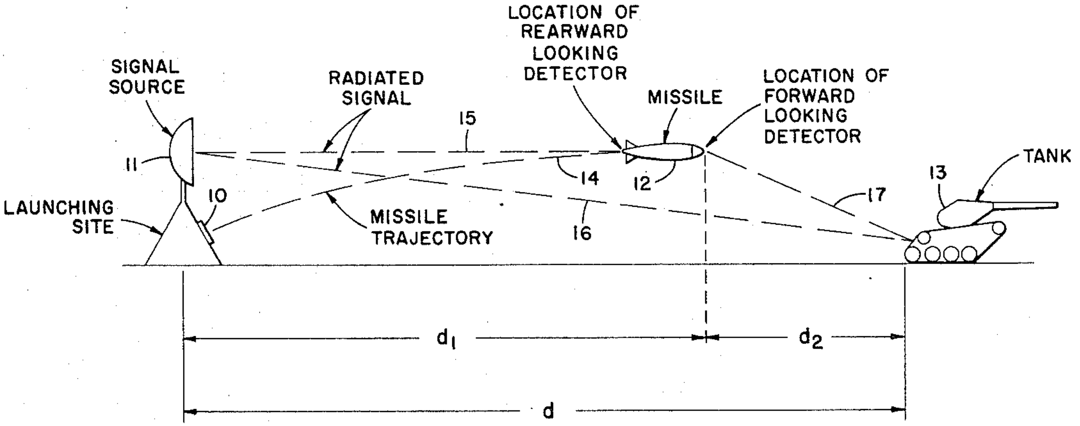
[57] **ABSTRACT**

A missile is traveling from its launch point towards an intended target. A signal source, located near the launch point, radiates a train of pulses towards said missile and towards said target. Each radiated pulse is received by the missile as a pair of pulses, one received directly from the signal source and the other received after being reflected from the target. Computing means on the missile determines the difference in arrival times of the two pulses of each pair of pulses, and then, from successive ones of such determinations, computes the distance between missile and target, missile velocity and acceleration, and finally the expected arrival time of the missile at the target; said computations being updated with the reception of each succeeding pair of pulses.

10 Claims, 10 Drawing Figures



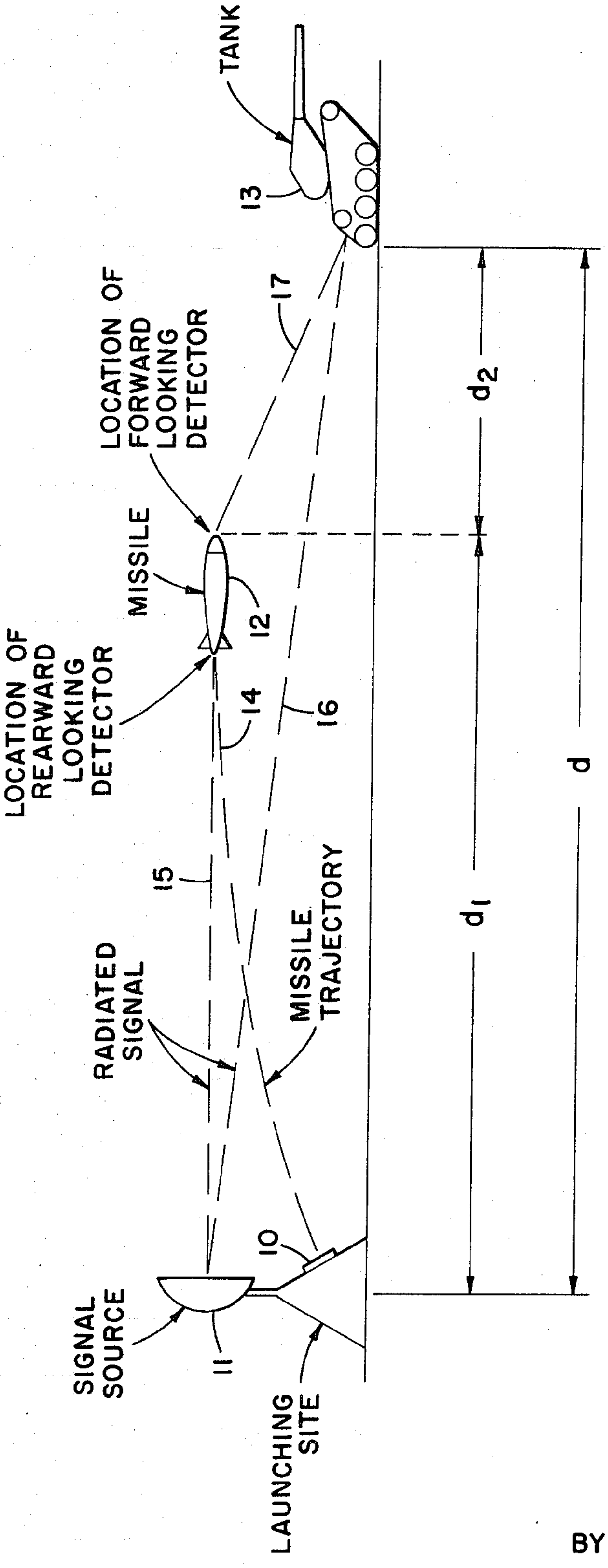


FIG 1

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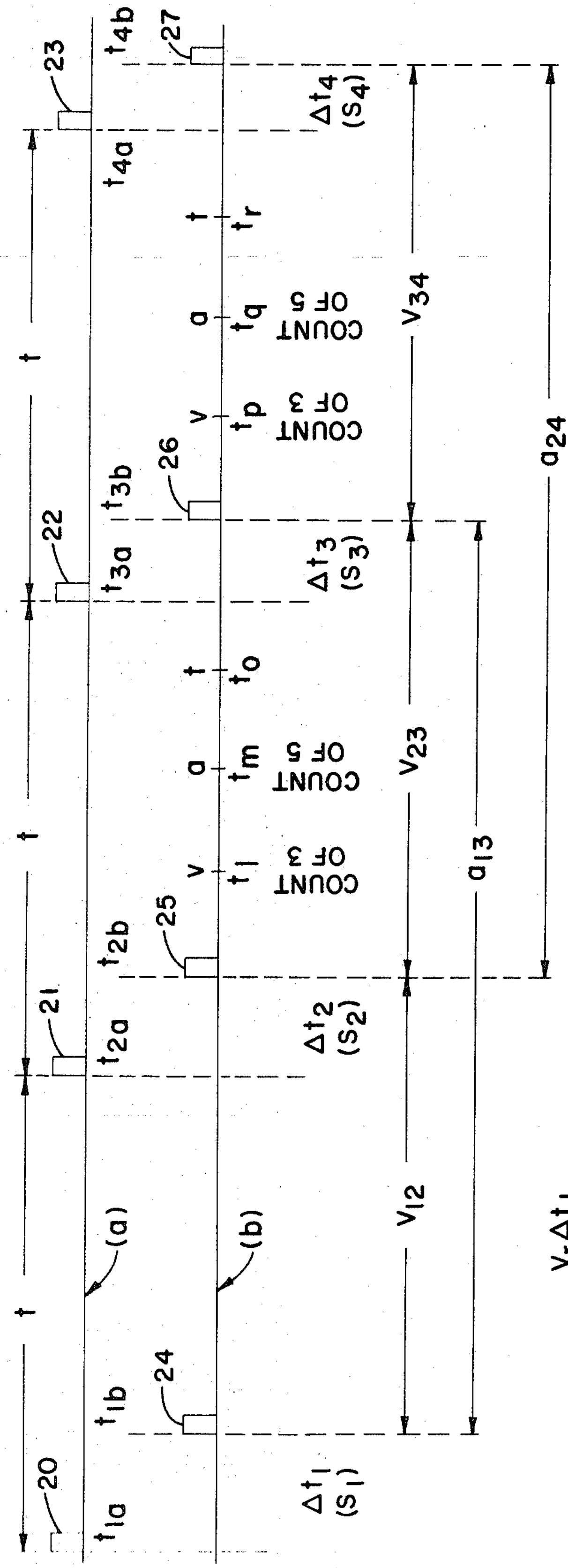

$$S_1 = \frac{V_r \Delta t_1}{2}$$

$$S_2 = \frac{V_r \Delta t_2}{2}$$

$$S_3 = \frac{V_r \Delta t_3}{2}$$

$$S_4 = \frac{V_r \Delta t_2}{2}$$

$$V_{12} = \frac{S_1 - S_2}{t}$$

$$V_{23} = \frac{S_2 - S_3}{t}$$

$$V_{34} = \frac{S_3 - S_4}{t}$$

$$a_{13} = \frac{V_{12} - V_{23}}{t}$$

$$a_{24} = \frac{V_{23} - V_{34}}{t}$$

FIG 2

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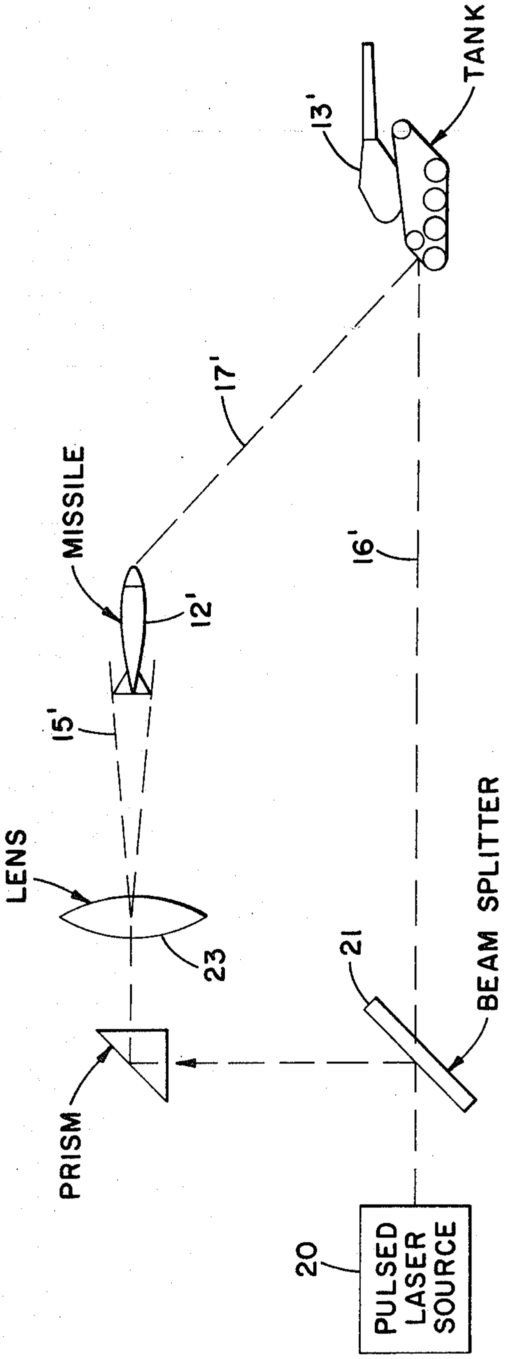

FIG 3

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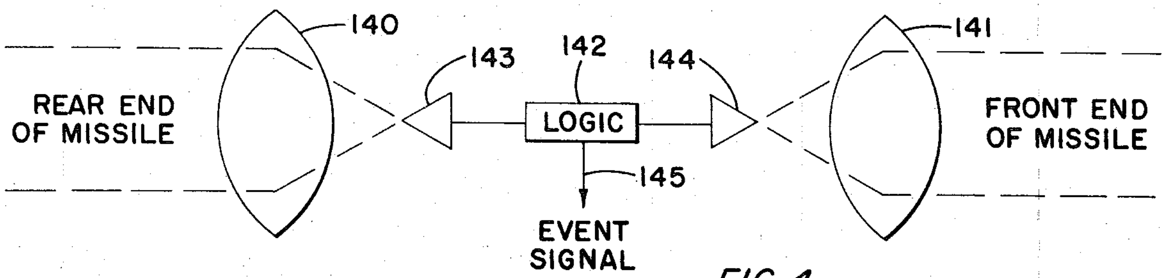

FIG 4

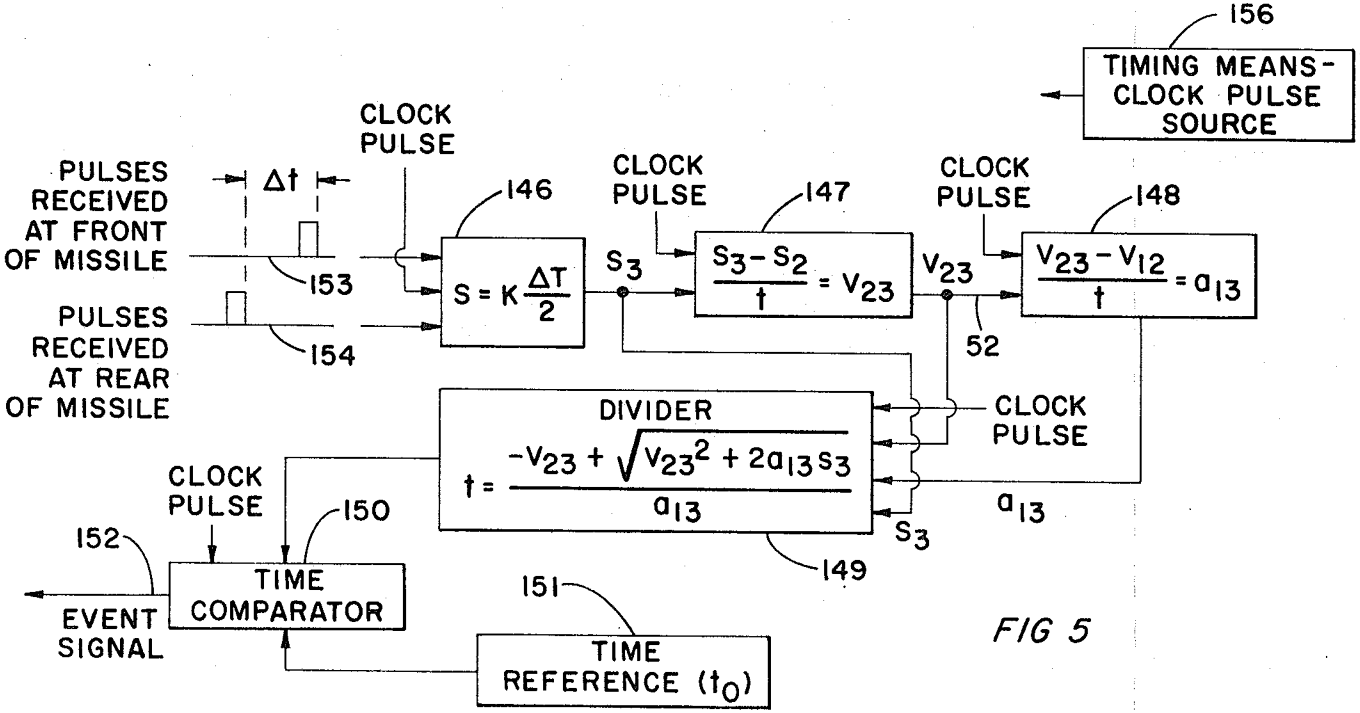

FIG 5

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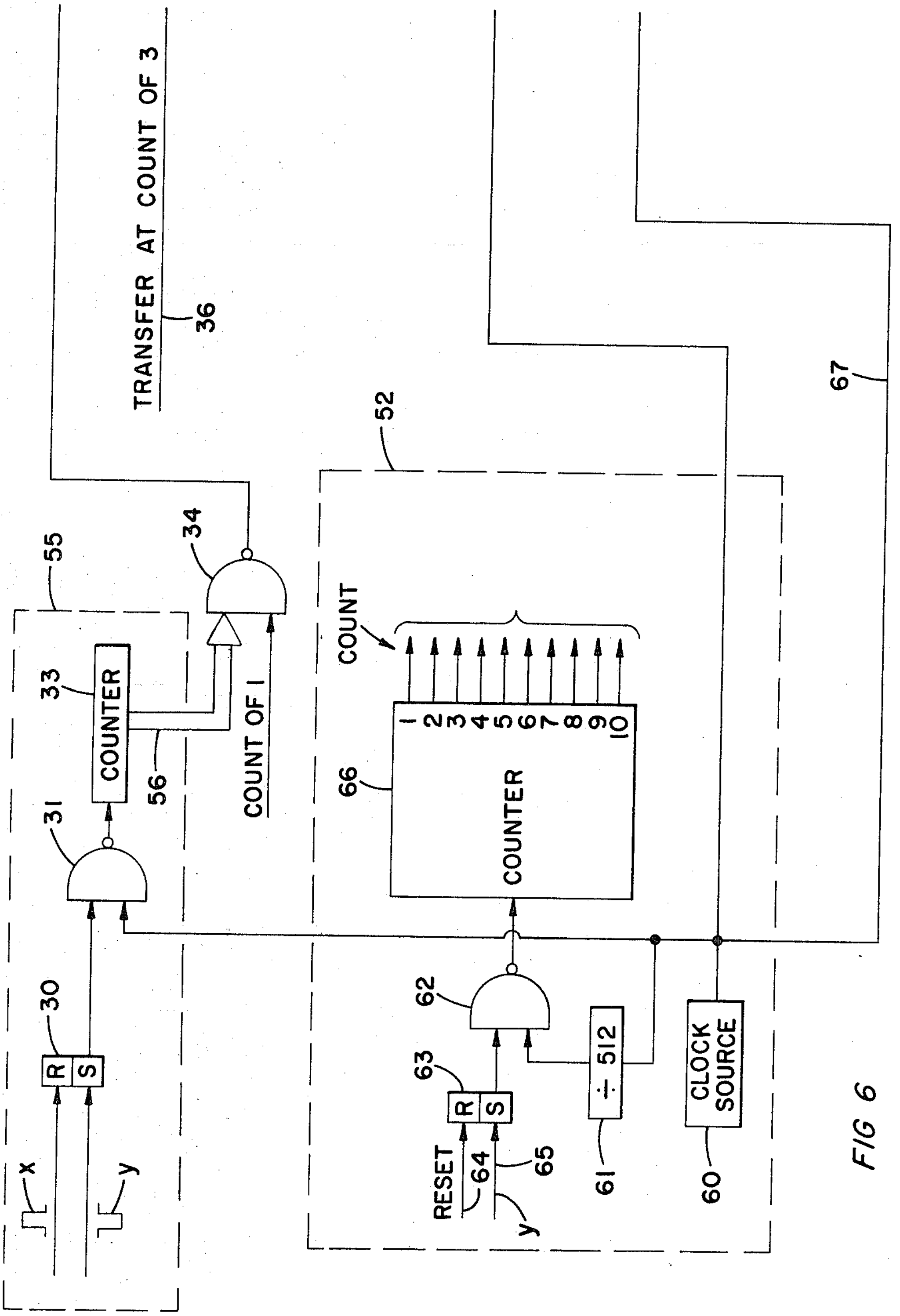

FIG 6

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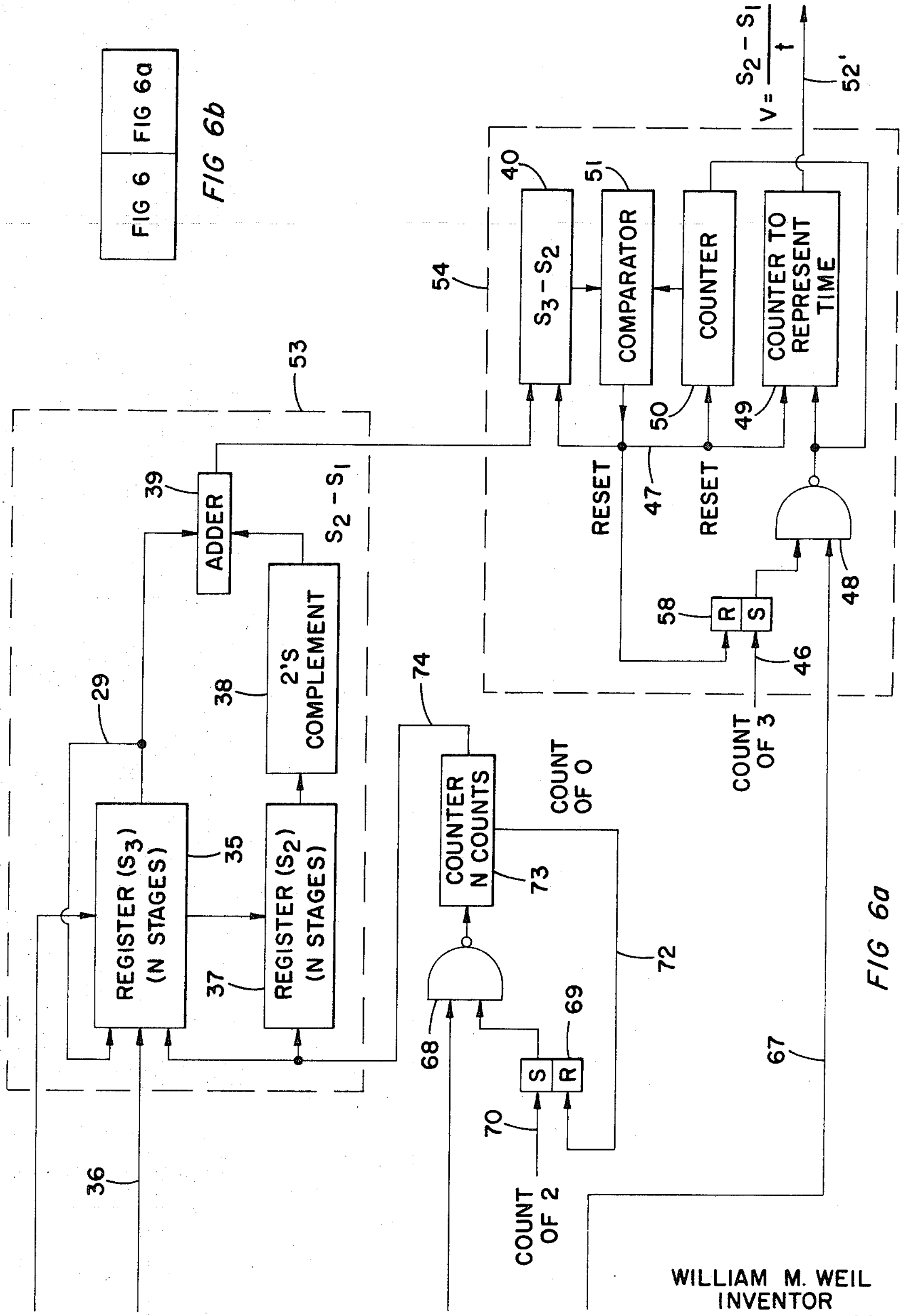

FIG 6b

FIG 6a

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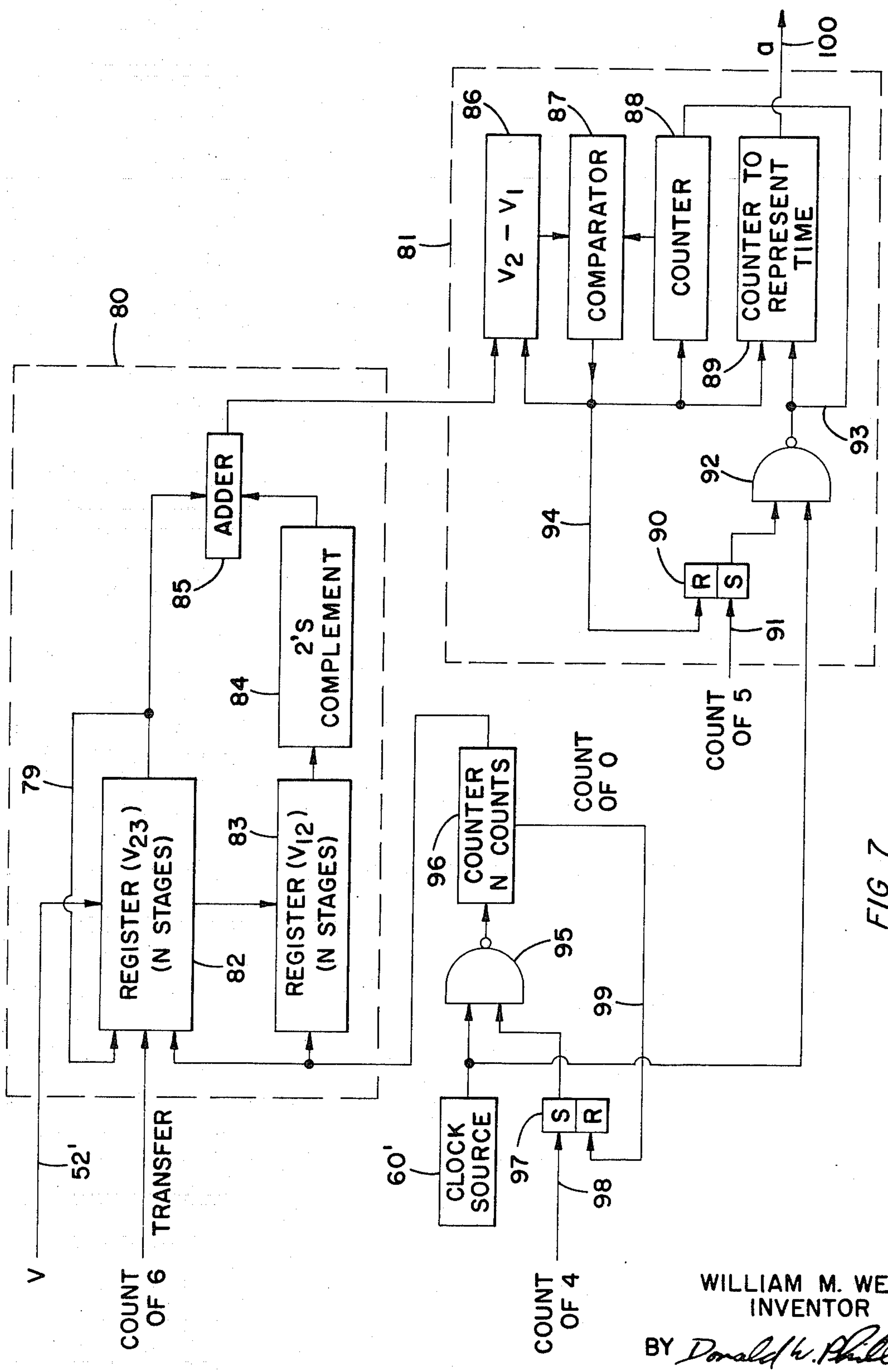

FIG 7

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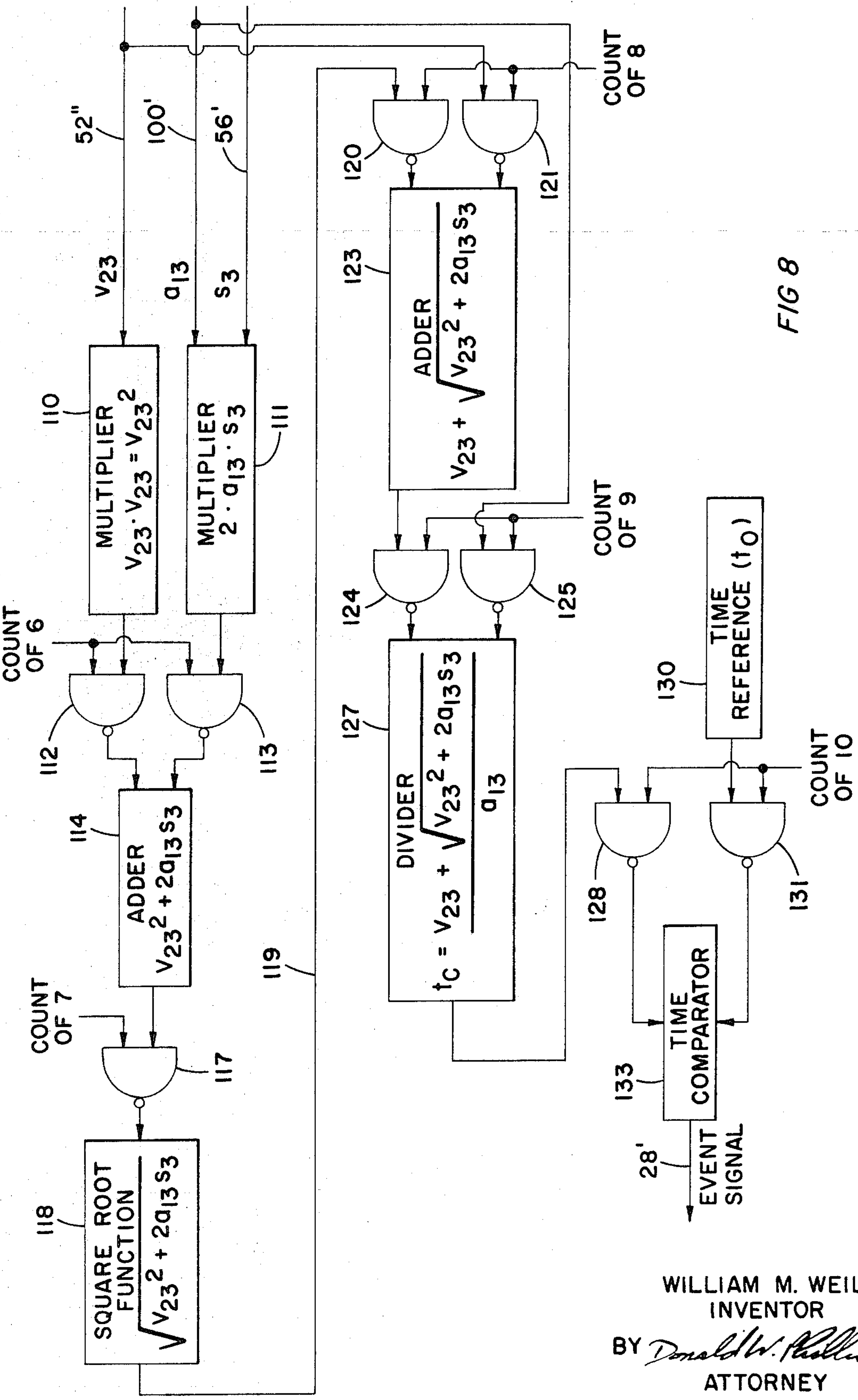

FIG 8

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DISTANCE RANGING SYSTEM

This invention relates generally to range detecting systems and more particularly to a range detecting system in which a missile contains means for receiving and detecting pulses radiated thereto both directly from a remote pulse signal generating source and also after reflection of the radiated pulses from an intended target, in order to determine the range of the target from the missile.

INTRODUCTION

There are many prior art systems for directing a missile towards an intended target. Some of such systems employ a trough of radiant energy in which the missile rides. More specifically a beam of radiant energy is directed at the target and the missile is then caused to assume a trajectory along this beam. The missile contains detecting means which restrict the missile path within said beam.

Other prior art structures flood the intended target with radiant energy and the missile then detects the radiant energy reflected from the target. By determining the maximum Doppler effect the missile can be guided towards the said intended target. Other prior art structures employ ambient light reflected from the target to guide the missile towards said target. However, none of the aforementioned prior art means provide means for determining when said missile is in close proximity to said target.

A primary object of the present invention is to provide a ranging system which determines when a missile has arrived at the intended target.

A second purpose of the invention is to provide a ranging system in which the missile is capable of detecting pulses radiated from a signal source at or near the launching site, both directly from said source and also indirectly after said pulses have been reflected from the intended target, to compute the missile's position with respect to said target.

A third aim of the invention is to provide a ranging system in which the missile contains means for computing its position from radiated pulses received directly from a source located at the launching site, and also received indirectly after being reflected form the intended target.

A fourth object of the invention is a ranging system in which the missile computes, in a continuously updating manner, the time interval remaining before said missile reaches the intended target.

A fifth aim of the invention is a ranging system in which a pulse train is radiated, from a source near the launching site, directly to the launched missile and is also radiated to the intended target and then reflected back to said missile, and in which the said missile contains means for computing its instantaneous position with respect to said intended target, and its expected time of arrival at said target.

A sixth purpose of the invention is the improvement of missile ranging systems generally.

STATEMENT OF INVENTION

In accordance with the invention there is provided a source of radiated pulses located near or at the launching site of the missile which is launched toward an intended target. Receiving and detecting means are located both at the forward end of the missile and at the rearward end of the missile, The detecting means at the rear end of the missile receives the pulses directly from the signal source while the detecting means at the front end of the missile receives the pulses reflected off the intended target. Computing means are provided within the missile to measure the time interval between each pulse received directly from the launching site and each corresponding pulse received after being reflected off the intended target.

The foregoing time measurements are proportional to the distance of the missile from the target, and therefore, from successive ones of such time measurements, the instantaneous velocity of the missile can be determined. Further means are provided to compute the instantaneous acceleration of the missile from the changes in successive computations of instantaneous velocity.

From each computed value of distance between missile and target, the velocity of the missile, and the acceleration of the missile, the computing means can then compute the instantaneous time interval required for the missile to reach the target. Minimum time interval detecting means are provided on the missile to indicate when said missile has arrived at the intended target.

STATEMENT OF DRAWINGS

The abovementioned and other objects and features of the invention will be more fully understood from the following detailed description thereof when read in conjunction with the drawings in which:

FIG. **1** is a pictorial diagram of the overall system showing the relationship between the launching site, the signal source, the missile and the intended target;

FIG. **2** is a timing diagram showing the time relation between pulses received directly from the signal source and corresponding pulses reflected off the intended target and then received by the missile;

FIG. **3** is another pictorial diagram similar to that of FIG. **1** but showing the signal source as a pulsed laser system;

FIG. **4** is a diagram showing the general arrangement of the forward and rearward located detecting means on the missile and the relation thereof to the computer logic means contained in the missile;

FIG. **5** is a generalized block diagram of the logic means of the entire system and corresponds to the single logic block of FIG. **4**;

FIGS. **6** and **6*a*** together comprise a detailed diagram of the logic employed to compute the instantaneous velocity of the system;

FIG. **6*b*** shows how FIGS. **6** and **6*a*** fit together;

FIG. **7** is a detailed diagram of the logic employed to compute the instantaneous acceleration of the missile; and

FIG. **8** is still another diagram showing the logic employed to compute the instantaneous time interval required for the missile to reach the target, and utilizing the velocity and acceleration computed by the logic diagrams of FIGS. **6**, **6*a***, and **7**.

GENERAL DESCRIPTION

Referring now to FIG. **1** the missile **12** is launched from a launching site **10** towards an intended target represented by tank **13**, the trajectory of the missile being along the dotted line **14**.

A signal source **11** is constructed to radiate a directive beam which propogates directly to the missile **12** along path **15**, and to the tank **13** along path **16**. The directive beam can consist of a series of pulses spaced an equal time distance apart.

It is apparent from FIG. **1** that a given pulse, propogating along path **15**, will be received by the missile before the same to propogating along path **16** and reflected off the tank **13**, will be received by the missile. Thus, as far as the missile is concerned, each single pulse radiated from source **11** is a pair of pulses, one pulse being received directly from source **11** and the other pulse being reflected off tank **13**. The term "pair of pulses" will be used herein to denote such a pair of received pulses.

The difference in the received times of the two pulses of each pair of pulses is indicative of the distance of the missile **12** from tank **13**. More specifically, since the velocity of radiation of the pulses is known, and the time difference between reception of the pulses is measured by logic means on the missile, to be described later herein, the distance represented by said time difference can be measured. It is apparent from FIG. **1** that since the pulse directed at tank **13** must pass beyond missile **12** and then be reflected back to the missile from tank **13**, the distance represented by said time difference is equal to twice the actual distance of missile **12** from tank **13**.

Four pairs of pulses received by missile **12** are shown in the timing waveforms of FIG. **2**. More specifically received pulses **20** and **24** originate from a single pulse radiated from signal source **11** in FIG. **1**. The pulse **20** is received directly by the rearward detector of missile **12** from signal source **11** along the path **15**, and the pulse **24** is received at the forward detector of missile **12** along path **17** after being reflected off tank **13**. PUlse **20** arrives at the missile at time t_{1a} and pulse **24** arrives at the missile at time t_{1b}.

The time differential between reception of pulses **20** and **24** is designated as Δt_1. The distance of missile **12** from tank **13** can then be represented by the following expression.

$$S_1=(Vr\,\Delta t_1/2) \qquad \text{Exp. (1)}$$

Where Vr is equal to the velocity of radiation of the pulses. Pulses **21** and **25** comprised the next occurring pair of time differentially received pulses. The pulses **22** and **26** comprise yet another pair of pulses received by the missile **12**, and the pair of pulses **23** and **27** comprise a fourth pair of such pulses. It is to be noted that the time increment Δt_1, Δt_2, Δt_3 and Δt_4 are progressively decreasing due to the fact that the missile is approaching its intended target, the tank **13** in FIG. **1**.

It can be seen then at the times t_{1b}, t_{2b}, t_{3b} and t_{4b}, calculations of the distance between missile **12** and intended target **13** can be made. Specifically the distance between missile **12** and the target **13** at times t_{2b}, t_{3b} and t_{4b} are given by the following expressions;

$$S_2=(V_r\,\Delta t_2/2) \qquad \text{Exp. (2)}$$

$$S_3=(V_r\,\Delta t_3/2) \qquad \text{Exp. (3)}$$

$$S_4=(V_r\,\Delta t_4/2) \qquad \text{Exp. (4)}$$

Since the time between each of the pulses **24**, **25**, **26**, and **27** is equal to t, the velocity of the missile can be obtained by computing the change in distance between missile **12** and target **13** during the time interval t. It is to be noted that the time intervals between the pulses **24**, **25**, **26** and **27** are not precisely equal to t since the reflected pulses will tend to move toward coincidence with the corresponding pulse in the waveform of FIG. 2a as the missile approaches very near to the target. However, since the pulses are traveling near the speed of light and the missile is traveling relatively very slowly, the time intervals Δt_1, Δt_2, Δt_3, Δt_n are all extremely small compared to the time interval t. Thus for all practical purposes the time intervals between the reflected pulses **24**, **25**, **26** and **27** are all equal to t.

Consequently at time t_{2b} the velocity of missile **12** can be computed by subtracting the distance S_2 between the missile and the target at time t_{2b} from the distance S_1 between the missile and the target at time t_{1b}, and dividing said difference by t, as shown in the following expression.

$$V_{12}=(S_1-S_2/t) \qquad \text{Exp. (5)}$$

Similarly at times t_{3b} and t_{4b} the velocity of the missile can be computed and represented by the following two expressions.

$$V_{23}=(S_2-S_3/t) \qquad \text{Exp. (6)}$$

$$V_{34}=(S_3-S_4/t) \qquad \text{Exp. (7)}$$

Next the average acceleration of the missile is determined by computing the change of velocity over a known time increment t and dividing said change of velocity by said known time increment. More specifically in FIG. **2** the acceleration a_{13} in waveform b is determined by computing the difference between the velocities V_{12} and V_{23} and dividing such difference by the time interval t, which is the time interval between the computations of the velocities V_{12} and V_{23}.

The mathematical expression for the accelerations a_{13} and a_{24} are as follows:

$$a_{13}=(V_{12}-V_{23}/t) \qquad \text{Exp. (8)}$$

$$a_{24}=(V_{23}-V_{34}/t) \qquad \text{Exp. (9)}$$

From the foregoing discussion it can be seen that computations of the distance of the missile from the target, the velocity of said missile with respect to said target and the acceleration of said missile with respect to said target, are made at every time interval t. From these various computations the length of time t_c required for the missile to reach the target, based on the calculated parameter and assuming that such parameters will remain constant, is computed. It is to be noted specifically, however, that said parameters are recalculated each time a pair of pulses is received by the missile so that the time interval required for the missile to reach the target is constantly updated. The logic for computing distance, velocity and acceleration is shown generally in FIG. **5**, which will be discussed later herein.

The radiated pulses employed in the system may be in the form of a pulsed laser beam as indicated generally in FIG. **3**. A pulse laser source **20** supplies a pulsed laser beam to a beam splitter **21** which functions to supply a portion of the beam directly to the tank **13′** along a path **16′**, from whence it is reflected back to the front end of missile **12′** via path **17′**.

The pulse laser beam also follows a path through the prism **22**, after being reflected off the beam splitter **21**, The said prism **22** redirects the beam through lens **23** and then along a path **15'** to the rear end of missile **12'**.

FIG. **4** is a very generalized block diagram of the means for detecting and processing the received pulses. MOre specifically, in FIG. **4**, the lenses **140** and **141** receive the pulsed laser beam at the rear end and the front end of the missile, respectively. The pulses are then supplied to a logic means **142** which computes the distance between missile and target, velocity, acceleration and expected time of arrival of missile at the target.

A more detailed but still quite general diagram of the logic as shown in FIG. **5**. The pulses received at the front end of the missile are received on input lead **153** and the pulses received at the rear end of the missile are supplied to the logic via input lead **154**.

In the logic of FIG. **5** the block **146** functions to compute the distance between the missile and the target after reception of each pair of pulses. The logic within the block **147** is responsive to successively determined computed distances to compute the velocity of the missile at the end of each received pair of pulses. The logic within block **148** functions to respond to consecutive computations of velocity to determine acceleration of the missile after each received pair of pulses.

The determined distance S, the computed velocity V, and the computed acceleration a, from blocks **146**, **147**, and **148** are then supplied to logic means **149** which functions to determine the time interval t_c required for the missile to reach the target, based on the latest computations of distance, velocity and acceleration.

When said time interval t_c is equal to a time reference interval t_o, which is stored in a logic block **151**, and which is compared with the computed time interval t_c in time comparator **150**, then an event signal is generated by said time comparator **150** and supplied to an output terminal **152**.

In the case were the missile and target are military in nature, the missile can be caused to detonate upon the occurrence of the event signal, thus presumably destroying the target (tank **13** in FIG. **1**).

As can be seen from FIG. **5** each of the major blocks **146** through **150** has an input labeled "clock pulse" thereto. The general purpose of such clock pulses is to step the data along from one logic block to another as the operation within each logic block is completed.

In FIG. **6** there is shown a more detailed logic diagram of the blocks **146** and **147** of FIG. **5**. More specifically in FIG. **6** the flip-flop **30**, the NAND gate **31** and the counter **33** comprise the logic elements included in block **146** of FIG. **5**. The logic within the dotted block **52** is a more detailed logic diagram of the timing means **156** of FIG. **5**. The remainder of FIG. **6** is a more detailed logic diagram of the block **147** of FIG. **5**.

Generally speaking the pair of pulses, **22** and **26**, function to set and reset flip-flop **30** to permit a number of pulses from clock source **60** to enter counter **33**; said number of pulses being proportional to the time differential between the two pulses **22** and **26**, and representing the distance S.

The subtraction of a currently determined distance S_3 from a previously determined distance S_2 is accomplished by means of the registers **35** and **37**, the two's complement logic **38**, and a binary full adder **39**. The subtrahend S_2 is stored in register **37** and the minuend S_3 is stored in register **35**. After the subtraction process is completed, S_3 is transferred to register **37** and becomes a subtrahend for the next subtract operation.

To perform the divide-by-t function, called for in block **147** of FIG. **5**, there is provided the logic within block **54** of FIG. **6***a*. Such logic includes storage register **40** in which the dividend is stored. The counter **50** and the comparator **51** function to provide the divisor. The output of counter **49** functions to provide the quotient, which is equal to V as indicated on the output terminal **52** of counter **49**. The specific operation of the division logic will be discussed in detail later herein.

The timing means for the entire system is contained within the dotted block **52** and comprises a main clock pulse source **60** from which all timing in the system is derived. More specifically, clock source **60** provides clock pulses through NAND gate **31** to counter **33** to provide an indication of computed distance. The clock source **60** also provides pulses through NAND gate **48**, when flip-flop **58** is set, to perform the division function, as will be described later herein. The clock pulse also supplies shift pulses through NAND gate **68** to the two shift registers **35** and **37** to initiate the subtract function, after two consecutive distance computations have been stored in the two registers **35** and **37**.

The sequence of the foregoing operations is controlled by the 11 outputs, **0** through **10**, of counter **66** which responds to the output of divider **61** to increment 1 count for each 512 clock pulses. For example, at the count of 1 of counter **66**, the NAND gate **34** becomes conductive to pass the contents of counter **33**, which represents distance, into storage register **35**. At the count of 2 of counter **66**, the flip-flop circuit **69** is set to permit the output from clock pulse **60** to pass through NAND gate **68** and into shift registers **35** and **37** to cause the data therein to shift serially therefrom and into the adder **39** to perform the subtract function. At the count of 3 of counter **66**, flip-flop **58** is set to energize NAND gate **48** and initiate the division function.

Referring now to FIG. **7** there is shown a more detailed block diagram of the block **148** of FIG. **5**. The diagram of FIG. **7** is quite similar to that of FIG. **6** in that a subtraction operation is performed between two binary quantities V_{23} and V_{21}, followed by a division function in which the results of the subtract operation are divided by the time t to produce the acceleration a. In FIG. **7** registers **82** and **83** are parallel input in-parallel out, and serial in-serial out registers of the same general type as registers **35** and **37** of FIG. **6**.

A two's complement function **84** is provided at the serial output of register **83** to permit the subtract operation to be done in adder **85** in a manner similar to that of the structure of FIG. **6**. The currently computed velocity V_{23} is stored in register **82** and the previously computed velocity V_{21} is stored in register **83**.

The computed difference in velocity is supplied to a dividing means **81** comprising a storage register **86** which stores the dividend $V_{23} - V_{21}$. The divisor is, in effect supplied by means of counter **88** and comparator **87**, and functions in a manner similar to the dividing function within the dotted block **54** of FIG. **6**. The quotient of the dividing function **81** of FIG. **7** appears at the output **100** of the counter **89** and represents the acceleration, *a*.

The output of counter **66** of FIG. **6** is employed to time the various operational steps of FIG. **7** in much the same manner as such output control the operational steps of FIG. **6**. More specifically the count of **4** of counter **66** functions via lead **98** to set flip-flop **97** to supply shift pulses to registers **82** and **83** to initiate the subtract operation within block **80**.

The count of **5** sets flip-flop **90** to initiate the division operation within logic block **81**. The count of **6** functions to transfer to contents of register **82** into the register **83** where it will be employed as a divisor for the next subsequent occurring computation of the acceleration a.

In FIG. **8** there is shown a detailed logic diagram of the logic block **149** of FIG. **4**. As can be seen from FIG. **8** each of the blocks performs a single arithmetic function. For example the multiplier blocks **110** and **111** function respectively to compute $V_{23}{}^2$ and the product '2*as*. The adder **114** adds together the products of the said blocks **110** and **111**. The square root function **118** then determines the square root of the output of adder **114**.

Another adder **123** sums the output of the square root function **118** plus V_{23}. The output from adder **123** is then supplied to divider **127** which divides said output by the acceleration *a*.

As will be discussed in more detail later the output of divider **127** is equal to time interval t_c needed for the missile to reach the target. Said time interval t_c is computed at the end of each pair of input pulses.

Since the missile is moving towards the target the computed time t_c becomes increasingly less in value, i.e., decreases with each computation thereof. A time comparator **133** functions to compare the computed time t_c from divider **127** with a time t_o generated in time reference **130**, and when said time intervals are equal produces an event signal on output lead **28'** which can function, for example, to detonate the missile as described in connection with FIG. **1**.

OPERATION OF THE SYSTEM

A detailed description of the operation of the system will now be set forth utilizing the timing waveforms of FIG. **2**. In FIG. **2** the train of pulses **20**, **21**, **22** and **23** are periodically received by the missile at substantially equal time intervals *t*. It is to be understood that such pulses **20** through **23** originate at the signal source **11** in FIG. **1** at equal time intervals *t*. The reception of said pulses by the missile at equal time intervals *t* is predicated upon the assumption that the missile velocity remains constant. However, even if the missile velocity should vary, the time spacing between the received pulses, for all practical purposes, is still equal to *t* since the speed of the missile is very small compared to the propagation velocity of the pulses.

Each of the transmitted pulses is also directed at a target such as tank **13** and then is reflected off the target along path **17** and back to the front end of the missile. Such reflected pulses are represented in waveform *b* of FIG. **2**. Specifically the received reflected pulses **24**, **25**, **26** and **27** correspond respectively to the pulses **20**, **21**, **22** and **23**, which are directly received by missile **12**.

The time intervals Δt_1, Δt_2, Δt_3, Δt_4 then represent the distance of the missile from the target at the time each pair of pulses is received by the missile. Such distances are represented by the four expression for S_1, S_2, S_3 and S_4 as shown in FIG. **2**. The specific logic by which the Δt time intervals can be converted into a train of pulses representing distance is best shown by the logic of FIG. **6**.

More specifically assume that the pair of pulses **22** and **26** are received by the missile,separated by a time interval Δt_3. The first received pulse **22** functions to set flip-flop **30**, thereby opening NAND gate **31** and permitting the output from clock pulse source **60** to pass therethrough and into counter **33**. A time interval later, **66** t_3, the pulse **26**, reflected off the target, arrives at the front end of the missile and functions to reset flip-flop **30**, thereby closing NAND gate **31** to cut off the supply of clock pulse to counter **33**. The counter **33** will now contain a count which is proportional to the time interval Δt_3.

It is now necessary to transfer the count contained in counter **33** to shift register **35** so that the subtract operation can be initiated Such transfer are accomplished in the following manner. The system is designed so that the count contained in counter **33** is always substantially less than a predetermined number, which in the present embodiment of the invention is assumed to be 512. Consequently, the output of the divide-by-512 circuit **61** will produce an output pulse only after the count in counter **33** is complete. Each the output pulses from divide circuit **61** passes through NAND gate **62** to cause the counter **66** to increment by one. It should be noted that while the output pulses from divide circuit **61** are continuous they will only enter the counter **66** when flip-flop circuit **63** is set. The setting of flip-flop **63** is effected by the occurrence of the corresponding received reflected pulse, such as pulse **26** of FIG. **2**. As will be discussed later the flip-flop **63** is reset at the end of a cycle of computations and before the reception by the missile of the next pair of pulses.

It is also to be noted that the counter **66** is reset to 0 at the end of the computation cycle initiated by the reception of each pair of pulses, in preparation for the computations to be made at the reception of the next pair of pulses. Thus the first output pulse from divider **61**, after the setting of flip-flop **63**, will advance the counter **66** from a count of **0** to a count of **1**, at which time the counter **33** will contain its distance representing count.

The count of **1** output of counter **66** is supplied to the input of NAND gate **34** and functions to transfer the count in the counter **33** to the register **35** which consists of N stages, where N is equal to **9** in the preferred form of the invention being described herein It is assumed that shift register **37**, which also has N stages, contains the count representing the Δt_2 time interval determined by the previous pair of received pulses **21** and **25** of FIG. **2**.

At the count of **2** of counter **66** the flip-flop **69** will be set, thereby permitting the output of clock pulse source **60** to pass through NAND gate **68** and into the shift inputs of the two registers **35** and **37**, and also into the counter **73**, whose maximum count capability is equal to N. The clock source supplied to the shift inputs of registers **35** and **37** functions to shift the contents of said registers therefrom in a serial manner and into the adder **39**, More specifically the contents of the shift register **35** is shifted directly into the adder **39** and the contents of the register **37** is shifted into adder **39** through two's complement **38**.

As is well known in the art, the use of the two's complement logic **38** and the adder **39** function to subtract the contents of register **37** from the contents of register **35**. Thus when register **35** contains a count representing a distance S_3, and resister **37** contains a count representing a distance of S_2, the output of adder **39** represents the difference $S_3 - S_2$. Such difference is supplied to a third shift register **40** in serial manner.

It is to be noted that the capacity of counter **73** is equal to the number of stages in registers **35** and **37**. Consequently when counter **73** counts to its capacity N and then recycles to 0, the flip-flop **69** is reset via the count of 0 lead **72**. It is to noted that the output of the shift register **35** has a feedback connection **29** which functions to recirculated the words shifted serially therefrom back into the input of the register **35**. Thus upon completion of the shift function the original word remains in register **35**.

Next the difference function $S_2 - S_1$ stored in register **40** is divided by the time t, as called for by the block **147** of FIG. **5**. Such division is performed in the following manner. At the count of 3 of counter **66**, the flip-flop **58** is set to permit clock pulses from clock pulse source **60** to pas through NAND gate **48** and into the time representing counter **49**, The clock pulses are also supplied through NAND gate **48** into counter **50**. The said counter **50** has a capacity which is at least equal to the greatest number to be stored in the register **40**. When said counter **50** reaches a count which is equal to the number stored in register **40** the comparator **51** function to produce an output signal on its output terminal **47**, which output signal performs several functions. Specifically said output signal resets flip-flop **58** to close NAND gate **48** and thereby cut off the supply of clock pulses to counter **49**. Also said output from comparator **51** functions to reset to **0** the shift register **40**, the counter **50**, and the counter **49**.

Referring more particularly to counter **49**, the function thereof is to produce at its output terminal **52'**, an output signal proportional to missile velocity. More specifically the counter **49** has a count capacity which is proportional to the time interval t as shown in block **147** of FIG. **5**. Each time the counter **49** fills to its capacity it produces a signal on its output terminal **52'**. The recycling of counter **49** will continue until the count in counter **50** is equal to the binary word in shift register **40** and the comparator **51** produces an output signal on its output terminal **47**, as discussed above. The number of recyclings of the counter **49** is indicated by the number of output pulses on its output terminal **52'** which in turn is directly proportional to the missile velocity V.

It is to be noted that the contents of register **35** are transferred to the register **37** by means of a count of **3** input signal supplied to lead **36** of register **35**. Thus the distance S_3 will be stored in the register **37** so that when the next distance S_4 is computed and stored in the register **35**, the next subtraction function $S_4 - S_3$ can be performed.

Referring now to FIG. **5** it can be seen that the velocity indicating signal V at the output terminal **52** of logic block **147** is supplied to the logic block **148** where the acceleration is computed. As discussed above the acceleration is computed by taking the difference between two consecutively computed velocities and dividing the difference by the time interval between said velocity computations. The detailed logic employed to compute acceleration is shown in FIG. **7** and is quite similar to the logic of FIG. **6** employed to compute velocity.

In FIG. **7** it is assumed that the velocity V_{12} has been previously computed and is stored in the shift register **83**, The velocity V_{23} has just been determined by the logic of FIG. **6** and stored in shift register **82** via lead **52'**.

It is to be understood that the completion of the computation of velocity occurs a finite time after the reception of the reflected pulse. Such finite time is required in order to perform the computations Thus in FIG. **2** the computation of V_{12} occurred a certain interval of time after the reception by the missile of reflected pulse **25**, and the computation of the velocity V_{23} occurs a finite time after the reception of reflected pulse **26**. The composition of the computation of the velocities V_{12} and V_{23} is indicated as occuring at the the count of **3** of counter **66** in the waveform of FIG. **2**, and specifically as occurring at times t_1 and t_p.

Counter **66** of FIG. **6** is also employed to control the operational steps of the logic of FIG. **7**. More specifically the counter **66** continues to count after the velocity computation has been completed and at the count of **4** will function to set flip-flop **97** of FIG. **7** via input lead **98**. The setting of flip-flop **97** opens NAND gate **95** to permit the output from clock pulse source **60'** to be supplied to the shift inputs of shift registers **82** and **83**, and also to the counter **96**. Both of the shift registers **82** and **83** have N stages therein, which is adequate to indicate the range of velocities that will be computed during the tracking of a missile from launch point to target.

The counter **96** has a capacity of N counts and performs a function similar to that of counter **73** of FIG. 6*a*.

More specifically counter **96** functions to reset flip-flop **97** after the N bit word stored in registers **82** and **83** have been serially transferred therefrom into adder **85**, thereby terminating the flow of shift pulses to registers **82** and **83**.

As in the case of the logic of FIG. **6** the adder **85** and the two's complement function **84** of FIG. **7** produce a subtract function between the contents of register **83** and register **82**. The resulting difference $V_{23} - V_{21}$ is supplied from adder **85** into shift register **86** as shown in FIG. **7**. Subsequently at the count of **5** of counter **66**, flip-flop **90** is set to open NAND gate **92** and thereby permit the output of clock pulse source **60'** to flow into time indicating counter **89** and also into counter **88**.

The counter **88** corresponds to the counter **50** of FIG. **6**. When the count in counter **88** reaches the value of the number stored in register **86** the comparator **87** will respond to produce an output signal on its output terminal **94**. Said output signal will reset to 0 the shift register **86**, the counter **88**, the counter **89**, and will also reset flip-flop **90** to block any further flow of clock pulses into counter **89** or counter **88**. Thus the division function is completed.

The counter **89** corresponds to the counter **49** of FIG. **6**. More specifically the counter **89** represents the time interval t and will recycle a number of times during the time required for the counter **88** to reach a value equal to the number contained in shift register **86**, thus in effect dividing the contents of register **86** by the count capacity of counter **89**. Each time the counter **89** fills to capacity it supplies an output pulse to its output terminal **100**. The number of such output pulses is representative of the acceleration a as defined in block **148** of FIG. **5**. As can be seen from FIG. **2** the acceleration a, computed from the velocities V_{23} and V_{12} is defined as acceleration a_{13} and is completed at the time t_q in the waveform of FIG. **2**.

Thus at time t_q the distance S_3, the velocity V_{23}, and the acceleration a_{13} have been computed, so that the estimated time of arrival of the missile at the target can be computed. More specifically the measured distance from missile to target S_3 can be expressed in terms of the measured velocity and acceleration in accordance with the following expression:

$$S_3 = \tfrac{1}{2} a_{13} t^2 + V_{23} t \qquad \text{Exp. (10)}$$

It can be seen that the expression set forth above is a quadratic expression in t having the following solution:

$$t = \frac{-V_{23} + \sqrt{V_{23}^2 + 2a_{13}S_3}}{A_{13}} \qquad \text{Exp. (11)}$$

Expression 11 is the relationship which must be solved by the logic within the block **149** of FIG. **5** to determine the expected time of arrival of the missile at the target. Reference is made to the logic of FIG. **8** which will perform the various arithmetic operations required in solving expression **11**. The velocity V_{23} is supplied to multiplier **110** which functions to square the said velocity V_{23}. The acceleration a_{13} and the measured distance S_3 are supplied to multiplier **111** via input leads **100'** and **56'** from the logic of FIGS. **6** and **7** to obtain the product $2a_{13} S_3$.

At the count of 6 of counter **66** of FIG. **6**, NAND gates **112** and **113** become conductive to pass the products of multipliers **110** and **111** into adder **114**, which produces the following sum.

$$V_{23}^2 + 2\, a_{13}\, S_3 \qquad \text{Exp. (12)}$$

At the count of 7, NAND gate **117** is opened to pass the sum computed in adder **114** to the square root function **118** which computes the square root of said sum as shown in the following expression.

$$\sqrt{V_{23}^2 + 2\, a_{13}\, S_3} \qquad \text{Exp. (13)}$$

Subsequently at the count of 8 of counter **66** of FIG. **6**, NAND gates **120** and **121** are made conductive to pass the output of the square root function **118**, and also the computed velocity V_{23}, to adder **123** which adds said two quantities together to obtain the following results

$$V_{23} + \sqrt{V_{23}^2 + 2\, a_{13}\, S_3} \qquad \text{Exp. (14)}$$

Then at the count of 9 of counter **66**, NAND gates **124** and **125** are opened to pass the sum computed in adder **123**, and also the acceleration a into divider **127**, which functions to divide the output of adder **123** by said acceleration a_{13} as shown in the following expression.

$$\frac{V_{23} + \sqrt{V_{23}^2 + 2a_{13}S_3}}{a_{13}} = t_c \qquad \text{Exp. (15)}$$

The output of divider **127** is the time interval t_c required for the missile to reach the target in accordance with the computed velocity V_{23}, and the acceleration a_{13} of the missile, at a distance S from the target. Such time interval t_c will be continuously decreasing since the missile presumably is getting increasingly closer to the target. When said computed time interval t_c decreases below a predetermined minimum t_o the missile detonates. Said predetermined minimum is determined by the time reference **130** which provides an output indicative of a small time interval t_o.

At the count of 10 of counter **66**, NAND gates **128** and **131** are caused to become conductive to supply the computed time t_c from divider **127**, and also the time interval t_o from time reference **130**, to the time comparator **133**. When said time intervals are equal or when the time interval t_c from divider **127** is less than the time interval t_o from time reference **130**, the said time comparator **128** will produce an event signal on its output lead **28'**. Such event signal can be employed to detonate the missile or to perform any other desired function.

It is to be understood that the form of the invention shown and described herein is but a preferred embodiment thereof and that various changes may be made therein and various other arrangements of logic be employed, without departing from the spirit or scope of the invention.

What is claimed is:

1. A missile ranging system for determining the position of a missile which is traveling towards an intended target and comprising:
   a signal source for radiating a train of electromagnetic pulses;
   each radiated pulse being propagated directly to said missile and also to said missile after being reflected off said intended target to form a pair of pulses;
   first receiving means positioned on said missile to receive and detect said train of radiated pulses directly from said signal source;
   second receiving means positioned on said missile to receive and detect said train of radiated pulses after said pulses have been reflected off said intended target;
   computing means constructed to measure the time difference in the arrival times of the two pulses forming each pair of pulses to compute, in a continuously updating manner, the time of arrival of said missile over said intended target.

2. A missile ranging system in accordance with claim 1 in which;
   said signal source is a pulsed laser signal source; and
   said train of radiated electromagnetic pulses are laser pulses.

3. A missile ranging system in accordance with claim 1 in which:
   said computing means is further constructed to determine the increment of distance traveled between each successive pair of received pulses from said signal source and to compute velocity and acceleration from successive measurements of said increments of distance.

4. A missile ranging system in accordance with claim 3 in which;
   said signal source is a pulsed laser signal source; and

said train of radiated electromagnetic pulses are laser pulses.

5. A missile ranging system in accordance with claim **1** in which said computing means comprises:

distance determining means for determining the distance of the missile from the intended target from the difference in arrival times at said missile of the two pulses of each pair of pulses;

velocity determining means constructed to compute the differences between successive measurements of distances from said missile to said target to determine the velocity vector of said missile towards said target;

acceleration determining means constructed to compare successive determinations of velocity of said missile to determine the acceleration vector of said missile towards said target; and

logic means responsive to the determined distance between said missile and intended target, and to the computed velocity and acceleration of said missile to determine the time interval required for said missile to reach said intended target.

6. A ranging system for determining the estimated time of arrival of a body with respect to an object destination towards which said body is moving and comprising:

a signal source located behind said moving body with respect to its forward movement and constructed to radiate a continuous train of periodically spaced pulses towards said moving body and also towards said object destination;

detecting means contained on said moving body for detecting each pair of pulses received from each radiated pulse, one pulse of said pair being received directly from said signal source and the other pulse of said pair being received after reflection off said object destination;

means for measuring the time intervals between the pulses of each pair of pulses received by said moving body;

computing means on said moving body constructed to determine the time interval required for the moving body to reach said object destination based on the measured time intervals between successively received pairs of pulses.

7. A missile ranging system in accordance with claim **6** in which;

said signal source is a pulsed laser signal source; and said train of radiated pulses are laser pulses.

8. A missile ranging system in accordance with claim **6** in which:

said computing means is further constructed to determine the increment of distance traveled between such successive pair of received pulses from said signal source and to compute velocity and acceleration from successive measurements of said increments of distance.

9. A missile ranging system in accordance with claim **8** in which;

said signal source is a pulsed laser signal source; and said train of radiated pulses are laser pulses.

10. A missile ranging system in accordance with claim **6** in which said computing means comprises:

distance determining means for determining the distance of the missile from the intended target from the difference in arrival times at said missile of the two pulses of each pair of pulses;

velocity determining means constructed to compute the differences between successive measurements of distances from said missile to said target to determine the velocity vector of said missile towards said target;

acceleration determining means constructed to compare successive determinations of velocity of said missile to determine the acceleration vector of said missile towards said target; and

logic means responsive to the determined distance between said missile and intended target, and to the computed velocity and acceleration of said missile to determine the time interval required for said missile to reach said intended target.

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