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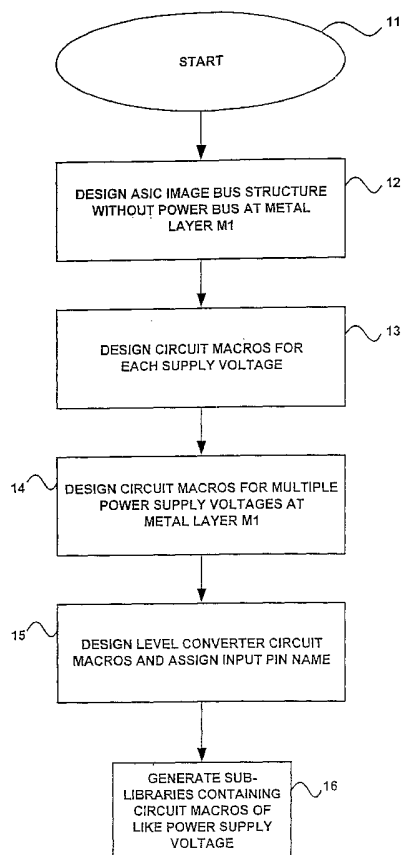
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(54) Title: ASIC DEVICE WITH MULTIPLE POWER SUPPLY VOLTAGES



(57) Abstract: A method for designing a cell-based ASIC device with multiple power supply voltages is disclosed. An ASIC chip image is made without applying power or ground buses to metal layer M1. All fast or high-power circuits are grouped together into high-power logic blocks and synthesized with high-power circuit macro libraries. All slow or low-power circuits are grouped together into low-power logic blocks and synthesized with low power circuit macro libraries. The associate power and ground buses are applied to metal layer M1 in each of the logic blocks. The logic blocks are placed on the ASIC so that different voltage groups are separated by at least one cell. The ASIC is then routed and tested before the mask is released.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ASIC Device with Multiple Power Supply Voltages

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to application specific integrated circuit (ASIC) designs in general, and in particular to a method for improving power performance in ASIC designs. Still more particularly, the present invention relates to a method for providing a cell-based ASIC device with multiple power supply voltages in order to achieve optimum power performance.

2. Description of the Related Art

Generally speaking, an application specific integrated circuit (ASIC) device has two main types of circuits, namely, primary input/output circuits and core circuits. The primary input/output circuits enable the ASIC device to communicate with other electronic components located within an electronic system. The core circuits perform various functions for which the ASIC device is intended, such as data processing, data computations, controls, etc. With the development of sub-micron technology processes, very large functions can be incorporated within a single ASIC device.

According to conventional ASIC design methods, all core circuits within an ASIC device are operated at one power supply voltage. However, in many system applications, power dissipation limits the logic functions that can be designed in an ASIC device. Since not all the parts of the logic functions within an ASIC device operate at a maximum system frequency, power supply voltage for those slower circuits that operate at a lower frequency can be reduced such that the total power dissipation of the ASIC device can be decreased accordingly. Consequently, it is desirable to provide a method for designing cell-based ASIC devices with multiple power supply voltages in order to achieve optimum power performances.

SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the present invention, an application specific integrated circuit (ASIC) chip image is made without applying power bus and ground bus to metal layer M1. All fast or high-power circuits are grouped together into a first set of logic blocks and synthesized with high-power circuit macro libraries. All slow or low-power circuits are grouped together into a second set of logic blocks and synthesized with low-power circuit macro libraries. The associated power and ground buses are applied for metal layer M1 in each of these logic blocks. The logic blocks are placed on the ASIC chip image so that different voltage groups are separated by at least one cell. The ASIC chip is then routed and tested before the mask is released.

All objects, features, and advantages of the present invention will become apparent in the following detailed written description.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention itself, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a high-level logic flow diagram of a method for developing the infrastructure of an ASIC device having multiple power supply voltages, in accordance with a preferred embodiment of the present invention;

Figure 2 is an outline of a circuit macro layout, wherein the power supply VDDA_M1 is part of the circuit macro layout;

Figure 3 is a layout of a filler cell used to fill spaces between circuit macros in a row to provide continuity for the VDDA_M1 and GND_M1 buses;

Figure 4 is a high-level logic flow diagram of a method for designing an ASIC chip having multiple power supply voltages, in accordance with a preferred embodiment of the present invention;

Figure 5 depicts a custom macro placement in an ASIC design;

Figure 6 shows the floor plan of an ASIC chip core; and

Figure 7 shows layout of logic Block A placed adjacent to layout of logic Block B in the core space of an ASIC with a unit space between them.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

A. Background

In a typical application specific integrated circuit (ASIC) chip, approximately 90% of the total power dissipation is attributed to charging and discharging of circuit and wiring capacitances. The switching power P , also known as *dynamic power*, of an ASIC chip is given by:

$$P \approx C (V^2) f S$$

1 *where* C is the internal capacitance of a circuit and circuit-to-circuit wiring capacitance, V is the
2 power supply voltage, f is the switching frequency, and S is the switching factor.

3
4 Within an ASIC chip, some logic sections must be operated at a maximum
5 frequency while the remaining logic sections can be operated at a reduced frequency without
6 degrading the overall system performance. The reduction of switching frequency can decrease
7 the total power consumption up to a certain extent because power is directly related to switching
8 frequency, as shown in the above-mentioned equation. More importantly, since power
9 dissipation in an ASIC chip is proportional to the square of the power supply voltage, the most
10 efficient way for reducing power dissipation is to reduce the power supply voltage. Hence,
11 power dissipation can be greatly reduced by lowering the power supply voltage to the logic
12 blocks that are operated at a relatively lower switching frequency.

13
14 **B. Invention**

15 Based on functional connectivity and performance requirements, a function within
16 an ASIC chip can be partitioned in various logic blocks. The logic blocks operating at a
17 relatively higher clock frequency are synthesized using a circuit macro library designed for
18 higher power supply voltages, and logic blocks operating at a relatively lower clock frequency
19 are synthesized using a circuit macro library designed for lower power supply voltages. All
20 circuits within a logic block use only one power supply voltage. Such voltage is distributed at
21 metal level M1 within the logic block, and metal level M1 is not utilized as a power supply bus
22 as part of the chip image busing structure.

23 The core area of a cell-based ASIC chip includes rows and columns of core cells,
24 where a core cell is defined to have specific width and height dimensions. The physical layout of
25 a logic function may use one or more core cells. As will be described in details, circuits for each
26 logic function are placed using a block of core cells. The block of core cell has a defined
27 boundary shape at a non-fabrication level around the core cell. One logic block area can be
28 different than another logic block area. All circuits within a logic block use only one of the
29 power supply voltages, which is distributed at metal level M1 bus within the block boundary

1 only. The logic blocks are placed in the core area of the ASIC chip in accordance with the floor
2 plan of the ASIC chip. Two logic blocks can be placed adjacent to each other or may have a gap
3 between them. Power supply voltage buses and ground buses at metal levels M2 and above are
4 placed in the core area of the ASIC chip. The ASIC physical design is checked for process
5 design rules and logical to physical connectivity. Mask data is then released to the fabrication
6 line.

7 8 C. Multiple Power Supply Voltage Infrastructure Development

9 Referring now to the drawings and in particular to Figure 1, there is depicted a
10 high-level logical flow diagram of a method for developing the infrastructure of an ASIC device
11 having multiple power supply voltages, in accordance with a preferred embodiment of the
12 present invention. Starting in block 11, an ASIC chip image bus structure without any power bus
13 at metal layer M1 is designed, as shown in block 12. Then, circuit macros are designed for each
14 power supply voltage, as depicted in block 13. Next, circuit macros are designed for multiple
15 power supply voltages at metal level M1 only, as shown in block 14. Level converter circuit
16 macros are designed and input pin names are assigned, as depicted in block 15. Finally, sub-
17 libraries containing circuit macros of like power supply voltage are generated, as shown in block
18 16.

19
20 In the prior art, when designing the library for one power supply voltage or
21 multiple power supply voltages, power bus at metal level M1 is part of the ASIC chip image bus
22 structure. In the present invention, the power supply bus at metal level M1 is part of the circuit
23 macro layout only. As an example, the layout of a Library_VDDA macro NAND3_ VDDA_1X
24 is shown in Figure 2. The interconnections between transistors that make up the NAND macro
25 function is well-known in the art. The source diffusions of p-channel transistors TP1, TP2 and
26 TP3 are connected to a power supply bus VDDA_M1 through contacts CA1 and CA2. The
27 source diffusion of n-channel transistor TN3 is connected to ground bus GND_M1 through
28 contact CA. The power buses and ground buses at metal level M1 are assigned netnames VDDA

(supply) and GND (ground). These netnames are used in the ASIC design checks, such as continuity in the voltage and ground nets, and for isolation between VDDA and VDDB nets.

Each circuit macro is designed and characterized at two or more power supply voltages, namely, VDDA, VDDB, VDDC, and so. For example, there are three sub-libraries in the main ASIC library, as follows:

1. Library_VDDA functions are designed for a high voltage VDDA;
2. Library_VDDB functions are designed for a low voltage VDDB; and
3. Library_IO functions are designed for one or two supply voltages.

Each of the above-mentioned three sub-libraries has a complete set of rules to perform ASIC logic synthesis and physical design. An example of the ASIC library organization is given below:

* Main ASIC Library *

High Power Library_VDDA	Lower Power Library_VDDB	Input output buffers Library_IO
-----	-----	-----
VDDA	VDDB	VDDB/VDDC
NAND3_VDDA_1X	NAND3_VDDB_1X	RECEIVER_VDDA_VDDB
NOR3_VDDA_2X	NOR3_VDDB_2X	DRIVER_VDDA_VDDB
ADDF_VDDA_2X	ADDF_VDDB_2X	
DFF_VDDA_3X	DFF_VDDB_3X	
FILLER1_VDDA	FILLER1_VDDB	
FILLER4_VDDA	FILLER4_VDDB	
LVCONV_VDDB_2X		

LVCONV_VDDB_2X is a level converter function macro and is used when a low supply voltage circuit drives a high supply voltage circuit. The LVCONV_VDDB_2X macro uses both low and high voltage supplies. The LVCONV_VDDB_2X macro is made part of the high supply voltage sub-library. The low supply voltage bus within the LVCONV_VDDB_2X macro is given an input pin name instead of the usual power supply netname. For example, the

low supply voltage bus can be called VDDIN instead of VDDA. In the ASIC netlist, the VDDIN nets are connected to VDDA and during the ASIC routing step, VDDIN pins are treated as signal pins and are connected to low power supply bus VDDA in the same manner as any other signal pin is wired.

The above-mentioned main library organization show only a few of the logic functions that the sub-libraries may have. Each macro entry in the sub-libraries has three qualifiers: logic function, power supply voltage, and capacitance load driving strength. The qualifiers make each of the macros and ASIC design rules for the same in the entire main library as unique entries. As will be described later, such uniqueness is necessary for performing ASIC level design checks.

A filler cell layout is shown in Figure 3. Power and ground buses in the filler cell marked as VDDA_M1 and GND_M1 are assigned net names VDDA and GND. Filler cells are used to fill unused core cell spaces in a row between circuit macros. In the same manner, physical design of other macros in the Library_VDDA can be completed. Library_VDDDB macro set and filler cells are generated using the same method as that for Library_VDDA macro set except the power bus in these macros is given VDDDB netname.

D. ASIC Logic Function Synthesis and Physical Design

With reference now to Figure 4, there is illustrated a high-level logical flow diagram of a method for designing an ASIC chip having multiple power supply voltages, in accordance with a preferred embodiment of the present invention. Starting in block 41, the circuit macros required by the ASIC chip are defined, as shown in block 42. Then, circuit macros of like power supply voltages are grouped into separate logic blocks, as depicted in block 43. For example, circuit macros that used a high supply voltage are grouped under a high-voltage supply logic block, and circuit macros that used a low supply voltage are grouped under a low-voltage supply logic block. Next, each logic block is synthesized using the sub-library corresponding to that voltage, as shown in block 44. For example, the high-voltage supply logic block is synthesized using the

high-voltage sub-library, and the low-voltage supply logic block is synthesized using the low-voltage sub-library. The appropriate power bus and ground bus must be added to each logic block at metal layer M1. Then, macro circuits are placed in logic blocks within an ASIC core, as depicted in block 45. Next, routing is performed on the ASIC core, as shown in block 46. After performing timing simulation, as depicted in block 47, and design rule check, as shown in block 48, the mask can be released, as shown in block 49.

In general, an ASIC logic function is partitioned hierarchically in functional logic blocks. In this example, high power logic blocks are synthesized using macro set in the sub-library Library_VDDA and low power logic blocks are synthesized using macro set in the sub-library Library_VDDB. The macro circuits of each logic block are placed, using ASIC design system, in a rectangular area needed to accommodate all the macros of the logic block. Each logic block has an associated name and a qualifier indicating the sub-library with which the logic block was synthesized. Similarly, the core space used by each logic block carries the name of the logic block and region type. For example, logic block Adder16_VDDA can be designed using sub-library Library_VDDA, its layout is named as Adder16_VDDA_RegionA.

E. Integration of IP Macros in an ASIC Design

Intellectual Property (IP) macros can be embedded in a cell-based ASIC design. As shown in Figure 5, an IP macro 50 is designed at power supply voltage VDDA. The boundary of IP macro 50 is indicated by a dotted line 51. Within the boundary of IP macro 50, there are power supply buses and ground buses, such as VDDA_M2, VDDA_M3, GND_M2, and GND_M3. In the same manner, IP macros designed using power supply voltage VDDB can be integrated in the ASIC design. One or more IP macros are placed in the ASIC core space in the same manner as the logic blocks configured with circuit macros from the sub-libraries.

Connections are made between the global power and ground buses and power and ground buses of IP macro 50. Vertical power and ground buses VDDA_M2, GND_M2 terminate on IP macro's horizontal VDDA_M3 and GND_M3 buses, respectively. Similarly,

global horizontal buses VDDA_M3 and GND_M3 terminate on macro's vertical VDDA_M2 and GND_M2 buses. Other vertical and horizontal VDDB_M2, VDDB_M3 terminate at the boundary of the IP macro without making a connection to the buses of IP macro 50.

F. ASIC Chip Floor Plan

With reference now to Figure 6, there is depicted a graphical illustration of a floor plan of an ASIC core. Chip area includes input/output circuit space indicated as Region C at the periphery of the ASIC chip on all four sides enclosing the core space. After the logic blocks and IP macros are placed in the ASIC core area, the core space is represented by Region A, Region B and unused space. The floor plan is based on the data flow or connectivity between all the logic blocks and IP macros in the ASIC logic function. Region A represents the space occupied by logic block or blocks designed using Library_VDDA and IP macros designed at power supply VDDA. In the same manner, Region B represents the space occupied by logic block or blocks designed using Library_VDDB and IP macros designed at power supply VDDB.

When logic block type A is placed next to a logic block type B, as shown in Figure 6, at least one unit space is left between the boundaries of these two types of blocks in the horizontal direction. The unit space is determined by the technology process rules. Such space provides isolation between the devices of logic block A connected to VDDA and devices of logic block B connected to VDDB. Such space also provides isolation between power supply buses VDDA_M1 and VDDB_M1. Logic blocks of the same type can be placed next to each other with their boundaries butted. Figure 6 also illustrates an example of how the chip area may get divided into regions A, B, C and unused core space.

G. Placement of Power and Ground Buses

After the logic blocks and IP macros have been placed in the ASIC core area, power and ground buses at metal level M2 to topmost metal level Mx are placed using a busing script. The busing script defines the width and space between the buses and also assigns netnames such as VDDA, VDDB and GND to the respective buses. The buses are continuous

1 metal strips and extend across the whole core area in the respective directions. Sections of these
2 buses at metal levels M2 and M3 are shown in logic blocks A and B of Figures 7. The busing
3 script also completes the interconnections between the VDDA buses at all metal levels including
4 M1 in the circuit macros, VDDDB buses at all metal levels and ground buses at all metal levels.

5 6 H. ASIC Global Routing

7 After the placement and power busing, the routing step can be completed with
8 well-known techniques. The routing step also includes the routing between the primary input
9 and output and core circuits.

10 11 I. ASIC Design Checks

12 Normal design rules checks are utilized. Since the multiple power supply buses
13 had their unique netnames, logical to physical checks will flag any open or short errors
14 associated with the power and ground nets.

15
16 As has been described, the present invention provides a method for designing a
17 cell-based ASIC device with multiple power supply voltages in order to achieve optimum power
18 performance. Although the present invention is described with the use of two power supply
19 voltages, the same concept can be extended to more than two power supply voltages.

20
21 It is also important to note that although the present invention has been described
22 in the context of a fully functional computer system, those skilled in the art will appreciate that
23 the mechanisms of the present invention are capable of being distributed as a program product in
24 a variety of forms, and that the present invention applies equally regardless of the particular type
25 of signal bearing media utilized to actually carry out the distribution. Examples of signal bearing
26 media include, without limitation, recordable type media such as floppy disks or CD ROMs and
27 transmission type media such as analog or digital communications links.

1 While the invention has been particularly shown and described with reference to a
2 preferred embodiment, it will be understood by those skilled in the art that various changes in
3 form and detail may be made therein without departing from the spirit and scope of the
4 invention.

CLAIMS

What is claimed is:

1. A method for designing a cell-based application specific integrated circuit (ASIC) device, said method comprising:
 - reserving metal layer M1 power supply bus when developing a bus structure ASIC device image;
 - grouping circuit macros of like power supply voltages into respective logic blocks;
 - synthesizing said logic blocks using sub-libraries corresponding to voltages for said logic blocks; and
 - adding power supply bus for said supply voltage to metal layer M1 in said logic blocks.
2. The method of Claim 1, wherein said method further includes separating said logic blocks of different voltages via a filler cell.
3. The method of Claim 1, wherein one of said logic blocks contains a custom intellectual property macro.
4. The method of Claim 1, wherein said method further includes utilizing a level convertor having multiple power supply voltages.
5. A computer program product residing on a computer usable medium for designing a cell-based application specific integrated circuit (ASIC) device, said computer program product comprising:

1 program code means for reserving metal layer M1 power supply bus when
2 developing a bus structure ASIC device image;

3
4 program code means for grouping circuit macros of like power supply voltages
5 into respective logic blocks;

6
7 program code means for synthesizing said logic blocks using sub-libraries
8 corresponding to voltages for said logic blocks; and

9
10 program code means for adding power supply bus for said supply voltage to metal
11 layer M1 in said logic blocks.

12
13 6. The computer program product of Claim 5, wherein said computer program product
14 further includes program code means for separating said logic blocks of different voltages via a
15 filler cell.

16
17 7. The computer program product of Claim 5, wherein one of said logic blocks contains a
18 custom intellectual property macro.

19
20 8. The computer program product of Claim 5, wherein said computer program product
21 further includes program code means for utilizing a level convertor having multiple power
22 supply voltages.

23
24 9. A system for designing a cell-based application specific integrated circuit (ASIC) device,
25 said system comprising:

26
27 program code means for reserving metal layer M1 power supply bus when
28 developing a bus structure ASIC device image;

1 program code means for grouping circuit macros of like power supply voltages
2 into respective logic blocks;

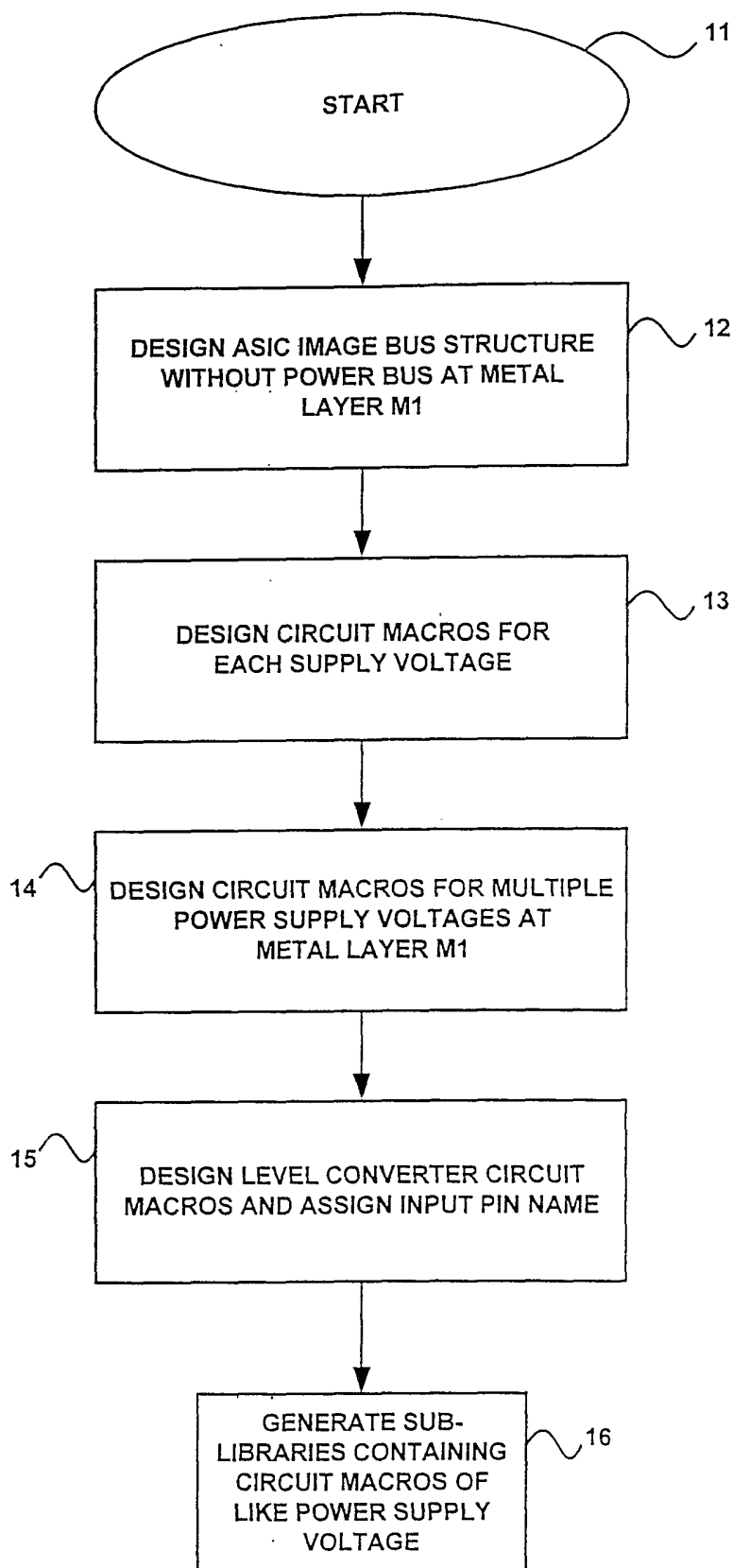
3
4 program code means for synthesizing said logic blocks using sub-libraries
5 corresponding to voltages for said logic blocks; and

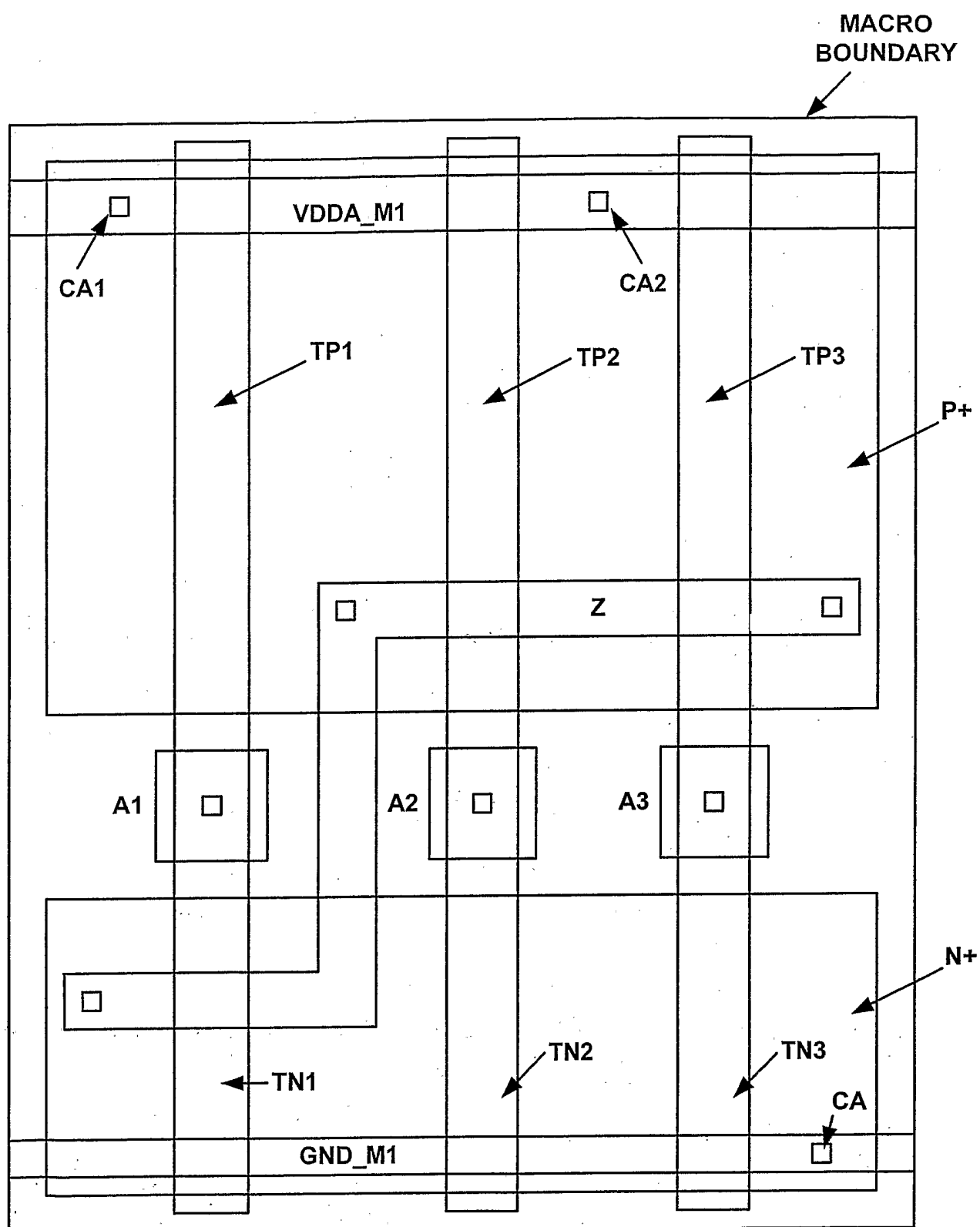
6
7 program code means for adding power supply bus for said supply voltage to metal
8 layer M1 in said logic blocks.

9
10 10. The system of Claim 9, wherein said system further includes means for separating said
11 logic blocks of different voltages via a filler cell.

12
13 11. The system of Claim 9, wherein one of said logic blocks contains a custom intellectual
14 property macro.

15
16 12. The system of Claim 9, wherein said system further includes means for utilizing a level
17 convertor having multiple power supply voltages.

*FIG. 1*

*FIG. 2*

MACRO
BOUNDARY

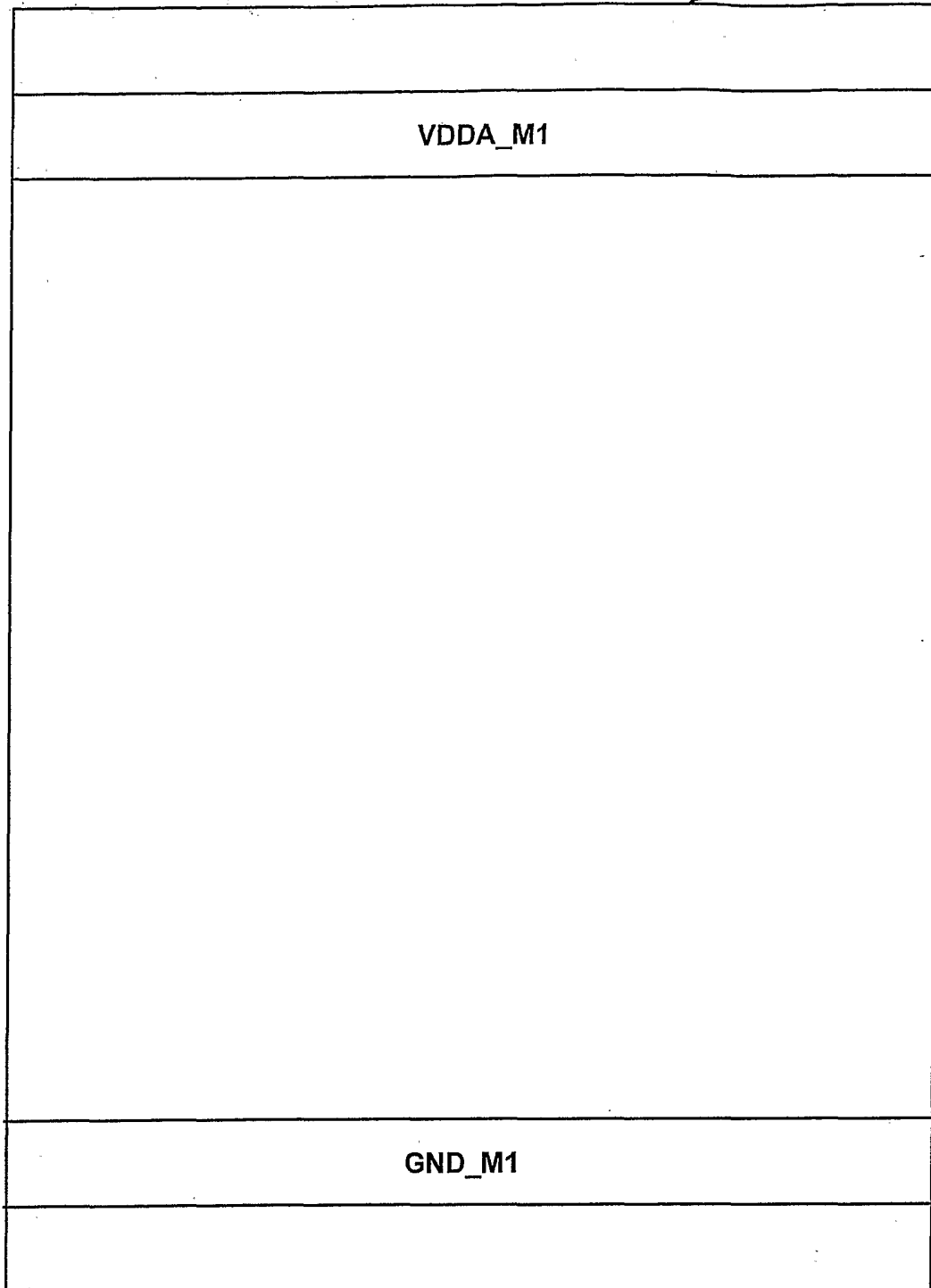


FIG. 3

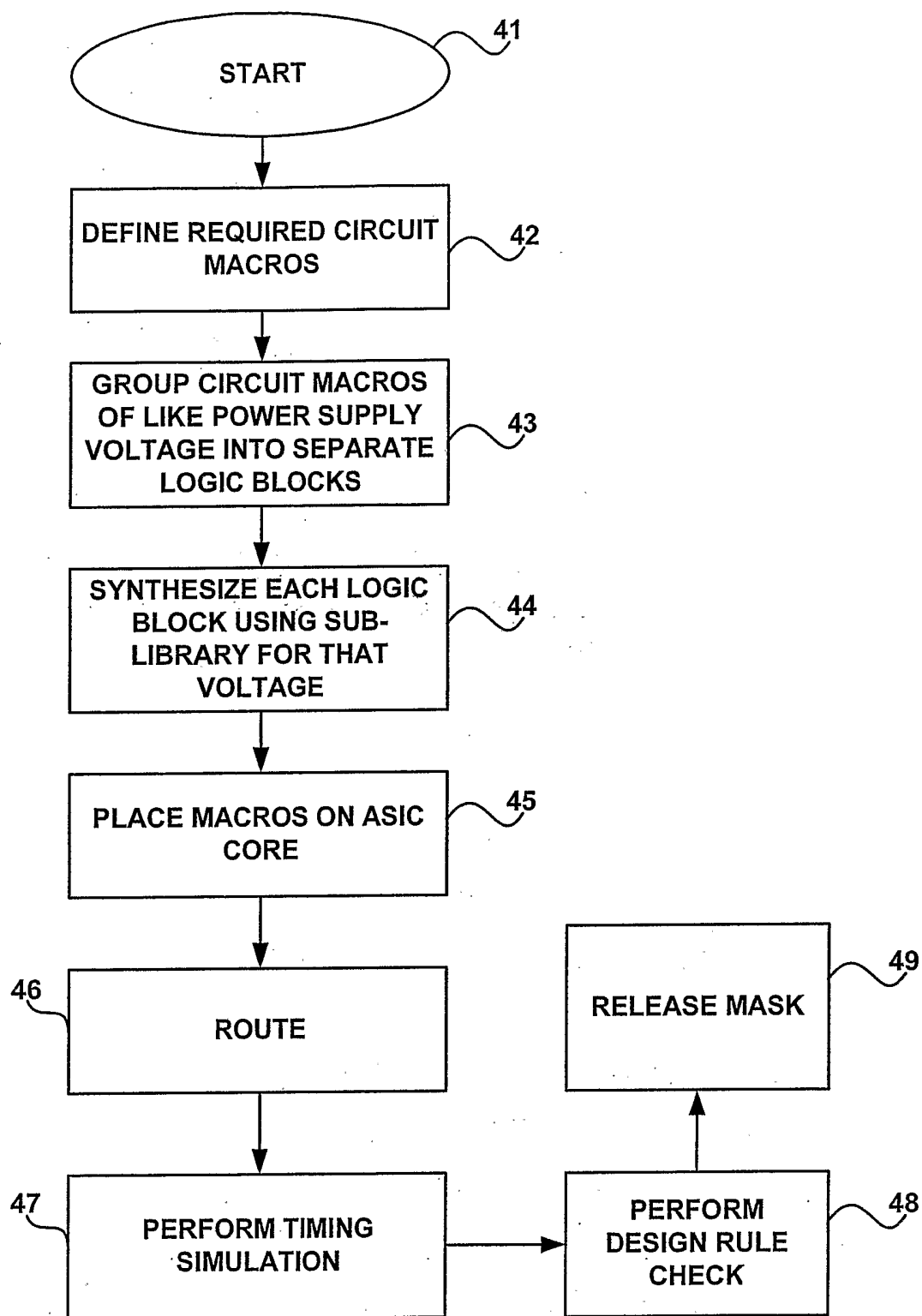
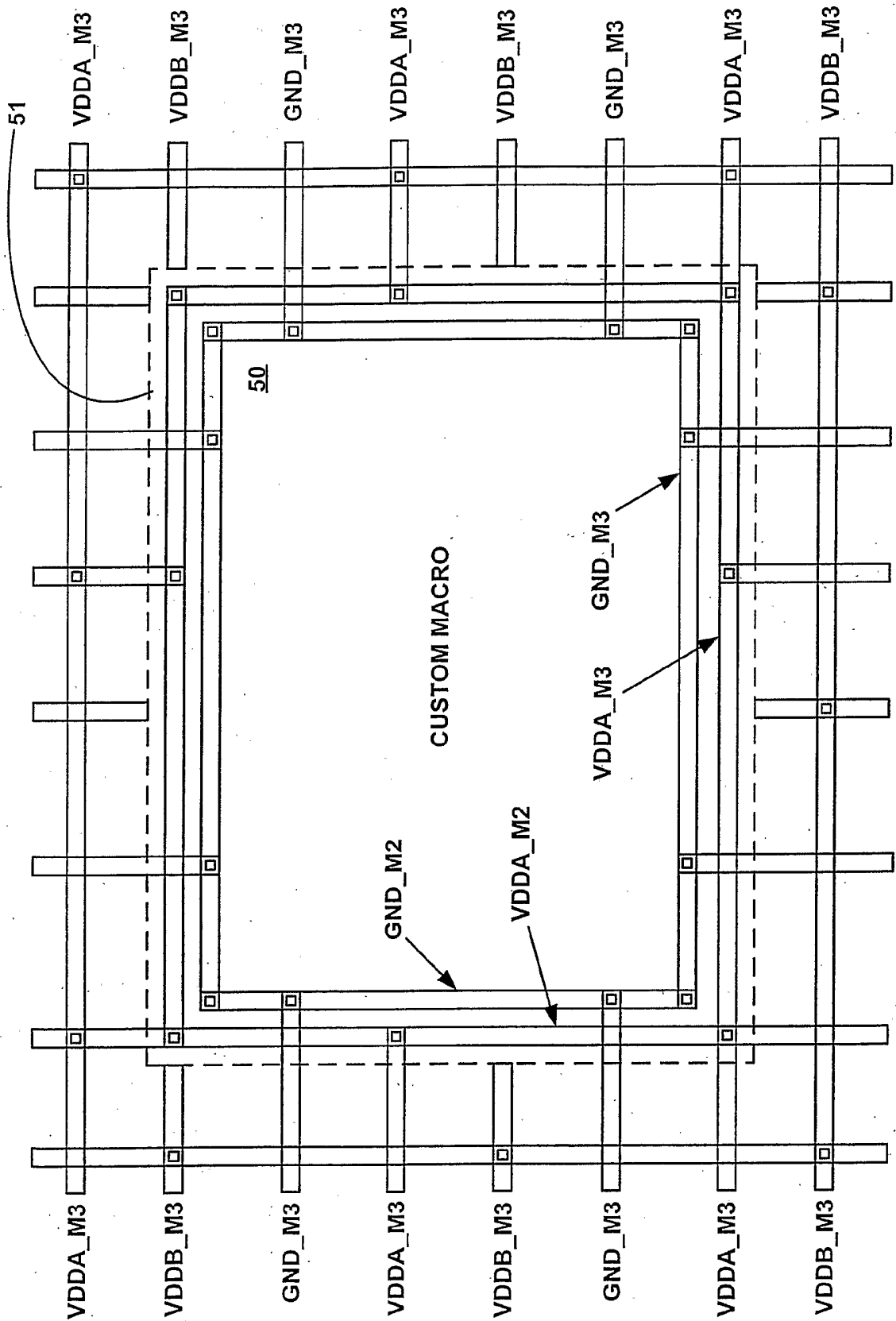
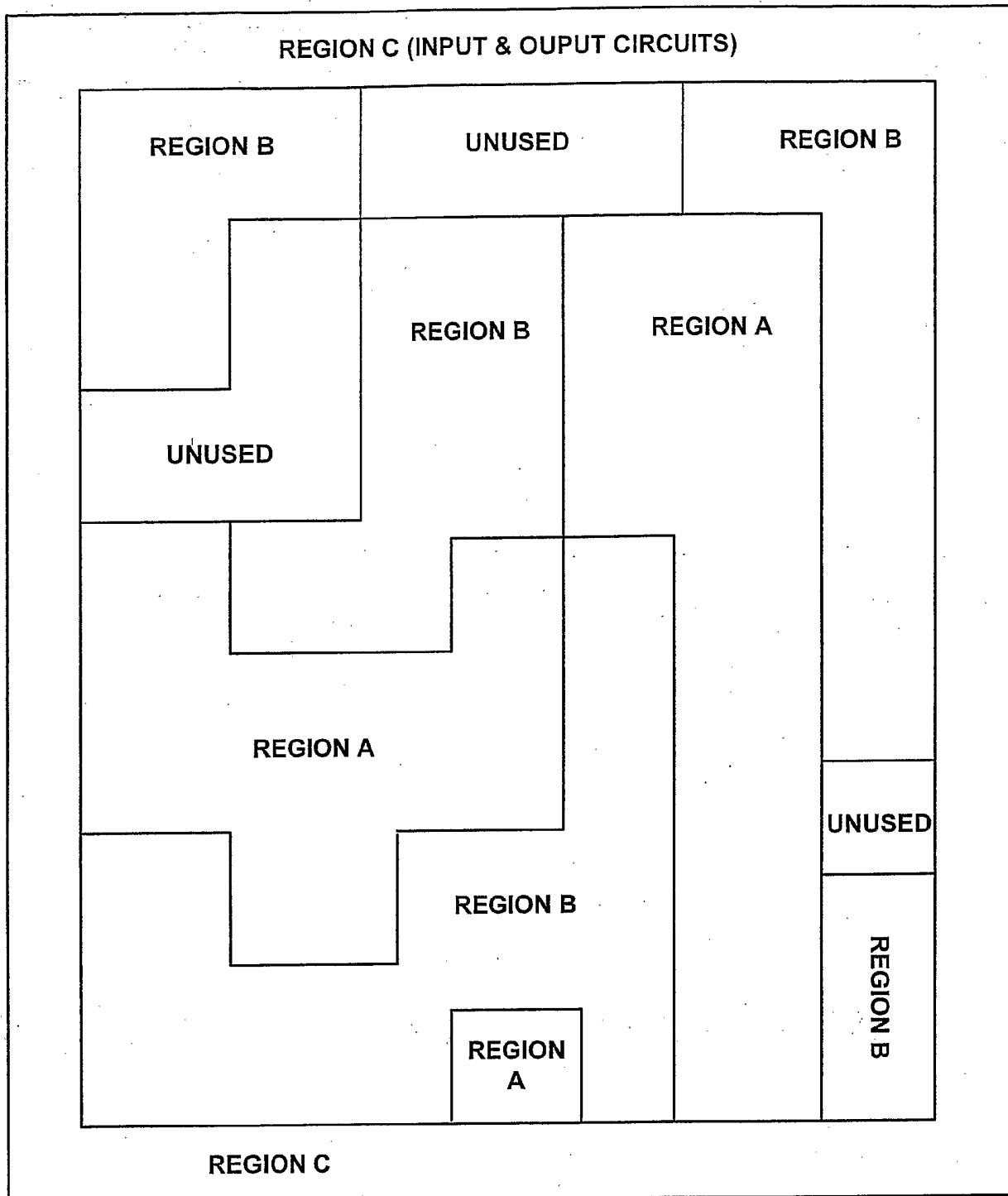


FIG. 4



VDDB_M2 VDDA_M2 GND_M2 VDDB_M2 VDDA_M2 GND_M2 VDDB_M2 VDDA_M2 *FIG. 5*

*FIG. 6*

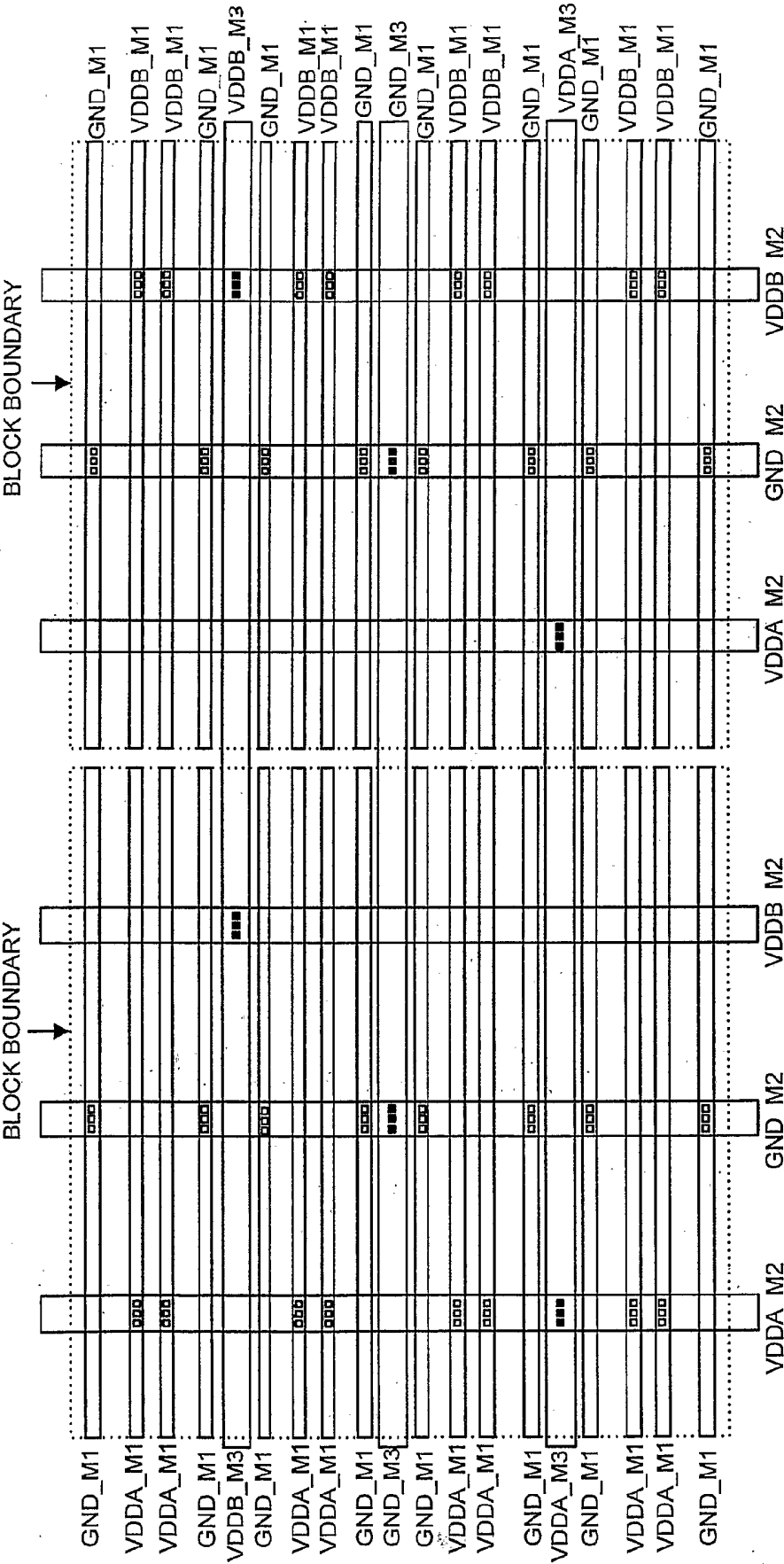


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/40768

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : g06f 17/50

US CL : 716/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 716/1,7,8,9,16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IEEE XPLORE; GOOGLE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,710,621 B2 (DEVLIN et al.) 23 March 2004 (23.03.2004), cols. 1 - 7, Figures 1 -5	1-12
X	Pub. No. US 2003/0101307 A1 (GEMELLI) 29 May 2003 (29.05.2003), paragraphs 0002 and 0003	3, 7 and 11
X	US 6,091,090 (GHEEWALA) 18 July 2000 (18.07.2000), col. 2, lines 8 - 13	1-12
Y,E	US 6,861,753 B1 (Chen et al.) 01 March 2005 (01.03.2005), Figs. 1-3, col. 1, lines 9-51.	1-12
Y	Pub. No. US 2004/0143797 A1 (Nguyen et al.) 22 July 2004 (22.07.2004), Fig. 10, Abstract, Paragraphs 0041-0048	1-12
Y	Pub. No. US 2002/0013931 A1 (Cano et al.) 31 January 2002 (31.01.2002) Figs. 5,13A-13E, paragraphs 0032,0037	1-12



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
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Date of the actual completion of the international search

31 August 2005 (31.08.2005)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US04/40768

Continuation of Item 4 of the first sheet:
The title is 13 words long.

NEW TITLE: ASIC Device with Multiple Power Supply Voltages

Continuation of B. FIELDS SEARCHED Item 3:

EAST; ALL DATABASES; SEARCH TERMS: "M1 or METAL 1 layer", "power supply", "bus structure", "macros", "logic blocks",
"reserv*", "multiple".