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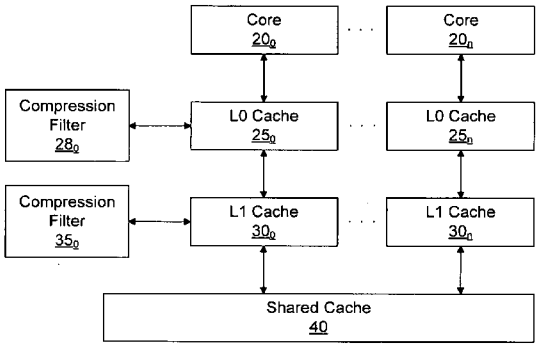


FIG. 1

(57) Abstract: In one embodiment, a cache memory can store a plurality of cache lines, each including a write-set field to store a write-set indicator to indicate whether data has been speculatively written during a transaction of a transactional memory, and a read-set field to store a plurality of read-set indicators each to indicate whether a corresponding thread has read the data before the transaction has committed. A compression filter associated with the cache memory includes a first filter storage to store a representation of a cache line address of a cache line read by a first thread of threads before the transaction has committed. Other embodiments are described and claimed.

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HYBRID CACHE STATE AND FILTER TRACKING OF MEMORY OPERATIONS DURING A TRANSACTION

Background

[0001] As the size and complexity of modern processors and software increases, the demands upon transactional memory have steadily increased. Transactional memory (TM) systems track speculative reads and buffer speculative writes that occur during the transaction to provide the illusion of atomicity. The transactional read-set refers to the set of memory addresses that are read but not written during the execution of a transaction. The transactional write-set refers to the set of memory addresses that are written during the execution of a transaction. The memory addresses in the read-set and write-set are typically of the same granularity as the underlying coherency units in the memory system (usually cache lines).

[0002] When applied to multicore processors, there is an increasing demand upon the transactional memory system to successfully manage the actions that occur amongst the distribution of caches present in the core. The increase in demand has led to an increased size in structures to support transactional memory, however these steadily become more inefficient as structure size increases. Another problem facing a programmer is that while these methods exist for the management of transactional memory and the processes by which to track their functions, these methods are unable to efficiently manage the volume of data present in current devices.

Brief Description of the Drawings

[0003] FIG. 1 is a high level block diagram of a processor in accordance with an embodiment of the present invention.

[0004] FIG. 2 is a block diagram illustrating further details of a cache hierarchy in accordance with an embodiment of the present invention.

[0005] FIG. 3 is a block diagram of a process in accordance with one embodiment of the present invention.

[0006] FIG. 4 is a flow diagram of operations within a transaction in accordance with an embodiment of the present invention.

[0007] FIG. 5 is a block diagram of a processor in accordance with an embodiment of the present invention.

[0008] FIG. 6 is a block diagram of a processor core in accordance with one embodiment of the present invention.

[0009] FIG. 7 is a block diagram of a multicore processor in accordance with another embodiment of the present invention.

[0010] FIG. 8 is a block diagram of a system in accordance with an embodiment of the present invention.

Detailed Description

[0011] In various embodiments, a transactional memory implementation can be provided within a processor such as a multicore processor having multiple levels of a cache hierarchy. More specifically, embodiments can provide read-set and write-set tracking state that can efficiently propagate through this cache hierarchy. To this end, one or more levels of the cache memory may provide for storage of read-set and write-set tracking information as state or status information within cache lines accessed during a transaction. Such status information can propagate throughout the levels of the cache hierarchy.

[0012] However, one or more such levels may not include this state information. To enable correct tracking even in the absence of such state information in one or more levels, a compression filter can be associated with at least certain levels of the cache hierarchy such that any cache lines including read-set tracking state information evicted from such cache level can have an entry stored in a corresponding compression filter to thus enable correct transaction operation. This compression-based filter thus maintains read-set tracking for all cases where a cache line is displaced from a cache level where the read-set status information cannot be propagated. In addition, embodiments may make greater and more efficient use of cache space for maintaining transactional write-set data, as

embodiments may provide a storage preference for cache lines associated with write-set data, as will be described herein.

[0013] Referring now to FIG. 1, shown is a high level block diagram of a processor in accordance with an embodiment of the present invention. As shown in FIG. 1, processor 10 may be a multicore processor including a plurality of cores 20_0-20_n (generically core 20). Each core may include various structures including front end units, execution units, and retirement units. To provide for temporary storage of information, each core 20 may be coupled to a low level cache, e.g., a level 0 (L0) cache 25_0-25_n (generically cache 25). Each cache line in the cache may store various information, including status information, tag information, and data. In various embodiments, the status information can include transaction indicators, such as the above-described read-set and write-set indicators. In turn, this cache level can be coupled to a next higher cache level, e.g., a level one (L1) cache 30_0-30_n (generically cache 30). This cache level can be further from the core and may provide for storage of greater amounts of information. In turn, this level of cache memory can be coupled to a shared cache 40, which may be shared by all cores within the processor. Note that in various implementations, these caches can be dedicated data caches, dedicated instruction caches, or combined instruction-data caches. Furthermore, while not shown for ease of illustration, understand that intermediate storage between these cache levels, such as fill buffers, write back buffers, and victim caches, may also be present.

[0014] As further seen in FIG. 1, at least certain levels of the cache hierarchy may be associated with a corresponding compression filter. Shown in the embodiment of FIG. 1 are compression filters 28_0 and 35_0 (similar filters may be associated with other caches). Each of these filters may in an embodiment be Bloom filter configured to store read-set information (such as a hash value of a cache line address) when a cache line including information of a transaction is to be evicted to another cache level that does not provide for the storage of the status information described above. In other embodiments, each cache level may have a compression filter associated with it, regardless of the read and write-set status support of a next level in the hierarchy. For example, an exclusive L1/L2 hierarchy with dead block

prediction and the transaction support described herein at both levels may include a filter at the L1 cache to hold blocks identified by the predictor as dead, instead of pushing them to the L2 cache.

[0015] Referring now to FIG. 2, shown is a block diagram illustrating further details of a cache hierarchy in accordance with an embodiment of the present invention. As shown in FIG. 2, cache hierarchy 100 may include multiple levels of a cache memory, along with certain intermediate structures and a compression filter as described herein. In the embodiment shown in FIG. 2, a lowest level cache may be an L1 cache memory 110 which can include a plurality of cache lines 115_0-115_n. Cache memory 110 may support storage of state information associated with read and write-sets. Specifically as seen, cache line 115_0 includes a read-set field 116_0 which may include a plurality of read-set indicators, e.g., a bit for each thread to indicate whether the corresponding thread has read the data of the corresponding cache line during a transaction. Field 116_1 may be a write-set indicator to indicate whether a thread has written to the cache line during the transaction. In addition, a tag field 116_2 may be provided to store tag information, and a data field 116_3 may provide for storage of data information.

[0016] Thus in various embodiments, to track transactional read-sets and write-sets two or more additional state bits can be stored per cache line in a data or shared instruction-data cache, namely W, R0, R1, ..., RN. Each Rx-bit indicates the line belongs to the transactional read-set of thread x, where the maximum value of x is the number of threads that can simultaneously share data in the given cache. The W-bit indicates that the line belongs to the transactional write-set of one of the threads. When the W-bit is 1, exactly one Rx bit is also set 1 to indicate the thread of the write-set. When the W-bit is 1, the data stored for the cache line is the speculatively written value from within the transaction of thread x. Note that the data is invisible to threads other than x. In addition to inclusion of this state information in a data or shared instruction-data cache, the same state information (as to the read-set state information) can be stored per cache line in an instruction cache. These state bits are referred to as R0-RN, and perform exactly like the corresponding bits in data or shared instruction-data caches.

[0017] One or more additional state bits can be stored per cache line in a write back buffer (WBB) or victim cache (VC) structure that hold lines evicted from other caches. These state bits are referred to as W0, W1,...,WN and indicate that the entry belongs to the transactional write-set of a thread. Exactly zero or one of the W-bits can be 1 for a single entry. When a Wx-bit is 1, the data stored in the WBB or VC entry is the speculatively written value from within the transaction of thread x. The data is invisible to threads other than x. For simplicity, the WBB or VC state bits can also be encoded as those in the conventional caches described above (W, R0, R1, R2, etc.). Similarly, one or more additional state bits can be stored per cache line in a fill buffer (FB) or prefetch buffer (PRFB) structure that temporarily holds cache lines prior to allocation into a cache. These state bits are defined and function identically to those described above (see WBBs).

[0018] As seen, when a cache line is evicted from cache memory 110, it may be provided to a second level cache, namely a L2 or second level cache memory 130 that also provides for support for read-set and write-set status information. As seen, each cache line 135_0-135_n in cache memory 130 may similarly include a read-set field 136_0 with read-set indicators for each thread, a write-set field 136_1 to store a write-set indicator, a tag field 136_2, and a data field 136_3. In the illustration of FIG. 2, an interim cache structure, namely a write back buffer/victim cache 120 may be present to receive and store a cache line in an entry 125_0 (with corresponding read-set field 126_0, write-set field 126_1, tag field 126_2, and data field 126_3) and, upon its eviction from this level, the cache line can be provided to cache memory 130.

[0019] Also shown in FIG. 2, another interim structure, namely a fill buffer/prefetch buffer 140 may be provided as an intermediate structure between cache memory 130 and cache memory 110. As seen here, each entry 145 within this storage may similarly include read and write-set indicators 146_0 and 146_1, along with tag and data portions 146_2 and 146_3.

[0020] Assume that a higher level cache to cache memory 130 such as a shared cache memory (not shown in FIG. 2) does not provide support for read and write-set indicators as described herein. Accordingly, a compression filter 150 may be associated with cache memory 130 to enable storage of certain information

associated with cache lines including read-set information to enable correct transactional memory processing. As shown in FIG. 2, compression filter 150, which may be a Bloom filter, includes a plurality of filters 155_0-155_n each associated with a given thread. Each such filter may store a vector or other collection of bits that can identify whether a corresponding address is represented in the filter. As such the Bloom filter collectively maintains a representation of addresses having set R bits. In an embodiment, a single bit with a logic one value within the vector indicates possible presence of a set R bit for cache line addresses that hash to this bit. More specifically, a cache line address (or a tag or other identifier) may be applied to a function generator 152 which may perform a plurality of hash functions to thus generate a set of bits for storage in the indicated filter, where multiple bits may be set to correspond to the input address. Then when checking whether an address is represented within the compression filter, the address to be checked may be similarly applied to function generator 152. If less than all of the resulting bits are of a set state, this indicates that the corresponding address is not represented in the compression filter. Thus filter 150 may serve as secondary storage of read-set addresses, separated by thread. Each thread's filter can be cleared upon commit of its current transaction. Although shown at this high level in the embodiment of FIG. 2, understand the scope of the present invention is not limited in this regard.

[0021] FIG. 3 shows a more detailed description of the process a line may follow between a supported and unsupported level. In FIG. 3 there exist two separate threads of data and examples for the two possible paths departing from and arriving to the supporting level.

[0022] Firstly in FIG. 3 there exists a cache 210 containing cache lines 215_0-215_n including read-set indicators 216_0, write-set indicators 216_1, tag portions 216_2, and data portions 216_3, as described herein. The first example discussed is of a cache line traveling to an unsupported level in the cache. In this example a cache line is evicted from cache 210 to a level that does not support the read and write state indicators. The data follows an eviction system that gives preference to the eviction of data without the read/write set indicators due to the nature of the destination level. Thus there is a bias against evicting lines containing the read/write set indicators.

However assume all elements within the cache contain active read/write set indicators, such that a least recently used (LRU) is used to determine which line is to be evicted to the adjacent level.

[0023] Once a cache line has been selected for eviction from the level, it undergoes a series of changes to allow for compatibility with the adjacent cache. Assume a cache line is evicted with a set write-set indicator. In this instance, the transaction is aborted, and accordingly the transaction is unrolled and either attempted again or a recovery mechanism is performed. For an eviction of a cache line with any set read-set indicators, an allocation into one or more compression filters may occur. In FIG. 3 a compression filter 220 contains a filter 225_{0-n} associated with each thread. Each filter can store a representation of a cache line address for evicted lines having set read-set indicators and will continue to hold such representations in order to track the transactional data until the transactional process commits. After these processes have been completed the datum is the transferred to the cache without the read/write set indicators, e.g., through a write back buffer 235.

[0024] Thus as shown, upon eviction from cache memory 210, if any read-set indicator associated with a given thread is of a set state (and the write-set indicator is clear), an allocation into a corresponding one of compression filters 225_0-225_n associated with the thread can occur. Then the given cache line (namely its tag and data portions) can be evicted to a write back buffer 235 which in an embodiment may be a first in first out buffer, such that upon reaching the head of the entry of this buffer, the given information can be evicted to a next higher cache level. Note however if a cache line to be evicted has a set write-set indicator, a transaction abort can occur. In various embodiments, handling of a transaction abort may include flushing the processor pipeline and so forth.

[0025] Additionally in FIG. 3 there exists the process through which datum may be entered into a supported level in the cache. In this case the data has been entered into a fill buffer 240. Within the fill buffer 240, the cache line exists as it would in any other supported level in the cache with the read and write set indicators intact. From the fill buffer the data can be read and subsequently written into the destination level.

[0026] As further seen in FIG. 3, data may further be written in cache memory 210 from a core or other processing engine (or a lower level cache). Incoming load or read operations which thus allocate a cache line within cache memory 110 may cause a given read-set indicator (namely associated with the thread issuing the load/read operation) can be set. Similarly, data from a lower cache level or processing engine may be written to cache memory 210 as a store/write operation. In these instances, the cache line to which this information is written may have its write-set indicator placed in a set state and similarly, a read-set indicator for the corresponding thread may also be set.

[0027] As further seen in FIG. 3, a cache controller 250 may be coupled to cache memory 210. In various embodiments, cache controller 250 may include logic to perform evictions of data from cache memory 210, e.g., due to a capacity constraint. In various embodiments, replacement state information 216_4 may be associated with each line and can be used to indicate a relative age of the data. In various embodiments, this relative age may be expressed as a timestamp to thus indicate which cache line is the least recently used. In various embodiments, cache controller 250 may be configured with a replacement policy that favors retention of lines having a set write-set indicator and also favors retention of lines having one or more read-set indicators of a set state.

[0028] In general, operation of a cache hierarchy in accordance with an embodiment of the present invention is as follows: read accesses from thread x set the corresponding Rx bit in the L1 cache entry (more generally, any level of cache that can directly provide data to load instructions); and write accesses from thread x set the corresponding Rx bit and the W-bit in the L1 cache entry (more generally, any level of cache directly updated by store instructions).

[0029] Lines evicted from any level of cache to any other level of cache that supports read-set and write-set tracking carry their R-bits and W-bits to the next level of cache. This operation may include transference though an intermediate structure, such as a WBB or VC described above. Lines filled from any level of cache to a lower-level cache carry their R-bits and W-bits with them. This operation may include transference though an intermediate structure for tracking misses, such as a FB or

prefetch buffer. Lines may also be refilled from a VC coupled between two levels of hierarchy rather than directly from the next level.

[0030] Note that read-set lines for which a corresponding Rx bit is set that are displaced from any level of cache and not transferred to a higher level of cache are instead transferred to each compression filter. Transferring the address to the compression filter maintains read-set tracking even though the cache line may no longer exist in the cache hierarchy with an R-bit set.

[0031] In various embodiments the replacement policies of all caches augmented with W-bits may be biased against eviction of lines with the W-bit set when the next level of cache hierarchy does not support W-bits for write-set tracking. For example, a cache implementing a least recently used (LRU) policy would choose the least recently used line without a W set when evicting to another level that does not have W-bits. This is so since loss of a W-bit line from the cache hierarchy aborts the speculative transaction for the corresponding thread, since the data from at least one transactional write is lost.) Similarly, the replacement policies of all caches augmented with R-bits are optionally biased against eviction of lines with any R-bit set. For example, a cache implementing a LRU policy would choose the least recently used line without any R set when evicting to another level that does not have R-bits. This can reduce capacity pressure on the compression-based filter. In various embodiments, W-bit lines may be favored over R-bit lines.

[0032] Embodiments thus provide read-set and write-set tracking state that can easily propagate through a cache hierarchy, making efficient use of existing hardware by using a compression-based filter to maintain read-set tracking for all cases in which a line is displaced and the R-bit information cannot be propagated elsewhere. Still further embodiments may give storage preference to W-bit lines to make the most efficient use of cache space for maintaining the transactional write-set data. In this way, embodiments can maintain larger transactional read-sets and write-sets and avoid pathological behavior caused by limited set-associated activity in caches. Still further, aliasing can be reduced or avoided by using the existing caches as the primary tracking mechanism, and can avoid additional storage and data paths for transactional write-set data.

[0033] Referring now to FIG. 4, shown is a flow diagram of example operations within a transaction in accordance with an embodiment of the present invention. Note that the flow shown in FIG. 4 is with regard to example operations that may occur during a transaction, and do not necessarily show a linear flow of actual operations that occur in a particular transaction. As shown in FIG. 4, method 300 may begin at block 310 by beginning a transaction. In various embodiments, a transaction may begin by setting up state for the transaction such as one or more storages for storage of information along with setting up various indicators and so forth to identify that a given thread is entering into a transaction. Next at block 320 read and/or write accesses may be performed by the thread to store data and to a given cache line in the cache memory and set appropriate read/write-set status indicators. That is, as described above, when a cache line is written into a cache during a transaction, a corresponding write-set status indicator may be set, along with a read-set status indicator associated with the thread that performs the write instruction. Similar operations to set a corresponding read-set status indicator may occur when a thread reads a cache line during a transaction.

[0034] Still referring to FIG. 4, it can be determined at diamond 330 whether a cache line is to be evicted that has a set write-set indicator. If so, control passes to diamond 335 to determine whether the next level cache includes write-set tracking support. If not, this could lead to an inconsistency in data during the transaction and as such, control passes to block 340 where the transaction can be aborted. Various operations in support of such transaction abort can occur such as cache and processor pipeline flushes among other operations. If such write-set support is present, control passes to block 370 where the cache line to be evicted can be stored in the next level cache along with its associated state data, including the write-set indicator (and at least one read-set indictor).

[0035] If the to-be-evicted cache line does not have a set write-set indicator, control passes from diamond 330 to diamond 350 where it can be determined if a cache line is evicted that has one more set read-set indicators. If so, control passes to diamond 360 where it can be determined whether the next level cache includes read/write set tracking support. If so, control passes to block 370 where the cache line that is to be

evicted can be stored in the next level cache along with its associated state data, including the various read-set and write-set indicators. Otherwise if the next level cache does not provide such support, control passes instead from diamond 360 to block 380 where a cache line address for the to-be-evicted cache line can be entered into a compression filter for the thread that is associated with this cache memory. In this way, read-set tracking support can be maintained. From both of blocks 380 and diamond 350 (when a to-be-evicted cache line does not have a set read-set indicator or a write-set indicator) control passes to block 390 where the cache line can be stored in the next level cache. Although shown at this high level in the embodiment of FIG. 4, understand the scope of the present invention is not limited in this regard.

[0036] Referring now to FIG. 5, shown is a block diagram of a processor in accordance with an embodiment of the present invention. As shown in FIG. 5, processor 400 may be a multicore processor including a plurality of cores 410_a – 410_n. In one embodiment, each such core may be configured to operate at multiple voltages and/or frequencies. In addition, each core may be independently controlled to operate at a selected voltage and/or frequency. To this end, each core may be associated with a corresponding voltage regulator 412a-412n. While not shown for ease of illustration, understand that each core 410 can include transactional memory logic and one or more cache levels including read/write-set tracking support, along with one or more compression filters as described herein. The various cores may be coupled via an interconnect 415 to an uncore or system agent logic 420 that includes various components. As seen, the uncore 420 may include a shared cache 430 which may be a last level cache that may not have the read/write-tracking support. In addition, the uncore may include an integrated memory controller 440, various interfaces 450 and a power control unit 455.

[0037] With further reference to FIG. 5, processor 400 may communicate with a system memory 460, e.g., via a memory bus. In addition, by interfaces 450, connection can be made to various off-chip components such as peripheral devices, mass storage and so forth. While shown with this particular implementation in the embodiment of FIG. 5, the scope of the present invention is not limited in this regard.

[0038] Referring now to FIG. 6, shown is a block diagram of a processor core in accordance with one embodiment of the present invention. As shown in FIG. 6, processor core 500 may be a multi-stage pipelined out-of-order processor. As seen in FIG. 6, core 500 includes front end units 510, which may be used to fetch instructions to be executed and prepare them for use later in the processor. For example, front end units 510 may include a fetch unit 501, an instruction cache 503, and an instruction decoder 505. In some implementations, front end units 510 may further include a trace cache, along with microcode storage as well as a micro-operation storage. Fetch unit 501 may fetch macro-instructions, e.g., from memory or instruction cache 503, and feed them to instruction decoder 505 to decode them into primitives, i.e., micro-operations for execution by the processor.

[0039] Coupled between front end units 510 and execution units 520 is an out-of-order (OOO) engine 515 that may be used to receive the micro-instructions and prepare them for execution. More specifically OOO engine 515 may include various buffers to re-order micro-instruction flow and allocate various resources needed for execution, as well as to provide renaming of logical registers onto storage locations within various register files such as register file 530 and extended register file 535. Register file 530 may include separate register files for integer and floating point operations. Extended register file 535 may provide storage for vector-sized units, e.g., 256 or 512 bits per register.

[0040] Various resources may be present in execution units 520, including, for example, various integer, floating point, and single instruction multiple data (SIMD) logic units, among other specialized hardware. For example, such execution units may include one or more arithmetic logic units (ALUs) 522, among other such execution units.

[0041] Results from the execution units may be provided to retirement logic, namely a reorder buffer (ROB) 540. More specifically, ROB 540 may include various arrays and logic to receive information associated with instructions that are executed. This information is then examined by ROB 540 to determine whether the instructions can be validly retired and result data committed to the architectural state of the processor, or whether one or more exceptions occurred that prevent a proper

retirement of the instructions. Of course, ROB 540 may handle other operations associated with retirement.

[0042] As shown in FIG. 6, ROB 540 is coupled to a cache 550 which in one embodiment may be a low level cache (e.g., an L1 cache) that includes read-set and write-set support. This tracking of read and write-sets can be performed by a transactional logic 555, which in an embodiment can be implemented via a cache controller. As further shown, a compression filter 560 may be coupled to cache 550 to maintain read-set tracking when cache lines having active read-set indicators are evicted to a different cache level. Also, execution units 520 can be directly coupled to cache 550. From cache 550, data communication may occur with higher level caches, system memory and so forth. While shown with this high level in the embodiment of FIG. 6, understand the scope of the present invention is not limited in this regard. For example, while the implementation of FIG. 6 is with regard to an out-of-order machine such as of a so-called x86 instruction set architecture (ISA), the scope of the present invention is not limited in this regard. That is, other embodiments may be implemented in an in-order processor, a reduced instruction set computing (RISC) processor such as an ARM-based processor, or a processor of another type of ISA that can emulate instructions and operations of a different ISA via an emulation engine and associated logic circuitry.

[0043] Referring now to FIG. 7, shown is a block diagram of a multicore processor in accordance with another embodiment of the present invention. As shown in the embodiment of FIG. 7, processor 600 includes multiple domains. Specifically, a core domain 610 can include a plurality of cores 610_0–610n, a graphics domain 620 can include one or more graphics engines, and a system agent domain 650 may further be present. In various embodiments, system agent domain 650 may handle power control events and power management. Each of domains 610 and 620 may operate at different voltage and/or power, and furthermore the individual units within the domains each may operate at an independent frequency and voltage. Note that while only shown with three domains, understand the scope of the present invention is not limited in this regard and additional domains can be present in other embodiments.

[0044] In general, each core 610 may further include low level caches (such as shown in FIG. 5) in addition to various execution units and additional processing elements. In turn, the various cores may be coupled to each other and to a shared cache memory formed of a plurality of units of a LLC $640_0 - 640_n$. In various embodiments, LLC 640 may be shared amongst the cores and the graphics engine, as well as various media processing circuitry. In some embodiments, this LLC may provide for read/write-set tracking support as described herein. As seen, a ring interconnect 630 thus couples the cores together, and provides interconnection between the cores, graphics domain 620 and system agent circuitry 650.

[0045] As further seen, system agent domain 650 may include display controller 652 which may provide control of and an interface to an associated display. System agent domain 650 also may include a power control unit 655.

[0046] As further seen in FIG. 7, processor 600 can further include an integrated memory controller (IMC) 670 that can provide for an interface to a system memory, such as a dynamic random access memory (DRAM). Multiple interfaces $680_0 - 680_n$ may be present to enable interconnection between the processor and other circuitry. For example, in one embodiment at least one direct media interface (DMI) interface may be provided as well as one or more Peripheral Component Interconnect Express (PCIe™) interfaces. Still further, to provide for communications between other agents such as additional processors or other circuitry, one or more interfaces in accordance with an Intel® Quick Path Interconnect (QPI) protocol may also be provided. Although shown at this high level in the embodiment of FIG. 7, understand the scope of the present invention is not limited in this regard.

[0047] Embodiments may be implemented in many different system types. Referring now to FIG. 8, shown is a block diagram of a system in accordance with an embodiment of the present invention. As shown in FIG. 8, multiprocessor system 700 is a point-to-point interconnect system, and includes a first processor 770 and a second processor 780 coupled via a point-to-point interconnect 750. As shown in FIG. 8, each of processors 770 and 780 may be multicore processors, including first and second processor cores (i.e., processor cores 774a and 774b and processor cores 784a and 784b), although potentially many more cores may be present in the

processors. Each of the processors can include transactional memory logic and one or more transaction-supported caches to enable efficient propagation of read and write-set tracking, as described herein.

[0048] Still referring to FIG. 8, first processor 770 further includes a memory controller hub (MCH) 772 and point-to-point (P-P) interfaces 776 and 778. Similarly, second processor 780 includes a MCH 782 and P-P interfaces 786 and 788. As shown in FIG. 8, MCH's 772 and 782 couple the processors to respective memories, namely a memory 732 and a memory 734, which may be portions of system memory (e.g., DRAM) locally attached to the respective processors. First processor 770 and second processor 780 may be coupled to a chipset 790 via P-P interconnects 752 and 754, respectively. As shown in FIG. 8, chipset 790 includes P-P interfaces 794 and 798.

[0049] Furthermore, chipset 790 includes an interface 792 to couple chipset 790 with a high performance graphics engine 738, by a P-P interconnect 739. In turn, chipset 790 may be coupled to a first bus 716 via an interface 796. As shown in FIG. 8, various input/output (I/O) devices 714 may be coupled to first bus 716, along with a bus bridge 718 which couples first bus 716 to a second bus 720. Various devices may be coupled to second bus 720 including, for example, a keyboard/mouse 722, communication devices 726 and a data storage unit 728 such as a disk drive or other mass storage device which may include code 730, in one embodiment. Further, an audio I/O 724 may be coupled to second bus 720. Embodiments can be incorporated into other types of systems including mobile devices such as a smart cellular telephone, tablet computer, netbook, Ultrabook™, or so forth.

[0050] Embodiments may be used in many different types of systems. For example, in one embodiment a communication device can be arranged to perform the various methods and techniques described herein. Of course, the scope of the present invention is not limited to a communication device, and instead other embodiments can be directed to other types of apparatus for processing instructions, or one or more machine readable media including instructions that in response to being executed on a computing device, cause the device to carry out one or more of the methods and techniques described herein.

[0051] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0052] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A processor comprising:

a cache memory to store a plurality of cache lines, each including a tag portion, a data portion, a write-set field to store a write-set indicator to indicate whether data in the data portion has been speculatively written during a transaction of a transactional memory, and a read-set field to store a plurality of read-set indicators each to indicate whether a corresponding thread has read the data before the transaction has committed; and

a compression filter associated with the cache memory, the compression filter including a first filter storage to store a representation of a cache line address of a cache line read by a first thread of the plurality of threads before the transaction has committed.

2. The processor of claim 1, further comprising a second cache memory coupled to the cache memory to store a plurality of second cache lines, wherein the second cache lines do not include a write-set field or a read-set field.

3. The processor of claim 2, further comprising a controller to store the representation when the cache line is evicted from the cache memory to the second cache memory.

4. The processor of claim 1, wherein the processor is to abort the transaction when a cache line including a write-set indicator having a first state to indicate that data in the data portion has been speculatively written during a transaction is evicted before the transaction is committed.

5. The processor of claim 4, wherein the processor is to commit the transaction when a plurality of cache lines speculatively written during the transaction have not been evicted from the cache memory.

6. The processor of claim 4, when the processor is to write a second state to the write-set indicator when the transaction has been committed.

7. The processor of claim 1, further comprising a write back buffer coupled between the cache memory and a second cache memory, the write back buffer including a plurality of entries each to store a tag portion and a data portion of a cache line evicted from the cache memory, the entries of the write back buffer not including a write-set field or a read-set field.

8. The processor of claim 1, further comprising a function generator to receive a cache line address and perform a plurality of hash functions on the cache line address to obtain the representation of the cache line address to store in the first filter storage.

9. A method comprising:

performing, via a first thread, a read transaction during a transaction of a transactional memory to read a first data and storing the first data in a first cache line of a first cache memory, the first cache line including a tag portion, a data portion, a write-set field, and a read-set field;

setting a read-set indicator of the read-set field associated with the first thread to indicate that the read transaction occurred during the transaction;

performing, via the first thread, a write transaction during the transaction to write a second data and storing the second data in a second cache line of the first cache memory, the second cache line including a write-set field; and

setting a write-set indicator of the write set field to indicate that the write transaction occurred during the transaction.

10. The method of claim 9, further comprising evicting the second cache line from the first cache memory prior to commitment of the transaction, and causing the transaction to abort responsive to the eviction.

11. The method of claim 9, further comprising:

evicting the first cache line from the first cache memory during the transaction; and

writing the first cache line including the read-set field into a second cache memory.

12. The method of claim 9, further comprising:

evicting the first cache line from the first cache memory during the transaction;

writing the first cache line without the read-set field into a second cache memory; and

storing a representation of an address of the first cache line in a storage associated with the first cache memory to maintain read-set tracking.

13. A system comprising:

a processor including a transaction logic, a first cache memory to store a plurality of cache lines each including a data portion, a write-set field to store a write-set indicator to indicate whether data in the data portion has been speculatively written during a transaction of a transactional memory, and a read-set field to store a plurality of read-set indicators each to indicate whether a corresponding thread has read the data during the transaction, and a first filter storage to store a representation of an address of a cache line having a set read-set indicator evicted from the first cache memory during the transaction, to maintain read-set tracking of a read-set of the transaction; and

a dynamic random access memory (DRAM) coupled to the processor.

14. The system of claim 13, wherein the processor further comprises a second cache memory to store a plurality of second cache lines, wherein the second cache lines do not include a write-set field or a read-set field.

15. The system of claim 14, wherein the transaction logic is to cause the address representation to be stored when the cache line is evicted from the first cache memory to the second cache memory.

16. The system of claim 13, wherein the transaction logic is to abort the transaction when a cache line including a write-set indicator having a first state to

indicate that data in the data portion has been speculatively written is evicted before the transaction is committed.

17. The system of claim 16, wherein the processor further comprises a Bloom filter including the first filter storage associated with a first thread and a second filter storage associated with a second thread.

18. The system of claim 14, wherein the processor further comprises a buffer coupled between the first cache memory and the second cache memory.

19. The system of claim 18, wherein the transaction logic is to cause the address representation to be stored into the first filter storage and to further cause the data portion of the cache line to be stored into an entry of the buffer and to discard the read-set field and the write-set field of the cache line.

20. The system of claim 13, wherein the processor further comprises a function generator to receive the address and perform a plurality of hash functions on the address to obtain and store the address representation in the first filter storage.

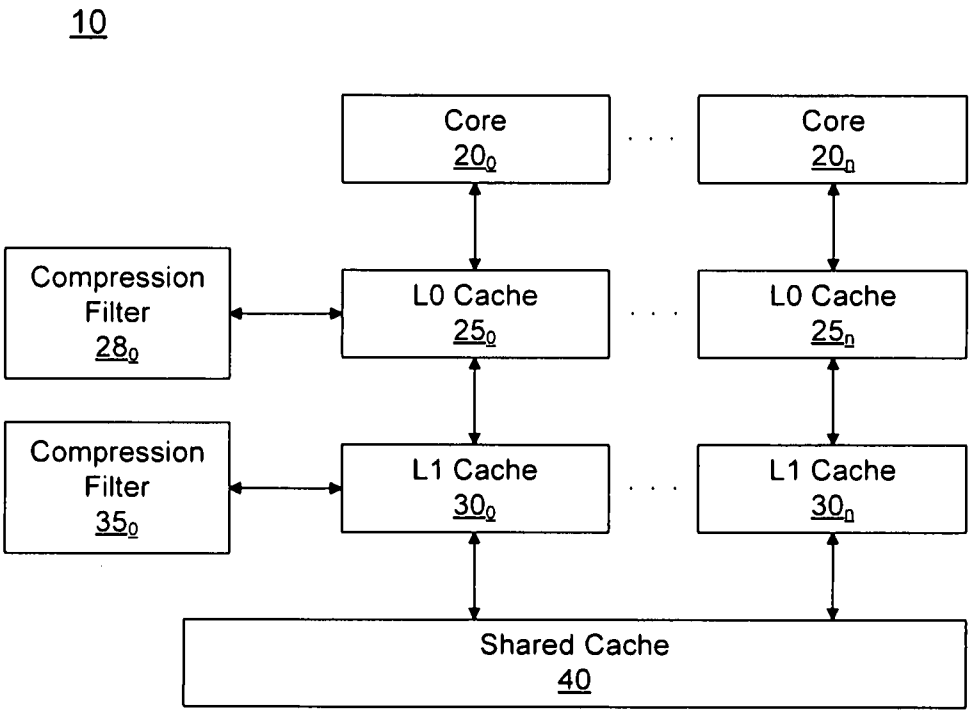

10
Core
20_0
Core
20_n
Compression
Filter
28_0
L0 Cache
25_0
L0 Cache
25_n
Compression
Filter
35_0
L1 Cache
30_0
L1 Cache
30_n
Shared Cache
40

FIG. 1

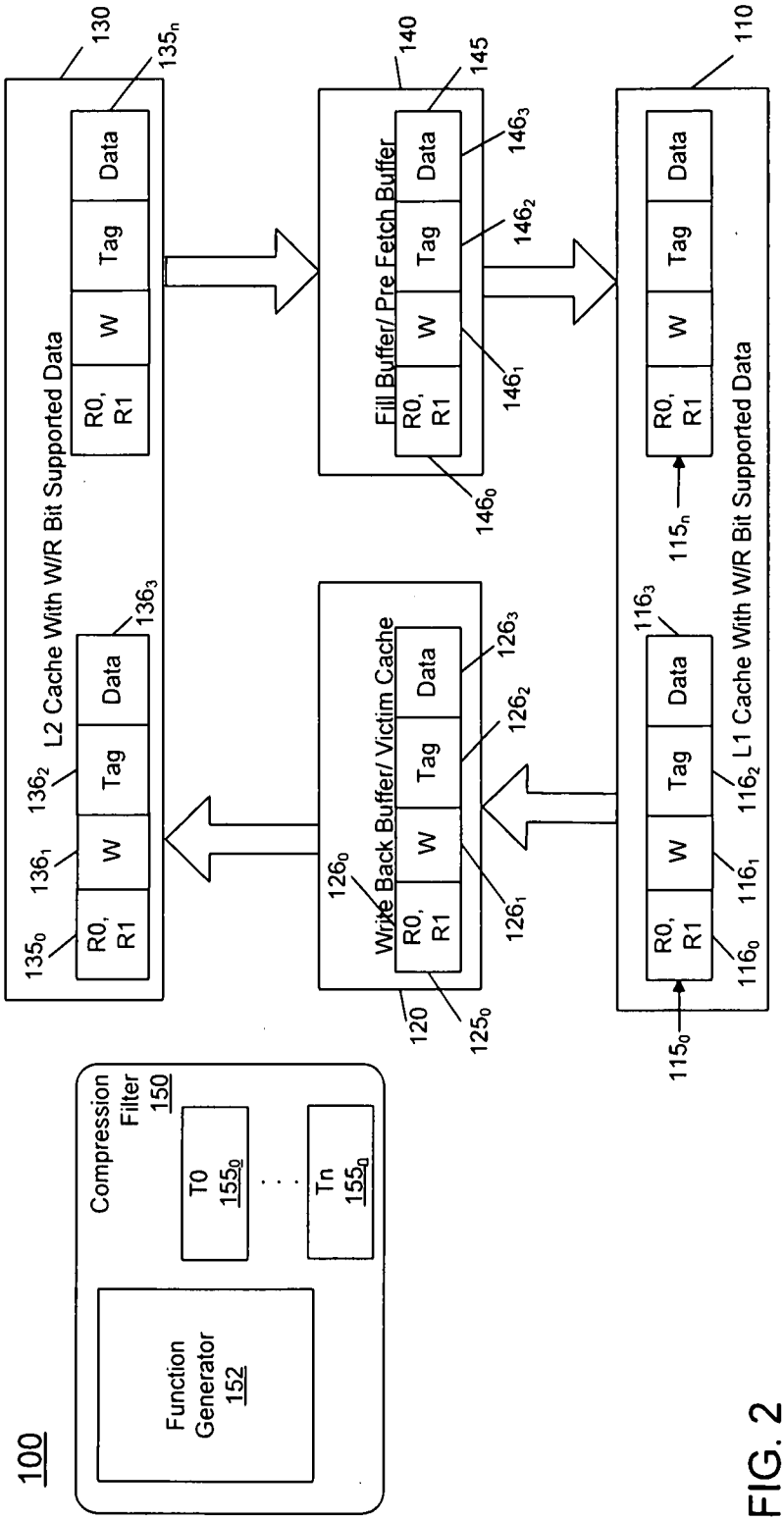

100
Compression Filter 150
Function Generator 152
T0 155$_0$
Tn 155$_0$
L2 Cache With W/R Bit Supported Data
130
135$_n$
135$_0$
136$_1$
136$_2$
136$_3$
R0, R1
W
Tag
Data
Write Back Buffer/ Victim Cache
120
125$_0$
126$_0$
126$_1$
126$_2$
126$_3$
Fill Buffer/ Pre Fetch Buffer
140
145
146$_0$
146$_1$
146$_2$
146$_3$
L1 Cache With W/R Bit Supported Data
110
115$_0$
115$_n$
116$_0$
116$_1$
116$_2$
116$_3$

FIG. 2

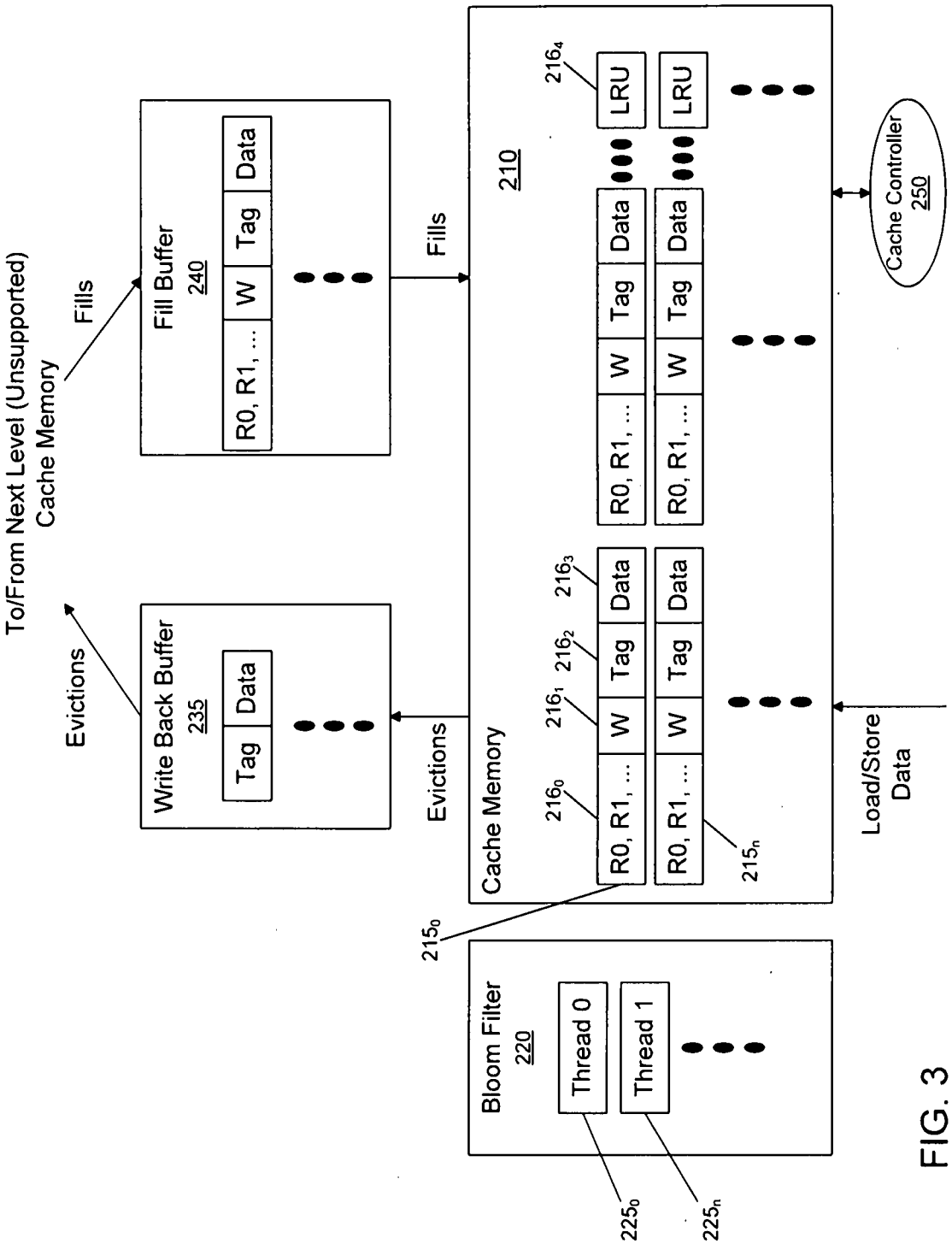

To/From Next Level (Unsupported) Cache Memory
Fills
Evictions
Fill Buffer
240
R0, R1, ...
W
Tag
Data
Write Back Buffer
235
Tag
Data
Fills
Evictions
210
Cache Memory
216_0
216_1
216_2
216_3
216_4
R0, R1, ...
W
Tag
Data
LRU
215_0
215_n
Cache Controller
250
Load/Store Data
Bloom Filter
220
Thread 0
Thread 1
225_0
225_n

FIG. 3

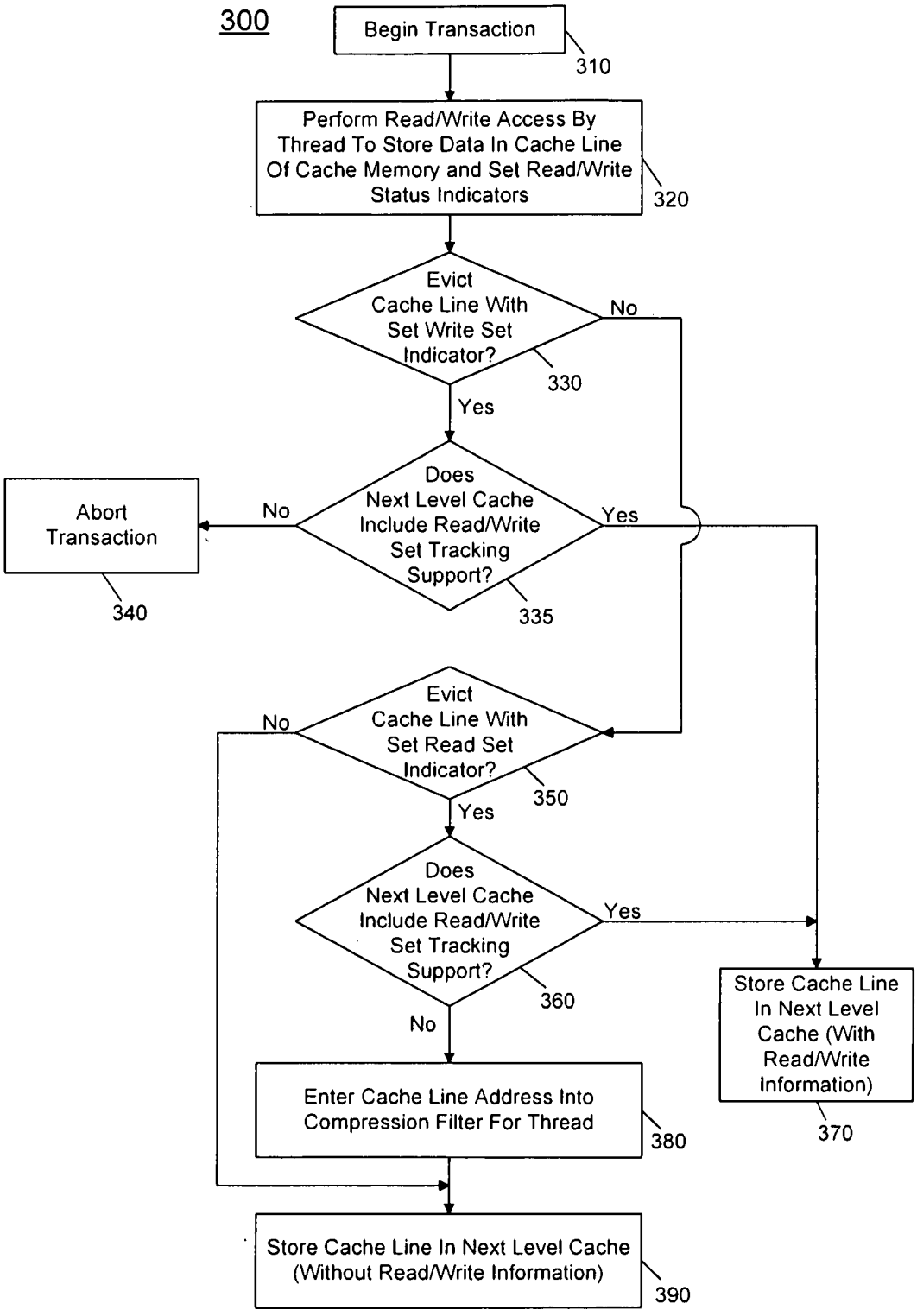

300
Begin Transaction
310
Perform Read/Write Access By Thread To Store Data In Cache Line Of Cache Memory and Set Read/Write Status Indicators
320
Evict Cache Line With Set Write Set Indicator?
330
No
Yes
Does Next Level Cache Include Read/Write Set Tracking Support?
335
No
Yes
Abort Transaction
340
Evict Cache Line With Set Read Set Indicator?
350
No
Yes
Does Next Level Cache Include Read/Write Set Tracking Support?
360
Yes
No
Store Cache Line In Next Level Cache (With Read/Write Information)
370
Enter Cache Line Address Into Compression Filter For Thread
380
Store Cache Line In Next Level Cache (Without Read/Write Information)
390

FIG. 4

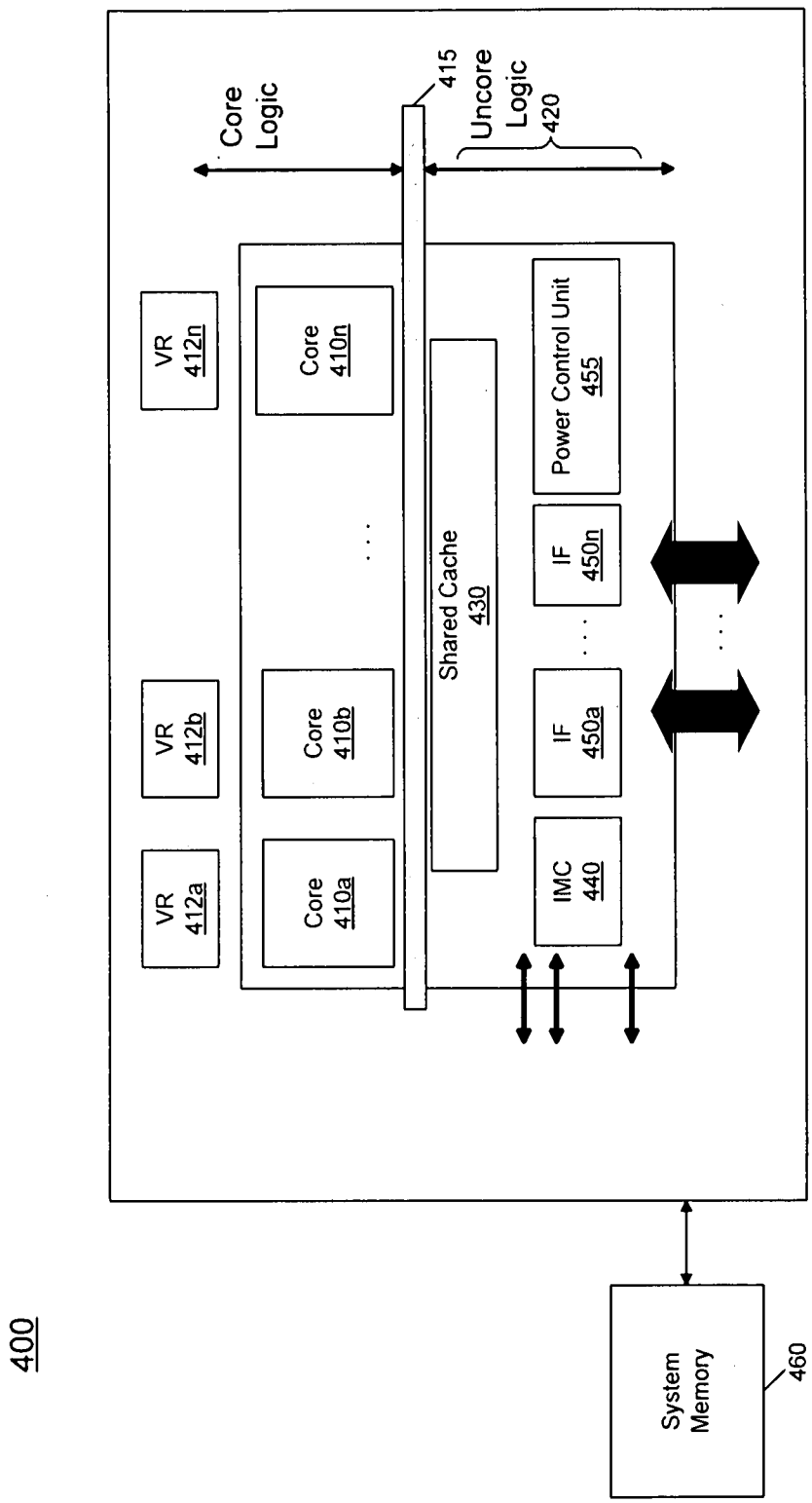

400
Core Logic
415
Uncore Logic
420
VR 412n
VR 412b
VR 412a
Core 410n
Core 410b
Core 410a
Shared Cache 430
Power Control Unit 455
IF 450n
IF 450a
IMC 440
System Memory
460

FIG. 5

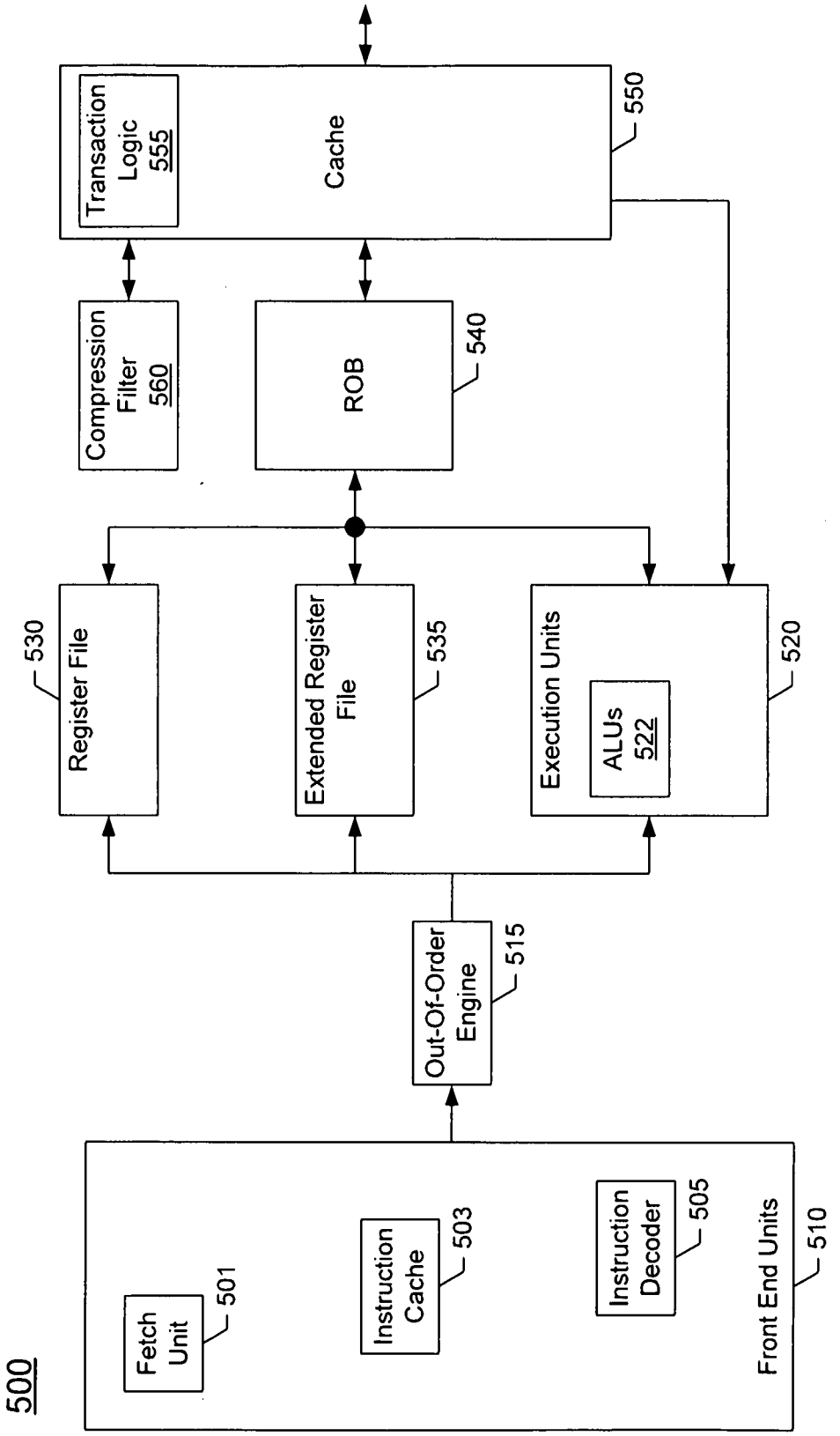

500
Fetch Unit
501
Instruction Cache
503
Instruction Decoder
505
Front End Units
510
Out-Of-Order Engine
515
Register File
530
Extended Register File
535
Execution Units
ALUs 522
520
Compression Filter 560
ROB
540
Transaction Logic 555
Cache
550

FIG. 6

600

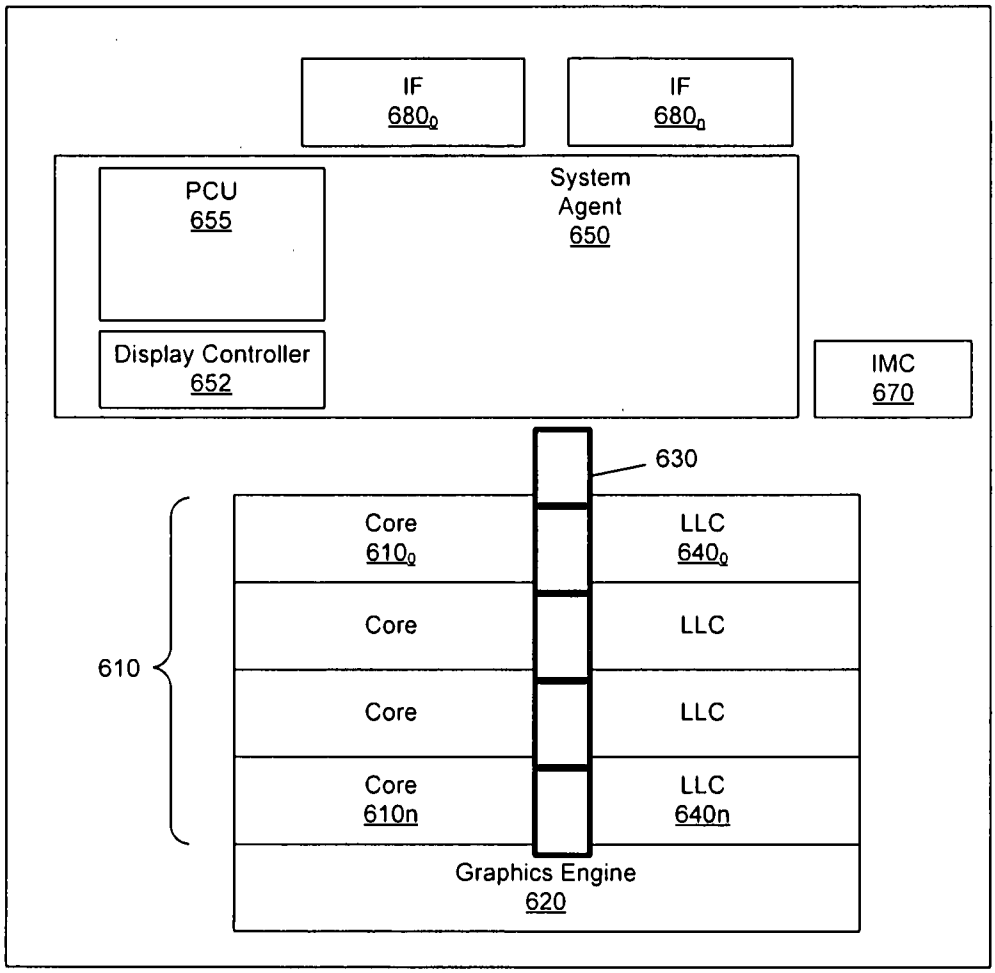

IF
680$_0$
IF
680$_n$
PCU
655
System
Agent
650
Display Controller
652
IMC
670
630
610
Core
610$_0$
LLC
640$_0$
Core
LLC
Core
LLC
Core
610n
LLC
640n
Graphics Engine
620

FIG. 7

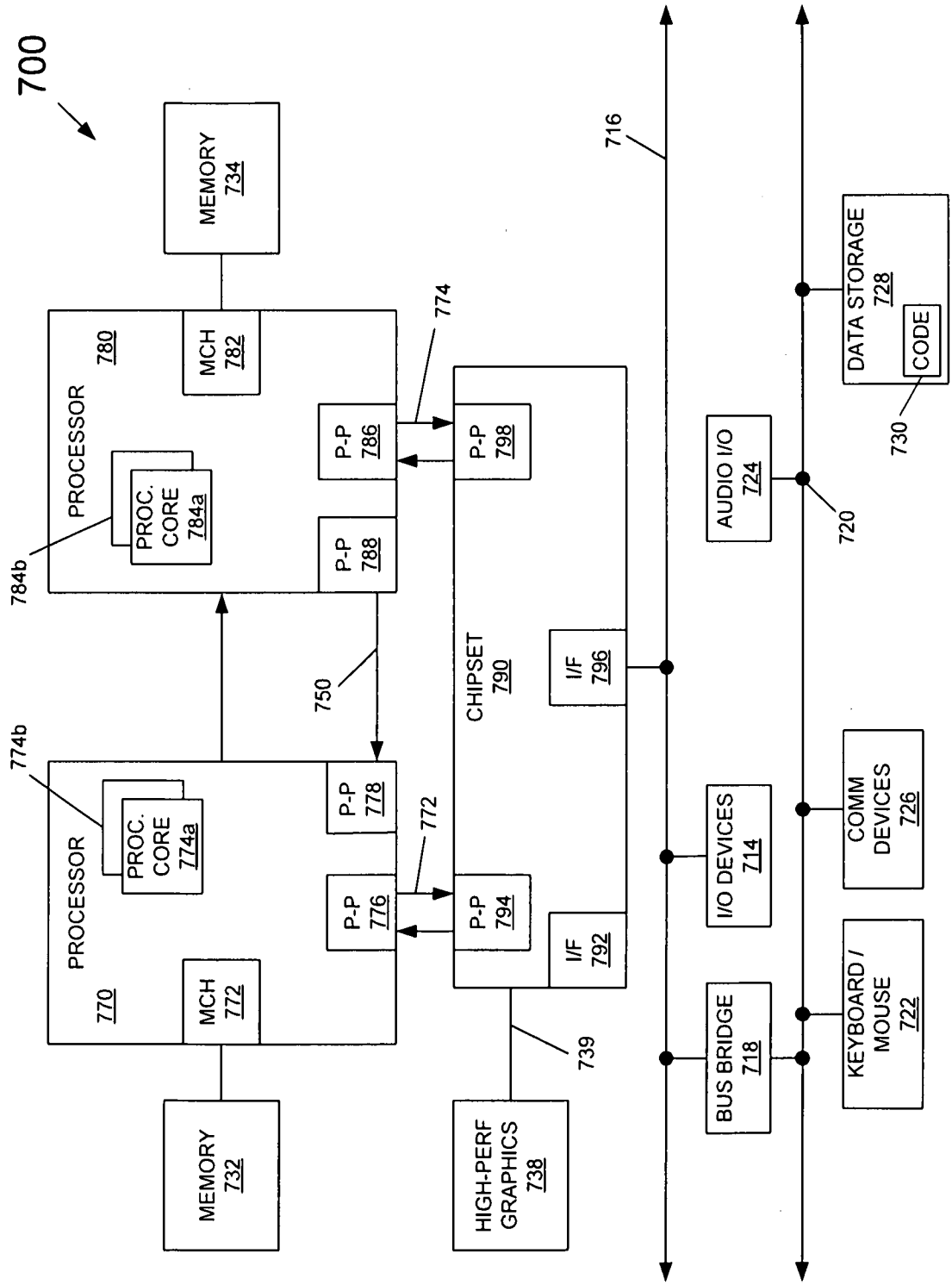

700
MEMORY 734
MCH 782
PROCESSOR 780
PROC. CORE 784a
784b
P-P 786
P-P 788
774
P-P 798
750
CHIPSET 790
I/F 796
716
774b
PROCESSOR 770
PROC. CORE 774a
P-P 778
P-P 776
772
P-P 794
I/F 792
MCH 772
739
MEMORY 732
HIGH-PERF GRAPHICS 738
AUDIO I/O 724
DATA STORAGE 728
CODE
730
720
I/O DEVICES 714
COMM DEVICES 726
BUS BRIDGE 718
KEYBOARD / MOUSE 722

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/046709

A. CLASSIFICATION OF SUBJECT MATTER

G06F 12/08(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 12/08; G06F 3/00; G06F 9/44; G06F 12/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: cache, memory, transaction, write, read, compression filter, buffer, DRAM, evict, multicore, indicator, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0037027 A1 (CHINNA PRUDVI et al.) 11 February 2010 See paragraphs [0008] and [0016]-[0026]; claim 1; and figures 1-2.	1-20
A	US 2007-0245099 A1 (JAN GRAY et al.) 18 October 2007 See paragraphs [0009]-[0011], [0036]-[0040], [0043]-[0049], and [0074]; claim 10; and figures 1, 4-5, and 14.	1-20
A	US 2008-0189487 A1 (SIMON JOHN CRASKE) 07 August 2008 See paragraphs [0009]-[0052] and [0061]-[0069]; and figure 1.	1-20
A	US 2010-0169579 A1 (GAD SHEAFFER et al.) 01 July 2010 See paragraphs [0017]-[0054] and [0063]-[0070]; and figures 1-2.	1-20
A	US 2010-0191930 A1 (DANA GROFF et al.) 29 July 2010 See paragraphs [0032]-[0047] and figures 1-2.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 2013 (17.10.2013)	**18 October 2013 (18.10.2013)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer KANG Sung Chul Telephone No. +82-42-481-8405

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/046709

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